FM25V10

1-Mbit (128K × 8) Serial (SPI) F-RAM

Features

- 1-Mbit ferroelectric random access memory (F-RAM) logically organized as 128K × 8
  - High-endurance 100 trillion (10^{14}) read/writes
  - 151-year data retention (See the Data Retention and Endurance table)
  - NoDelay™ writes
  - Advanced high-reliability ferroelectric process
- Very fast serial peripheral interface (SPI)
  - Up to 40-MHz frequency
  - Direct hardware replacement for serial flash and EEPROM
  - Supports SPI mode 0 (0, 0) and mode 3 (1, 1)
- Sophisticated write protection scheme
  - Hardware protection using the Write Protect ($\overline{WP}$) pin
  - Software protection using Write Disable instruction
  - Software block protection for 1/4, 1/2, or entire array
- Device ID and Serial Number
  - Manufacturer ID and Product ID
  - Unique Serial Number (FM25VN10)
- Low power consumption
  - 300 µA active current at 1 MHz
  - 90 µA (typ) standby current
  - 5 µA sleep mode current
- Low-voltage operation: V_{DD} = 2.0 V to 3.6 V
- Industrial temperature: –40 °C to +85 °C
- Packages
  - 8-pin small outline integrated circuit (SOIC) package
  - 8-pin dual flat no-leads (DFN) package
- Restriction of hazardous substances (RoHS) compliant

Functional Description

The FM25V10 is a 1-Mbit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or F-RAM is nonvolatile and performs reads and writes similar to a RAM. It provides reliable data retention for 151 years while eliminating the complexities, overhead, and system-level reliability problems caused by serial flash, EEPROM, and other nonvolatile memories.

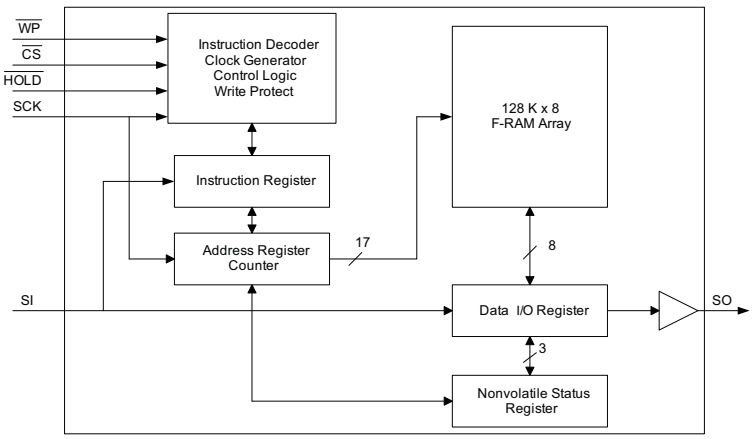
Unlike serial flash and EEPROM, the FM25V10 performs write operations at bus speed. No write delays are incurred. Data is written to the memory array immediately after each byte is successfully transferred to the device. The next bus cycle can commence without the need for data polling. In addition, the product offers substantial write endurance compared with other nonvolatile memories. The FM25V10 is capable of supporting 10^{14} read/write cycles, or 100 million times more write cycles than EEPROM.

These capabilities make the FM25V10 ideal for nonvolatile memory applications, requiring frequent or rapid writes. Examples range from data collection, where the number of write cycles may be critical, to demanding industrial controls where the long write time of serial flash or EEPROM can cause data loss.

The FM25V10 provides substantial benefits to users of serial EEPROM or flash as a hardware drop-in replacement. The FM25V10 uses the high-speed SPI bus, which enhances the high-speed write capability of F-RAM technology. The FM25VN10 is offered with a unique serial number that is read-only and can be used to identify a board or system. Both the devices incorporates a read-only Device ID that allows the host to determine the manufacturer, product density, and product revision. The device specifications are guaranteed over an industrial temperature range of –40 °C to +85 °C.

For a complete list of related documentation, click here.

Logic Block Diagram



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Pinouts

Figure 1. 8-pin SOIC pinout

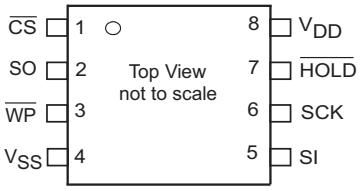
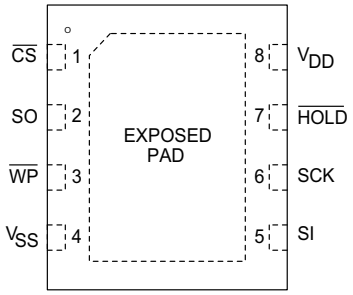


Figure 2. 8-pin DFN pinout



Pin Definitions

Pin Name	I/O Type	Description
$\overline{CS}$	Input	**Chip Select**. This active LOW input activates the device. When HIGH, the device enters low-power standby mode, ignores other inputs, and the output is tristated. When LOW, the device internally activates the SCK signal. A falling edge on $\overline{CS}$ must occur before every opcode.
SCK	Input	**Serial Clock**. All I/O activity is synchronized to the serial clock. Inputs are latched on the rising edge and outputs occur on the falling edge. Because the device is synchronous, the clock frequency may be any value between 0 and 40 MHz and may be interrupted at any time.
SI [1]	Input	**Serial Input**. All data is input to the device on this pin. The pin is sampled on the rising edge of SCK and is ignored at other times. It should always be driven to a valid logic level to meet IDD specifications.
SO [1]	Output	**Serial Output**. This is the data output pin. It is driven during a read and remains tristated at all other times including when $\overline{HOLD}$ is LOW. Data transitions are driven on the falling edge of the serial clock.
$\overline{WP}$	Input	**Write Protect**. This Active LOW pin prevents write operation to the Status Register when WPEN is set to '1'. This is critical because other write protection features are controlled through the Status Register. A complete explanation of write protection is provided in Status Register and Write Protection on page 7. This pin must be tied to V_{DD} if not used.
$\overline{HOLD}$	Input	**$\overline{HOLD}$ Pin**. The $\overline{HOLD}$ pin is used when the host CPU must interrupt a memory operation for another task. When $\overline{HOLD}$ is LOW, the current operation is suspended. The device ignores any transition on SCK or $\overline{CS}$. All transitions on $\overline{HOLD}$ must occur while SCK is LOW. This pin has a weak internal pull-up (Refer DC Electrical Characteristics table for R_{IN} spec). However, if it is not used, the $\overline{HOLD}$ pin should be tied to V_{DD}.
V_{SS}	Power supply	Ground for the device. Must be connected to the ground of the system.
V_{DD}	Power supply	Power supply input to the device.
EXPOSED PAD	No connect	The EXPOSED PAD on the bottom of 8-pin DFN package is not connected to the die. The EXPOSED PAD should not be soldered on the PCB.

Note
1. SI may be connected to SO for a single pin data interface.

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Functional Overview

The FM25V10 is a serial F-RAM memory. The memory array is logically organized as 131,072 × 8 bits and is accessed using an industry-standard serial peripheral interface (SPI) bus. The functional operation of the F-RAM is similar to serial flash and serial EEPROMs. The major difference between the FM25V10 and a serial flash or EEPROM with the same pinout is the F-RAM's superior write performance, high endurance, and low power consumption.

Memory Architecture

When accessing the FM25V10, the user addresses 64K locations of eight data bits each. These eight data bits are shifted in or out serially. The addresses are accessed using the SPI protocol, which includes a chip select (to permit multiple devices on the bus), an opcode, and a three-byte address. The upper 7 bits of the address range are 'don't care' values. The complete address of 17 bits specifies each byte address uniquely.

Most functions of the FM25V10 are either controlled by the SPI interface or handled by on-board circuitry. The access time for the memory operation is essentially zero, beyond the time needed for the serial protocol. That is, the memory is read or written at the speed of the SPI bus. Unlike a serial flash or EEPROM, it is not necessary to poll the device for a ready condition because writes occur at bus speed. By the time a new bus transaction can be shifted into the device, a write operation is complete. This is explained in more detail in the interface section.

Serial Peripheral Interface – SPI Bus

The FM25V10 is a SPI slave device and operates at speeds up to 40 MHz. This high-speed serial bus provides high-performance serial communication to a SPI master. Many common microcontrollers have hardware SPI ports allowing a direct interface. It is quite simple to emulate the port using ordinary port pins for microcontrollers that do not. The FM25V10 operates in SPI Mode 0 and 3.

SPI Overview

The SPI is a four-pin interface with Chip Select ($\overline{CS}$), Serial Input (SI), Serial Output (SO), and Serial Clock (SCK) pins.

The SPI is a synchronous serial interface, which uses clock and data pins for memory access and supports multiple devices on the data bus. A device on the SPI bus is activated using the $\overline{CS}$ pin.

The relationship between chip select, clock, and data is dictated by the SPI mode. This device supports SPI modes 0 and 3. In both of these modes, data is clocked into the F-RAM on the rising edge of SCK starting from the first rising edge after $\overline{CS}$ goes active.

The SPI protocol is controlled by opcodes. These opcodes specify the commands from the bus master to the slave device. After $\overline{CS}$ is activated, the first byte transferred from the bus master is the opcode. Following the opcode, any addresses and data are then transferred. The $\overline{CS}$ must go inactive after an operation is complete and before a new opcode can be issued. The commonly used terms in the SPI protocol are as follows:

SPI Master

The SPI master device controls the operations on a SPI bus. An SPI bus may have only one master with one or more slave devices. All the slaves share the same SPI bus lines and the master may select any of the slave devices using the $\overline{CS}$ pin. All of the operations must be initiated by the master activating a slave device by pulling the $\overline{CS}$ pin of the slave LOW. The master also generates the SCK and all the data transmission on SI and SO lines are synchronized with this clock.

SPI Slave

The SPI slave device is activated by the master through the Chip Select line. A slave device gets the SCK as an input from the SPI master and all the communication is synchronized with this clock. An SPI slave never initiates a communication on the SPI bus and acts only on the instruction from the master.

The FM25V10 operates as an SPI slave and may share the SPI bus with other SPI slave devices.

Chip Select ($\overline{CS}$)

To select any slave device, the master needs to pull down the corresponding $\overline{CS}$ pin. Any instruction can be issued to a slave device only while the $\overline{CS}$ pin is LOW. When the device is not selected, data through the SI pin is ignored and the serial output pin (SO) remains in a high-impedance state.

Note A new instruction must begin with the falling edge of $\overline{CS}$. Therefore, only one opcode can be issued for each active Chip Select cycle.

Serial Clock (SCK)

The Serial Clock is generated by the SPI master and the communication is synchronized with this clock after $\overline{CS}$ goes LOW.

The FM25V10 enables SPI modes 0 and 3 for data communication. In both of these modes, the inputs are latched by the slave device on the rising edge of SCK and outputs are issued on the falling edge. Therefore, the first rising edge of SCK signifies the arrival of the first bit (MSB) of a SPI instruction on the SI pin. Further, all data inputs and outputs are synchronized with SCK.

Data Transmission (SI/SO)

The SPI data bus consists of two lines, SI and SO, for serial data communication. SI is also referred to as Master Out Slave In (MOSI) and SO is referred to as Master In Slave Out (MISO). The master issues instructions to the slave through the SI pin, while the slave responds through the SO pin. Multiple slave devices may share the SI and SO lines as described earlier.

The FM25V10 has two separate pins for SI and SO, which can be connected with the master as shown in Figure 3.

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For a microcontroller that has no dedicated SPI bus, a general-purpose port may be used. To reduce hardware resources on the controller, it is possible to connect the two data pins (SI, SO) together and tie off (HIGH) the $\overline{HOLD}$ and $\overline{WP}$ pins. Figure 4 shows such a configuration, which uses only three pins.

Most Significant Bit (MSB)

The SPI protocol requires that the first bit to be transmitted is the Most Significant Bit (MSB). This is valid for both address and data transmission.

The 1-Mbit serial F-RAM requires a 3-byte address for any read or write operation. Because the address is only 17 bits, the first seven bits, which are fed in are ignored by the device. Although these seven bits are 'don't care', Cypress recommends that these bits be set to 0s to enable seamless transition to higher memory densities.

Serial Opcode

After the slave device is selected with $\overline{CS}$ going LOW, the first byte received is treated as the opcode for the intended operation. FM25V10 uses the standard opcodes for memory accesses.

Invalid Opcode

If an invalid opcode is received, the opcode is ignored and the device ignores any additional serial data on the SI pin until the next falling edge of $\overline{CS}$, and the SO pin remains tristated.

Status Register

FM25V10 has an 8-bit Status Register. The bits in the Status Register are used to configure the device. These bits are described in Table 3 on page 7.

Figure 3. System Configuration with SPI Port

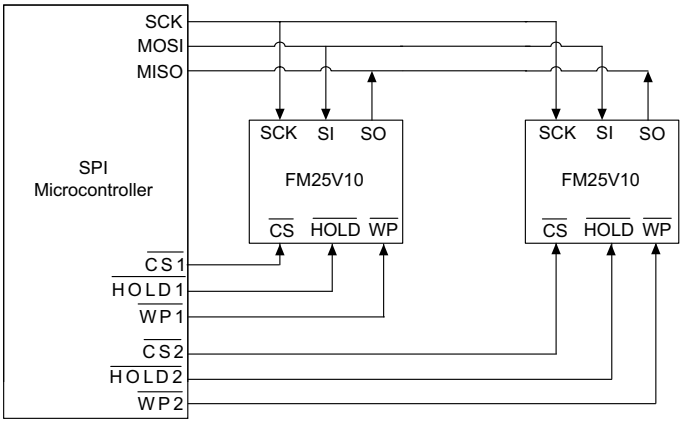
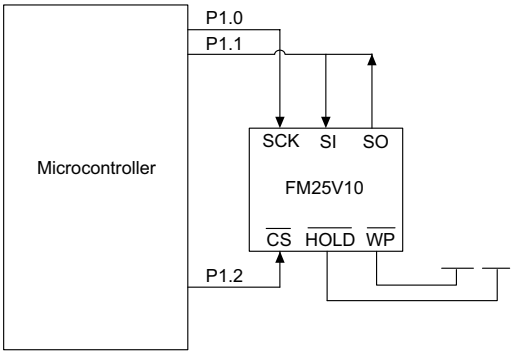


Figure 4. System Configuration without SPI Port



SPI Modes

FM25V10 may be driven by a microcontroller with its SPI peripheral running in either of the following two modes:

- SPI Mode 0 (CPOL = 0, CPHA = 0)
- SPI Mode 3 (CPOL = 1, CPHA = 1)

For both these modes, the input data is latched in on the rising edge of SCK starting from the first rising edge after $\overline{CS}$ goes active. If the clock starts from a HIGH state (in mode 3), the first rising edge after the clock toggles is considered. The output data is available on the falling edge of SCK.

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The two SPI modes are shown in Figure 5 on page 6 and Figure 6 on page 6. The status of the clock when the bus master is not transferring data is:

- SCK remains at 0 for Mode 0
- SCK remains at 1 for Mode 3

The device detects the SPI mode from the status of the SCK pin when the device is selected by bringing the $\overline{CS}$ pin LOW. If the SCK pin is LOW when the device is selected, SPI Mode 0 is assumed and if the SCK pin is HIGH, it works in SPI Mode 3.

Figure 5. SPI Mode 0

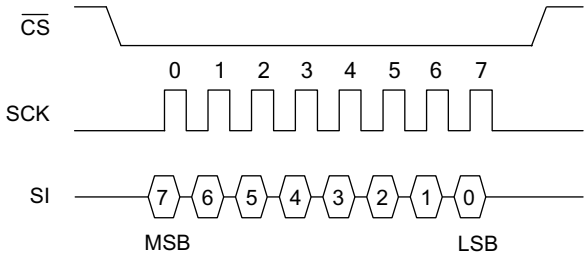
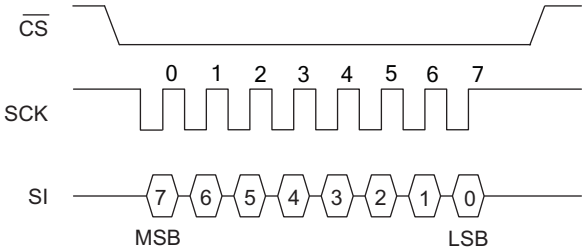


Figure 6. SPI Mode 3



Power Up to First Access

The FM25V10 is not accessible for a t_{PU} time after power-up. Users must comply with the timing parameter, t_{PU}, which is the minimum time from V_{DD} (min) to the first $\overline{CS}$ LOW.

Command Structure

There are ten commands, called opcodes, that can be issued by the bus master to the FM25V10. They are listed in Table 1. These opcodes control the functions performed by the memory.

Table 1. Opcode Commands

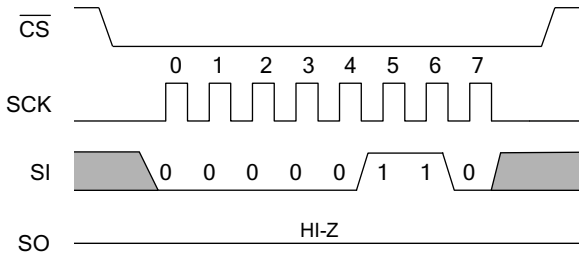
Name	Description	Opcode
WREN	Set write enable latch	0000 0110b
WRDI	Reset write enable latch	0000 0100b
RDSR	Read Status Register	0000 0101b
WRSR	Write Status Register	0000 0001b
READ	Read memory data	0000 0011b
FSTRD	Fast read memory data	0000 1011b
WRITE	Write memory data	0000 0010b
SLEEP	Enter sleep mode	1011 1001b
RDID	Read device ID	1001 1111b
SNR	Read S/N	1100 0011b

WREN - Set Write Enable Latch

The FM25V10 will power up with writes disabled. The WREN command must be issued before any write operation. Sending the WREN opcode allows the user to issue subsequent opcodes for write operations. These include writing the Status Register (WRSR) and writing the memory (WRITE).

Sending the WREN opcode causes the internal Write Enable Latch to be set. A flag bit in the Status Register, called WEL, indicates the state of the latch. WEL = '1' indicates that writes are permitted. Attempting to write the WEL bit in the Status Register has no effect on the state of this bit – only the WREN opcode can set this bit. The WEL bit will be automatically cleared on the rising edge of $\overline{CS}$ following a WRDI, a WRSR, or a WRITE operation. This prevents further writes to the Status Register or the F-RAM array without another WREN command. Figure 7 illustrates the WREN command bus configuration.

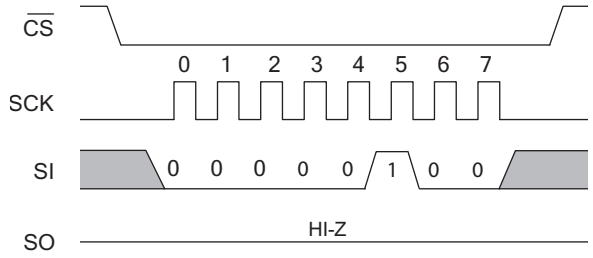
Figure 7. WREN Bus Configuration



WRDI - Reset Write Enable Latch

The WRDI command disables all write activity by clearing the Write Enable Latch. The user can verify that writes are disabled by reading the WEL bit in the Status Register and verifying that WEL is equal to '0'. Figure 8 illustrates the WRDI command bus configuration.

Figure 8. WRDI Bus Configuration



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Status Register and Write Protection

The write protection features of the FM25V10 are multi-tiered and are enabled through the status register. The Status Register is organized as follows. (The default value shipped from the factory for bit 0, WEL, BP0, BP1, bits 4–5, WPEN is ‘0’, and for bit 6 is ‘1’).

Table 2. Status Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN (0)	X (1)	X (0)	X (0)	BP1 (0)	BP0 (0)	WEL (0)	X (0)

Table 3. Status Register Bit Definition

Bit	Definition	Description
Bit 0	Don’t care	This bit is non-writable and always returns ‘0’ upon read.
Bit 1 (WEL)	Write Enable	WEL indicates if the device is write enabled. This bit defaults to ‘0’ (disabled) on power-up. WEL = '1' --> Write enabled WEL = '0' --> Write disabled
Bit 2 (BP0)	Block Protect bit ‘0’	Used for block protection. For details, see Table 4 on page 7.
Bit 3 (BP1)	Block Protect bit ‘1’	Used for block protection. For details, see Table 4 on page 7.
Bit 4-5	Don’t care	These bits are non-writable and always return ‘0’ upon read.
Bit 6	Don’t care	This bit is non-writable and always return ‘1’ upon read.
Bit 7 (WPEN)	Write Protect Enable bit	Used to enable the function of Write Protect Pin ($\overline{WP}$). For details, see Table 5 on page 7.

Bits 0 and 4-5 are fixed at ‘0’ and bit 6 is fixed at ‘1’; none of these bits can be modified. Note that bit 0 (“Ready or Write in progress” bit in serial flash and EEPROM) is unnecessary, as the F-RAM writes in real-time and is never busy, so it reads out as a ‘0’. An exception to this is when the device is waking up from sleep mode, which is described in Sleep Mode on page 11. The BP1 and BP0 control the software write-protection features and are nonvolatile bits. The WEL flag indicates the state of the Write Enable Latch. Attempting to directly write the WEL bit in the Status Register has no effect on its state. This bit is internally set and cleared via the WREN and WRDI commands, respectively.

BP1 and BP0 are memory block write protection bits. They specify portions of memory that are write-protected as shown in Table 4.

Table 4. Block Memory Write Protection

BP1	BP0	Protected Address Range
0	0	None
0	1	18000h to 1FFFFh (upper 1/4)
1	0	10000h to 1FFFFh (upper 1/2)
1	1	00000h to 1FFFFh (all)

The BP1 and BP0 bits and the Write Enable Latch are the only mechanisms that protect the memory from writes. The remaining write protection features protect inadvertent changes to the block protect bits.

The write protect enable bit (WPEN) in the Status Register controls the effect of the hardware write protect ($\overline{WP}$) pin. When the WPEN bit is set to '0', the status of the $\overline{WP}$ pin is ignored. When the WPEN bit is set to '1', a LOW on the $\overline{WP}$ pin inhibits a write to the Status Register. Thus the Status Register is write-protected only when WPEN = '1' and $\overline{WP}$ = '0'.

Table 5 summarizes the write protection conditions.

Table 5. Write Protection

WEL	WPEN	$\overline{WP}$	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

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RDSR - Read Status Register

The RDSR command allows the bus master to verify the contents of the Status Register. Reading the status register provides information about the current state of the write-protection features. Following the RDSR opcode, the FM25V10 will return one byte with the contents of the Status Register.

WRSR - Write Status Register

The WRSR command allows the SPI bus master to write into the Status Register and change the write protect configuration by setting the WPEN, BP0 and BP1 bits as required. Before issuing a WRSR command, the $\overline{WP}$ pin must be HIGH or inactive. Note that on the FM25V10, $\overline{WP}$ only prevents writing to the Status Register, not the memory array. Before sending the WRSR command, the user must send a WREN command to enable writes. Executing a WRSR command is a write operation and therefore, clears the Write Enable Latch.

Figure 9. RDSR Bus Configuration

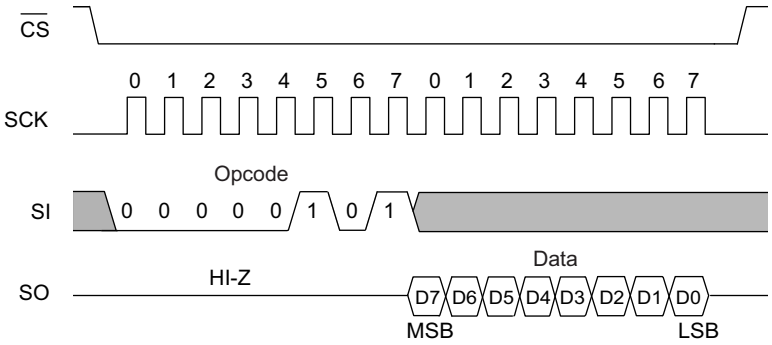
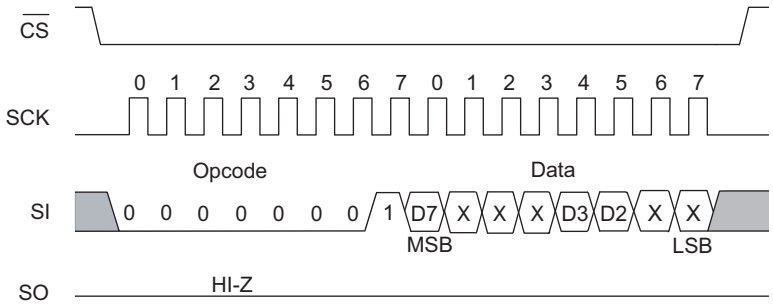


Figure 10. WRSR Bus Configuration (WREN not shown)



Memory Operation

The SPI interface, which is capable of a high clock frequency, highlights the fast write capability of the F-RAM technology. Unlike serial flash and EEPROMs, the FM25V10 can perform sequential writes at bus speed. No page register is needed and any number of sequential writes may be performed.

Write Operation

All writes to the memory begin with a WREN opcode with $\overline{CS}$ being asserted and deasserted. The next opcode is WRITE. The WRITE opcode is followed by a three-byte address containing the 17-bit address (A16-A0) of the first data byte to be written into the memory. Subsequent bytes are data bytes, which are written sequentially. Addresses are incremented internally as long as the bus master continues to issue clocks and keeps $\overline{CS}$ LOW. If the last address of 1FFFFh is reached, the counter will roll over to 00000h. Data is written MSB first. The rising edge of $\overline{CS}$ terminates a write operation. A write operation is shown in Figure 11.

Note When a burst write reaches a protected block address, the automatic address increment stops and all the subsequent data bytes received for write will be ignored by the device.

EEPROMs use page buffers to increase their write throughput. This compensates for the technology's inherently slow write operations. F-RAM memories do not have page buffers because each byte is written to the F-RAM array immediately after it is clocked in (after the eighth clock). This allows any number of bytes to be written without page buffer delays.

Note If the power is lost in the middle of the write operation, only the last completed byte will be written.

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Read Operation

After the falling edge of $\overline{CS}$, the bus master can issue a READ opcode. Following the READ command is a three-byte address containing the 17-bit address (A16–A0) of the first byte of the read operation. After the opcode and address are issued, the device drives out the read data on the next eight clocks. The SI input is ignored during read data bytes. Subsequent bytes are data bytes, which are read out sequentially. Addresses are incremented internally as long as the bus master continues to issue clocks and $\overline{CS}$ is LOW. If the last address of 1FFFFh is reached, the counter will roll over to 00000h. Data is read MSB first. The rising edge of $\overline{CS}$ terminates a read operation and tristates the SO pin. A read operation is shown in Figure 12.

Fast Read Operation

The FM25V10 supports a FAST READ opcode (0Bh) that is provided for code compatibility with serial flash devices. The FAST READ opcode is followed by a three-byte address containing the 17-bit address (A16-A0) of the first byte of the read operation and then a dummy byte. The dummy byte inserts a read latency of 8-clock cycle. The fast read operation is otherwise the same as an ordinary read operation except that it requires an additional dummy byte. After receiving opcode, address, and a dummy byte, the FM25V10 starts driving its SO line with data bytes, with MSB first, and continues transmitting as long as the device is selected and the clock is available. In case of bulk read, the internal address counter is incremented automatically, and after the last address 1FFFFh is reached, the counter rolls over to 00000h. When the device is driving data on its SO line, any transition on its SI line is ignored. The rising edge of $\overline{CS}$ terminates a fast read operation and tristates the SO pin. A Fast Read operation is shown in Figure 13.

Figure 11. Memory Write (WREN not shown) Operation

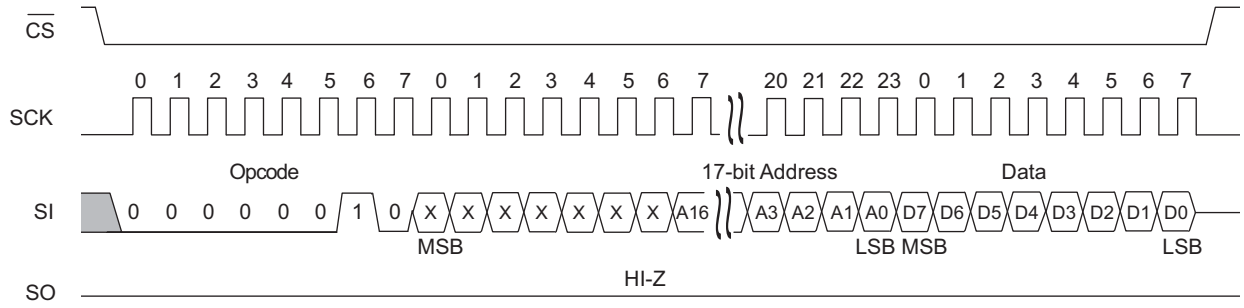

Figure 12. Memory Read Operation

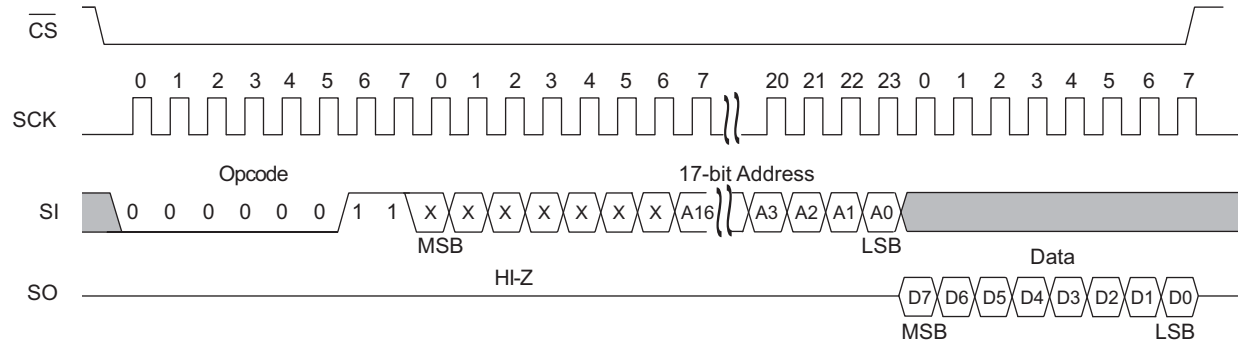

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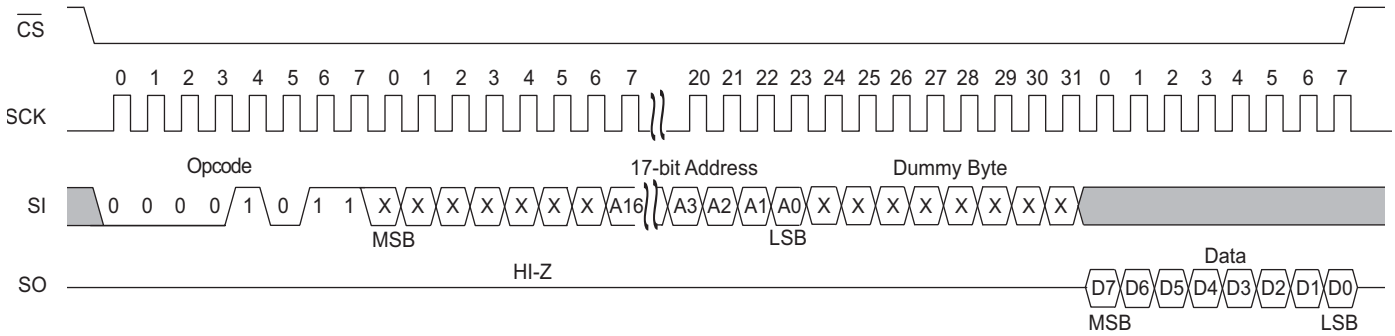
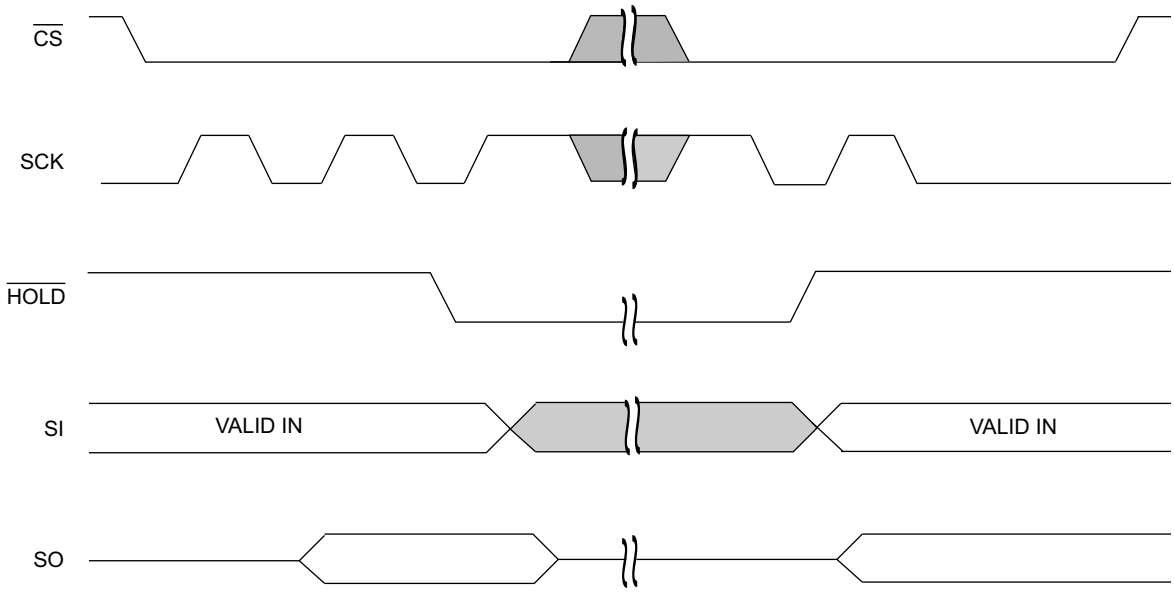
Figure 13. Fast Read Operation



HOLD Pin Operation

The HOLD pin can be used to interrupt a serial operation without aborting it. If the bus master pulls the HOLD pin LOW while SCK is LOW, the current operation will pause. Taking the HOLD pin HIGH while SCK is LOW will resume an operation. The transitions of HOLD must occur while SCK is LOW, but the SCK and CS pin can toggle during a hold state.

Figure 14. HOLD Operation [2]



Note
2. Figure shows HOLD operation for input mode and output mode.

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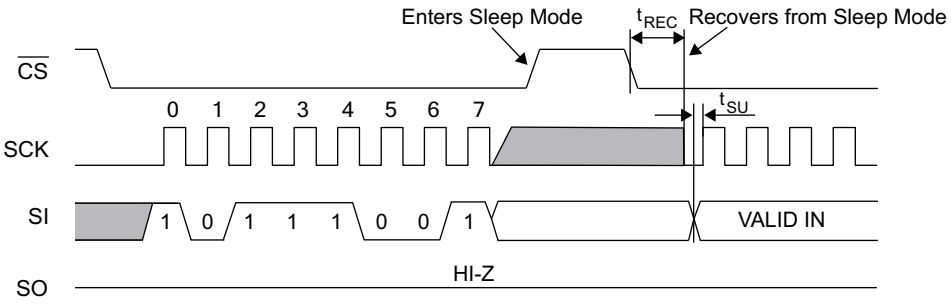
Sleep Mode

A low-power sleep mode is implemented on the FM25V10 device. The device will enter the low-power state when the SLEEP opcode B9h is clocked in and a rising edge of $\overline{CS}$ is applied. When in sleep mode, the SCK and SI pins are ignored and SO will be HI-Z, but the device continues to monitor the $\overline{CS}$ pin. On the next falling edge of $\overline{CS}$, the device will return to normal operation within t_{REC} time. The SO pin remains in a HI-Z state during the wakeup period. The device does not necessarily respond to an opcode within the wakeup period. To start the wakeup procedure, the controller may send a "dummy" read, for example, and wait the remaining t_{REC} time.

Figure 15. Sleep Mode Operation



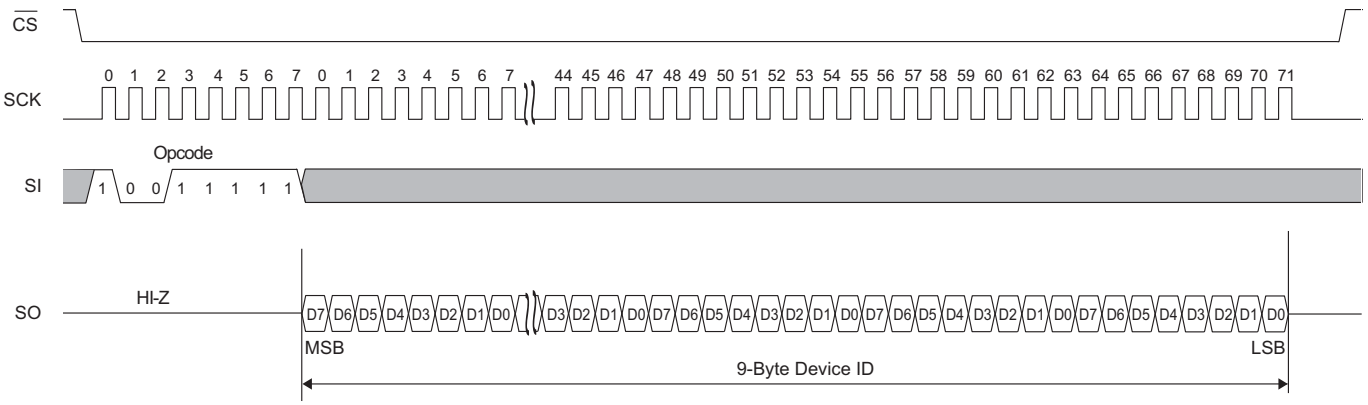
Device ID

The FM25V10 device can be interrogated for its manufacturer, product identification, and die revision. The RDID opcode 9Fh allows the user to read the manufacturer ID and product ID, both of which are read-only bytes. The JEDEC-assigned manufacturer ID places the Cypress (Ramtron) identifier in bank 7; therefore, there are six bytes of the continuation code 7Fh followed by the single byte C2h. There are two bytes of product ID, which includes a family code, a density code, a sub code, and the product revision code.

Table 6. Device ID

Device ID (9 bytes)	Device ID Description					
	71–16 (56 bits)	15–13 (3 bits)	12–8 (5 bits)	7–6 (2 bits)	5–3 (3 bits)	2–0 (3 bits)
	Manufacturer ID	Product ID				
		Family	Density	Sub	Rev	Rsvd
7F7F7F7F7F7FC22400h	01111111011111110111111110111 11110111111110111111111000010	001	00100	00	000	000

Figure 16. Read Device ID



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Unique Serial Number (FM25VN10 only)

The FM25VN10 device incorporates a read-only 8-byte serial number. It can be used to uniquely identify a pc board or system. The serial number includes a 40-bit unique number, an 8-bit CRC, and a 16-bit number that can be defined upon request by the customer. If a customer-specific number is not requested, the 16-bit Customer Identifier is 0x0000.

The serial number is read by issuing the SNR op-code (C3h).

The 8-bit CRC value can be used to compare to the value calculated by the controller. If the two values match, then the communication between slave and master was performed without errors. The function (shown below) is used to calculate the CRC value. To perform the calculation, 7 bytes of data are filled into a memory buffer in the same order as they are read from the part – i.e. byte 7, byte 6, byte 5, byte 4, byte 3, byte 2, byte 1 of the serial number. The calculation is performed on the 7 bytes, and the result should match the final byte out from the part which is byte 0, the 8-bit CRC value.

Table 7. 8-Byte Serial Number (Read only)

Customer Identifier		40-bit Unique number					8-bit CRC
SN (63:56)	SN (55:48)	SN (47:40)	SN (39:32)	SN (31:24)	SN (23:16)	SN (15:8)	SN (7:0)

Note Contact factory for requesting a customer identifier number.

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Function to Calculate CRC

```
BYTE calcCRC8( BYTE* pData, int nBytes )
{
static BYTE crctable [256] = {

0x00,  0x07,  0x0E,  0x09,  0x1C,  0x1B,  0x12,  0x15,
0x38,  0x3F,  0x36,  0x31,  0x24,  0x23,  0x2A,  0x2D,
0x70,  0x77,  0x7E,  0x79,  0x6C,  0x6B,  0x62,  0x65,
0x48,  0x4F,  0x46,  0x41,  0x54,  0x53,  0x5A,  0x5D,
0xE0,  0xE7,  0xEE,  0xE9,  0xFC,  0xFB,  0xF2,  0xF5,
0xD8,  0xDF,  0xD6,  0xD1,  0xC4,  0xC3,  0xCA,  0xCD,
0x90,  0x97,  0x9E,  0x99,  0x8C,  0x8B,  0x82,  0x85,
0xA8,  0xAF,  0xA6,  0xA1,  0xB4,  0xB3,  0xBA,  0xBD,
0xC7,  0xC0,  0xC9,  0xCE,  0xDB,  0xDC,  0xD5,  0xD2,
0xFF,  0xF8,  0xF1,  0xF6,  0xE3,  0xE4,  0xED,  0xEA,
0xB7,  0xB0,  0xB9,  0xBE,  0xAB,  0xAC,  0xA5,  0xA2,
0x8F,  0x88,  0x81,  0x86,  0x93,  0x94,  0x9D,  0x9A,
0x27,  0x20,  0x29,  0x2E,  0x3B,  0x3C,  0x35,  0x32,
0x1F,  0x18,  0x11,  0x16,  0x03,  0x04,  0x0D,  0x0A,
0x57,  0x50,  0x59,  0x5E,  0x4B,  0x4C,  0x45,  0x42,
0x6F,  0x68,  0x61,  0x66,  0x73,  0x74,  0x7D,  0x7A,
0x89,  0x8E,  0x87,  0x80,  0x95,  0x92,  0x9B,  0x9C,
0xB1,  0xB6,  0xBF,  0xB8,  0xAD,  0xAA,  0xA3,  0xA4,
0xF9,  0xFE,  0xF7,  0xF0,  0xE5,  0xE2,  0xEB,  0xEC,
0xC1,  0xC6,  0xCF,  0xC8,  0xDD,  0xDA,  0xD3,  0xD4,
0x69,  0x6E,  0x67,  0x60,  0x75,  0x72,  0x7B,  0x7C,
0x51,  0x56,  0x5F,  0x58,  0x4D,  0x4A,  0x43,  0x44,
0x19,  0x1E,  0x17,  0x10,  0x05,  0x02,  0x0B,  0x0C,
0x21,  0x26,  0x2F,  0x28,  0x3D,  0x3A,  0x33,  0x34,
0x4E,  0x49,  0x40,  0x47,  0x52,  0x55,  0x5C,  0x5B,
0x76,  0x71,  0x78,  0x7F,  0x6A,  0x6D,  0x64,  0x63,
0x3E,  0x39,  0x30,  0x37,  0x22,  0x25,  0x2C,  0x2B,
0x06,  0x01,  0x08,  0x0F,  0x1A,  0x1D,  0x14,  0x13,
0xAE,  0xA9,  0xA0,  0xA7,  0xB2,  0xB5,  0xBC,  0xBB,
0x96,  0x91,  0x98,  0x9F,  0x8A,  0x8D,  0x84,  0x83,
0xDE,  0xD9,  0xD0,  0xD7,  0xC2,  0xC5,  0xCC,  0xCB,
0xE6,  0xE1,  0xE8,  0xEF,  0xFA,  0xFD,  0xF4,  0xF3

   };
BYTE crc = 0;
while( nBytes-- ) crc = crctable[crc ^ *pData++];
return crc;
}
```


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Endurance

The FM25V10 devices are capable of being accessed at least 10^{14} times, reads or writes. An F-RAM memory operates with a read and restore mechanism. Therefore, an endurance cycle is applied on a row basis for each access (read or write) to the memory array. The F-RAM architecture is based on an array of rows and columns of 16K rows of 64-bits each. The entire row is internally accessed once, whether a single byte or all eight bytes are read or written. Each byte in the row is counted only once in an endurance calculation. Table 7 shows endurance calculations for a 64-byte repeating loop, which includes an opcode, a starting address, and a sequential 64-byte data stream. This causes each byte to experience one endurance cycle through the loop. F-RAM read and write endurance is virtually unlimited even at a 40-MHz clock rate.

Table 8. Time to Reach Endurance Limit for Repeating 64-byte Loop

SCK Freq (MHz)	Endurance Cycles/sec	Endurance Cycles/year	Years to Reach Limit
40	73,520	2.32×10^{12}	43.2
25	36,760	1.16×10^{12}	86.4
10	18,380	5.79×10^{11}	172.7
5	9,190	2.90×10^{11}	345.4

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Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –55 °C to +125 °C

Maximum accumulated storage time
At 125 °C ambient temperature ..... 1000 h
At 85 °C ambient temperature ..... 10 Years

Ambient temperature
with power applied ..... –55 °C to +125 °C

Supply voltage on V_{DD} relative to V_{SS} .....–1.0 V to +4.5 V

Input voltage ..... –1.0 V to +4.5 V and $V_{IN} < V_{DD} + 1.0$ V

DC voltage applied to outputs
in High-Z state ..... –0.5 V to V_{DD} + 0.5 V

Transient voltage (< 20 ns) on
any pin to ground potential ..... –2.0 V to V_{DD} + 2.0 V

Package power dissipation
capability (T_A = 25 °C) ..... 1.0 W

Surface mount lead soldering
temperature (3 seconds) ..... +260 °C

DC output current
(1 output at a time, 1s duration) ..... 15 mA

Electrostatic Discharge Voltage
Human Body Model (AEC-Q100-002 Rev. E) 4k

Charged Device Model (AEC-Q100-011 Rev. B) ..... 1.25 kV

Machine Model (AEC-Q100-003 Rev. E) ..... 200 V

Latch-up current ..... > 140 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{DD}
Industrial	–40 °C to +85 °C	2.0 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [3]	Max	Unit
V_{DD}	Power supply			2.0	3.3	3.6	V
I_{DD}	V_{DD} supply current	SCK toggling between V_{DD} – 0.2 V and V_{SS}, other inputs V_{SS} or V_{DD} – 0.2 V. SO = Open	f_{SCK} = 1 MHz	–	–	0.3	mA
			f_{SCK} = 40 MHz	–	1.5	3.0	mA
I_{SB}	V_{DD} standby current	$\overline{CS}$ = V_{DD}. All other inputs V_{SS} or V_{DD}.		–	90	150	µA
I_{ZZ}	Sleep mode current	$\overline{CS}$ = V_{DD}. All other inputs V_{SS} or V_{DD}.		–	5	8	µA
I_{LI}	Input leakage current (except $\overline{HOLD}$ pin)	$V_{SS} \le V_{IN} \le V_{DD}$		–	–	±1	µA
I_{LO}	Output leakage current	$V_{SS} \le V_{OUT} \le V_{DD}$		–	–	±1	µA
V_{IH}	Input HIGH voltage			0.7 × V_{DD}	–	V_{DD} + 0.3	V
V_{IL}	Input LOW voltage			– 0.3	–	0.3 × V_{DD}	V
V_{OH1}	Output HIGH voltage	I_{OH} = –1 mA, V_{DD} = 2.7 V.		2.4	–	–	V
V_{OH2}	Output HIGH voltage	I_{OH} = –100 µA		V_{DD} – 0.2	–	–	V
V_{OL1}	Output LOW voltage	I_{OL} = 2 mA, V_{DD} = 2.7 V		–	–	0.4	V
V_{OL2}	Output LOW voltage	I_{OL} = 150 µA		–	–	0.2	V
R_{IN} [4]	Input resistance ($\overline{HOLD}$ pin)	For V_{IN} = V_{IH}(min)		40	–	–	kΩ
		For V_{IN} = V_{IL}(max)		1	–	–	MΩ

Note
3. Typical values are at 25 °C, V_{DD} = V_{DD}(typ). Not 100% tested.
4. The input pull-up circuit is strong (> 40 kΩ) when the input voltage is above V_{IH} and weak (>1 MΩ) when the input voltage is below V_{IL}.

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Data Retention and Endurance

Parameter	Description	Test condition	Min	Max	Unit
T_{DR}	Data retention	T_A = 85 °C	10	–	Years
		T_A = 75 °C	38	–	
		T_A = 65 °C	151	–	
NV_C	Endurance	Over operating temperature	10^{14}	–	Cycles

Capacitance

Parameter [5]	Description	Test Conditions	Max	Unit
C_O	Output pin capacitance (SO)	T_A = 25 °C, f = 1 MHz, V_{DD} = V_{DD}(typ)	8	pF
C_I	Input pin capacitance		6	pF

Thermal Resistance

Parameter	Description	Test Conditions	8-pin SOIC	8-pin DFN	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	138	31	°C/W
Θ_{JC}	Thermal resistance (junction to case)		40	35	°C/W

AC Test Conditions

Input pulse levels .....10% and 90% of V_{DD}
Input rise and fall times .....3 ns
Input and output timing reference levels .....0.5 × V_{DD}
Output load capacitance ..... 30 pF

Note
5. This parameter is characterized and not 100% tested.

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AC Switching Characteristics

Over the Operating Range

Parameters [6]		Description	V_{DD} = 2.0 V to 2.7 V		V_{DD} = 2.7 V to 3.6 V		Unit
Cypress Parameter	Alt. Parameter		Min	Max	Min	Max	
f_{SCK}	–	SCK clock frequency	0	25	0	40	MHz
t_{CH}	–	Clock HIGH time	20	–	11	–	ns
t_{CL}	–	Clock LOW time	20	–	11	–	ns
t_{CSU}	t_{CSS}	Chip select setup	12	–	10	–	ns
t_{CSH}	t_{CSH}	Chip select hold	12	–	10	–	ns
t_{OD} [7, 8]	t_{HZCS}	Output disable time	–	20	–	12	ns
t_{ODV}	t_{CO}	Output data valid time	–	18	–	9	ns
t_{OH}	–	Output hold time	0	–	0	–	ns
t_D	–	Deselect time	60	–	40	–	ns
t_R [9, 10]	–	Data in rise time	–	50	–	50	ns
t_F [9, 10]	–	Data in fall time	–	50	–	50	ns
t_{SU}	t_{SD}	Data setup time	8	–	5	–	ns
t_H	t_{HD}	Data hold time	8	–	5	–	ns
t_{HS}	t_{SH}	$\overline{\text{HOLD}}$ setup time	12	–	10	–	ns
t_{HH}	t_{HH}	$\overline{\text{HOLD}}$ hold time	12	–	10	–	ns
t_{HZ} [7, 8]	t_{HHZ}	$\overline{\text{HOLD}}$ LOW to HI-Z	–	25	–	20	ns
t_{LZ} [8]	t_{HLZ}	$\overline{\text{HOLD}}$ HIGH to data active	–	25	–	20	ns

Notes

6. Test conditions assume a signal transition time of 3 ns or less, timing reference levels of 0.5 × V_{DD}, input pulse levels of 10% to 90% of V_{DD}, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance shown in AC Test Conditions on page 16.
7. t_{OD} and t_{HZ} are specified with a load capacitance of 5 pF. Transition is measured when the outputs enter a high impedance state
8. This parameter is characterized and not 100% tested.
9. Rise and fall times measured between 10% and 90% of waveform.
10. These parameters are guaranteed by design and are not tested.

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Figure 17. Synchronous Data Timing (Mode 0)

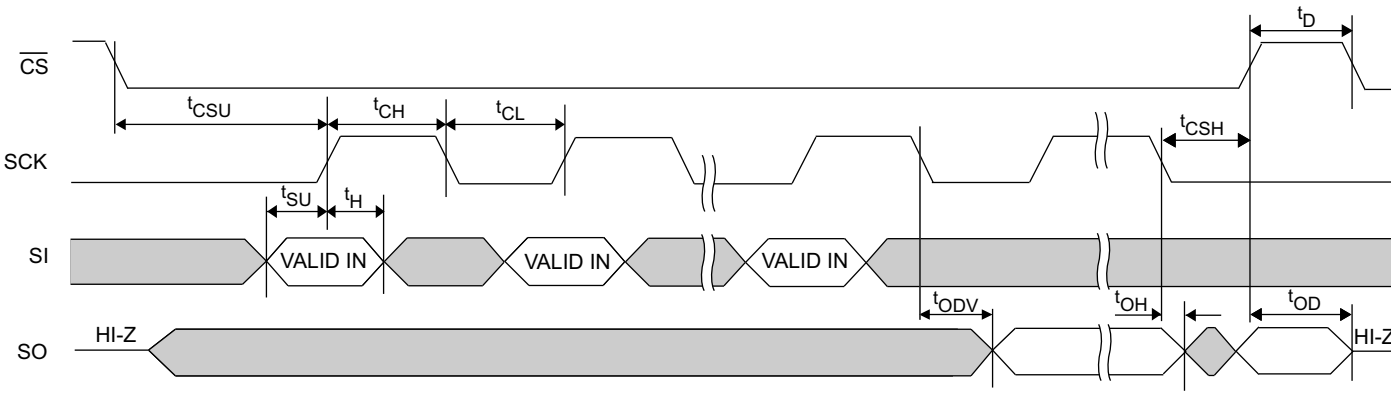
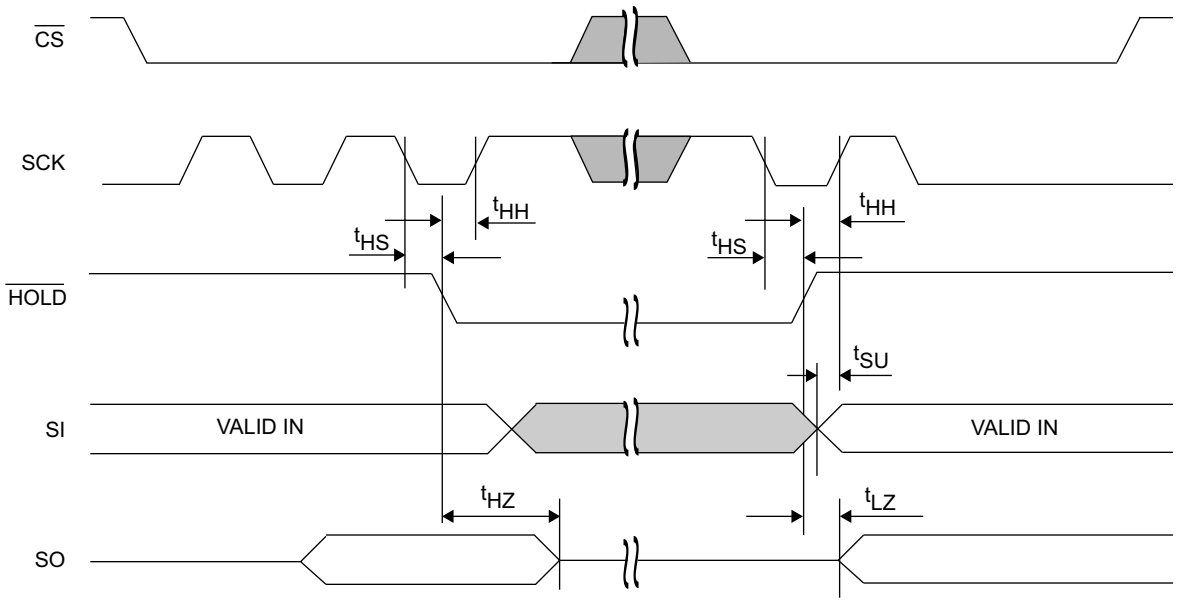


Figure 18. HOLD Timing



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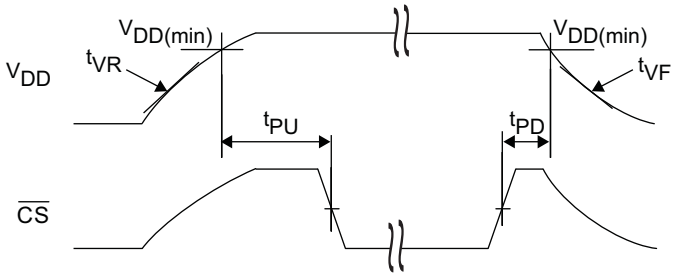
Power Cycle Timing

Over the Operating Range

Parameter	Description	Min	Max	Unit
t_{PU}	Power-up V_{DD}(min) to first access ($\overline{CS}$ LOW)	250	–	µs
t_{PD}	Last access ($\overline{CS}$ HIGH) to power-down (V_{DD}(min))	0	–	µs
t_{VR} [11, 12]	V_{DD} power-up ramp rate	50	–	µs/V
t_{VF} [11, 12]	V_{DD} power-down ramp rate	100	–	µs/V
t_{REC} [13]	Recovery time from sleep mode	–	400	µs

Figure 19. Power Cycle Timing



Notes
11. Slope measured at any point on the V_{DD} waveform.
12. This parameter is characterized and not 100% tested.
13. Guaranteed by design. Refer to Figure 15 for sleep mode recovery timing.

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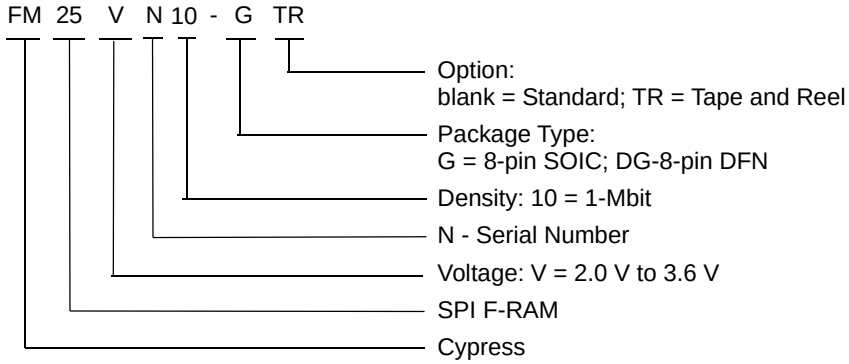
Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Range
FM25V10-G	51-85066	8-pin SOIC	Industrial
FM25V10-GTR	51-85066	8-pin SOIC	
FM25V10-DG	001-85579	8-pin DFN	
FM25V10-DGTR	001-85579	8-pin DFN	
FM25VN10-G	51-85066	8-pin SOIC, Serial Number	
FM25VN10-GTR	51-85066	8-pin SOIC, Serial Number	

All these parts are Pb-free. Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



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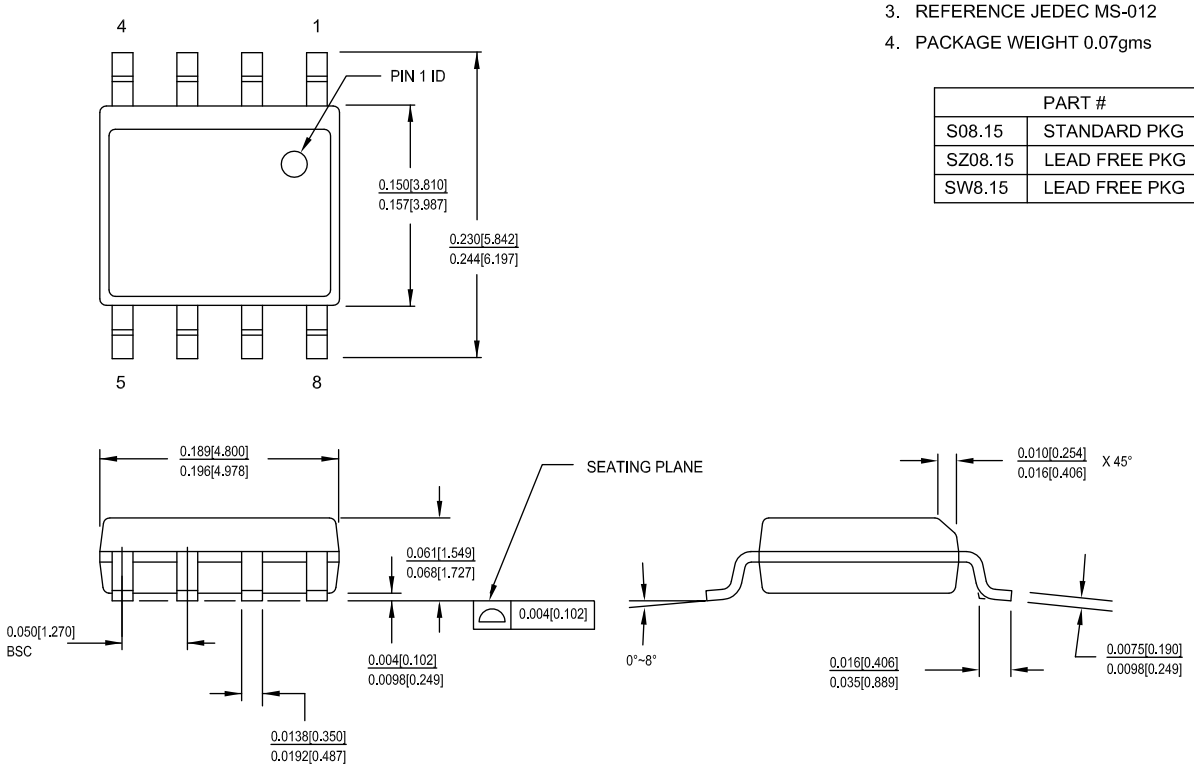
Package Diagrams

Figure 20. 8-pin SOIC (150 Mils) Package Outline, 51-85066



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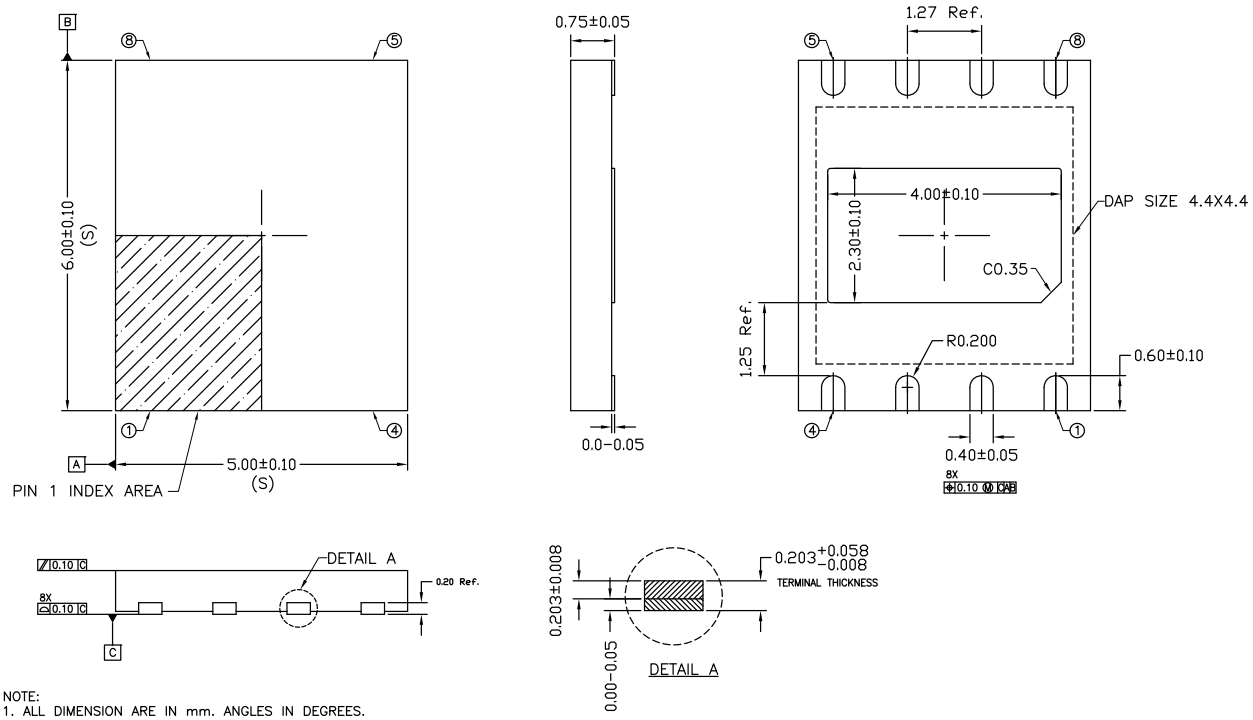
Package Diagrams (continued)

Figure 21. 8-pin DFN (5 mm × 6 mm × 0.75 mm) Package Outline, 001-85579



NOTE:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
3. WARPAGE SHALL NOT EXCEED 0.10mm.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTICS.(S)
5. REFER TO JEDEC MO-229.
6. FRAME STOCK# FL0106 (Ag Ring Plate), UTL PKG CODE TD56G008A OR TD500X600G008A OR TD500T600G008A OR TD500L600G008A OR TD500U600G008A.
7. L/F STOCK# FR0221 (Ag Ring), UTL PKG CODE TD500E600G008A OR TD500S600G008A OR TD500M600G008A OR TD500D600G008A.

001-85579 *A

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Acronyms

Acronym	Description
CPHA	Clock Phase
CPOL	Clock Polarity
DFN	Dual Flat No-lead
EEPROM	Electrically Erasable Programmable Read-Only Memory
EIA	Electronic Industries Alliance
F-RAM	Ferroelectric Random Access Memory
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
JESD	JEDEC Standards
LSB	Least Significant Bit
MSB	Most Significant Bit
RoHS	Restriction of Hazardous Substances
SPI	Serial Peripheral Interface
SOIC	Small Outline Integrated Circuit

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
kHz	kilohertz
kΩ	kilohm
Mbit	megabit
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

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Document History Page

Document Title: FM25V10, 1-Mbit (128K × 8) Serial (SPI) F-RAM Document Number: 001-84499				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3912930	GVCH	02/25/2013	New spec
*A	3994285	GVCH	05/14/2013	Added Appendix A - Errata for FM25V10 and FM25VN10
*B	4045438	GVCH	06/30/2013	Removed Errata (As all errata items are fixed).
*C	4227815	GVCH	01/24/2014	Converted to Cypress standard format Updated Maximum Ratings: - Removed Moisture Sensitivity Level (MSL) - Added junction temperature and latch up current Updated Data Retention and Endurance: Added Thermal Resistance. Removed Package Marking Scheme (top mark) Removed Ramtron revision history Completing Sunset Review.
*D	4563141	GVCH	11/06/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*E	4875900	ZSK / PSR	08/07/2015	Updated Maximum Ratings: Removed “Maximum junction temperature”. Added “Maximum accumulated storage time”. Added “Ambient temperature with power applied”. Updated Package Diagrams: spec 51-85066 – Changed revision from *F to *G. Updated to new template.
*F	5033012	GVCH	12/02/2015	Updated Status Register and Write Protection: Updated Table 3: Fixed typo error (Replaced “Bit 7” with “Bit 6” in “Bit” column). Updated Package Diagrams: spec 51-85066 – Changed revision from *G to *H.
*G	5327775	GVCH	06/28/2016	Added 8-pin DFN package related information in all instances across the document. Updated Ordering Information: Updated part numbers. Updated Package Diagrams: Added spec 001-85260 *B. Updated to new template.
*H	5420173	ZSK	08/30/2016	Updated Ordering Information: No change in part numbers. Replaced “001-85260” with “001-85579” in “Package Diagram” column. Updated Package Diagrams: Removed spec 001-85260 *B. Added spec 001-85579 *A. Updated to new template.

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Worldwide Sales and Design Support

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Lighting & Power Control	cypress.com/powerpsoc
Memory	cypress.com/memory
PSoC	cypress.com/psoc
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