ESD1LIN24 24-V, 1-Channel ESD Protection Diode

1 Features

- IEC 61000-4-2 level 4 ESD protection:
  - ±30-kV contact discharge
  - ±30-kV air-gap discharge
- Robust surge protection:
  - IEC 61000-4-5 (8/20 µs): 4.3 A
- 24-V working voltage
- Bidirectional ESD protection
- Low clamping voltage protects downstream components
- Temperature range: –55°C to +150°C
- I/O capacitance = 2.3 pF (typical)
- Offered in industry standard package: SOD-323 (DYF)
- Leaded packages used for automatic optical inspection (AOI)

2 Applications

- USB power delivery (USB-PD)
  - VBUS protection
  - IO protection
- Industrial control networks:
  - Local interconnect network (LIN)
  - Single line CAN ESD protection
  - DeviceNet
  - Smart distribution systems

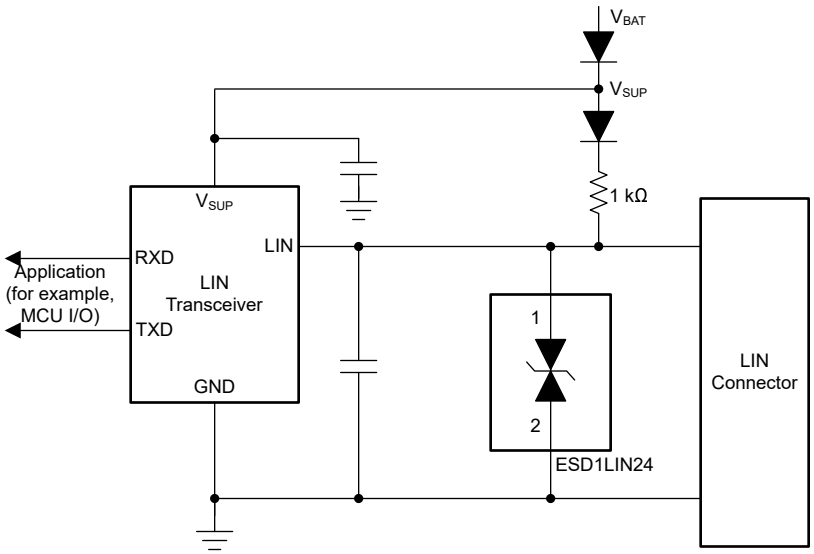
3 Description

The ESD1LIN24 is a single-channel low capacitance bidirectional ESD protection device for local interconnect network (LIN). This device is rated to dissipate contact ESD strikes beyond the maximum level specified in the IEC 61000-4-2 international standard (±30-kV Contact, ±30-kV Airgap). The low dynamic resistance and low clamping voltage help protect systems against transient events. This protection is key in safety systems that require a high level of robustness and reliability.

Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ESD1LIN24	DYF (SOD-323, 2)	2.50 mm × 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2022) to Revision A (December 2022)	Page
• Changed the status of the data sheet from: *Advanced Information* to: *Production Data*	1

5 Pin Configuration and Functions

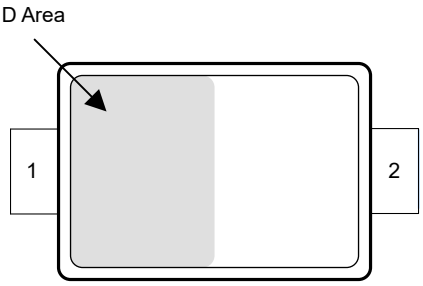


Figure 5-1. DYF Package, 2-Pin SOD-323 (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IO	1	I/O	ESD protected IO
GND	2	G	Connect to ground.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Peak pulse	IEC 61000-4-5 Power (t_p - 8/20 µs) at 25°C		159.1	W
	IEC 61000-4-5 current (t_p - 8/20 µs) at 25°C		4.3	A
T_A	Operating free-air temperature	-55	150	°C
T_{stg}	Storage temperature	-65	155	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings—JEDEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	± 2500	V
		Charged device model (CDM), per JEDEC specification JS-002(2)	± 1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000	V
		IEC 61000-4-2 Air-gap Discharge, all pins	±30000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	-24		24	V
T_A	Operating free-air temperature	-55		150	°C

6.5 Thermal Information

THERMAL METRIC(1)		ESD1LIN24 DYF (SOD-323) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	705.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	315	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	561.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	145	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	550.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Electrical Characteristics

over T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage		–24		24	V
V_{BRF}	Breakdown voltage(1)	I_{IO} = 10 mA	25.5		35.5	V
V_{BRR}		I_{IO} = –10 mA	–35.5		–25.5	
V_{CLAMP}	Clamping voltage(2)	I_{PP} = 4.3 A, t_p = 8/20 µs, from IO to GND		37	42	V
	Clamping voltage(3)	I_{PP} = 16 A, TLP, from IO to GND		40		
I_{LEAK}	Leakage current, any IO pin to GND	V_{IO} = ±24 V	-50	1	50	nA
R_{DYN}	Dynamic resistance(3)			0.5		Ω
C_L	Line capacitance, any IO to GND	V_{IO} = 0 V, f = 1 MHz, V_{p-p} = 30 mV		2.3	3.8	pF

(1) V_{BRF} and V_{BRR} are defined as the voltage when ±10 mA is applied in the positive-going direction, before the device latches into the snapback state.
(2) Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
(3) Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

7 Typical Characteristics – ESD1LIN24

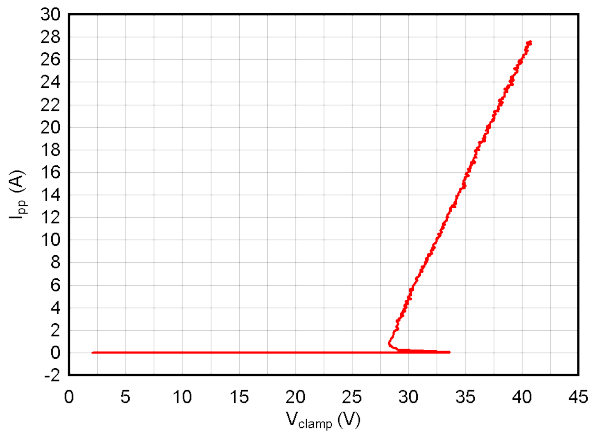


Figure 7-1. Positive TLP Curve

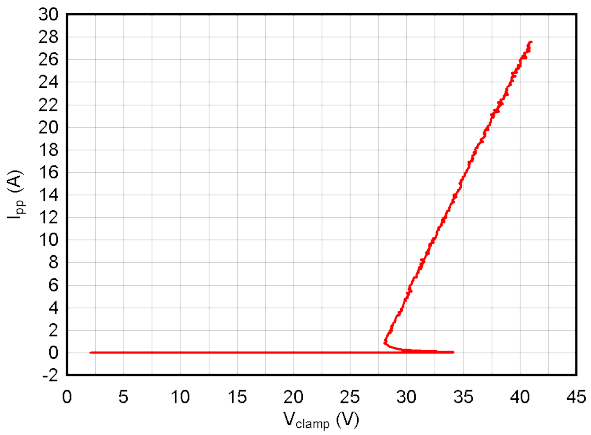


Figure 7-2. Negative TLP Curve

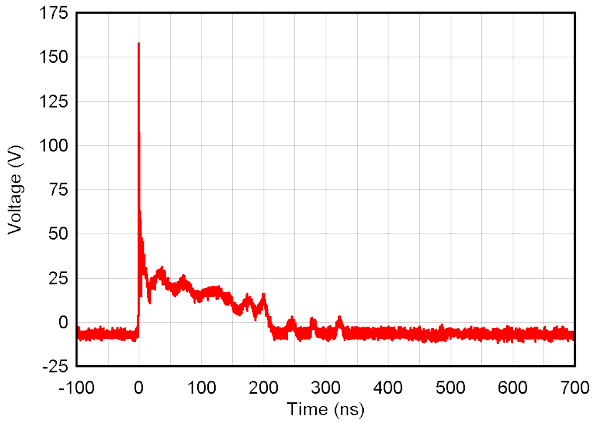


Figure 7-3. +8-kV Clamped IEC Waveform

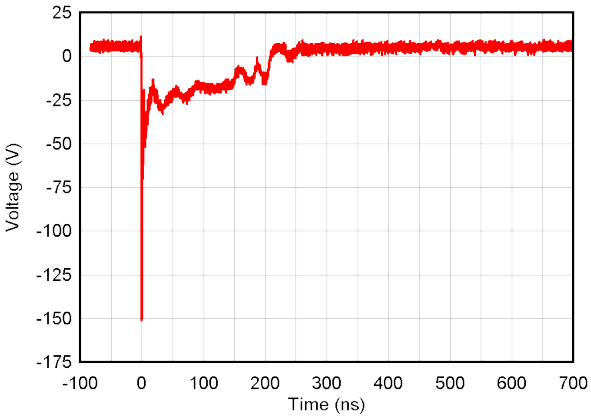


Figure 7-4. −8-kV Clamped IEC Waveform

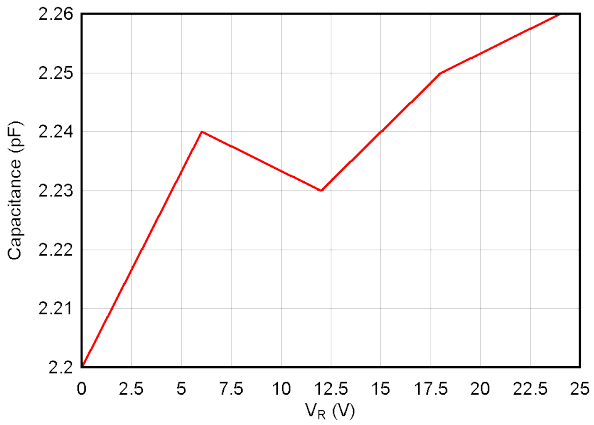


Figure 7-5. Capacitance vs. Bias Voltage

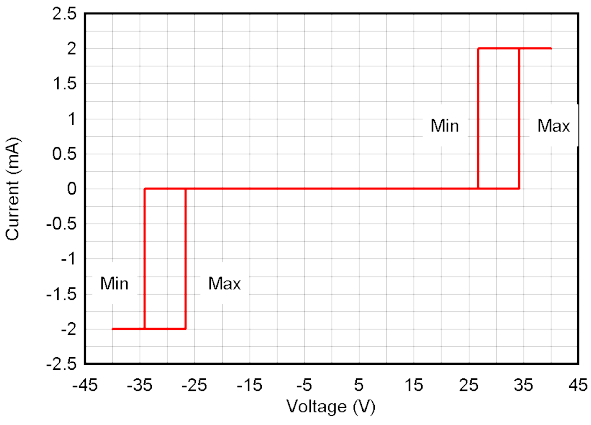


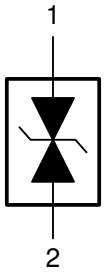
Figure 7-6. DC Voltage Sweep I-V Curve

8 Detailed Description

8.1 Overview

The ESD1LIN24 is a single-channel bidirectional ESD diode. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 standard. The low capacitance between the I/O pins make this device suitable for slower speed signals such as LIN, USB-PD, or industrial I/O applications. The surge current capability is suitable for VBUS protection or industrial I/Os requiring 4.3 A of surge current protection.

8.2 Functional Block Diagram



8.3 Feature Description

This clamping device has a small dynamic resistance, which makes the clamping voltage low when the device is actively protecting other circuits. The breakdown is bidirectional so these protection devices are a good fit for applications requiring postive and negative polarity protection. Low leakage allows the diode to conserve power when working below the V_{RWM}. The temperature range of −55°C to +150°C makes this device work at extensive temperatures in most environments. The leaded SOD-323 package is good for applications requiring autmotic optical inspection (AOI).

8.3.1 IO Capacitance

The capacitance between the I/O pins is 2.3 pF. The capacitance of this device can support data rates up to 1 Gbps.

8.3.2 IEC 61000-4-5 Surge Protection

The I/O pins of this device have a surge rating of 4.3 A (8/20 µs waveform).

8.4 Device Functional Modes

The ESD1LIN24 is a single channel passive clamp that has low leakage during normal operation when the voltage between I/O and GND is below V_{RWM}, and activate when the voltage between I/O and GND goes above V_{BR}. During ESD events, transient voltages up to ±30 kV can be clamped on either channel. When the voltages on the protected lines fall below the V_{HOLD}, the device reverts back to the low leakage passive state.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The ESD1LIN24 is a single channel TVS diode which is used to provide a path to ground for dissipating ESD events on USB-PD or industrial I/O lines. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

9.2 Typical Application

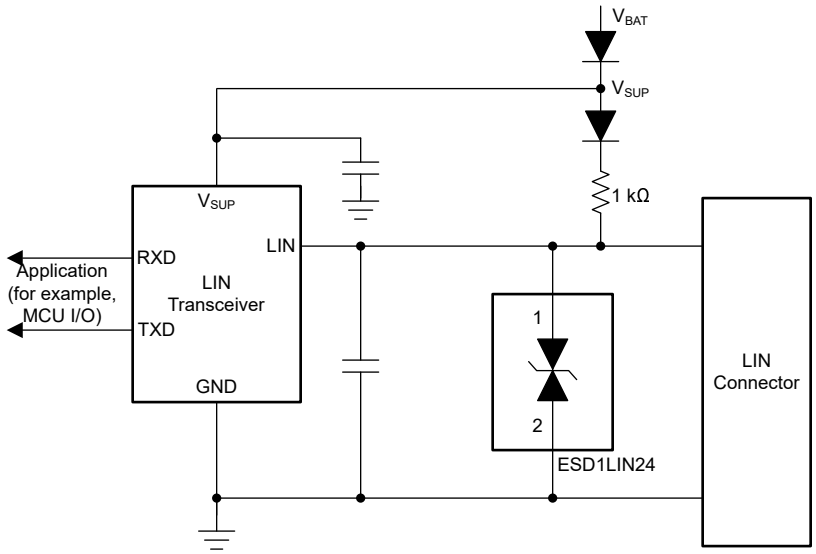


Figure 9-1. Typical Application

9.2.1 Design Requirements

For this design example, the ESD1LIN24 is used to provide ESD protection to a LIN transceiver. Table 9-1 lists the known design paramters for this application.

Table 9-1. Design Parameters for Typical Applications

Design Parameter	Value
Diode configuration	Bidirectional
V_{IO} signal range	Up to 18 V
V_{RWM}	±24 V
Jumpstart short to battery event on V_{IO}	±24 V
Data rate	Up to 10 Mbps
Pullup resistor	1 kΩ

9.2.2 Detailed Design Procedure

The ESD1LIN24 has a V_{RWM} of ±24 V to prevent the diode from being damaged during a short event. The bidirectional characteristic ensures both positive and negative polarity are protected. The low capacitance of 2.3 pF permits data rates up to 1 Gbps, which allows the designer to meet the requirements for LIN. The 1 kΩ and V_{SUP} diode allows the LIN signal to be pulled up to a diode drop below the battery voltage.

9.2.3 Application Curves

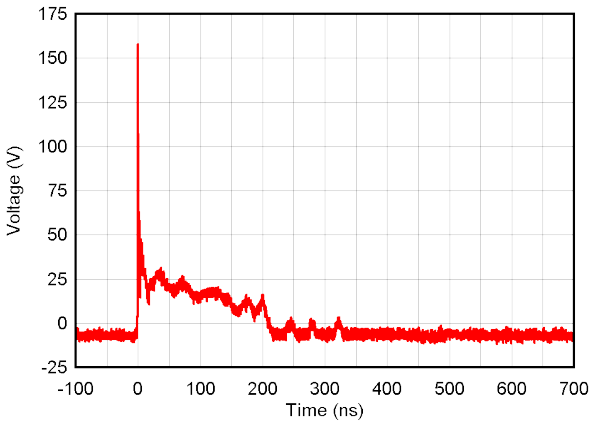


Figure 9-2. +8-kV Clamped IEC Waveform

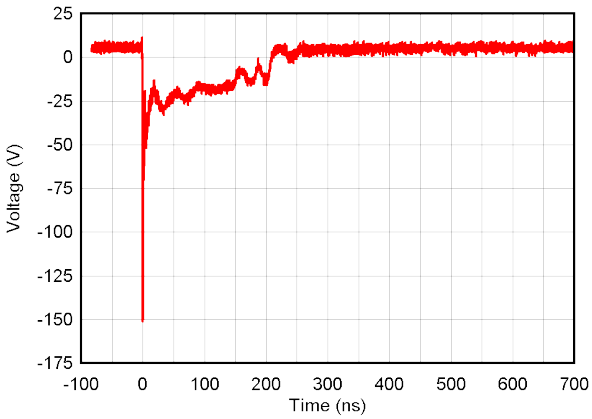


Figure 9-3. -8-kV Clamped IEC Waveform

10 Power Supply Recommendations

These devices are passive TVS diode-based ESD protection devices, therefore there is no requirement to power them. Ensure that the maximum voltage specifications for each pin is not violated.

11 Layout

11.1 Layout Guidelines

- The optimum placement of the device is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 1 or 2 is connected to ground, use a thick and short trace for this return path.

11.2 Layout Example

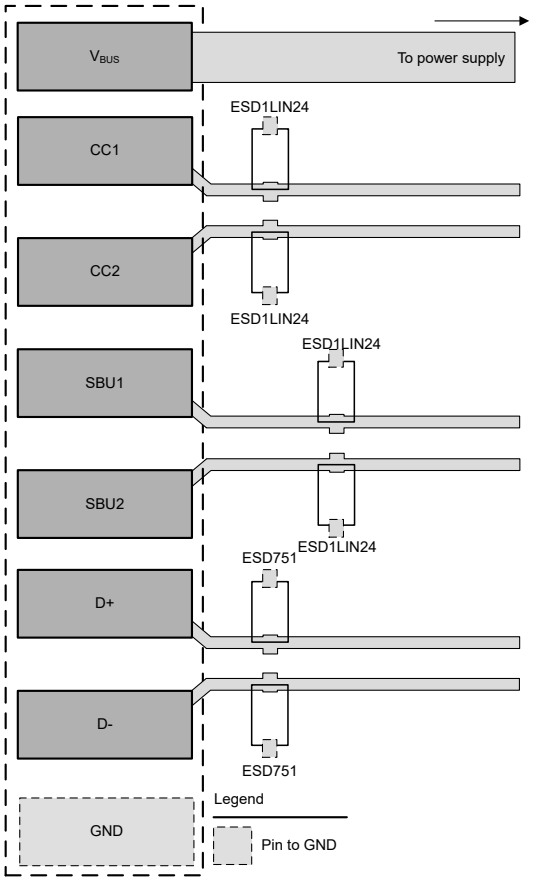


Figure 11-1. Layout Recommendation

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Layout Guide* application reports
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Picking ESD Diodes for Ultra High-Speed Data Lines* application reports
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESD1LIN24DYFR	Active	Production	SOT (DYF) | 2	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-50 to 150	2QJF

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF ESD1LIN24 :

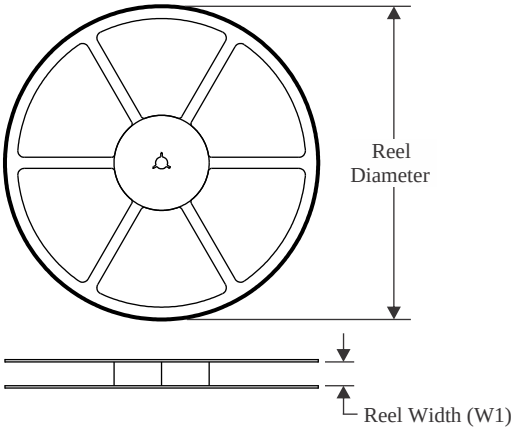
- Automotive : ESD1LIN24-Q1

NOTE: Qualified Version Definitions:

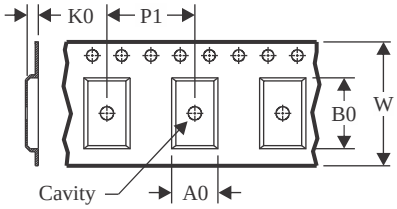
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

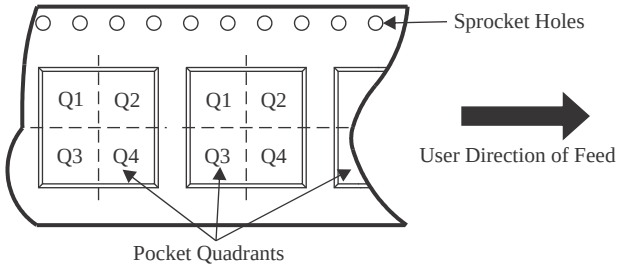


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

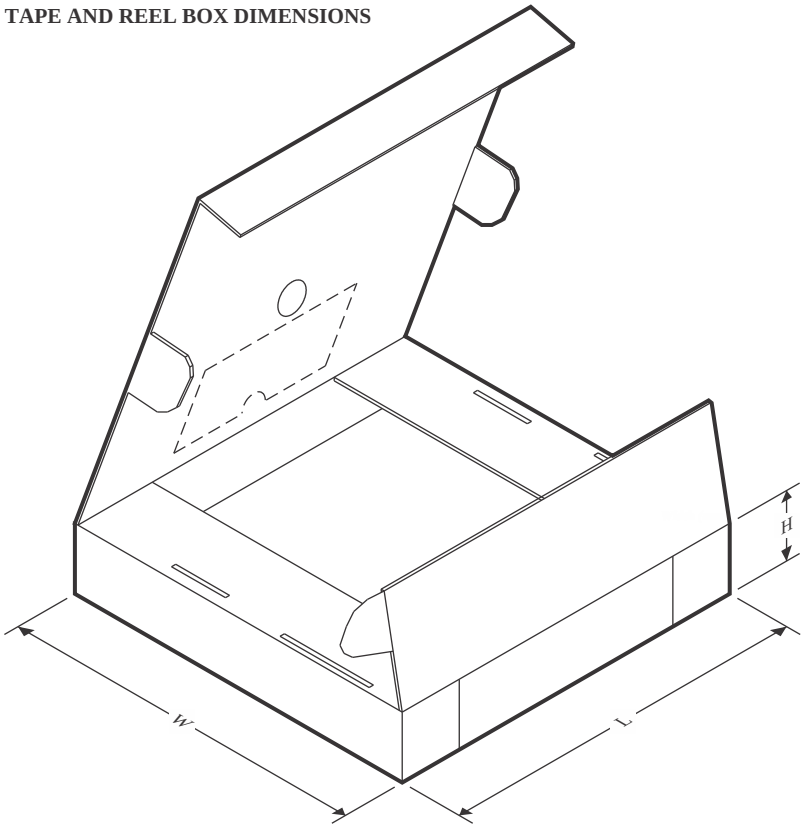
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD1LIN24DYFR	SOT	DYF	2	3000	178.0	9.5	1.48	3.3	1.25	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

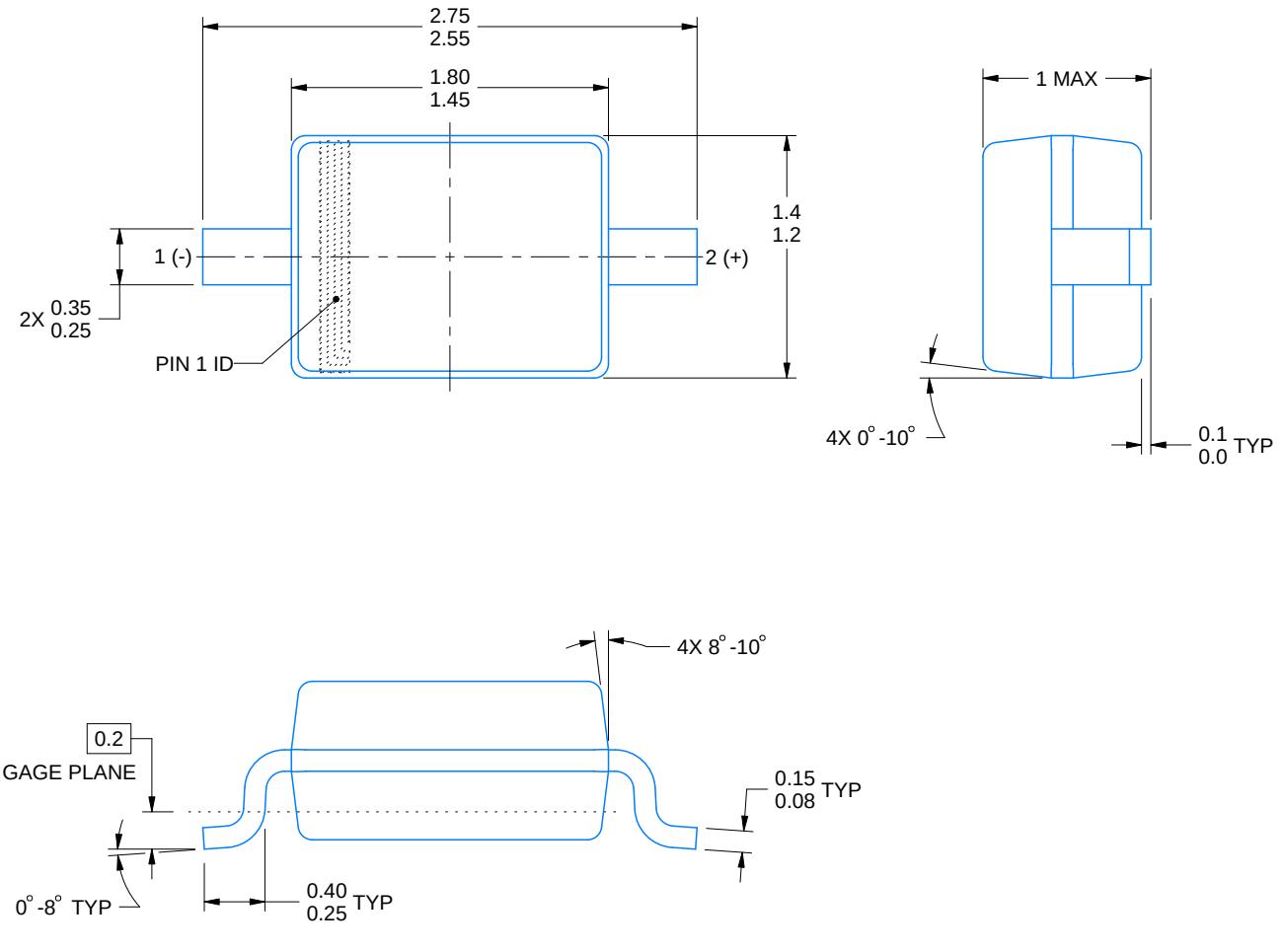
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD1LIN24DYFR	SOT	DYF	2	3000	210.0	200.0	42.0

PACKAGE OUTLINE

DYF0002A

SOT(SOD-323) - 1 mm max height

SMALL OUTLINE TRANSISTOR



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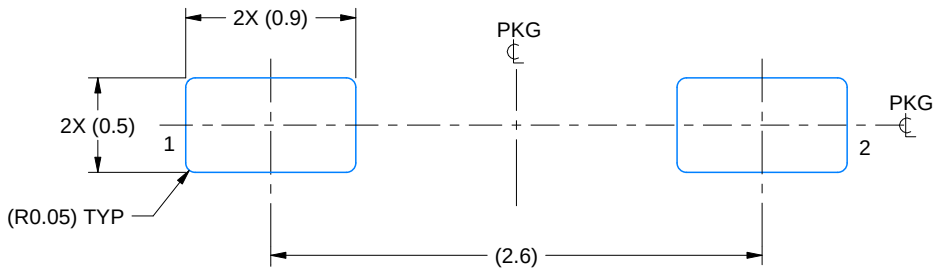
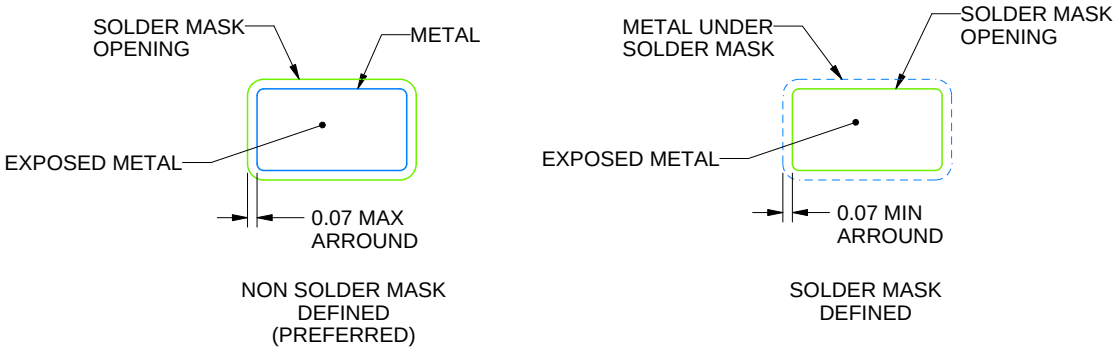
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS

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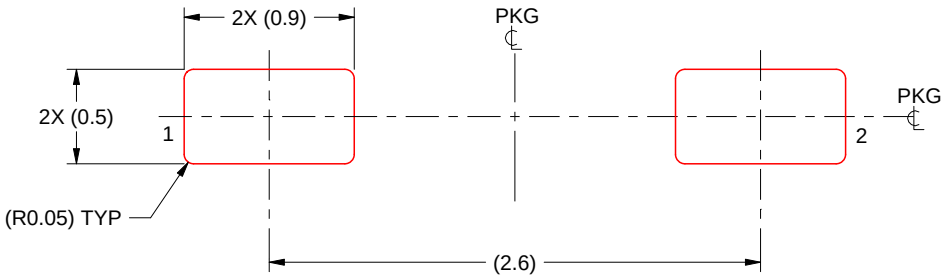
NOTES: (continued)

3. Publication IPC-7351 may have alternate designs.
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:25X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
6. Board assembly site may have different recommendations for stencil design.

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