

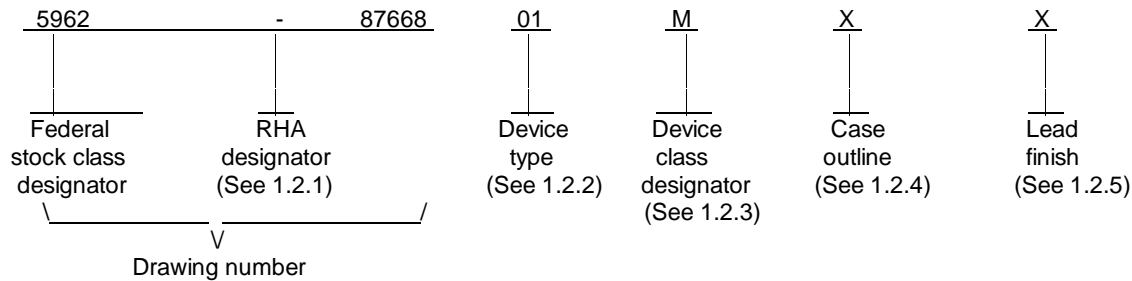
REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change C _{IN} and C _{OUT} limits. Add ac test points to figure 4. Editorial changes throughout.	1988 SEP 29	Monica Poelking
B	Table I, ac test limits corrected. Table II, subgroup 4 added to group A inspection. Added device type 03 and 04. Added case outline Y. Editorial changes throughout.	1989 SEP 14	Monica Poelking
C	Technical changes to absolute maximum ratings. Technical changes to table I. Clarifications and corrections on figure 1, figure 2, and figure 4. Editorial changes throughout.	91-09-24	Monica Poelking

REV																											
SHEET																											
REV	C	C	C	C	C	C	C	C	C	C	C																
SHEET	15	16	17	18	19	20	21	22	23	24	25																
REV STATUS OF SHEETS				REV			C	C	C	C	C	C	C	C	C	C	C	C	C	C							
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14							
PMIC N/A				PREPARED BY TIM H. NOH								DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444															
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A				CHECKED BY TIM H. NOH																							
				APPROVED BY MONICA POELKING																							
				DRAWING APPROVAL DATE 87-08-14																							
				REVISION LEVEL C																							
				SIZE A				CAGE CODE 67268				5962-87668															
				SHEET 1 OF 25																							

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>	<u>Frequency</u>
01	80386-16	32-bit microprocessor	16 MHz
02	80386-12	32-bit microprocessor	12.5 MHz
03	80386-20	32-bit microprocessor	20 MHz
04	80386-25	32-bit microprocessor	25 MHz

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

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1.2.4 Case outline(s). For device classes M, B, and S, case outline(s) shall meet the requirements in appendix C of MIL-M-38510 and as listed below. For device classes Q and V, case outline(s) shall meet the requirements of MIL-I-38535, appendix C of MIL-M-38510, and as listed below.

Outline letter

Case outline

X	P-AF (132-terminal, 1.480" x 1.480" x .345"), pin grid array
Y	See figure 1 (164-terminal, 1.140" x 1.140" x .115"), leaded chip carrier with unformed leads

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Storage temperature range -65° C to +150° C
Supply voltage with respect to ground -0.5 V dc to +6.5 V dc
Voltage on other pins -0.5 V dc to V_{CC} +0.5 V dc
Lead temperature (soldering, 10 seconds) +275° C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case X See MIL-M-38510, appendix C
Case Y 4° C/W
Junction temperature (T_J) +130° C
Maximum power dissipation (P_D) 3.6 W

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) 5.0 V dc \pm 5 percent
Minimum high level input voltage (V_{IH}):	
Logic inputs 2.0 V dc to V_{CC} +0.3 V dc
Clock input V_{CC} -0.8 V dc to V_{CC} +0.3 V dc
Maximum low level input voltage (V_{IL}) -0.3 V dc to 0.8 V dc
Frequency of operation:	
Device 01 16 MHz
Device 02 12.5 MHz
Device 03 20 MHz
Device 04 25 MHz
Case operating temperature range (T_C) -55° C to +125° C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing	
logic tests (MIL-STD-883, test method 5012)	.. 98.4 percent

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2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

- MIL-M-38510 - Microcircuits, General Specification for.
- MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

- MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
- MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

- MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

- MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

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3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-ECC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

3.12 PIN supersession information. The PIN supersession information shall be as specified in the appendix.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

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4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

(2) $T_A = +125^\circ\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IO} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of five devices with zero rejects shall be required.

d. For device class M, subgroups 7 and 8 tests shall include verification of the device functionality. These tests shall be maintained and available from the approved source of supply upon request. For device classes B and S, subgroups 7 and 8 tests shall include verification of the device functionality. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $\frac{1}{4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}}$ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ unless otherwise specified	Group A Subgroups	Device types	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}		1, 2, 3	All	-0.3 <u>2/</u>	0.8	V
Input high voltage	V_{IH}		1, 2, 3	All	2.0	$V_{CC} + 0.3$ <u>2/</u>	
CLK2 input low voltage	V_{ILC}		1, 2, 3	All	-0.3 <u>2/</u>	0.8	
CLK2 input high voltage	V_{IHC}		1, 2, 3	All	$V_{CC} - 0.8$	$V_{CC} + 0.3$ <u>2/</u>	
Output low voltage	V_{OL}	$I_{OL} = 4\text{ mA}$; A2-A31, D0-D31 $I_{OL} = 5\text{ mA}$; BEO-BE3, W/ R, D/C, M/IO, LOCK, ADS, HLDA	1, 2, 3	All		0.45 0.45	
Output high voltage	V_{OH}	$I_{OH} = -1\text{ mA}$; A2-A31, D0-D31	1, 2, 3	All	2.4		uA
		$I_{OH} = -9\text{ mA}$; BEO-BE3, W/R, D/C, M/IO, LOCK, ADS, HLDA			2.4		
Input leakage current (for all pins except BS16, PEREQ, BUSY, and ERROR)	I_{LI}	$0\text{ V} < V_{IN} < V_{CC}$	1, 2, 3	All	-15	+15	
Input leakage current (PEREQ pin)	I_{IH}	$V_{IH} = 2.4\text{ V}$	1, 2, 3	All		200	
Input leakage current (BS16, BUSY, and ERROR pins)	I_{IL}	$V_{IL} = 0.45\text{ V}$	1, 2, 3	All		-400	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 4.75 V ≤ V _{CC} ≤ 5.25 V -55° C ≤ T _C ≤ +125° C unless otherwise specified	Group A Subgroups	Device types	Limits		Unit
					Min	Max	
Output Leakage current	I _{LO}	0.45 V ≤ V _{OUT} ≤ V _{CC}	1, 2, 3	All	-15	+15	uA
Supply current	I _{CC}	CLK2 = 32 MHz	1, 2, 3	01		450	mA
		CLK2 = 25 MHz		02		400	
		CLK2 = 40 MHz		03		550	
		CLK2 = 50 MHz		04		680	
Input capacitance	C _{IN}	Fc = 1 Mhz, see 4.4.1c	4	All		20	pF
Output or I/O capacitance	C _{OUT}		4	All		25	
CLK2 capacitance	C _{CLK}		4	All		20	
Functional tests		V _{CC} = 4.75 V, 5.25 V, see 4.4.1d	7, 8	All			
Operating frequency		Half of CLK2 frequency		01	4	16	MH z
				02		12.5	
				03		20	
				04		25	
CLK2 period	t ₁	See figure 4	9,10,11	01	30	125	ns
				02	40		
				03	25		
				04	20		
CLK2 high time	t _{2a}	At 2V See figure 4	9,10,11	01	9		
				02	11		
				03	8		
				04	7		

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 4.75 V ≤ V _{CC} ≤ 5.25 V -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A Subgroups	Device types	Limits		Unit
					Min	Max	
CLK2 high time 2/	t _{2b}	At (V _{CC} -0.8 V) See figure 4	9, 10, 11	01	5		ns
				02	7		
				03	5		
				04	4		
CLK2 low time	t _{3a}	At 2 V See figure 4	9, 10, 11	01	9		
				02	11		
				03	8		
				04	7		
CLK2 low time 2/	t _{3b}	At 0.8 V See figure 4	9, 10, 11	01	7		
				02	9		
				03	6		
				04	5		
CLK2 fall time 2/	t ₄	(V _{CC} = -0.8 V) to 0.8 V See figure 4	9, 10, 11	01, 02, 03		8	
				04		7	
CLK2 rise time 2/	t ₅	0.8 V to (V _{CC} = -0.8 V) See figure 4	9, 10, 11	01, 02, 03		8	
				04		7	
A2-A31 valid delay 3/	t ₆	C _L = 120 pF See figure 4	9,10,11	01	4	36	
				02	2	44	
				03	4	27	
				04	4	20	
A2-A31 float delay 2/ 4/	t ₇	See figure 4	9,10,11	01	4	40	
				02	1	45	
				03	4	32	
				04	4	30	

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions ^{1/} 4.75 V \leq V _{CC} \leq 5.25 V -55°C \leq T _C \leq +125°C unless otherwise specified	Group A Subgroups	Device types	Limits		Unit
					Min	Max	
BEO-BE3, LOCK, valid delay _{3/}	t ₈	C _L = 75 pF See figure 4	9, 10, 11	01	4	36	ns
				02	2	44	
				03	4	27	
				04	4	24	
BEO-BE3, LOCK, ADS float delay _{2/ 4/}	t ₉	See figure 4	9, 10, 11	01	4	40	
				02	1	45	
				03	4	32	
				04	4	30	
W/ R, D/C, M/ IO, ADS valid delay _{3/}	t ₁₀	C _L = 75 pF See figure 4	9, 10, 11	01	6	33	
				02	5	39	
				03	6	28	
				04	4	19	
W/ R, D/C, M/ IO, float delay _{2/ 4/}	t ₁₁	See figure 4	9, 10, 11	01	6	35	
				02	4	40	
				03	6	30	
				04	4	30	
D0-D31 write data valid delay _{3/}	t ₁₂	C _L = 120 pF See figure 4	9,10,11	01	4	48	
				02	2	54	
				03	6	38	
				04	8	27	
D0-D31 write data float delay _{2/ 4/}	t ₁₃	See figure 4	9,10,11	01	4	35	
				02	1	44	
				03	4	27	
				04	4	22	

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}$ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ unless otherwise specified	Group A Subgroups	Device types	Limits		Unit
					Min	Max	
HLDA valid delay 3/	t_{14}	$C_L = 75\text{ pF}$ See figure 4	9, 10, 11	01	6	33	ns
				02	3	39	
				03	6	28	
				04	4	22	
NA setup time	t_{15}	See figure 4	9, 10, 11	01	11		
				02	15		
				03	9		
				04	7		
NA hold time	t_{16}		9, 10, 11	01	14		
				02	23		
				03	14		
				04	3		
BS16 setup time	t_{17}		9, 10, 11	01	13		
				02	13		
				03	13		
				04	7		
BS16 hold time	t_{18}		9,10,11	01	21		
				02	23		
				03	21		
				04	3		
READY setup time	t_{19}		9,10,11	01	21		
				02	23		
				03	12		
				04	8		

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 4.75 V ≤ V _{CC} ≤ 5.25 V -55° C ≤ T _C ≤ +125° C unless otherwise specified	Group A Subgroups	Device types	Limits		Unit
					Min	Max	
READY hold time	t ₂₀	C _L = 75 pF See figure 4	9, 10, 11	01	4		ns
				02	6		
				03	4		
				04	4		
D0-D31 read setup time	t ₂₁	See figure 4	9, 10, 11	01	11		
				02	13		
				03	11		
				04	6		
D0-D31 read hold time	t ₂₂		9, 10, 11	01	6		
				02	8		
				03	6		
				04	5		
HOLD setup time	t ₂₃		9, 10, 11	01	26		
				02	28		
				03	17		
				04	15		
HOLD hold time	t ₂₄		9,10,11	01	5		
				02	6		
				03	5		
				04	3		
RESET setup time	t ₂₅		9,10,11	01	13		
				02	16		
				03	12		
				04	10		

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions ^{1/} $4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}$ $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ unless otherwise specified	Group A Subgroups	Device types	Limits		Unit
					Min	Max	
RESET hold time ^{2/}	t_{26}	See figure 4	9, 10, 11	01, 02, 03	4		ns
				04	3		
NMI, INTR setup time ^{5/}	t_{27}		9, 10, 11	01	16		
				02	19		
				03	16		
				04	6		
NMI, INTR hold time time ^{5/}	t_{28}		9, 10, 11	01	16		
				02	19		
				03	16		
				04	6		
PEREQ, BUSY, ERROR setup time ^{5/}	t_{29}		9, 10, 11	01	16		
				02	19		
				03	14		
				04	6		
PEREQ, BUSY, ERROR hold time ^{5/}	t_{30}		9,10,11	All	5		

^{1/} All tests shall be performed using the worst case conditions, unless otherwise specified.

^{2/} Guaranteed if not tested to the limits specified.

^{3/} For 25 MHz, $C_L = 50\text{ pF}$.

^{4/} Float condition occurs when maximum output current becomes less than I_{LO} in magnitude.

^{5/} These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes to assure recognition within a specific CLK2 period.

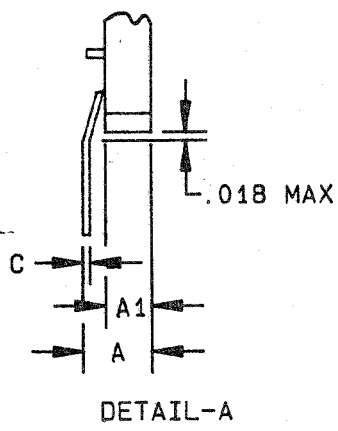
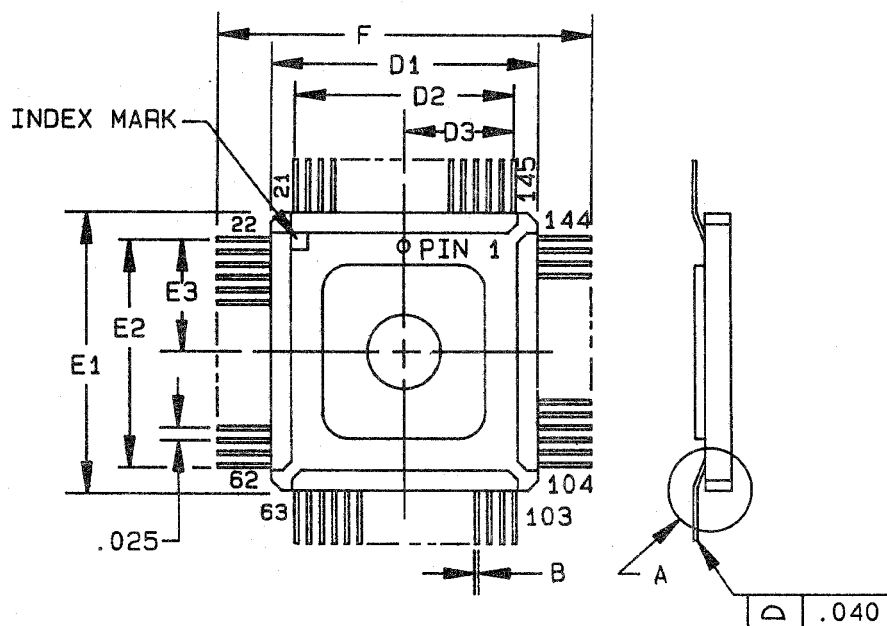
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Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.086	.115	2.18	2.92
A1	.078	.094	1.98	2.39
B	.007	.010	0.18	0.25
C	.004	.006	0.10	0.15
D1, E1	1.120	1.140	28.45	28.96
D2, E2	1.000 BSC		28.40 BSC	
D3, E3	.500 BSC		12.70 BSC	
F	2.470	2.530	62.74	64.26

NOTES:

1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Symbols B and C dimensions shall be increased by .002 inch (0.05 mm) when soldering coat is added.

FIGURE 1. Case outline Y.

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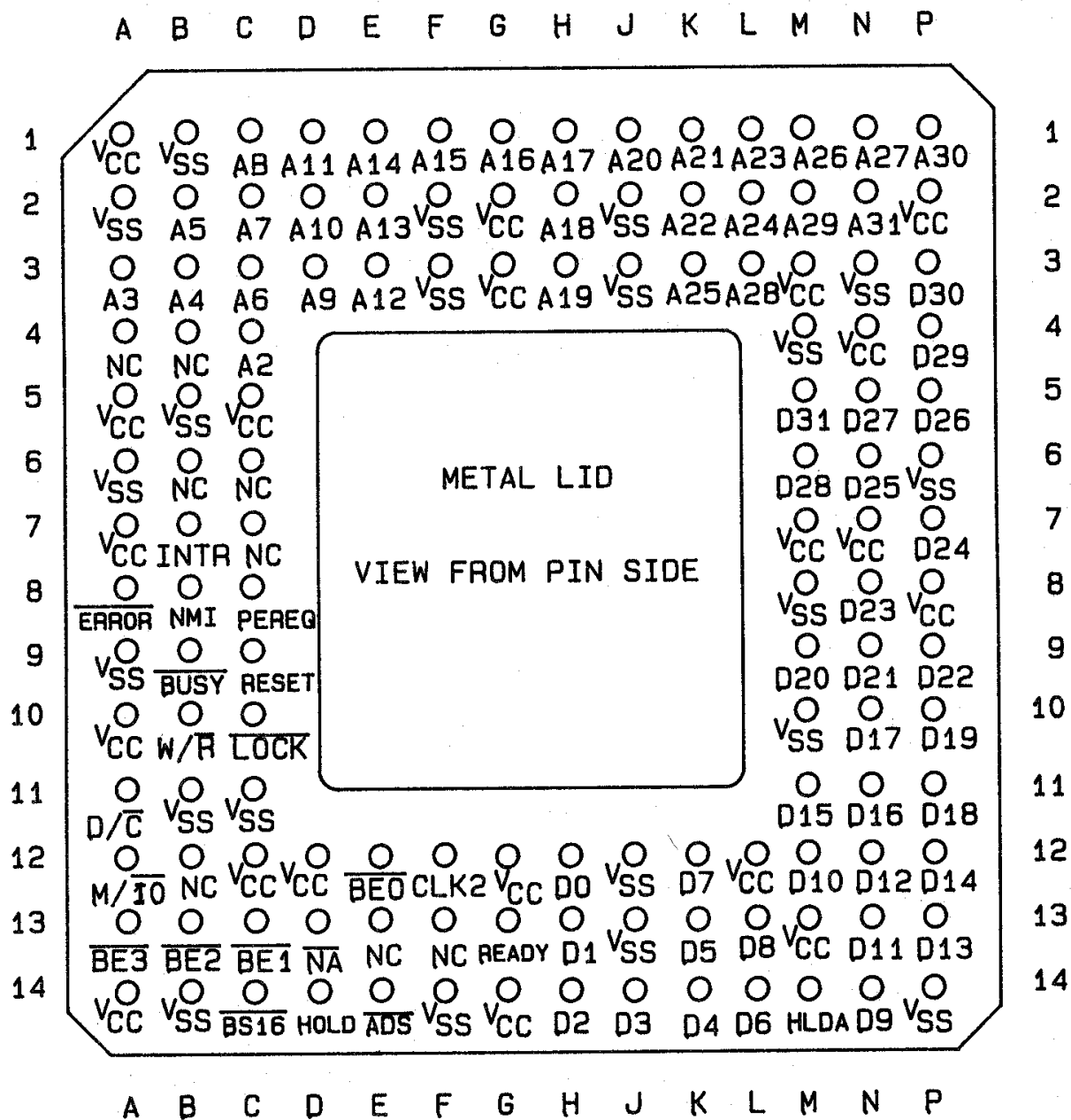


FIGURE 2. Terminal connections.

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Device types	All	Device types	All	Device types	All	Device types	All
Case outline	Y	Case outline	Y	Case outline	Y	Case outline	Y
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
01	A16	42	PEREQ	83	READY	124	D19
02	A17	43	V _{SS}	84	NC	125	NC
03	A15	44	V _{CC}	85	D1	126	NC
04	A14	45	ERROR	86	NC	127	D24
05	A13	46	RESET	87	D2	128	D21
06	A12	47	NC	88	NC	129	NC
07	A11	48	NC	89	D4	130	NC
08	NC	49	BUSY	90	D0	131	D25
09	A9	50	V _{CC}	91	V _{CC}	132	D23
10	A10	51	V _{SS}	92	V _{SS}	133	NC
11	V _{SS}	52	V _{CC}	93	D6	134	NC
12	A7	53	V _{SS}	94	D3	135	D27
13	A8	54	V _{CC}	95	V _{SS}	136	D26
14	V _{CC}	55	V _{SS}	96	V _{CC}	137	V _{CC}
15	V _{SS}	56	V _{CC}	97	D8	138	V _{SS}
16	A5	57	V _{SS}	98	D5	139	D29
17	A6	58	V _{CC}	99	V _{CC}	140	D28
18	NC	59	LOCK	100	V _{SS}	141	V _{CC}
19	NC	60	W/R	101	HLDA	142	V _{SS}
20	A3	61	V _{SS}	102	D7	143	D31
21	A4	62	V _{CC}	103	NC	144	D30
22	NC	63	M/I/O	104	D10	145	NC
23	NC	64	D/C	105	D9	146	A31
24	A2	65	NC	106	NC	147	A30
25	NC	66	NC	107	NC	148	A29
26	V _{CC}	67	BE2	108	D12	149	A28
27	V _{SS}	68	NC	109	D11	150	V _{CC}
28	NC	69	V _{CC}	110	V _{CC}	151	V _{SS}
29	NC	70	V _{SS}	111	V _{SS}	152	A27
30	NC	71	BE0	112	D14	153	A26
31	V _{CC}	72	BE3	113	D13	154	A25
32	V _{SS}	73	NC	114	NC	155	NC
33	NC	74	BE1	115	D15	156	A23
34	V _{CC}	75	NA	116	D16	157	A24
35	V _{SS}	76	NC	117	V _{CC}	158	A21
36	NC	77	NC	118	V _{SS}	159	A22
37	INTR	78	BS16	119	D18	160	NC
38	NC	79	HOLD	120	D17	161	A20
39	NC	80	CLK2	121	D20	162	A19
40	NC	81	ADS	122	V _{SS}	163	A18
41	NMI	82	NC	123	D22	164	NC

FIGURE 2. Terminal connections - Continued.

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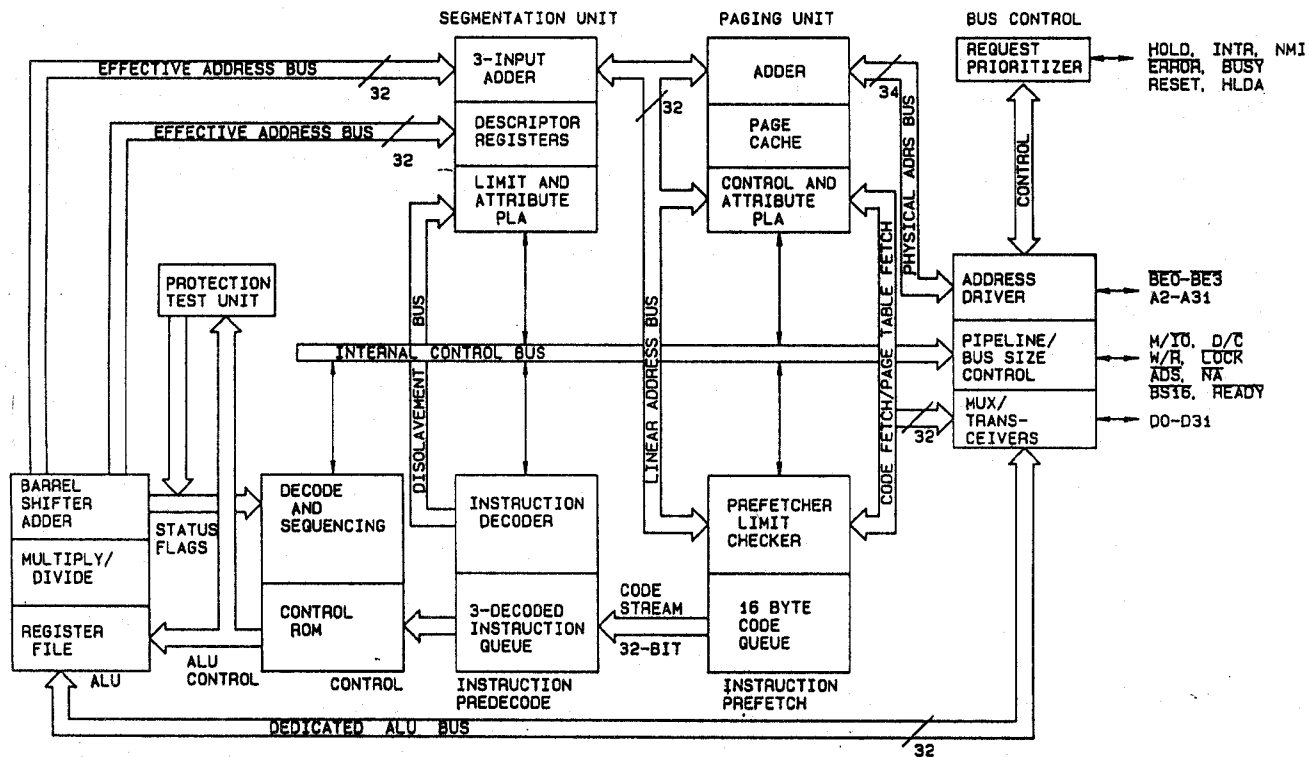


FIGURE 3. Block diagram.

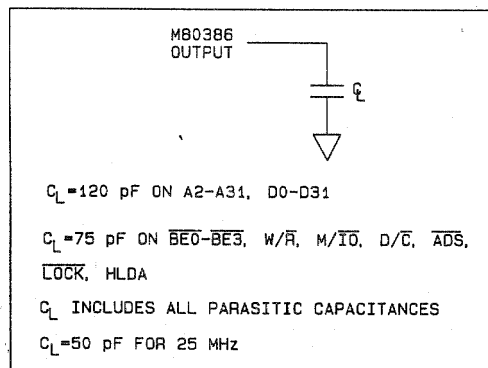
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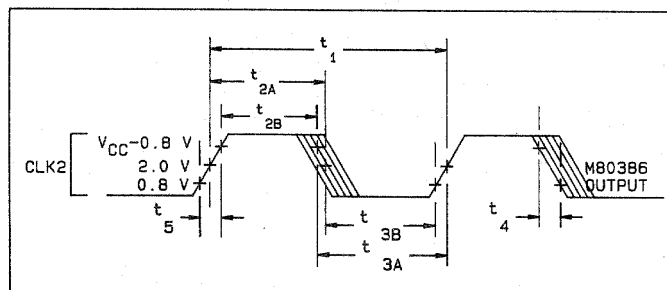
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AC TIMING WAVEFORMS



CLK2 TIMING

FIGURE 4. Test circuit and switching waveforms.

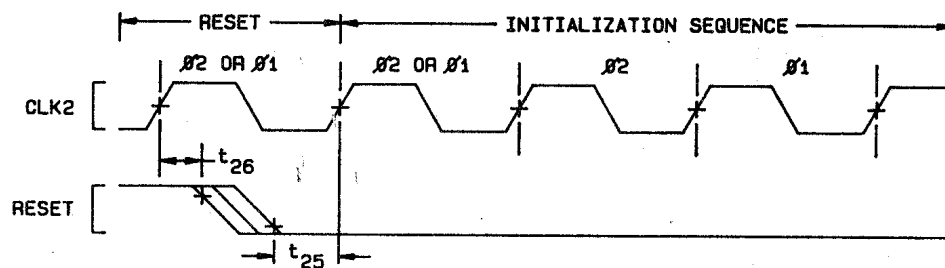
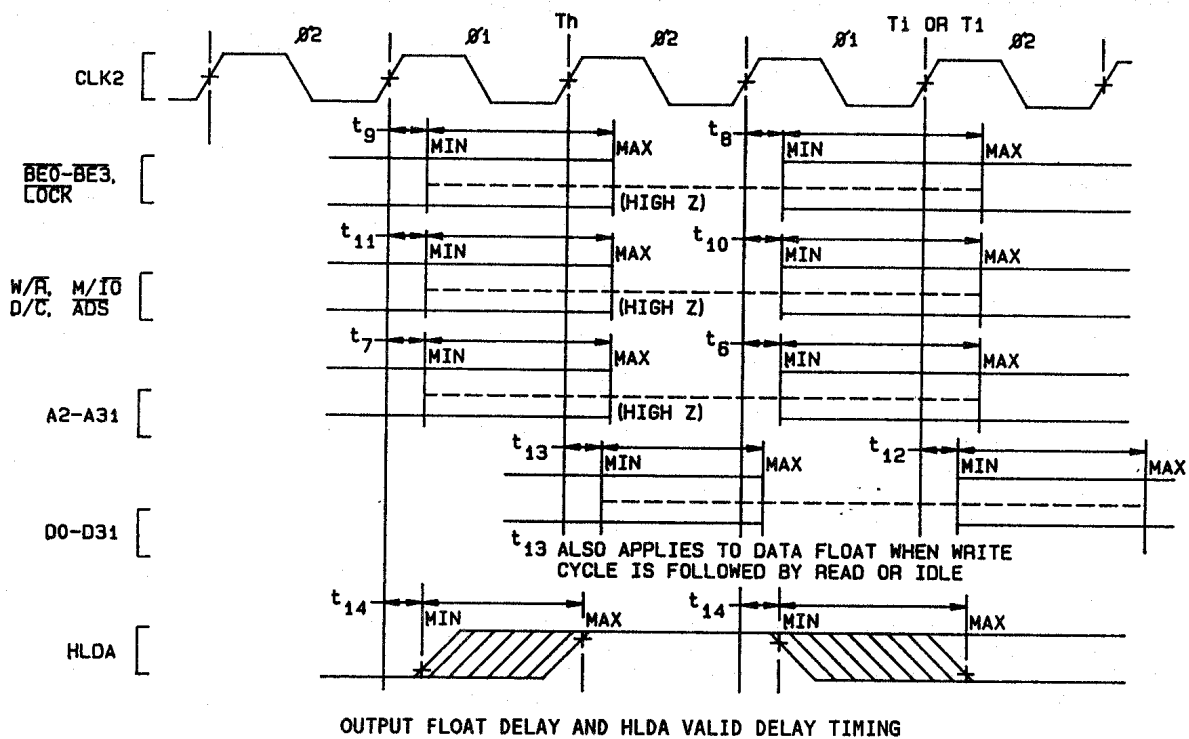
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The second internal processor phase following RESET high-to-low transistion (provided t_{25} and t_{26} are met) is $\phi 2$.

RESET SETUP AND HOLD TIMING, AND INTERNAL PHASE

FIGURE 4. Test circuit and switching waveforms - Continued.

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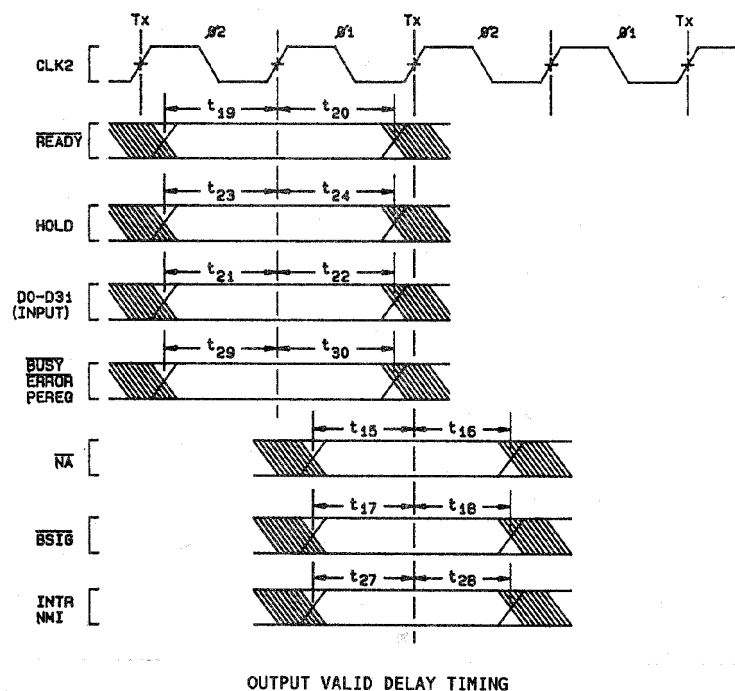
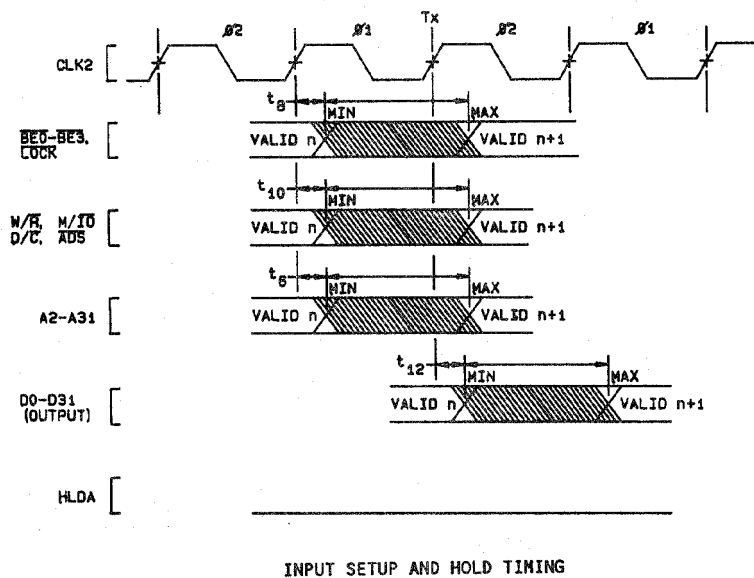


FIGURE 4. Test circuit and switching waveforms - Continued.

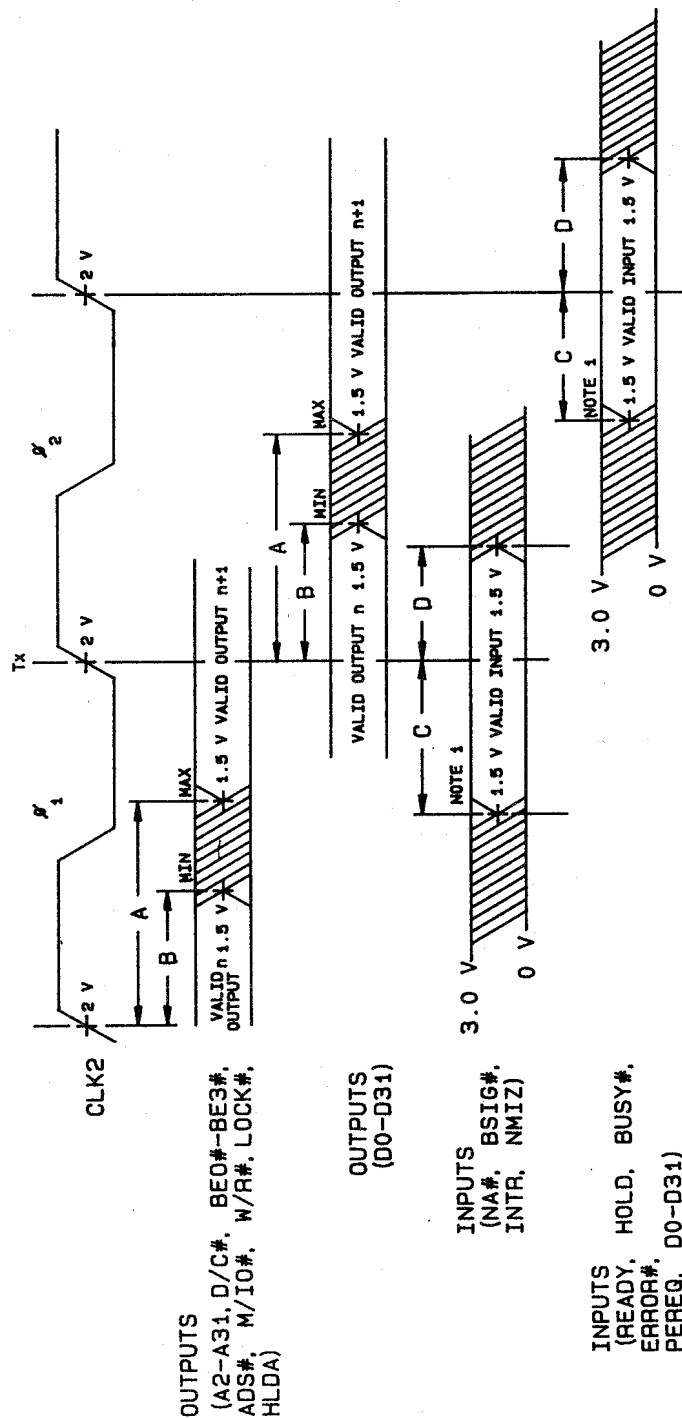
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Legend:

- A - Maximum output delay specification.
- B - Minimum output delay specification.
- C - Minimum input setup specification.
- D - Minimum input hold specification.

NOTE: Input waveforms have $t_r \leq 2.0$ ns from 0.8 V to 2.0 V.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	1, 7, 9	---	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/	1, 2, 3, 7, 8, 9, 10, 11 2/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group B end-point electrical parameters (see 4.4)	---	---	2, 8, 10	---	2, 8, 10
Group C end-point electrical parameters (see 4.4)	2, 8A, 10	2, 8, 10	---	2, 8, 10	---
Group D end-point electrical parameters (see 4.4)	2, 8A, 10	2, 8, 10	2, 8, 10	2, 8, 10	2, 8, 10
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1 and 7.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3.1 Additional criteria for device classes M, B, and S. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.
- b. $T_A = +125^\circ\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

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TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100%
Internal visual	2010, condition A or approved alternate	100%
Nondestructive bond pull	2023 or approved alternate	100%
reverse bias burn-in	1015	100%
Burn-in	1015, total of 240 hours at 125° C	100%
Radiographic	2012	100%

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

- a. RHA tests for device classes B and S for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.
- b. End-point electrical parameters shall be as specified in table IIA herein.
- c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table IIA herein.
- d. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5$ percent, after exposure.
- e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.
- f. For device classes M, B, and S, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.
- g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.4 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8525.

6.5 Symbols, definitions, and functional descriptions. See vendor's data book.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

<u>Military documentation format</u>	<u>Example PIN under new system</u>	<u>Manufacturing source listing</u>	<u>Document listing</u>
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.

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APPENDIX

PIN SUPERSESSION INFORMATION

10. SCOPE

10.1 Scope. This appendix contains the PIN supersession information to support the one part-one part number system. For new system designs, after the date of this document the NEW PIN shall be used in lieu of the OLD PIN. For existing system designs prior to the date of this document, the NEW PIN can be used in lieu of the OLD PIN. This is a mandatory part of the document. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS

This section is not applicable to this appendix.

30. PIN SUPERSESSION DATA

<u>NEW PIN</u>	<u>OLD PIN</u>
5962-8766801MXX	5962-8766801XX
5962-8766801MYX	5962-8766801YX
5962-8766802MXX	5962-8766802XX
5962-8766802MYX	5962-8766802YX
5962-8766803MXX	5962-8766803XX
5962-8766803MYX	5962-8766803YX
5962-8766804MXX	5962-8766804XX
5962-8766804MYX	5962-8766804YX

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STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 91-09-24

Approved sources of supply for SMD 5962-88726 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-ECS. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8766801MXX 5962-8766801MYX	34649 34649	MG80386-16/B MG80386-16/B	M38510/560XXBXX M38510/560XXBXX
5962-8766802MXX 5962-8766802MYX	34649 34649	MG80386-12/B MG80386-12/B	M38510/560XXBXX M38510/560XXBXX
5962-8766803MXX 5962-8766803MYX	34649 34649	MG80386-20/B MG80386-20/B	M38510/560XXBXX M38510/560XXBXX
5962-8766804MXX 5962-8766804MYX	34649 34649	MG80386-25/B MG80386-25/B	M38510/560XXBXX M38510/560XXBXX

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE
number

34649

Vendor name
and address

Intel Corporation
5000 W. Williams Field Road
Chandler, AZ 85224

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 91-09-24

Approved sources of supply for SMD 5962-88726 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-ECS. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN <u>1/</u>
5962-8766803QXX	34649	MG80386-20
5962-8766803QYX	34649	MG80386-20
5962-8766804QXX	34649	MG80386-25
5962-8766804QYX	34649	MG80386-25

1/ Caution. Do not use this number for item acquisition.
Items acquired to this number may not satisfy the
performance requirements of this drawing.

Vendor CAGE
number

Vendor name
and address

34649

Intel Corporation
5000 W. Williams Field Road
Chandler, AZ 85224

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