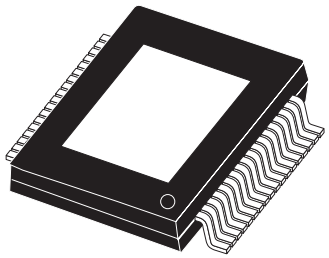
STA510F

44 V, 5.5 A, quad power half-bridge

Datasheet - production data



PSSO36 (slug up)

Features

- Minimum input/output pulse width distortion
- 150 mΩ $R_{DS(on)}$ complementary DMOS output stage
- CMOS compatible logic inputs
- Thermal protection
- Thermal warning output
- Undervoltage protection
- No power-on, power-off sequence required

Description

The STA510F is a monolithic, quad, half-bridge stage in multipower BCD technology. The device can be used as dual-bridge or reconfigured, by connecting the CONFIG pin to the Vdd pin, as single-bridge with double current capability, and as half-bridge (binary mode).

The device is particularly designed to make the output stage of a stereo all-digital high-efficiency (FFX) amplifier capable of delivering 100 W + 100 W output power into 6 Ω loads with THD = 10% and V_{CC} = 36 V. In single BTL configuration the device can deliver 200 W into a 3 Ω load with THD = 10% and V_{CC} = 36 V.

The device is fully compatible with the FFX® driver device.

The input pins have a threshold proportional to V_L pin voltage.

Table 1. Device summary

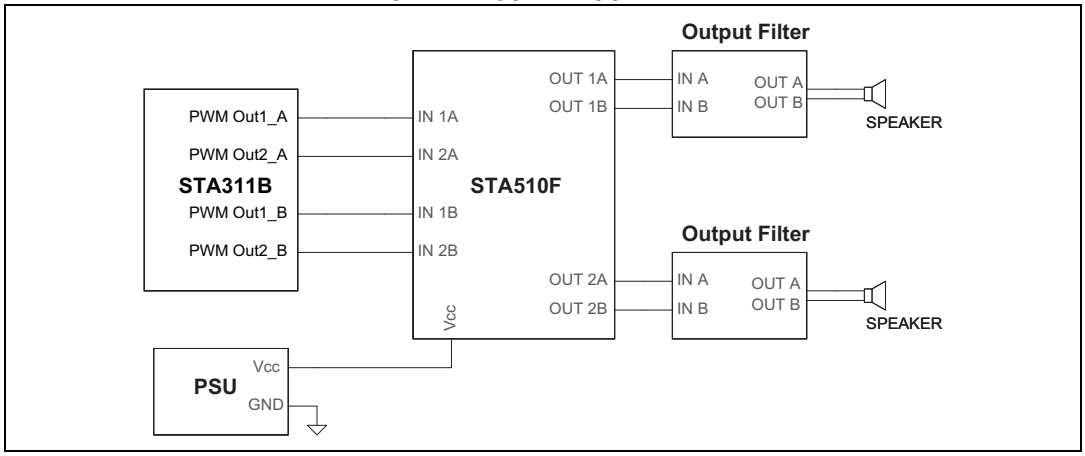
Order code	Operating temp. range	Package	Packing
STA510FTR	0° to 70° C	PSSO36 (slug up)	Tape and reel

This is information on a product in full production. www.st.com

Contents

1 Application diagram

Figure 1. Typical application



2 Pin description

Figure 2. Pin connections (top view)

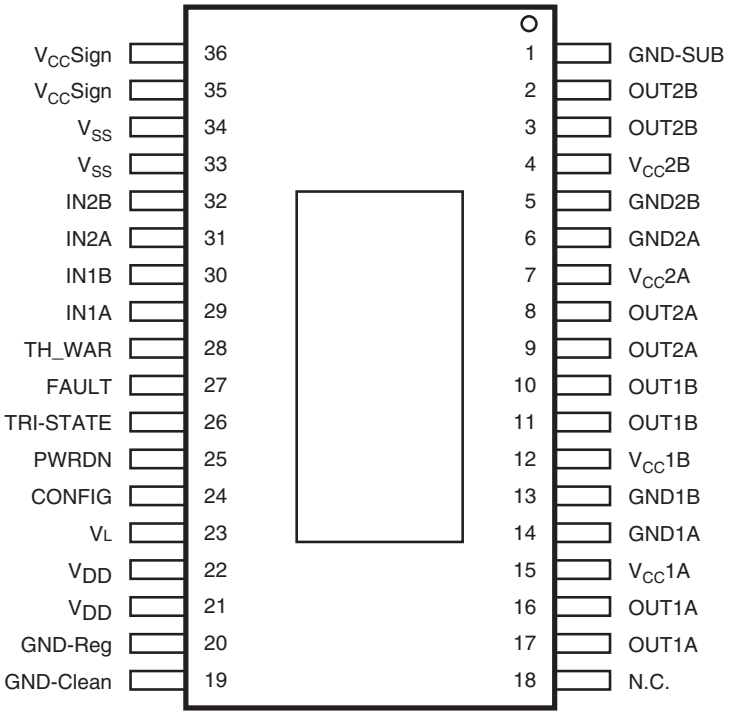


Table 2. Pin list

Pin	Name	Description
1	GND-SUB	Substrate ground
2, 3	OUT2B	Output half-bridge 2B
4	Vcc2B	Positive supply
5	GND2B	Negative supply
6	GND2A	Negative supply
7	Vcc2A	Positive supply
8, 9	OUT2A	Output half-bridge 2A
10, 11	OUT1B	Output half-bridge 1B
12	Vcc1B	Positive supply
13	GND1B	Negative supply
14	GND1A	Negative supply
15	Vcc1A	Positive supply
16, 17	OUT1A	Output half-bridge 1A
18	NC	Not connected

Table 2. Pin list (continued)

Pin	Name	Description
19	GND-clean	Logical ground
20	GND-Reg	Ground for regulator Vdd
21, 22	V_{DD}	5-V regulator referred to ground
23	V_L	High logical state setting voltage
24	CONFIG	Configuration
25	PWRDN	Standby
26	TRI-STATE	Hi-Z
27	FAULT	Fault pin advisor
28	TH-WAR	Thermal warning advisor
29	IN1A	Input of half-bridge 1A
30	IN1B	Input of half-bridge 1B
31	IN2A	Input of half-bridge 2A
32	IN2B	Input of half-bridge 2B
33, 34	Vss	5-V regulator referred to $+V_{CC}$
35, 36	VCCSIGN	Signal positive supply

Table 3. Pin values

Pin	Logical value	Device status
FAULT (1)	0	Fault detected (short-circuit, or thermal)
	1	Normal operation
TRI-STATE	0	All power stages in Hi-Z state
	1	Normal operation
PWRDN	0	Low-power mode
	1	Normal operation
THWAR (1)	0	Temperature of the IC = 130 °C
	1	Normal operation
CONFIG (2)	0	Normal operation
	1	OUT1A = OUT1B, OUT2A = OUT2B (IF IN1A = IN1B and IN2A = IN2B)

1. The pin is open collector. To have the high logic value, it needs a pull-up resistor.
2. CONFIG = 1 means connect pin 24 (CONFIG) to pins 21, 22 (V_{DD}).

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage (pin 4, 7, 12, 15)	44	V
V_{max}	Maximum voltage on pins 23 to 32	5.5	V
ESD	Max ESD on pins (HBM)	±1000	V
T_{op}	Operating temperature range	0 to 70	°C
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

3.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Min.	Typ.	Max.	Unit
$T_{j\text{-}case}$	Thermal resistance junction to case (thermal pad)		1	2.5	°C/W
T_{jSD}	Thermal shut-down junction temperature		150		°C
T_{warn}	Thermal warning temperature		130		°C
t_{hSD}	Thermal shutdown hysteresis		25		°C

3.3 Electrical specifications

The results in *Table 6* below are given for the conditions: V_L = 3.3 V, V_{CC} = 37 V and T = 25 °C unless otherwise specified.

Table 6. Electrical specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R_{dsON}	Power P-channel/N-channel MOSFET $R_{DS(on)}$	Id = 1 A		150	200	mΩ
I_{dss}	Power P-channel/N-channel leakage current				100	µA
g_N	Power P-channel $R_{DS(on)}$ matching	Id = 1 A	95			%
g_P	Power N-channel $R_{DS(on)}$ matching	Id = 1 A	95			%
Dt_s	Low current deadtime (static)	See test circuit *Figure 3*		10	20	ns
Dt_d	High current deadtime (dynamic)	L = 22 µH, C = 470 nF, R_L = 8 Ω, Id = 4.5 A, see test circuit *Figure 4*			50	ns
$t_{d\ ON}$	Turn-on delay time	Resistive load			100	ns

Table 6. Electrical specifications (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{d\ OFF}$	Turn-off delay time	Resistive load			100	ns
t_r	Rise time	Resistive load, as *Figure 4*			25	ns
t_f	Fall time	Resistive load, as *Figure 4*			25	ns
V_{CC}	Supply voltage operating voltage		10		40	V
$V_{IN\text{-}High}$	High level input voltage		$V_L/2$ + 300 mV			V
$V_{IN\text{-}Low}$	Low level input voltage				$V_L/2$ – 300 mV	V
$I_{IN\text{-}H}$	High level input current	Pin voltage = V_L		1		µA
$I_{IN\text{-}L}$	Low level input current	Pin voltage = 0.3 V		1		µA
$I_{PWRDN\text{-}H}$	High level PWRDN pin input current	V_L= 3.3 V		35		µA
V_{Low}	Low logical state voltage (pins PWRDN, TRISTATE) (see *Table 7*)	V_L = 3.3 V			0.8	V
V_{High}	High logical state voltage (pins PWRDN, TRISTATE) (see *Table 7*)	V_L = 3.3 V	1.7			V
$I_{VCC\text{-}PWRDN}$	Supply current from V_{CC} in power down	PWRDN = 0			3	mA
I_{FAULT}	Output current pins FAULT -TH-WARN when FAULT CONDITIONS	V_{PIN} = 3.3 V		1		mA
$I_{VCC\text{-}hiz}$	Supply current from V_{CC} in tri-state	Pin TRI-STATE = 0		22		mA
I_{VCC}	Supply current from V_{CC} in operation both channel switching)	Input pulse width duty cycle = 50%, switching frequency = 384 kHz, no LC filters;		70		mA
$I_{OUT\text{-}SH}$	Overcurrent protection threshold I_{SC} (short-circuit current limit)		5.5	7	9	A
V_{UV}	Undervoltage protection threshold			7		V
t_{pw_min}	Output minimum pulse width	No load	25		40	ns

Table 7. V_{low}, V_{high} threshold variation with V_L

V_L	V_{Low} max.	V_{High} min.	Unit
2.7	0.7	1.5	V
3.3	0.8	1.7	V
5	0.85	1.85	V

Table 8. Logic truth table

TRI-STATE	INxA	INxB	Q1	Q2	Q3	Q4	Output mode
0	x	x	OFF	OFF	OFF	OFF	Hi-Z
1	0	0	OFF	OFF	ON	ON	DUMP
1	0	1	OFF	ON	ON	OFF	NEGATIVE
1	1	0	ON	OFF	OFF	ON	POSITIVE
1	1	1	ON	ON	OFF	OFF	Not used

Figure 3. Test circuit for low current deadtime

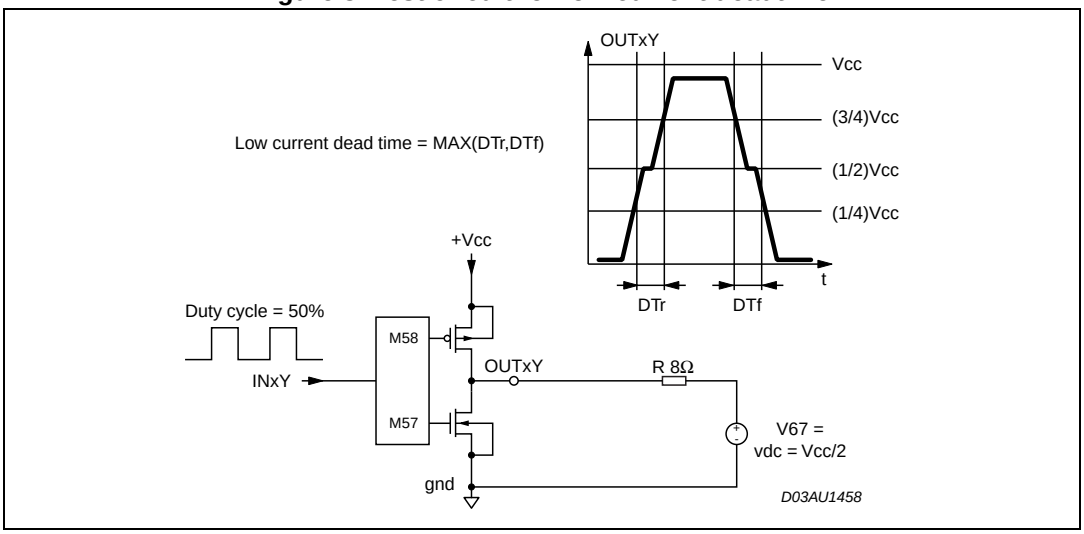


Figure 4. Test circuit for high current deadtime

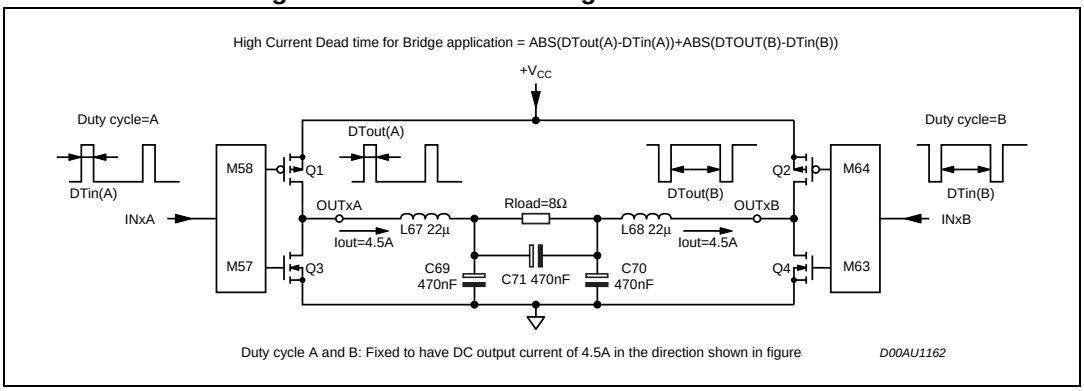


Figure 5. STA311B connections with STA510F

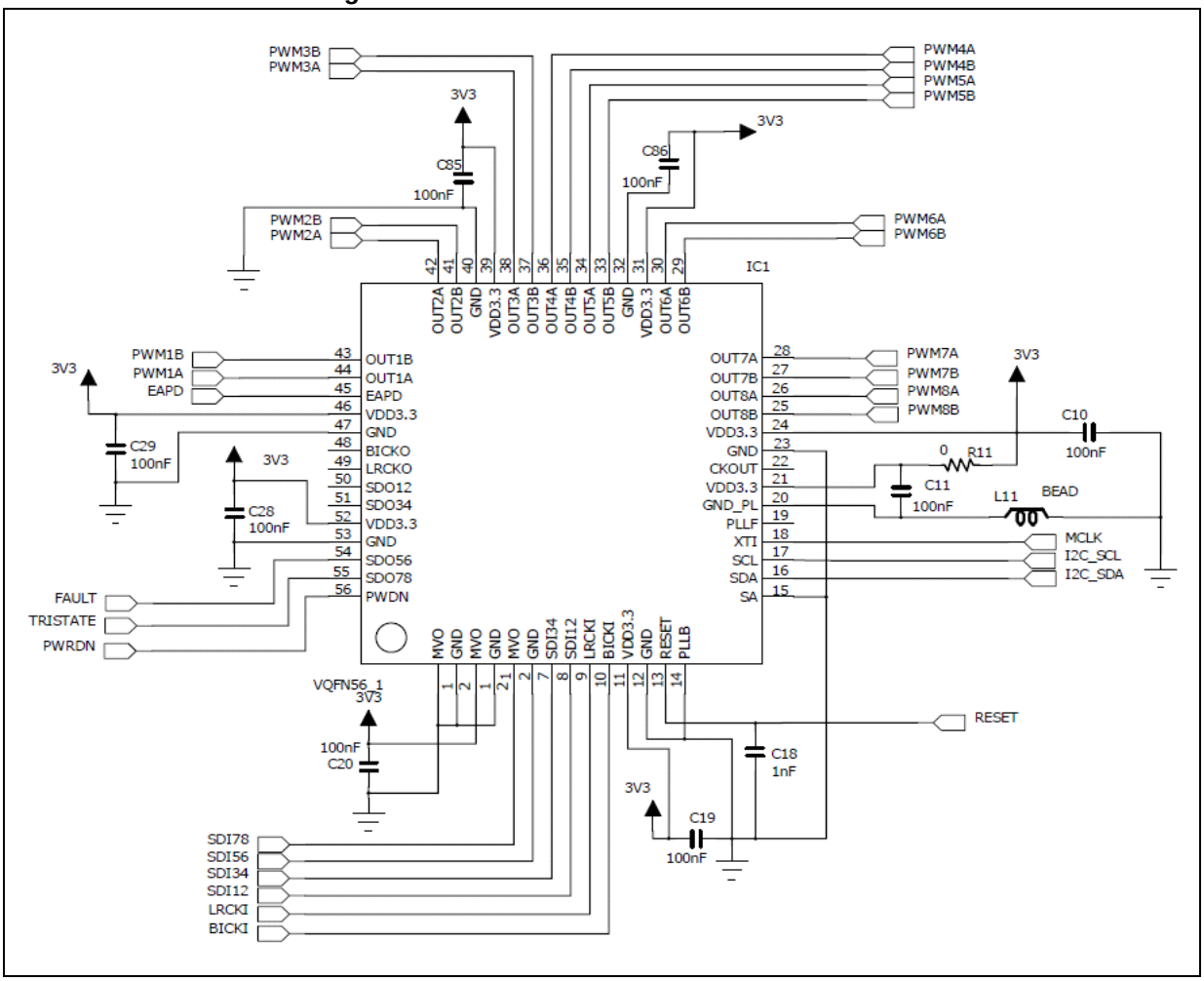


Figure 6. Typical stereo BTL configuration

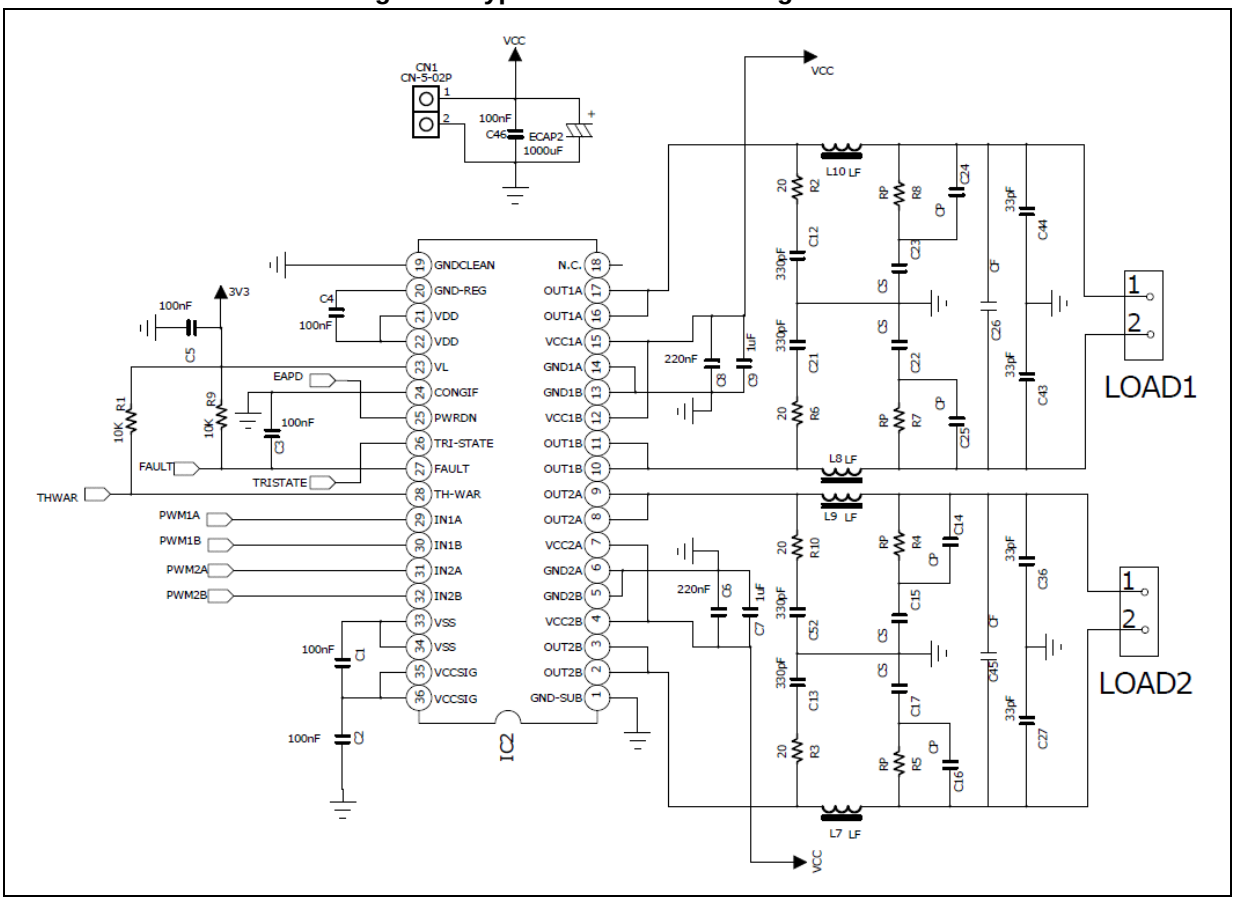


Figure 7. Typical mono BTL configuration

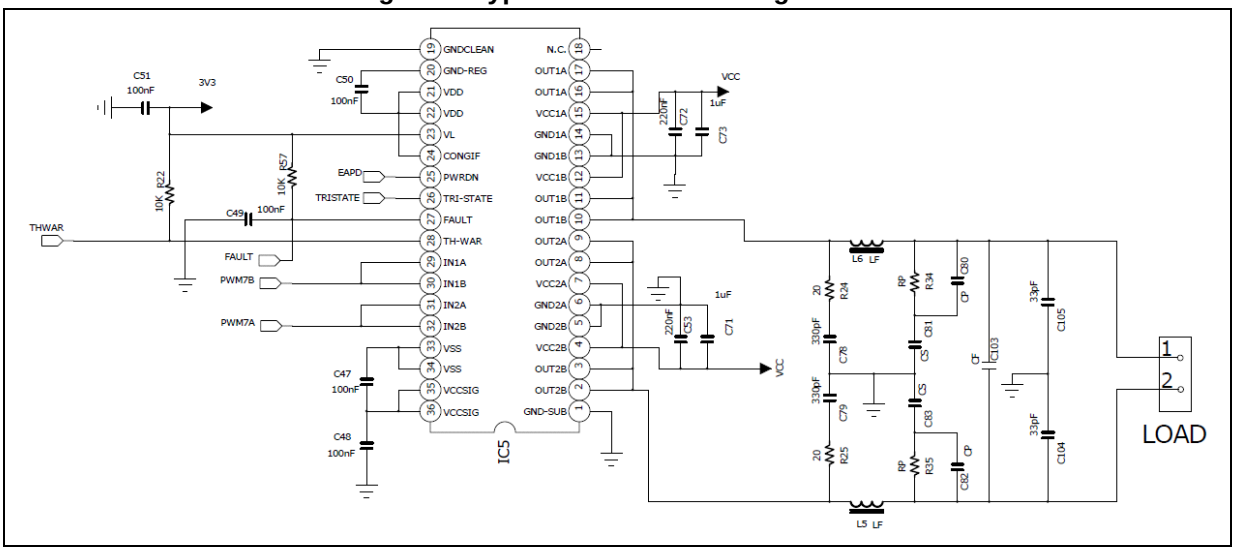
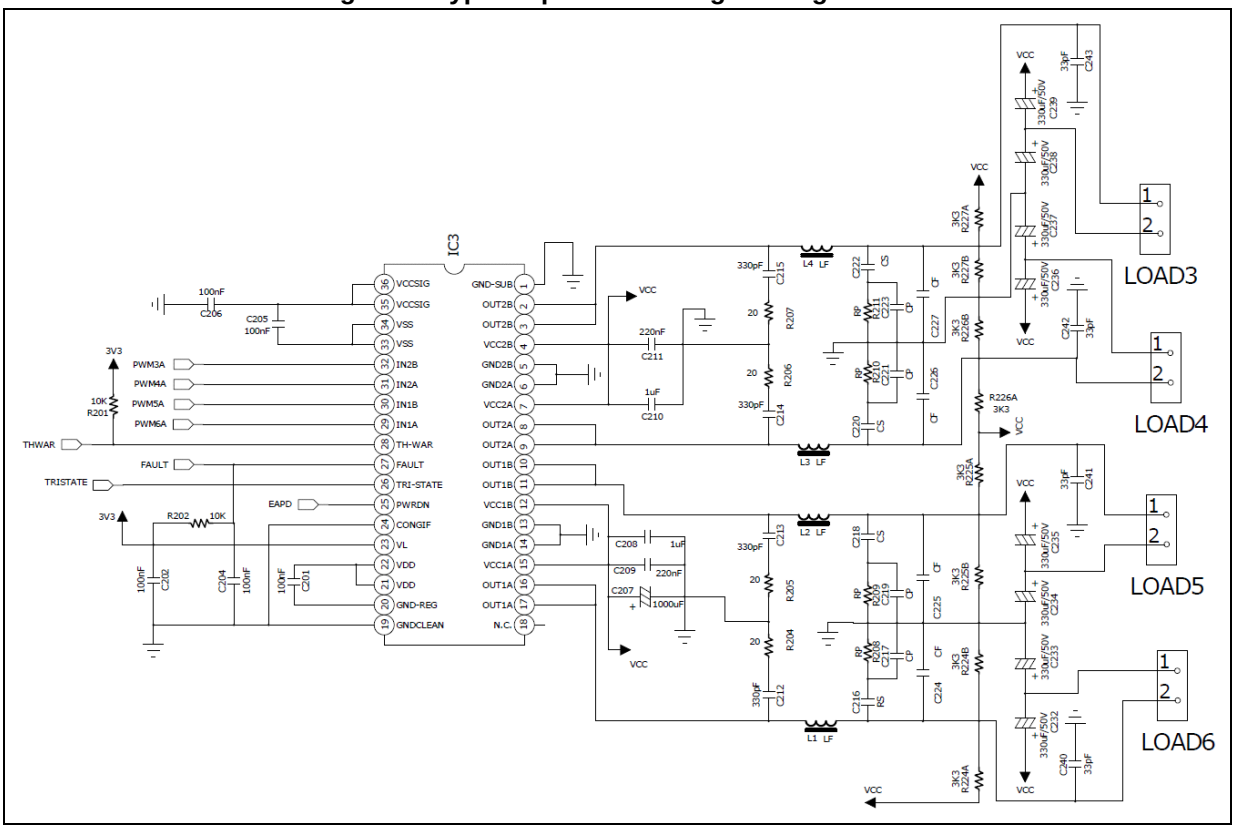


Figure 8. Typical quad half-bridge configuration



4 Characterization curves

Figure 9. THD+N vs. P_{OUT} 36 V 6 Ω BTL time slot 13, 0x03 = BB

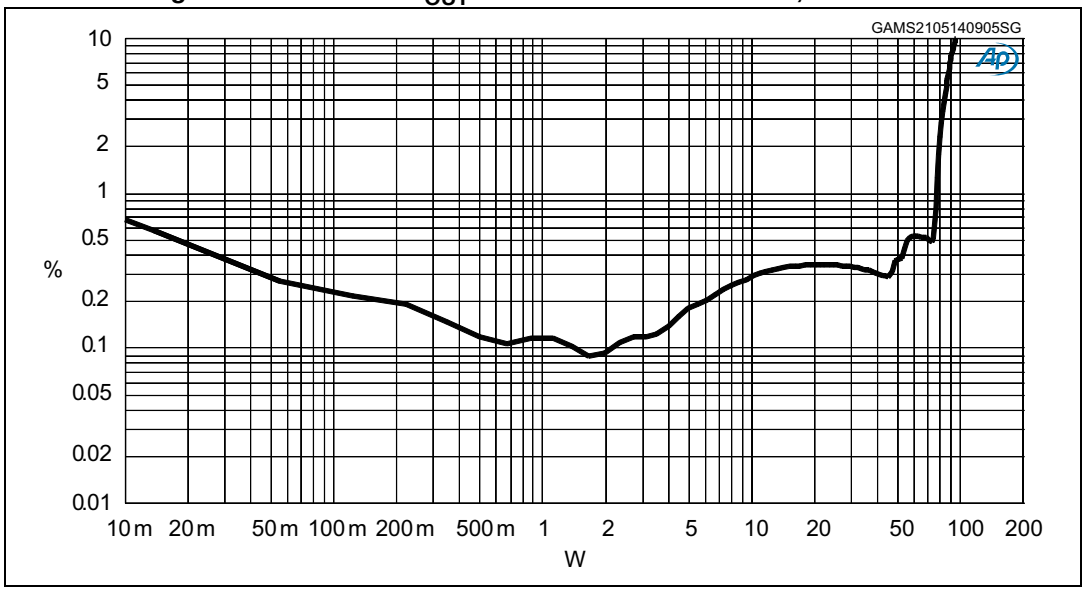


Figure 10. THD+N vs. P_{OUT} 36 V 3 Ω SE

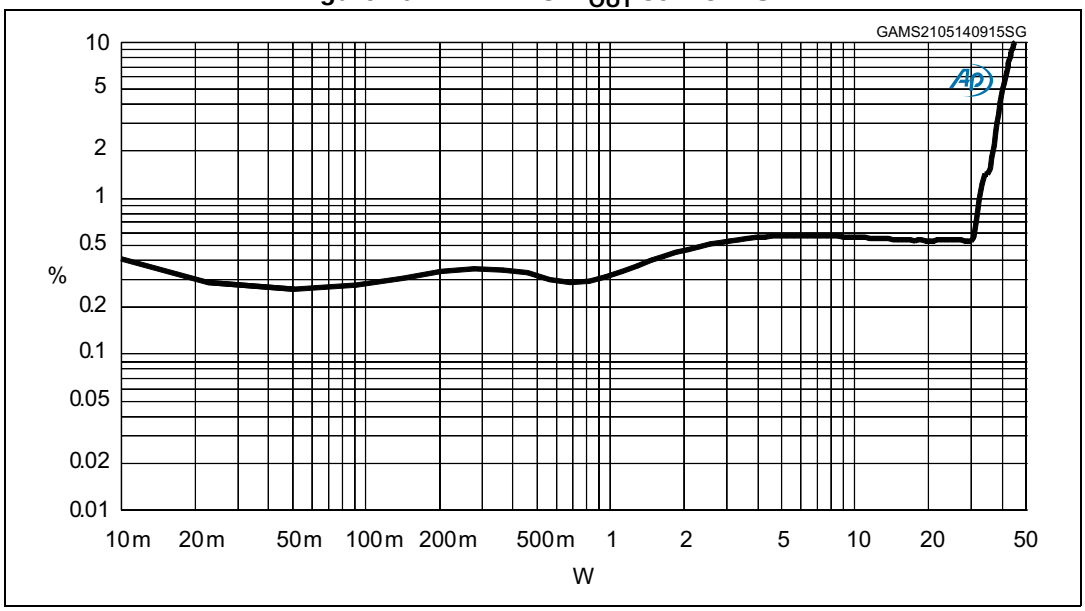


Figure 11. THD+N vs. P_{OUT} 36V 3 Ω mono BTL

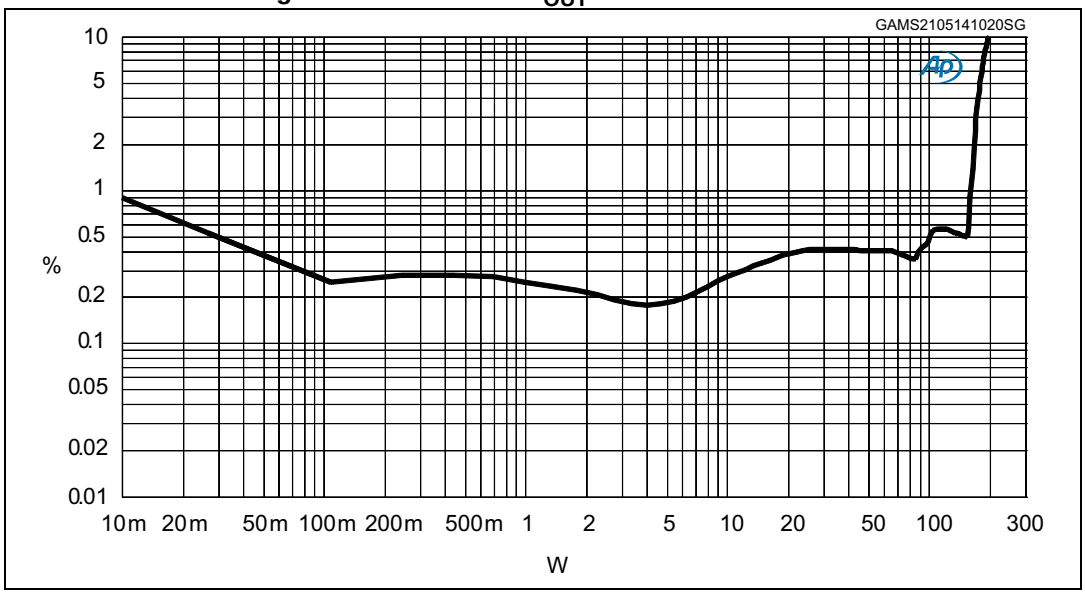


Figure 12. P_{OUT} vs. V_{CC} 6 Ω BTL

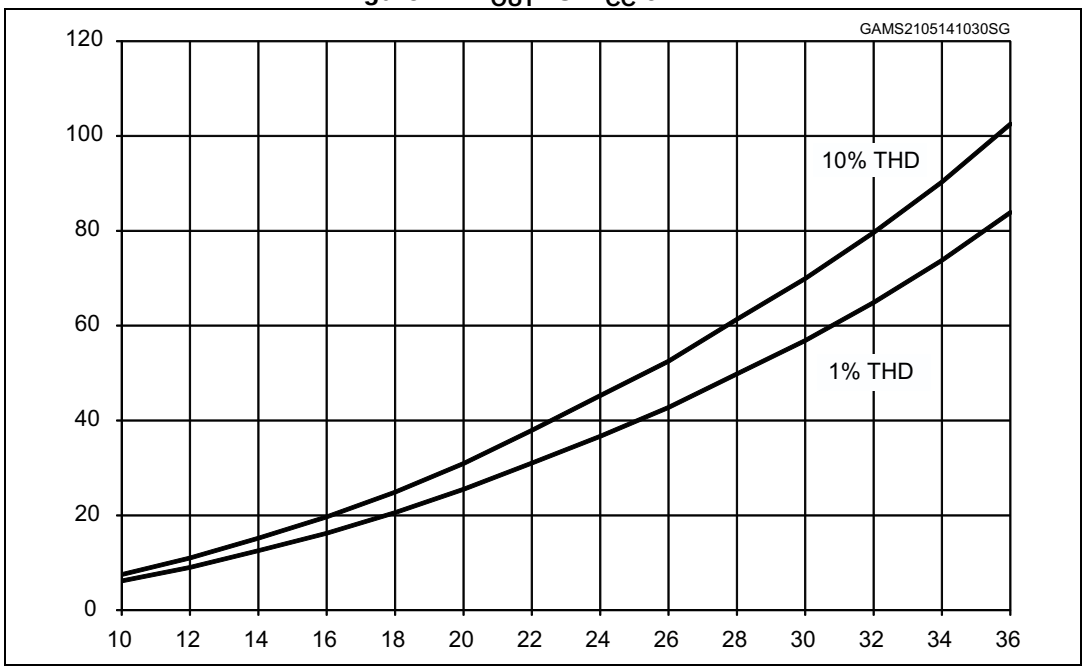


Figure 13. P_{OUT} vs. V_{CC} 3 Ω SE

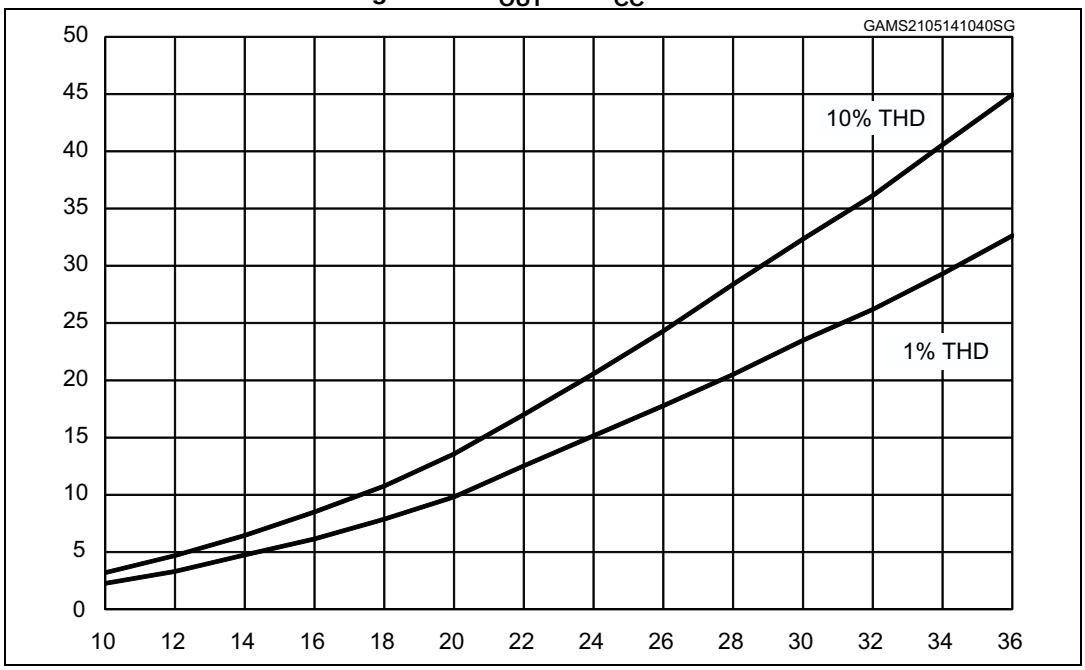


Figure 14. P_{OUT} vs. V_{CC} 3 Ω mono BTL

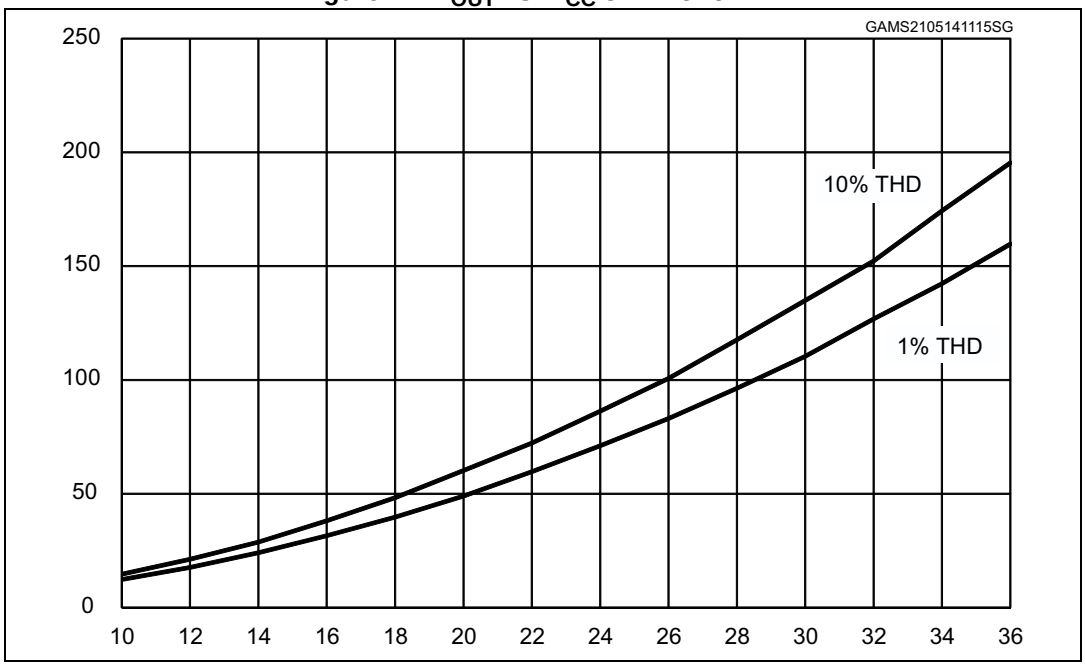


Figure 15. FFT 6 Ω BTL -6dBFs

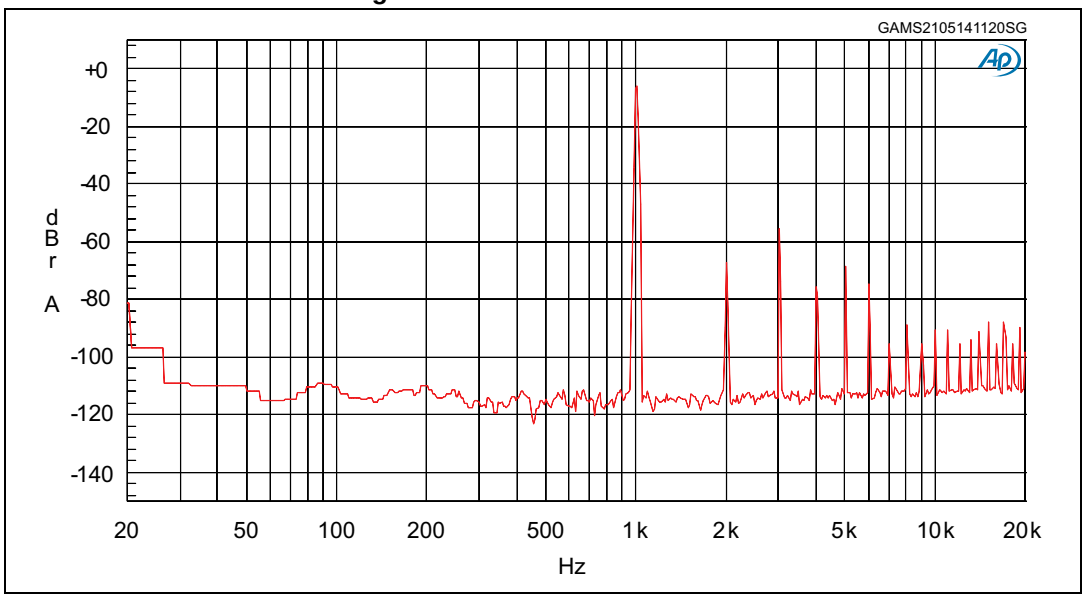


Figure 16. FFT 6 Ω BTL -60dBFs

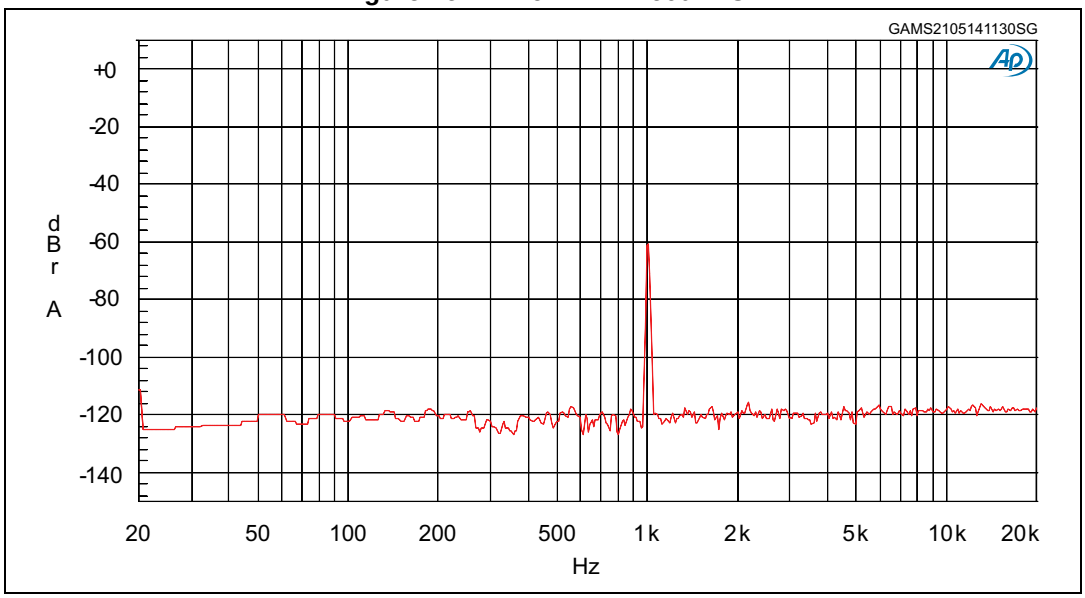


Figure 17. FFT 3 Ω SE -6dBFs

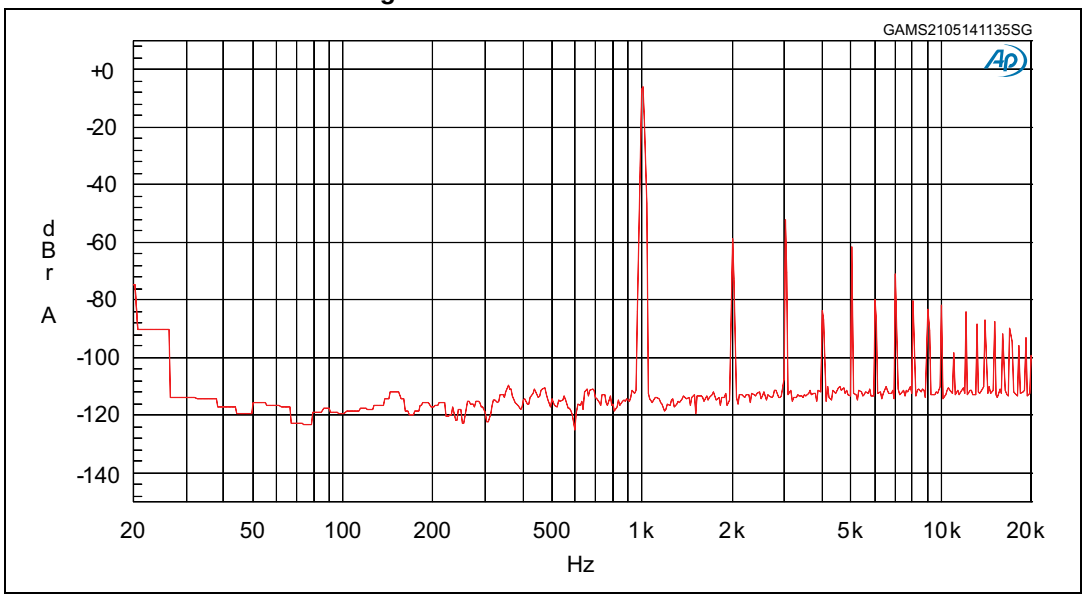


Figure 18. FFT 3 Ω SE -60dBFs

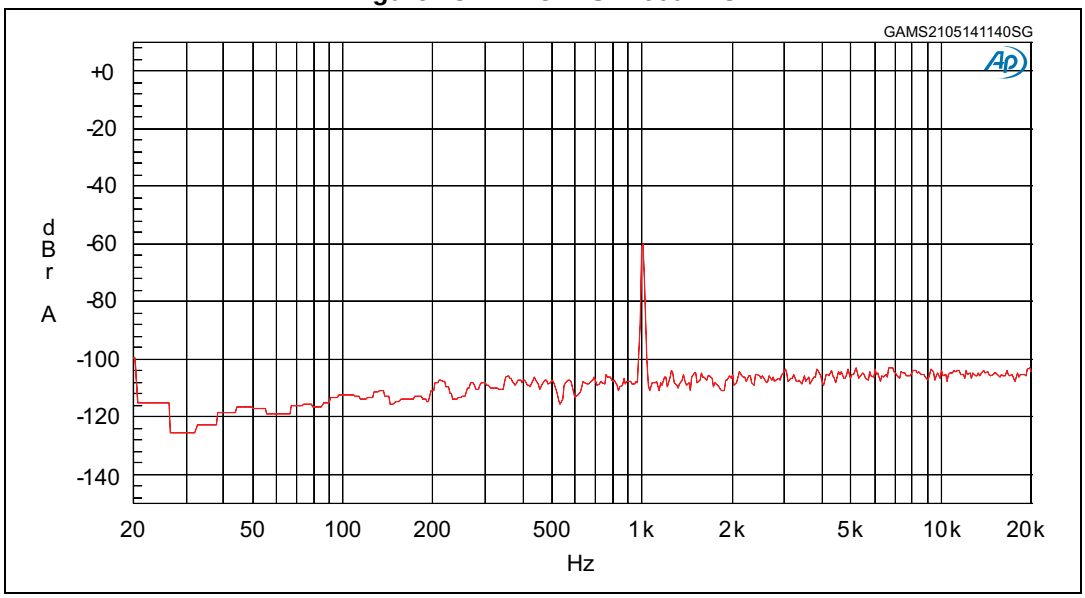


Figure 19. FFT 3 Ω mono BTL -6dBFs

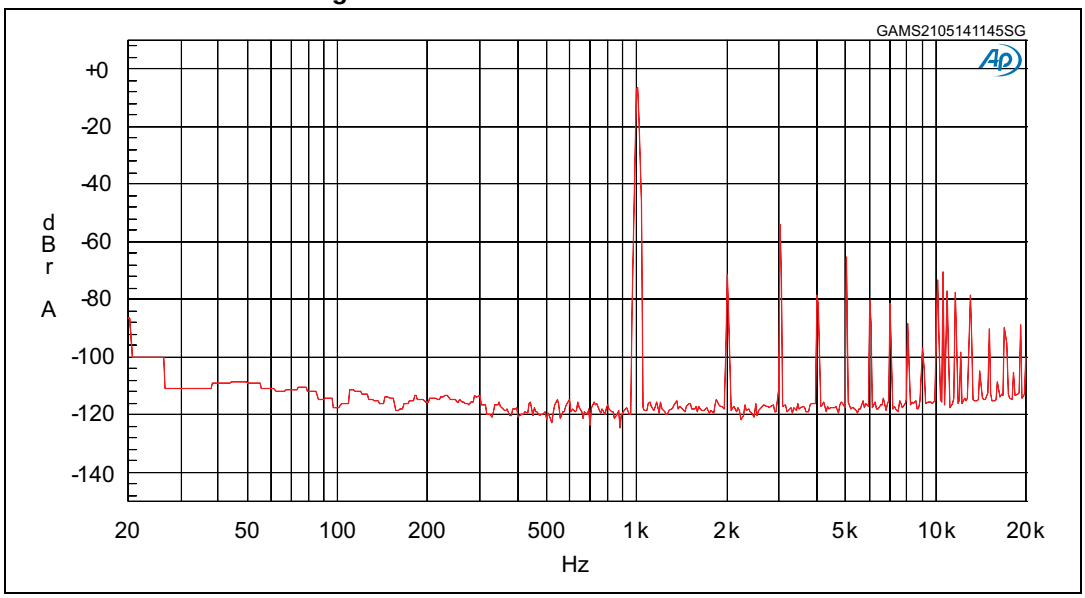


Figure 20. FFT 3 Ω mono BTL -60dBFs

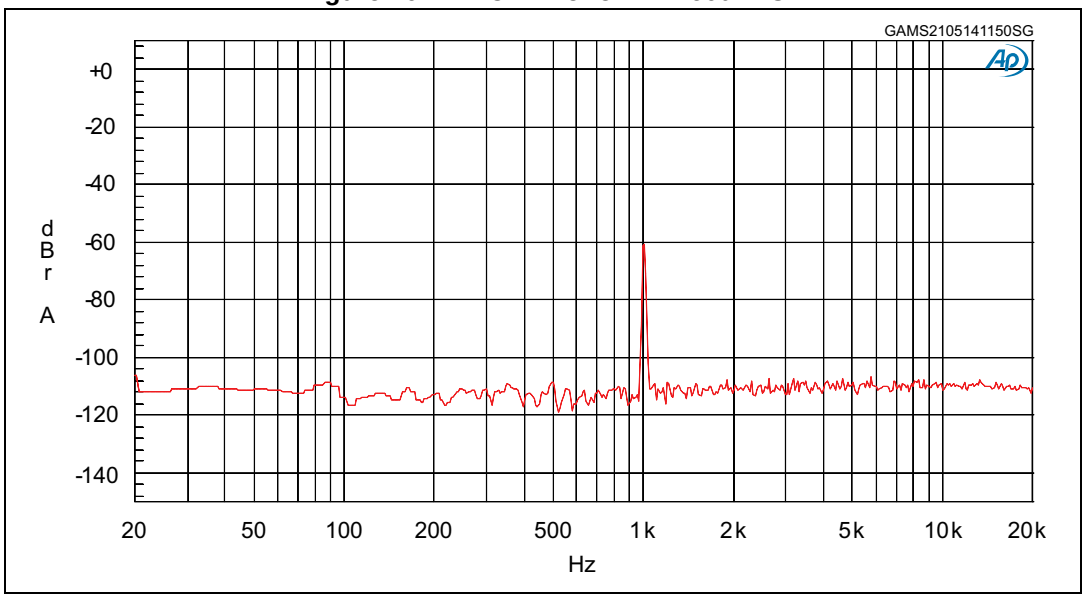


Figure 21. Crosstalk 36 V 6 BTL Ω 1 W

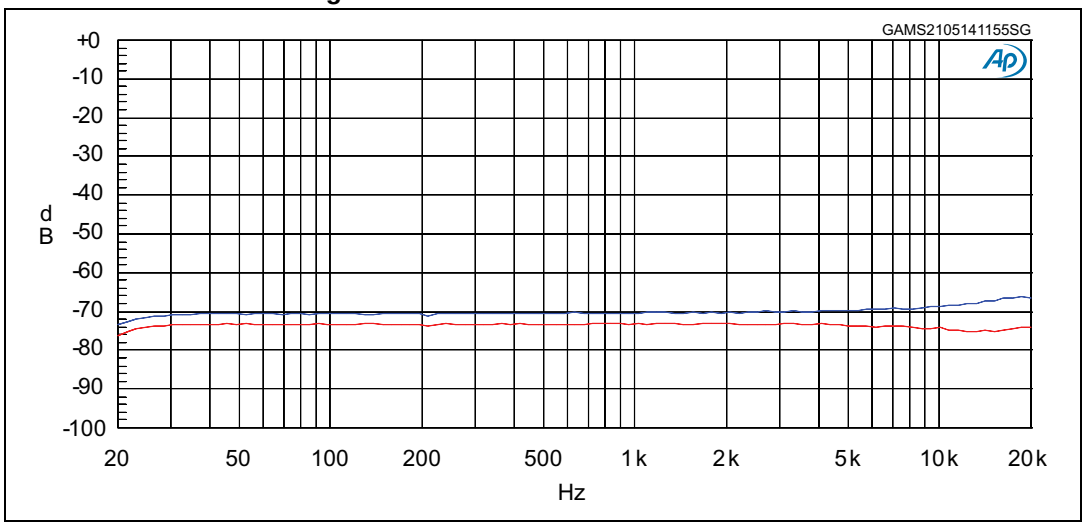
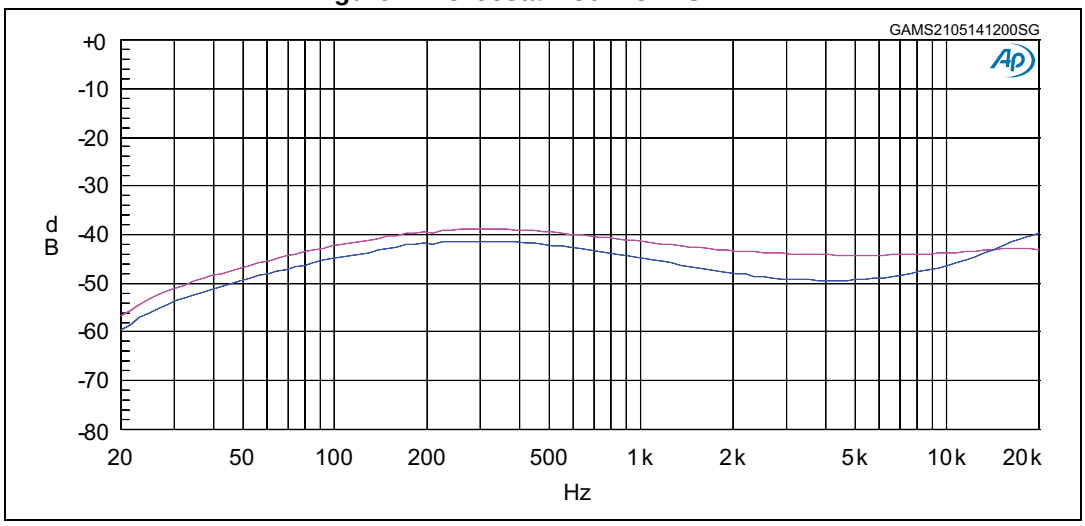


Figure 22. Crosstalk 36 V 3 Ω SE 1 W

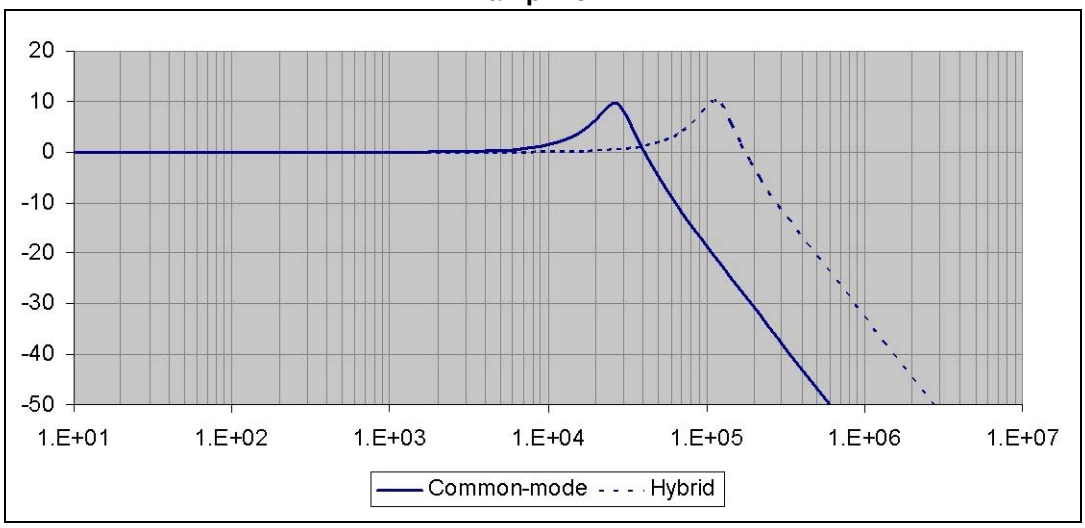


5 Output filter

The differential-mode damping of a hybrid filter under no-load conditions is not as good as a pure common-mode filter because most of the high-frequency current flows through the larger capacitor across the speaker terminals. Normally this isn't a problem because the speaker provides the differential-mode damping, but if the amplifier is operated without the speaker connected, for instance when doing testing in production line, then the damping will not be as good.

Care needs to be taken to insure that the damping of a hybrid filter is good enough to protect the amplifier under no-load conditions, thus avoiding peak of voltage that exceed the absolute maximum voltage of the amplifier.

Figure 23. Output filter frequency response with and without load connected to the amplifier



To allow the right filter selection both sets of coefficients are provided.

5.1 Theoretical filter

Perfect when using amplifiers always connected to speakers

Table 9. Theoretical table SE

Load impedance	LC Low-pass filter		Damping network		
	LF	CF	CS	CP	RP
3	15 µH	1 µF	100 nF	100 nF	6.2 Ω
4	22 µH	680 nF	100 nF	100 nF	6.2 Ω
6	33 µH	470 nF	100 nF	100 nF	6.2 Ω
8	47 µH	330 nF	100 nF	100 nF	6.2 Ω

See *Figure 8*.

Table 10. Theoretical table BTL

Load Impedance	LC Low-Pass Filter		Damping network		
	LF	CF	CS	CP	RP
3	10 µH	1 µF	220 nF	220 nF	3.3 Ω
4	10 µH	1 µF	220 nF	220 nF	3.3 Ω
6	15 µH	680 nF	100 nF	100 nF	4.7 Ω
8	22 µH	470 nF	100 nF	100 nF	6.2 Ω

See *Figure 6*.

Table 11. Theoretical table PBTL

Load Impedance	LC Low-Pass Filter		Damping network		
	LF	CF	CS	CP	RP
3	10 µH	1 µF	220 nF	220 nF	2.7 Ω
4	10 µH	1 µF	220 nF	220 nF	3.3 Ω
6	15 µH	680 nF	100 nF	100 nF	6.2 Ω
8	22 µH	470 nF	100 nF	100 nF	6.2 Ω

See *Figure 7*.

5.2 Optimized filter

Suggest to avoid resonant peak when running amplifiers without load

Table 12. Filter optimized to minimize the peak SE

Load impedance	LC Low-pass filter		Damping network		
	LF	CF	CS	CP	RP
3	15 µH	680 µF	100 nF	100 nF	6.2 Ω
4	22 µH	470 nF	100 nF	100 nF	6.2 Ω
6	33 µH	330 nF	100 nF	100 nF	6.2 Ω
8	47 µH	220 nF	100 nF	100 nF	6.2 Ω

See *Figure 8*.

Table 13. Filter optimized to minimize the peak BTL

Load impedance	LC low-pass filter		Damping network		
	LF	CF	CS	CP	RP
3	10 µH	680 nF	220 nF	220 nF	3.3 Ω
4	10 µH	680 nF	220 nF	220 nF	3.3 Ω
6	15 µH	470 nF	100 nF	100 nF	4.7 Ω
8	22 µH	330 nF	100 nF	100 nF	6.2 Ω

See *Figure 6*.

Table 14. Filter optimized to minimize the peak PBTL

Load impedance	LC low-pass filter		Damping network		
	LF	CF	CS	CP	RP
3	10 µH	680 nF	220 nF	220 nF	2.7 Ω
4	10 µH	680 nF	220 nF	220 nF	3.3 Ω
6	15 µH	470 nF	100 nF	100 nF	6.2 Ω
8	22 µH	330 nF	100 nF	100 nF	6.2 Ω

See *Figure 7*.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 24. PSSO36 (slug up) package outline

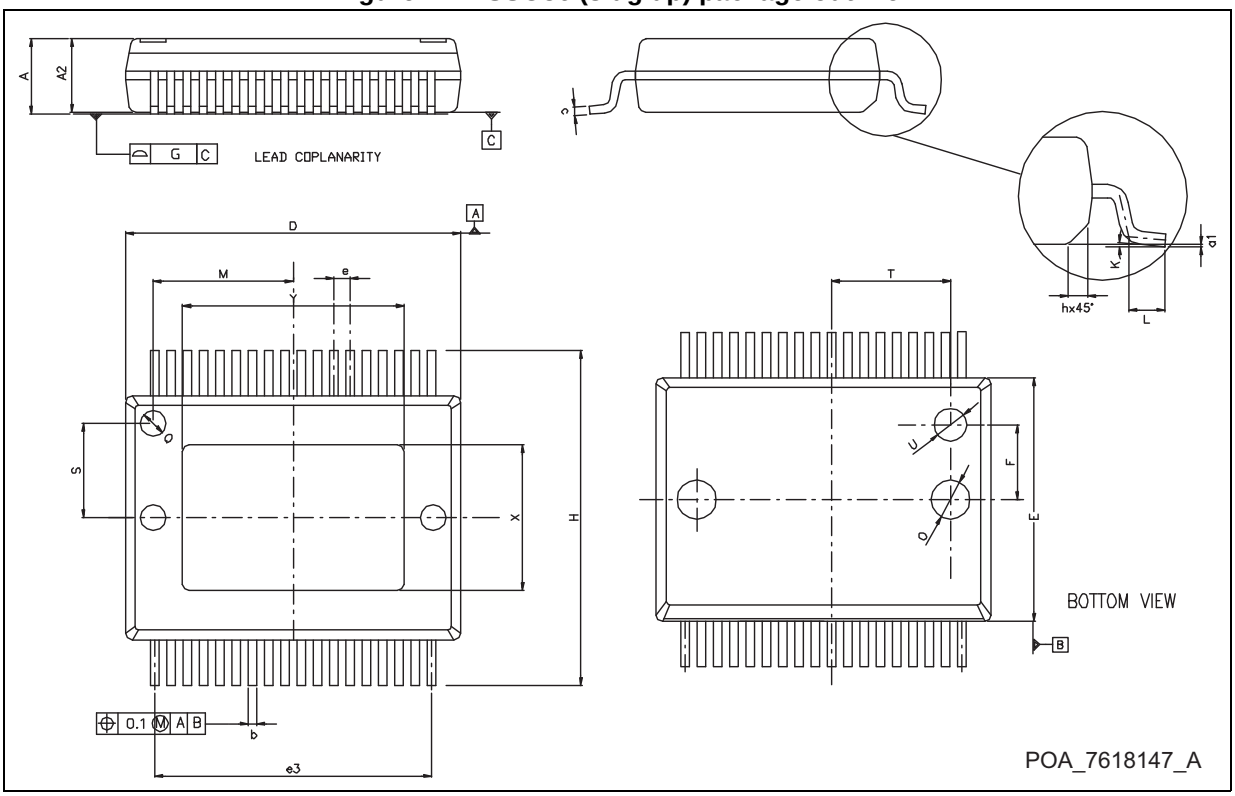


Table 15. PSSO36 (slug up) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.15		2.47	0.084		0.097
A2	2.15		2.40	0.084		0.094
a1	0		0.075	0		0.003
b	0.18		0.36	0.007		0.014
c	0.23		0.32	0.009		0.012
D (1)	10.10		10.50	0.398		0.413
E (1)	7.4		7.6	0.291		0.299
e		0.50			0.020	
e3		8.50			0.035	
F		2.3			0.090	
G			0.10			0.004
G1			0.06			0.002
H	10.10		10.50	0.398		0.413
h			0.40			0.016
L	0.55		0.85	0.022		0.033
M		4.3			0.169	
N	10° (max.)			10° (max.)		
O		1.2			0.047	
Q		0.8			0.031	
S		2.9			0.114	
T		3.65			0.144	
U		1.0			0.039	
X	4.10		4.70	0.161		0.185
Y	6.50		7.10	0.256		0.279

1. “D and E” do not include mold flash or protrusion. Mold flash or protrusion shall not exceed 0.15 mm (0.006”).

7 Trademarks and other acknowledgments

FFX is a STMicroelectronics proprietary digital modulation technology.

ECOPACK is a registered trademark of STMicroelectronics.

8 Revision history

Table 16. Document revision history

Date	Revision	Changes
13-Dec-2007	1	Initial release.
28-Jun-2011	2	Added part number STA510FTR to *Table 1: Device summary* Updated ECOPACK® text in *Section 6: Package information* Minor textual updates
02-Sep-2011	3	Updated package to PowerSSO36 throughout datasheet Corrected typographical error in *Features* Updated *Figure 1* Updated *Figure 2* Updated *Figure 21*
03-Jun-2014	4	Added: – *Figure 5 on page 9*, *Figure 6 on page 10*, *Figure 7 on page 10* and *Figure 8 on page 11* – *Section 4: Characterization curves* – *Section 5: Output filter*
11-Dec-2018	5	Updated *Table 1: Device summary*