HI-6200

Fully Integrated
MIL-STD-1553 BC/RT/MT

HI-6200, HI-6202 Families

January 2024

DS6200 Rev. P

NOTES:

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1. OVERVIEW

The HI-6200 family is a fully integrated and dual redundant MIL-STD-1553 BC/RT/MT interface solution which includes 1553 protocol, SRAM and dual transceivers in single 80-pin plastic PQFP and QFN package configurations. The devices are software compatible with the Data Device Corporation (DDC®) Mini-ACE®, Enhanced Mini-ACE®, Micro-ACE®, Mini-ACE® Mark3 and Total-ACE® families of MIL-STD-1553 Terminals and offer additional features such as Error-Correcting Code (ECC) SRAM. The compact single-chip monolithic design offers a significant space and cost saving over the older traditional multi-chip module approach.

1.1. Bus Controller

The BC is a programmable message-sequencing engine programmed using a set of 20 instruction op codes. It greatly reduces the host's processing workload by autonomously supporting multi-frame message scheduling, message retry schemes, storage of message data in on-chip RAM, asynchronous message insertion and status/error reporting. The Enhanced BC mode also includes a General Purpose Queue and user-defined interrupts to further enhance host communication.

1.2. Remote Terminal

The RT has been fully validated by a recognized independent third party. RT memory management options include single, double, and 2 circular buffer modes for individual subaddresses. The RT performs comprehensive error checking including word and format validation and checks for various transfer errors. The RT supports flexible interrupt conditions, command illegalization and a programmable busy bit by subaddress. In addition, the devices have an “auto-boot” feature necessary for MIL-STD-1760 compliance, whereby the terminal can initialize as an online RT with the busy bit set following power turn-on. The HI-6202 provides a cost effective RT-only device.

1.3. Monitor Terminal

The family supports three monitor modes including a word monitor mode, a selective message monitor mode and a combined RT/Monitor Mode. For new applications it is recommended to implement the selective message monitor mode. Selective Message Monitor allows monitoring of 1553 messages and provides the ability to filter based on RT address, $T/\overline{R}$ bit and subaddress with no host processor intervention.

1.4. Host Processor Interface

Each device provides an 8/16-bit parallel host bus interface supporting a variety of processor configurations including shared RAM and DMA. The host interface supports both non-multiplexed and multiplexed address/data buses, non-zero wait mode for interfacing to processor address/data buses, and zero wait mode for interfacing to microcontroller I/O ports.

1.5. Built-In Test

The family provides an autonomous built-in self-test capability. The testing includes both RAM and protocol logic tests which may be initiated by the host processor.

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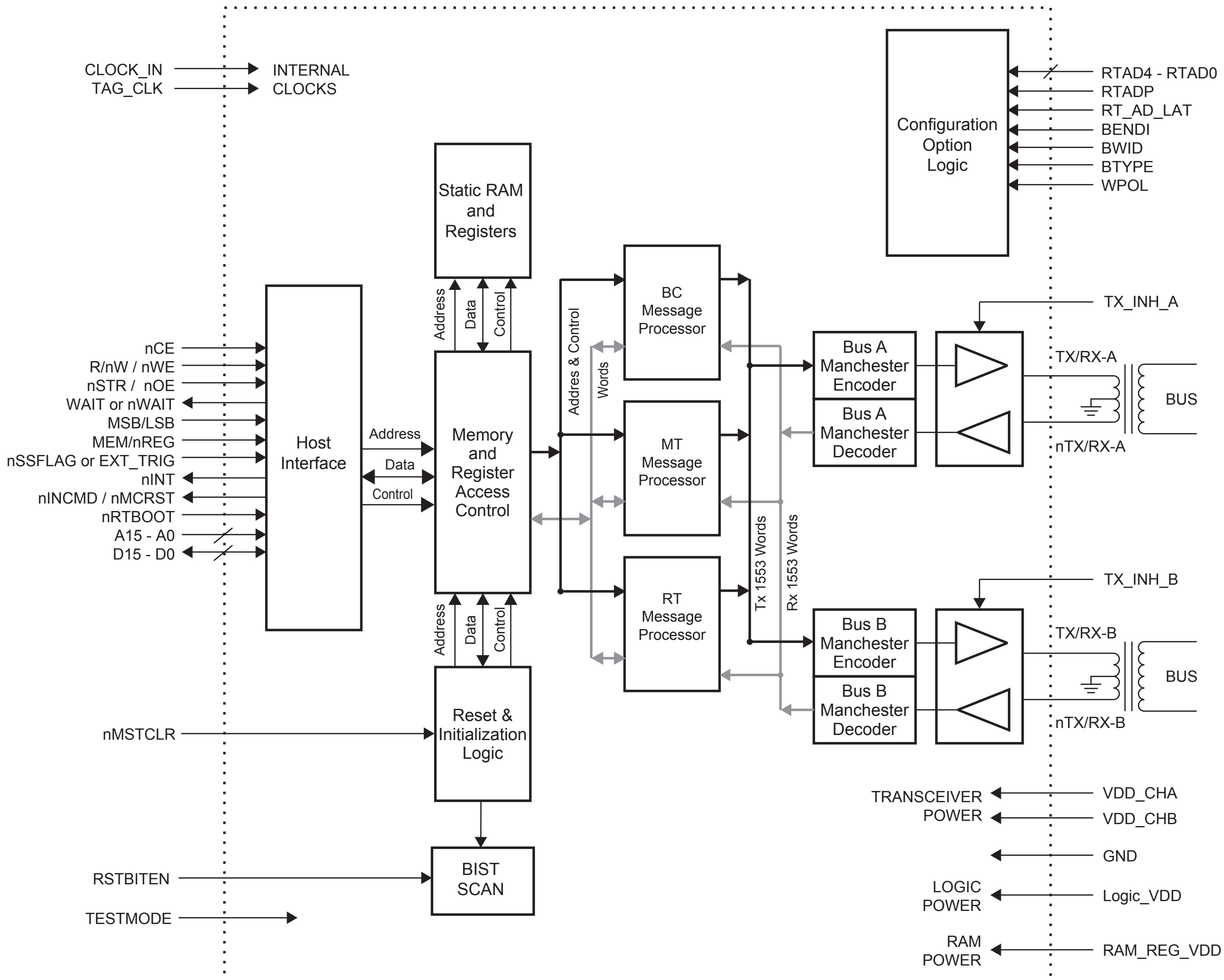
1.6. Features

- Dual Redundant MIL-STD-1553A/B/C/1760 Channel
- SAE AS15531A and STANAG 3838 compliant
- BC/RT/MT or RT/MT Modes
- RT-only device available (HI-6202)
- 64Kx16 ECC SRAM
- External RT Address Inputs
- MIL-STD-1760 RT “Auto Boot”
- +3.3V single supply operation
- Built-in Self-Test
- Generic 8/16-bit Processor Interface
- -40°C to +85°C or -55°C to +125°C
  - No Limitations on transmit duty cycle
- 80-Pin PQFP package
  - 12mm x 12mm x 1.6mm
- 80-Pin QFN package
  - 12mm x 12mm x 0.8mm

1.7. Application Benefits

- Simplified Board Design and Layout
- Third Party RT Validated
- Single Die for Improved Reliability
- Fully Software Compatible to DDC® ACE, Mini-ACE®, Enhanced Mini-ACE®, Micro-ACE®, Mini-ACE® Mark3 and Total-ACE®.

1.8. Block Diagram



2. REGISTERS AND COMMAND/STATUS WORDS

Table 1 summarizes the device registers and corresponding addresses.

Table 1. Register Summary

Hex Address	Access	Register Name	Hard Reset Default
0x0000	RD/WR	"Interrupt Enable Register #1, Read/Write 0x0000"	0x0000
0x0001	RD/WR	"Configuration Register #1, Read/Write 0x0001"	0x0000
0x0002	RD/WR	"Configuration Register #2, Read/Write 0x0002"	0x0000
0x0003	WR	"Start/Reset Register, Write Only 0x0003"	0x0000
0x0003	RD	"Command Stack Pointer Register/ Enhanced BC Instruction List Register, Read Only 0x0003"	0x0000
0x0004	RD/WR	"BC Control Word Register, Read/Write 0x0004" / "RT Subaddress Control Word Register, Read/Write 0x0004"	0x0000
0x0005	RD/WR	"Time Tag Register, Read/Write 0x0005"	0x0000
0x0006	RD	"Interrupt Status Register #1, Read Only 0x0006"	0x0000
0x0007	RD/WR	"Configuration Register #3, Read/Write 0x0007"	0x0000
0x0008	RD/WR	"Configuration Register #4, Read/Write 0x0008"	0x0000
0x0009	RD/WR	"Configuration Register #5, Read/Write 0x0009"	Note 1
0x000A	RD/WR	"RT/Monitor Data Stack Address Register, Read/Write 0x000A"	0x0000
0x000B	RD	"BC Frame Time Remaining Register, Read Only 0x000B"	0x0000
0x000C	RD	"BC Message Time Remaining Register, Read Only 0x000C"	0x0000
0x000D	RD/WR	"Non-Enhanced BC Frame Time / Enhanced BC Initial Instruction Pointer / RT Last Command / MT Trigger Register, Read/Write 0x000D"	0x0000
0x000E	RD	"RT Status Word Register, Read Only 0x000E"	0x0000
0x000F	RD	"RT BIT Word Register, Read Only 0x000F"	0x0000
0x0010	–	Test Mode Register 0	0x0000
0x0011	–	"Test Mode Register 1, ETest Register, Read/Write 0x0011"	0x0000
0x0012	–	Test Mode Register 2	0x0000
0x0013	–	Test Mode Register 3	0x0000
0x0014	–	Test Mode Register 4	0x0000
0x0015	–	Test Mode Register 5	0x0000
0x0016	–	Test Mode Register 6	0x0000

Registers and Command/Status Words

Hex Address	Access	Register Name	Hard Reset Default
0x0017	–	Test Mode Register 7	0x0000
0x0018	RD/WR	"Configuration Register #6, Read/Write 0x0018"	0x0000
0x0019	RD/WR	"Configuration Register #7, Read/Write 0x0019"	0x0000
0x001A	–	Reserved	0x0000
0x001B	RD	"BC Condition Code Register, Read Only 0x001B"	0x0000
0x001B	WR	"BC General Purpose Flag Register, Write Only 0x001B"	0x0000
0x001C	RD	"BIT Test Status Flag Register, Read Only 0x001C"	Note 2
0x001D	RD/WR	"Interrupt Enable Register #2, Read/Write 0x001D"	0x0000
0x001E	RD	"Interrupt Status Register #2, Read Only 0x001E"	Note 2
0x001F	RD/WR	"BC General Purpose Queue Pointer Register / RT, MT Interrupt Status Queue Pointer Register, Read/Write 0x001F"	0x0000

NOTES:

1. Bits SNGLEND, TXINHA, TXINHB, RTAD[4:0] and RTADP will reflect the logic values of their respective input pins.
2. Following Built-in Self Test, registers 0x001C (BIT Test Status Register) and 0x001E (Interrupt Status Register 2) will be non-zero. The value of register 0x001C will depend on the result of the Built-in Self Test. In register 0x001E, bit 2, BIST, will be set to logic "1" following Built-in Self Test.

2.1. Interrupt Enable Register #1, Read/Write 0x0000

Setting a respective bit below to logic “1” will cause an interrupt to be generated when the corresponding event occurs. The equivalent bit in Interrupt Status Register #1 will also be set to logic “1” regardless of whether the enable bit is set or not. Setting a respective bit below to logic “0” will disable (mask) the interrupt.

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)		–	0	Reserved
14	RAMPE	R/W	0	Two Bit RAM Error Detected Set RAMPE to logic “1” to generate an interrupt when a two bit RAM error occurs. Bit 14 in Configuration Register #2 must be set to logic “1” to enable two bit error detection. Note: The device ECC SRAM will automatically detect and correct single bit RAM errors. Corrected single bit errors are not logged.
13	TXTO	R/W	0	Set TXTO to logic “1” to generate an interrupt when a transmitter time-out occurs.
12	STKRO	R/W	0	Set STKRO to logic “1” to generate an interrupt when a command stack rollover occurs. When in BC Mode, this applies to the BC Command Stack. When in RT Mode, this applies to the RT Command Stack.
11	MTRO	R/W	0	Set MTRO to logic “1” to generate an interrupt when an MT command stack rollover occurs.
10	MTDRO	R/W	0	Set MTDRO to logic “1” to generate an interrupt when an MT data stack rollover occurs.
9	HSKF	R/W	0	Set HSKF to logic “1” to generate an interrupt when a handshake failure occurs between the device and external RAM in Transparent Mode.
8	BCRTY	R/W	0	Set BCRTY to logic “1” to generate an interrupt when the BC tries to re-send a message, regardless of whether the retry was successful or not.
7	RTAPF	R/W	0	Set RTAPF to logic “1” to generate an interrupt when the The Remote Terminal address and parity bits do not exhibit odd parity.
6	TTRO	R/W	0	Set TTRO to logic “1” to generate an interrupt when the time tag counter rolls over.
5	RTCIRO	R/W	0	Set RTCIRO to logic “1” to generate an interrupt when the RT circular buffer rolls over
4	CWEOM	R/W	0	Set CWEOM to logic “1” to generate an interrupt at the end of the current message provided the EOM interrupt is enabled in the respective BC or RT subaddress control word.
3	BCEOF	R/W	0	Set BCEOF to logic “1” to generate an interrupt at the end of the current BC frame
2	ERR	R/W	0	Set ERR to logic “1” to generate an interrupt when a 1553 Message Error, loopback failure or response timeout is detected

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th colspan="2">Bit Description</th></tr>
<tr><td rowspan="4">1</td><td rowspan="4">BRMINT</td><td rowspan="4">R/W</td><td rowspan="4">0</td><td colspan="2">The function of this bit depends on whether the device is operating in BC, RT or MT mode as follows:
Set BRMINT to logic “1” to generate an interrupt when the conditions below are met:</td></tr>
<tr><td>BC Mode</td><td>A received RT Status Word contains the wrong RT address or an unexpected status bit value.</td></tr>
<tr><td>Enhanced RT Mode</td><td>A valid Mode Command is received.</td></tr>
<tr><td>Word Monitor Mode</td><td>A valid received command word matches the value programmed in the Monitor Trigger Register.</td></tr>
<tr><td>0 (LSB)</td><td>EOM</td><td>R/W</td><td>0</td><td colspan="2">Set EOM to logic “1” to generate an interrupt at the end of every message.</td></tr>
</table>

2.2. Configuration Register #1, Read/Write 0x0001

Configuration Register #1 is used to select the device’s mode of operation and for software control of operational features such as RT Status Word bits, Time-Tagging, etc. Specific bit functionality depends on the selected mode of operation as outlined in the Tables below.

Table 2. Configuration Register #1, Non-Enhanced BC Mode (Legacy).

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	MODE1	R/W	1	Set to logic “0” for BC mode of operation.
14	MODE2	R/W	0	Initializes logic “0” in BC mode.
13	MEMAB	R/W	0	This bit indicates which fixed memory location is used. If MEMAB is logic “0”, Location A is used If MEMAB is logic “1”, Location B is used.
12	ABRTME	R/W	0	Set ABORTME to logic “1” to abort message processing at the end of the current message when the BC encounters a message error. BC Message processing will continue if an optional message retry is successful.
11 − 0	-	R/W	0	Used only in Enhanced BC Mode (see below)

Table 3. Configuration Register #1, Enhanced BC Mode.

To enable Enhanced BC Mode, bit 15 of Configuration Register #1 should be set to logic “0” **AND** bit 15 of Configuration Register #3 should be set to logic “1”.

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	MODE1	R/W	1	Set to logic “0” for BC mode of operation.
14	MODE2	R/W	0	Initializes logic “0” in BC mode.
13	MEMAB	R/W	0	Current Memory Pointer. Logic “0” for Location A, logic “1” for Location B.
12	ABRTME	R/W	0	Abort at End of Message if Error. Set to logic “1” to abort message processing at the end of the current message when the BC encounters an error. BC Message processing will continue if the message retry feature is enabled and retry is successful.
11	ABRTFE	R/W	0	Abort at End of Frame if Error. Set to logic “1” to abort message processing at the end of the current frame when the BC encounters an error. BC Message processing will continue if the message retry feature is enabled and retry is successful.
10	ABRTMES	R/W	0	Abort at End of Message if Status Bits Set. Set to logic “1” to abort message processing at the end of the current message when non-masked Status Word bits are set unexpectedly. BC Message processing will continue if the message retry feature is enabled and retry is successful.
9	ABRTFES	R/W	0	Abort at End of Frame if Status Bits Set. Set to logic “1” to abort message processing at the end of the current frame (even if Auto Frame Repeat is enabled) when non-masked Status Word bits are set unexpectedly. BC Message processing will continue if the message retry feature is enabled and retry is successful.
8	AFR	R/W	0	Auto Frame Repeat. Logic “0”: The host manually starts each BC frame. Logic “1”: BC frame will repeat indefinitely provided none of the conditions outlined in bits 12:9 occur or the part is not reset. A fixed frame time may be set by setting bit 6, Internal Trigger below.
7	ETRIG	R/W	0	External Trigger. Set to logic “1” to start BC message processing via rising edge of EXT_TRIG signal.

Bit No.	Mnemonic	R/W	Reset	Bit Description
6	ITRIG	R/W	0	Internal Trigger. This bit is used in conjunction with bit 8, Auto Frame Repeat, to automatically repeat the BC frame with a fixed frame time. The time is set in increments of 100µs (up to 6.55 sec.) according to the value specified by the BC Frame Time Register. Logic “1”: Enable. Logic “0”: Disable. Stop after a single frame.
5	GAPTMR	R/W	0	Message Gap Timer. Logic “0”: Default message gap (~10µs). Logic “1”: The message gap is defined in steps of 1µs in the third word of the BC Message Block Descriptor (the defined value may be 10µs − 65.535 ms)
4	RTY	R/W	0	Message Retry. Logic “1”: Enable BC message retries by setting bit 8 in the respective BC control word. Logic “0”: Disable message retries.
3	RTY2X	R/W	0	If RTY2X is set to logic “1” and retries are enabled by setting bit 4 above, then the BC will retry again if the first attempt was unsuccessful. If RTY2X is set to logic “0”, then retry only once.
2	BCEN	R	0	BC Enabled. Logic “1” indicates the BC state machine is enabled, i.e. is active and processing messages. Logic “0” indicates the BC is in Idle mode.
1	BCFIP	R	0	This bit will read logic “1” for the start of the first message to the end of the last message in a BC frame.
0 (LSB)	BCMIP	R	0	This bit will read logic “1” for the duration of all BC messages.

Table 4. Configuration Register #1, RT Mode (without Alternate Status Word).

Configuration Register #3, bit 5 = logic “0”. For Enhanced RT operation, bit 15 of Configuration Register #3 should be set to logic “1”.

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	MODE1	R/W	1	Set to logic “1” for RT mode of operation.
14	MODE2	R/W	0	If bit 15 is logic “1” for RT operation, this bit should be logic “0”. In this case, enable MT mode (i.e. RT/MT) by setting bit 12 of this register.
13	MEMAB	R/W	0	Current Memory Pointer. Logic “0” for Location A, logic “1” for Location B.
12	MTEN	R/W	0	Message Monitor Enable Logic “1”: Enable Message Monitor. Logic “0”: Disable Message Monitor.
11	DBAC	R/W	0	Dynamic Bus Control Acceptance, active low. Logic “0”: The RT will respond to a Dynamic Bus Control Mode Code Command by setting the Dynamic Bus Control Acceptance bit in the RT Status Word. Logic “1”: The Dynamic Bus Control Acceptance bit in the RT Status Word will always be zero.
10	BUSY	R/W	0	Busy Bit, active low. Logic “0” will result in “busy” status set. The RT will not respond to commands and will transmit the RT Status Word with the busy bit set. Logic “1” results in the busy bit not set in the RT Status Word and the RT will respond to commands in the normal way.
9	SVCREQ	R/W	0	Service Request Bit, active low. Logic “0” will result in the Service Request bit set in the RT Status Word. Logic “1” will result in the Service Request bit not set in the RT Status Word.
8	SSYS	R/W	0	Subsystem Flag Bit, active low. Logic “0” will result in the Subsystem Flag bit set in the RT Status Word. Logic “1” will result in the Subsystem Flag bit not set in the RT Status Word.

Bit No.	Mnemonic	R/W	Reset	Bit Description
7	TF	R/W	0	Terminal Flag Bit, active low. Enhanced Mode only (Configuration Register #3, bit 15 = logic “1”). Logic “0” will result in the Terminal Flag bit set in the RT Status Word. Logic “1” will result in the Terminal Flag bit not set in the RT Status Word.
6 − 1		-	-	Not used.
0 (LSB)	RTMIP	R	0	RT Message in Progress. Enhanced Mode only (Configuration Register #3, bit 15 = logic “1”). Logic “1” indicates the RT is processing a message. Set just before SOM and reset just after EOM.

Table 5. Configuration Register #1, RT Mode (with Alternate Status Word).

Configuration Register #3, bit 5 = logic “1”. Bits 11 − 1 of the RT status word are programmable directly by the host. For use of the RT Alternate Status word, Enhanced RT operation must be activated (bit 15 of Configuration Register #3 should be set to logic “1”).

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	MODE1	R/W	1	Set to logic “1” for RT mode of operation.
14	MODE2	R/W	0	Set to logic “0” for RT mode of operation.
13	MEMAB	R/W	0	Current Memory Pointer. Logic “0” for Location A, logic “1” for Location B.
12	MTEN	R/W	0	Message Monitor Enable Logic “1”: Enable Message Monitor. Logic “0”: Disable Message Monitor.
11	MERR	R/W	0	If this bit is logic “1”, the Message Error bit (bit 9) of the RT Status Word will be set.
10	INS	R/W	0	If this bit is logic “1”, the Instrumentation bit (bit 10) of the RT Status Word will be set.
9	SVCREQ	R/W	0	If this bit is logic “1”, the Service Request bit (bit 11) of the RT Status Word will be set.
8	RSRV1	R/W	0	If this bit is logic “1”, bit 12 of the RT Status Word will be set.
7	RSRV2	R/W	0	If this bit is logic “1”, bit 13 of the RT Status Word will be set.
6	RSRV3	R/W	0	If this bit is logic “1”, bit 14 of the RT Status Word will be set.

Bit No.	Mnemonic	R/W	Reset	Bit Description
5	BCST	R/W	0	If this bit is logic “1”, Broadcast Command Received bit (bit 15) of the RT Status Word will be set.
4	BUSY	R/W	0	If this bit is written logic “1”, the Busy bit (bit 16) of the RT Status Word will be set.
3	SSYS	R/W	0	If this bit is written logic “1”, the Subsystem Flag bit (bit 17) of the RT Status Word will be set.
2	DBAC	R/W	0	If this bit is written logic “1”, bit 18 of the RT Status Word will be set.
1	TF	R/W	0	If this bit is written logic “1”, the Terminal Flag bit (bit 19) of the RT Status Word will be set.
0 (LSB)	RTMIP	R	0	RT Message in Progress. Logic “1” indicates the RT is processing a message. Set just before SOM and reset just after EOM.

Table 6. Configuration Register #1, Enhanced Monitor Mode.

Enhanced mode is activated by setting bit 15 of Configuration Register #3 to logic “1”. Bits 15 − 13 apply to both Enhanced and non-Enhanced Modes. Bits 12 − 0 only apply in Enhanced Mode.

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	MODE1	R/W	1	Set to logic “0” for MT mode of operation.
14	MODE2	R/W	0	Set to logic “1” for MT mode of operation.
13	MEMAB	R/W	0	Current Memory Pointer. Logic “0” for Location A, logic “1” for Location B.
12	MTEN	R/W	0	Message Monitor Enable Logic “1”: Enable Message Monitor. Logic “0”: Disable Message Monitor.
11	TRIGEN	R/W	0	Word Monitor Trigger Enable. Enable with logic “1”. This bit must be set in Word Monitor Mode to enable a monitor start via EXT_TRIG (bit 7 below set to logic “1”) or via successful comparison between a received valid word and the word stored in the MT Trigger Resister (0x00D).
10	TRSTRT	R/W	0	Start Word Monitor on Trigger. Enable with logic “1”. The Word Monitor will start monitoring following successful comparison between a received valid word and the word stored in the MT Trigger Resister (0x00D).

Bit No.	Mnemonic	R/W	Reset	Bit Description
9	TRSTOP	R/W	0	Stop Word Monitor on Trigger. Enable with logic "1". The Word Monitor will stop monitoring following successful comparison between a received valid word and the word stored in the MT Trigger Resister (0x00D).
8	-	-	-	Not used.
7	EXTTRIG	R/W	0	External Trigger. Set to logic "1" to start MT via rising edge of EXT_TRIG signal. Monitor trigger must also be enabled by setting bit 11 of this register.
6 − 3	-	-	-	Not used.
2	MEN	R	0	Monitor Enabled. A logic "1" indicates the Monitor is enabled.
1	MTR	R	0	Monitor Triggered. A logic "1" indicates the Monitor was triggered either by successful comparison with the word in the MT Trigger Resister (0x00D) or via rising edge of the EXT_TRIG signal..
0 (LSB)	MACT	R	0	Monitor Active. In the Word Monitor mode, this bit will return a logic "1" after the Word Monitor has been started. In the Message Monitor mode, MACT will return logic "1" only when the Message Monitor is currently storing the words of a selected message. MONITOR ACTIVE will return logic "0" when the monitor is in its off-line state.

2.3. Configuration Register #2, Read/Write 0x0002

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	EINTEN	R/W	0	Set EINTEN to logic “1” to enable Enhanced Interrupts.
14	RAMP	R/W	0	Two Bit RAM Error Detect Setting RAMP bit to logic “1” enables **two** bit RAM error detection. An interrupt may be generated for detection of two bit errors by setting bit 14, RAMPE, in the Interrupt Enable Register #1 to logic “1”. **Note:** The device ECC SRAM will automatically detect and correct single bit RAM errors, regardless of the state of this bit. Corrected single bit errors are not logged.
13	BUSYLU	R/W	0	Set BUSYLU to logic “1” to enable the Busy Lookup Table.
12	DBUF	R/W	0	Set DBUF to logic “1” to enable Double Buffering for Rx messages (see bit 1 below).
11	OVINV	R/W	0	Setting OVINV to logic “1” will cause invalid circular buffer data to be overwritten.
10	256RO	R/W	0	If 256RO is logic “0”, data buffers in RAM will rollover at 256-word boundaries. That is memory addresses will rollover from 0xXXFF to 0xXX00, rather than incrementing to 0x(XX+1)00. If 256RO is logic “1”, this will enable 256-word boundaries to be crossed for both Legacy BC Message/Data Blocks and RT Data Blocks. In this case the address will increment from 0xXXFF to 0x(XX+1)00. This bit has no effect on the Legacy BC Command Stack or the RT Command Stack. This bit is ignored in the Enhanced BC Mode. Note: If 256RO is programmed to logic “1” in Remote Terminal mode, the size for all circular buffers effectively becomes 65,536 words regardless of how the Subaddress Control Words are set. It is recommended that this bit is set to logic “1” for BC mode and to logic “0” for RT mode.

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th colspan="4">Bit Description</th></tr>
<tr><td rowspan="10">9 − 7</td><td rowspan="10">TTRES</td><td rowspan="10">R/W</td><td rowspan="10">0</td><td colspan="4">Time Tag Resolution bits. Bits 9 − 7 set the time tag resolution as follows:</td></tr>
<tr><td>Bit 9</td><td>Bit 8</td><td>Bit 7</td><td>Time Tag Resolution</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>64 μs</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>32 μs</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>16 μs</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>8 μs</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4 μs</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>2 μs</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>The Time Tag is incremented by writing logic “1” to bit 4 of the Start/Reset Register.</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>The Time Tag is incremented by means of an external clock connected to TAG_CLK.</td></tr>
<tr><td>6</td><td>TTSYNC</td><td>R/W</td><td>0</td><td colspan="4">In RT Mode, setting this bit to logic “1” will clear the Time Tag counter when a Synchronize Without Data mode command is received.</td></tr>
<tr><td>5</td><td>SYNCDAT</td><td>R/W</td><td>0</td><td colspan="4">In RT Mode, setting this bit to logic “1” will cause the data word in a received Synchronize With Data mode command to loaded into the Time Tag Register.
In BC Mode, setting this bit to logic “1” will allow the value of the Time Tag Register to be transmitted as the data word in a Synchronize With Data mode command.</td></tr>
<tr><td>4</td><td>CLRSTAT</td><td>R/W</td><td>0</td><td colspan="4">Logic “1”: Clear Interrupt Status Registers #1 or #2 when read respectively.
Logic “0”: Clear both Interrupt Status Registers #1 and #2 by writing logic “1” to bit 2, Start/Reset Register 0x003.</td></tr>
<tr><td>3</td><td>LEVEL</td><td>R/W</td><td>0</td><td colspan="4">This bit sets whether the interrupt output signal INT is a continuous level or a pulse.
Logic “1”: The $\overline{INT}$ output signal will be a level that will remain low until Interrupt Status Registers #1 and #2 are cleared.
Logic “0”: The $\overline{INT}$ output signal will be a 500ns pulse.</td></tr>
<tr><td>2</td><td>SRREQ</td><td>R/W</td><td>0</td><td colspan="4">Logic “0”: The Service Request bit in the RT Status Word may only be controlled by the host.
Logic “1”: The Service Request bit in the RT Status Word may be controlled by the host, but is cleared when the RT responds to a Transmit Vector Word mode code command</td></tr>
</table>

Bit No.	Mnemonic	R/W	Reset	Bit Description
1	ENRTBUF	R/W	0	This bit is used to set the Enhanced RT buffering mode. ENRTBUF = logic “0”: If bit 12 of this register is logic “1”, double buffer mode will be set globally for all Rx commands. If bit 12 is logic “0”, single buffer mode will be set. ENRTBUF = logic “1”: Each Rx subaddress can have a different buffering mode, set by the individual subaddress control word.
0 (LSB)	NOTICE2	R/W	0	Notice 2 Broadcast Data Storage. If this bit is logic “1”, the terminal stores data associated with broadcast commands separately from data associated with non-broadcast commands to meet the requirements of MIL-STD-1553B Notice 2. If this bit is logic “0”, broadcast command data is stored in the same buffer with data from nonbroadcast commands.

2.4. Command Stack Pointer Register/ Enhanced BC Instruction List Register, Read Only 0x0003

When read, this register contains the current value of the Stack Pointer for RT, MT and non-enhanced BC modes. In Enhanced BC Mode, this register will contain a pointer to the BC Instruction List.

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0 (LSB)	R	0	Command Stack Pointer, bits[15 − 0] respectively.

2.5. Start/Reset Register, Write Only 0x0003

When writing to this register, all reserved bits must be written logic “0”.

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB) − 12		W	0	Reserved.
11	RTON	W	0	If the RT goes offline following receipt of an Initiate Self-Test mode command (RTOFF bit 4 of Configuration Register #7 set), then the RT will automatically restart following completion of the self-test. However, if the host does not run the self-test by setting bit 7 of this register, then this bit should be set in order to bring the RT back online.
10	CLRST	W	0	Setting CLRST to logic “1” will clear the Self-Test Register
9	RAMST	W	0	Setting RAMST to logic “1” will initiate a RAM Self-Test
8	-	W	0	Reserved
7	PROST	W	0	Setting PROST to logic “1” will initiate a Protocol Self-Test
6	STOPMSG	W	0	In BC Mode, setting this bit will stop operation at End-of-Message. In MT Mode, setting this bit will stop message monitoring.
5	BCSTOPFR	W	0	In BC Mode, setting this bit will stop operation at End-of-Frame.
4	TTINC	W	0	Setting this bit will increment the Time Tag Counter by “1” LSB when Time Tag Resolution bits 9-7 of Configuration Register #2 are set to “110”.
3	TTRST	W	0	Setting TTRST to logic “1” will reset the Time Tag Counter.
2	INTRST	W	0	Setting this bit will clear Interrupt Status Registers #1 and #2.
1	BCMTSTRT	W	0	In BC Mode, setting this bit will start the BC. In MT Mode, setting this bit will start the MT.
0 (LSB)	SFTRESET	W	0	Setting this bit will initiate a software reset.

2.6. BC Control Word Register, Read/Write 0x0004

The BC Control Word is the first word in each Message Control / Status Block. The BC Control Word is not transmitted on the MIL-STD-1553 bus. This word is initialized and maintained by the host to specify message attributes such as bit masks for the received RT Status Word, which bus to use, enabling self test, BC message format, etc.

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	TXTTMC17	R/W	0	Transmit Time Tag for Synchronize (with data) Mode Code Command (MC17). If TXTTMC17 bit is logic "0" the BC transmits the value contained in the Message Data Block as the data word for a "synchronize" mode code command MC17. If TXTTMC17 bit is logic "1", the "synchronize" mode data word value originates from the value of the Time Tag Register. Bit 5 of Configuration Register #2 must also be set.
14	MEMASK	R/W	0	Message Error Bit Mask. If MEMASK bit is logic "0" and the Message Error bit is logic 1 in the received RT Status Word, the BC will recognise the Message Error status. If MEMASK bit is logic "1", the Message Error bit in the received RT Status Word is masked and is treated by the BC as "Don't Care".
13	SRQMASK	R/W	0	Service Request Bit Mask. If SRQMASK bit is logic "0" and the Service Request bit is logic 1 in the received RT Status Word, the BC will recognise the Service Request status. If SRQMASK bit is logic "1", the Service Request bit in the received RT Status Word is masked and is treated by the BC as "Don't Care".
12	BSYMASK	R/W	0	Busy Bit Mask. If BSYMASK bit is logic "0" and the Busy bit is logic 1 in the received RT Status Word, the BC will recognise the Busy status. If BSYMASK bit is logic "1", the Busy bit in the received RT Status Word is masked and is treated by the BC as "Don't Care".
11	SSYSMASK	R/W	0	Subsystem Flag Bit Mask. If SSYSMASK bit is logic "0" and the Subsystem Flag bit is logic 1 in the received RT Status Word, the BC will recognise the Subsystem Flag status. If SSYSMASK bit is logic "1", the Subsystem Flag bit in the received RT Status Word is masked and is treated by the BC as "Don't Care".

Bit No.	Mnemonic	R/W	Reset	Bit Description
10	TFMASK	R/W	0	Terminal Flag Bit Mask. If TFMASK bit is logic “0” and the Terminal Flag bit is logic 1 in the received RT Status Word, the BC will recognise the Terminal Flag status. If TFMASK bit is logic “1”, the Terminal Flag bit in the received RT Status Word is masked and is treated by the BC as “Don’t Care”.
9	RSVMASK	R/W	0	Reserved Bits Mask. If RSVMASK bit is logic “0” and one or more of the three Reserved bits is logic “1” in the received RT Status Word, the BC will recognise the Reserved status. If RSVMASK bit is logic “1”, the Reserved bits in the received RT Status Word are masked and are treated by the BC as “Don’t Care”.
8	RTRYENA	R/W	0	Retry Enabled. If RTRYENA is set to logic “1”, failed messages will be retried according to Configuration Register settings.
7	USEBUSA	R/W	0	Use Bus A/$\overline{B}$. If this Control Word bit is logic “1”, the BC transmits the command on Bus A. If this Control Word bit is logic “0”, the BC transmits the command on Bus B.
6	SELFTST	R/W	0	Self-Test Message Off-Line. If SELFTST is logic “1”, an internal loopback test (bus transmission disabled) is performed.
5	MASKBCR	R/W	0	Mask Broadcast Command Received Bit. If MASKBCR bit is logic “0” and the Broadcast Command Received bit is logic “1” in the received RT Status Word, the BC will recognise the Broadcast status. If MASKBCR bit is logic “1”, the Broadcast Command Received bit in the received RT Status Word is masked and is treated by the BC as “Don’t Care”.
4	EOMINT	R/W	0	End of Message Interrupt. If EOMINT is logic “1”, an interrupt request will be generated (if not masked in Interrupt Mask Register #1) upon message completion.
3	1553AB	R/W	0	1553A/B Select. If 1553AB is Logic “1”, RT response will comply with MIL-STD-1553A. If 1553AB is Logic “0”, RT response will comply with MIL-STD-1553B.

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th colspan="4">Bit Description</th></tr>
<tr><td rowspan="10">2 − 0 (LSB)</td><td rowspan="10">BCMSGFT</td><td rowspan="10">R/W</td><td rowspan="10">0</td><td colspan="4">BC Message Format.
The BC Message format is defined by these three bits as follows:</td></tr>
<tr><td>Bit 2</td><td>Bit 1</td><td>Bit 0</td><td>BC Message Format</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>BC-to-RT</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>RT-to-RT</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Broadcast</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Broadcast RT-to-RTs</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Mode Code</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Not Used</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Broadcast Mode Code</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Not Used</td></tr>
</table>

2.7. RT Subaddress Control Word Register, Read/Write 0x0004

This register enables the buffering mechanism for transmit, receive and broadcast subaddresses, either globally or for individual subaddresses (via the subaddress control word lookup table). It is Read-Only when the RT is active and reads back the value of the last received control word. It may be written for test purposes when the RT is Idle.

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	DBGB	R/W	0	If this bit is logic "0" then circular or single message buffering will be enabled for individual subaddresses (see MEMx bits below). If this bit is logic "1", then double buffering will be enabled for individual subaddresses. Note, DBUF bit 12 of Configuration Register #2 should be also be set. For individual subaddress buffering, enhanced RT buffering must be enabled (set ENRTBUF bit 1 of Configuration Register #2). Combinations of the MEMx bits below set the size of the buffer. To enable double buffering, DBUF bit 12 of Configuration Register #2 should be set. To enable circular buffering, CIRCEN bit 12 of Configuration Register #6 should be set. **Note:** This bit is ignored for Tx subaddresses.
14	TXEOM	R/W	0	TXEOM = logic "1" enables an interrupt to be generated when the end of a message occurs for a transmit subaddress.
13	TXCIR	R/W	0	TXCIR = logic "1" enables an interrupt to be generated when a transmit subaddress circular buffer rolls over.

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th colspan="4">Bit Description</th></tr>
<tr><td rowspan="10">12 − 10</td><td rowspan="10">TXMEM[2:0]</td><td rowspan="10">R/W</td><td rowspan="10">0</td><td colspan="4">These bits set the buffer type and size for transmit subaddress buffering as follows:</td></tr>
<tr><td>TXMEM2 bit 12</td><td>TXMEM1 bit 11</td><td>TXMEM0 bit 10</td><td>Buffering Mode</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Individual Tx subaddress single message buffering</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Individual Tx subaddress circular buffering, 128 Words</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Individual Tx subaddress circular buffering, 256 Words</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Individual Tx subaddress circular buffering, 512 Words</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Individual TX subaddress circular buffering, 1024 Words</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Individual TX subaddress circular buffering, 2048 Words</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Individual Tx subaddress circular buffering, 4096 Words</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Individual Tx subaddress circular buffering, 8192 Words</td></tr>
<tr><td>9</td><td>RXEOM</td><td>R/W</td><td>0</td><td colspan="4">RXEOM = logic “1” enables an interrupt to be generated when the end of a message occurs for a receive subaddress.</td></tr>
<tr><td>8</td><td>RXCIR</td><td>R/W</td><td>0</td><td colspan="4">RXCIR = logic “1” enables an interrupt to be generated when a receive subaddress circular buffer rolls over.</td></tr>
</table>

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th colspan="5">Bit Description</th></tr>
<tr><td rowspan="12">7 − 5</td><td rowspan="12">RXMEM[2:0]</td><td rowspan="12">R/W</td><td rowspan="12">0</td><td colspan="5">These bits set the buffer type and size for receive subaddress buffering as follows:</td></tr>
<tr><td>DBGB bit 15</td><td>RXMEM2 bit 7</td><td>RXMEM1 bit 6</td><td>RXMEM0 bit 5</td><td>Buffering Mode</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Individual Rx subaddress single message buffering</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Individual Rx subaddress circular buffering, 128 Words</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Individual Rx subaddress circular buffering, 256 Words</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Individual Rx subaddress circular buffering, 512 Words</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Individual RX subaddress circular buffering, 1024 Words</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Individual RX subaddress circular buffering, 2048 Words</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Individual Rx subaddress circular buffering, 4096 Words</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Individual Rx subaddress circular buffering, 8192 Words</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Double buffering for individual Rx subaddresses.</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Global circular buffering for all Rx subaddresses. The size of the buffer is set by bits CIRSZE[11:9] of Configuration Register #6.</td></tr>
<tr><td>4</td><td>BCSTEOM</td><td>R/W</td><td>0</td><td colspan="5">BCSTEOM = logic “1” enables an interrupt to be generated when the end of a message occurs for a broadcast subaddress.</td></tr>
<tr><td>3</td><td>BCSTCIR</td><td>R/W</td><td>0</td><td colspan="5">BCSTCIR = logic “1” enables an interrupt to be generated when a broadcast subaddress circular buffer rolls over.</td></tr>
</table>

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th colspan="5">Bit Description</th></tr>
<tr><td rowspan="12">2 − 0</td><td rowspan="12">BCSTMEM[2:0]</td><td rowspan="12">R/W</td><td rowspan="12">0</td><td colspan="5">These bits set the buffer type and size for broadcast subaddress buffering as follows:</td></tr>
<tr><td>DBGB bit 15</td><td>BCSTMEM2 bit 2</td><td>BCSTMEM1 bit 1</td><td>BCSTMEM0 bit 0</td><td>Buffering Mode</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Individual BCST subaddress single message buffering</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Individual BCST subaddress circular buffering, 128 Words</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Individual BCST subaddress circular buffering, 256 Words</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Individual BCST subaddress circular buffering, 512 Words</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Individual BCST subaddress circular buffering, 1024 Words</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Individual BCST subaddress circular buffering, 2048 Words</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Individual BCST subaddress circular buffering, 4096 Words</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Individual BCST subaddress circular buffering, 8192 Words</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Double buffering for individual BCST subaddresses.</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Global circular buffering for all BCST subaddresses. The size of the buffer is set by bits CIRSZE[11:9] of Configuration Register #6.</td></tr>
</table>

2.8. Time Tag Register, Read/Write 0x0005

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0 (LSB)	R/W	0	This register contains the current value of the time tag counter. The resolution of the Time Tag (in µs/LSB) is programmable through bits 9 − 7 of Configuration Register #2.

2.9. Interrupt Status Register #1, Read Only 0x0006

The bits in this register will be set when the respective event occurs, regardless of whether the interrupt is enabled (equivalent bit set in the Interrupt Enable Register #1) or not.

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	MINT	R	0	This bit only applies when Enhanced Interrupts are enabled by setting bit 15 of Configuration Register #2. MINT will be set to logic “1” if an interrupt request has been generated on the $\overline{\text{INT}}$ output signal.
14	RAMPE	R	0	Two Bit RAM Error Detected This bit, if enabled by bit 14, Interrupt Enable Register #1, will be set to logic “1” when a two bit RAM error is detected. Bit 14, RAMP, in Configuration Register #2, must be set to logic “1” to enable two bit error detection. **Note:** Single bit RAM errors are automatically detected and corrected by the on-chip ECC SRAM.
13	TXTO	R	0	TXTO will be set to logic “1” when a transmitter timeout occurs.
12	STKRO	R	0	STKRO will be set to logic “1” when a command stack rollover occurs. When in BC Mode, this applies to the BC Command Stack. When in RT Mode, this applies to the RT Command Stack.
11	MTRO	R	0	MTRO will be set to logic “1” when an MT command stack rollover occurs.
10	MTDRO	R	0	MTDRO will be set to logic “1” when an MT data stack rollover occurs.
9	HSKF	R	0	HSKF will be set to logic “1” when a handshake failure occurs between the device and external RAM in Transparent Mode.
8	BCRTY	R	0	BCRTY will be set to logic “1” when the BC tries to re-send a message, regardless of whether the retry was successful or not.
7	RTAPF	R	0	RTAPF will be set to logic “1” when the RT address and parity bits do not exhibit odd parity.
6	TTRO	R	0	TTRO will be set to logic “1” when the time tag counter rolls over.
5	RTCIRRO	R	0	RTCIRRO will be set to logic “1” when the RT circular buffer rolls over.

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th colspan="2">Bit Description</th></tr>
<tr><td>4</td><td>CWEOM</td><td>R</td><td>0</td><td colspan="2">CWEOM will be set to logic “1” at the end of the current message provided the EOM interrupt is enabled in the respective BC or RT subaddress control word.</td></tr>
<tr><td>3</td><td>BCEOF</td><td>R</td><td>0</td><td colspan="2">BCEOF will be set to logic “1” at the end of the current BC frame</td></tr>
<tr><td>2</td><td>ERR</td><td>R</td><td>0</td><td colspan="2">ERR will be set to logic “1” when a 1553 Message Error, loopback failure or response timeout is detected</td></tr>
<tr><td rowspan="4">1</td><td rowspan="4">BRMINT</td><td rowspan="4">R/W</td><td rowspan="4">0</td><td colspan="2">The function of this bit depends on whether the device is operating in BC, RT or MT mode as follows:
BRMINT will be set to logic “1” when the conditions below are met:</td></tr>
<tr><td>BC Mode</td><td>A received RT Status Word contains the wrong RT address or an unexpected status bit value.</td></tr>
<tr><td>Enhanced RT Mode</td><td>A valid Mode Command is received.</td></tr>
<tr><td>Word Monitor Mode</td><td>A valid received command word matches the value programmed in the Monitor Trigger Register.</td></tr>
<tr><td>0 (LSB)</td><td>EOM</td><td>R/W</td><td>0</td><td colspan="2">EOM will be set to logic “1” at the end of every message.</td></tr>
</table>

2.10. Configuration Register #3, Read/Write 0x0007

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th colspan="3">Bit Description</th></tr>
<tr><td>15 (MSB)</td><td>ENHANC</td><td>R/W</td><td>0</td><td colspan="3">Set ENHANC to logic “1”, to enable Enhanced Mode operation.</td></tr>
<tr><td rowspan="6">14 − 13</td><td rowspan="6">BCRTSTK[1:0]</td><td rowspan="6">R/W</td><td rowspan="6">0</td><td colspan="3">The BCRTSTK[1:0] bits set the size of the BC (BC Mode) or RT (RT Mode) command stack size as follows:</td></tr>
<tr><th>BCRTSTK 1</th><th>BCRTSTK 0</th><th>BC OR RT Command Stack Size</th></tr>
<tr><td>0</td><td>0</td><td>256 words (64 messages)</td></tr>
<tr><td>0</td><td>1</td><td>512 words (128 messages)</td></tr>
<tr><td>1</td><td>0</td><td>1024 words (256 messages)</td></tr>
<tr><td>1</td><td>1</td><td>2048 words (512 messages)</td></tr>
</table>

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Bit Description</th></tr>
<tr><td>12 − 11</td><td>MTSTK[1:0]</td><td>R/W</td><td>0</td><td>The MTSTK[1:0] bits set the size of the MT command stack size as follows:
<table>
<tr><th>MTSTK 1</th><th>MTSTK 0</th><th>MT Command Stack Size</th></tr>
<tr><td>0</td><td>0</td><td>256 words (64 messages)</td></tr>
<tr><td>0</td><td>1</td><td>1024 words (256 messages)</td></tr>
<tr><td>1</td><td>0</td><td>4096 words (1024 messages)</td></tr>
<tr><td>1</td><td>1</td><td>16384 words (4096 messages)</td></tr>
</table></td></tr>
<tr><td>10 − 8</td><td>MTDATA[2:0]</td><td>R/W</td><td>0</td><td>The MTDATA[2:0] bits set the size of the MT data stack size as follows:
<table>
<tr><th>MTSTK 2</th><th>MTSTK 1</th><th>MTSTK 0</th><th>MT Data Stack Size</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>65,536 words</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>32,768 words</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>16,384 words</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>8,192 words</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4,096 words</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>2,048 words</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1,024 words</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>512 words</td></tr>
</table></td></tr>
<tr><td>7</td><td>ILLOFF</td><td>R/W</td><td>0</td><td>If ILLOFF bit is logic “0”, Command Illegalization is enabled.
If ILLOFF bit is logic “1”, Command Illegalization is disabled and the Illegalizaton Table memory space may be used for data storage. .</td></tr>
<tr><td>6</td><td>MCRSVME</td><td>R/W</td><td>0</td><td>The MCRSVME decides how the RT responds to a received reserved mode command:
Logic “0”: RT doesn’t respond to reserved mode commands. Message Error bit is set.
Logic “1”: RT will respond to reserved mode commands. Message Error bit is not set.</td></tr>
<tr><td>5</td><td>ALTSTAT</td><td>R/W</td><td>0</td><td>Setting ALTSTAT to logic “1” enables the Alternate RT Status Word as follows:
Logic “1”: All RT Status Word response bits may be controlled directly by the Host by setting their respective bits 11 − 1 in Configuration Register #1.
Logic “0”: The Alternate RT Status Word is disabled and only the Dynamic Bus Control Acceptance bit, Busy bit, Service Request bit, Subsystem Flag bit and Terminal Flag bits are programmable by the Host by setting their respective bits 11 − 7 in Configuration Register #1.</td></tr>
</table>

Bit No.	Mnemonic	R/W	Reset	Bit Description
4	NOILLRX	R/W	0	If NOILLRX is set to logic “1”, illegal command data words received by the RT are not stored in RAM. If NOILLRX is set to logic “0”, illegal command data words received by the RT are stored in RAM.
3	NOBUSYRX	R/W	0	If NOBUSYRX is set to logic “1”, the RT responds “Busy status” with the BUSY bit set, but does not store the received data words in RAM. If NOBUSYRX is set to logic “0”, the RT responds “Busy status” with the BUSY bit set and stores the received data words in RAM.
2	RTTFF	R/W	0	Active low. If RTTFF is logic “1” the Terminal Flag bit in the RT status word will be automatically set following a transmitter timeout or loopback failure and control of the Terminal Flag bit is not accessable to the host. If RTTFF is logic “0” the Terminal Flag bit in the RT status word will be automatically set following a transmitter timeout or loopback failure **and** the Terminal Flag bit is also programmable by the host.
1	1553A	R/W	0	If 1553A is set to logic “1”, Mode Codes are processed according to MIL-STD-1553A. If 1553A is set to logic “0”, Mode Codes are processed according to MIL-STD-1553B.
0 (LSB)	ENHMC	R/W	0	If ENHMC is set to logic “1”, enhanced features are enabled for mode command processing. Mode code data words may be stored separately according to whether they are receive, transmit or broadcast and interrupts may be enables for individual mode codes. If ENHMC is set to logic “0”, all mode code data is stored in the same location in RAM.

2.11. Configuration Register #4, Read/Write 0x0008

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	BITW	R/W	0	If BITW is set to logic “0” the RT will respond to a Transmit BIT word mode command with the data word stored in the internal BIT Word Register. If BITW is set to logic “1” the RT will respond to a Transmit BIT word mode command with the data word stored by the host in RAM location 0x0123.

Bit No.	Mnemonic	R/W	Reset	Bit Description
14	INBITW	R/W	0	Setting INBITW to logic “1” will inhibit transmission of the BIT word (in response to a Transmit BIT word mode command) if the Busy bit is set. The RT will respond with the Busy bit set in the RT Status word but no BIT word will be transmitted. If INBITW is logic “0”, the BIT word will be transmitted (in response to a Transmit BIT word mode command), following transmission of the RT Status word with the Busy bit set.
13	MCBUSY	R/W	0	This bit affects RT response to Transmit Vector Word or the Reserved Mode Commands 22 to 31 (decimal) when the busy bit is set. If MCBUSY is logic “1” the RT will respond to the above mode commands with the busy bit set in the RT Status Word, followed by a data word. If MCBUSY is logic “0”, no data word will be transmitted,
12	EBCCW	R/W	0	In BC Mode, setting EBCCW to logic “1” enables all bits of the Expanded BC Control Word. In BC Mode, if EBCCW is logic “0” or if ENHANC bit 15 in Configuration Register #3 is logic “0”, then only bits 7, 6, 5, 2, 1, and 0 in the BC Control Word are enabled.
11	BCSTMEN	R/W	0	In BC Mode, if BCSTMEN is logic “1”, the function of the MASKBCR bit in the BC Control Word is enabled, i.e. if BCSTMEN is logic “1” and MASKBCR bit is logic “0”, the BC will recognise Broadcast status if the Broadcast Command Received bit is logic “1” in the received RT Status Word. If MASKBCR bit is logic “1”, the Broadcast Bit in the received RT Status Word is “Don’t Care”. In BC Mode, if BCSTMEN is logic “0”, the value of the MASKBCR bit in the BC Control Word is XORed with the Broadcast bit in the received RT Status Word.
10	RTY1553A	R/W	0	Setting this bit to logic “1” will cause the BC to try to resend a message in 1553A mode when the Message Error bit in the received RT Status word is set. This is in addition to the normal criteria for retrying failed messages, provided retries are enabled (e.g. response timeout, etc.).
9	RTYSTAT	R/W	0	If RTYSTAT is logic “0”, the BC will not retry to send a message in response to a received RT Status Word bit being set. If RTYSTAT is logic “1”, the BC will retry to send a message in response to a received RT Status Word bit being set, provided retries are enabled.
8	RTY1ALT	R/W	0	If this bit is set to logic “0”, the first retry will be on the same bus as the original failed message. If this bit is set to logic “1”, the first retry will be on the opposite bus from the original failed message.

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th colspan="4">Bit Description</th></tr>
<tr><td>7</td><td>RTY2ALT</td><td>R/W</td><td>0</td><td colspan="4">If this bit is set to logic “0”, the second retry will be on the same bus as the original failed message.
If this bit is set to logic “1”, the second retry will be on the opposite bus from the original failed message.
Note that the second retry option must be enabled by setting RTY2X, bit 3 of Configuration Register #1.</td></tr>
<tr><td>6</td><td>MERVAL</td><td>R/W</td><td>0</td><td colspan="4">When an RT responds to a valid message with the Message Error bit set in the status word, the requested number of data words must follow the status word in order for the response to be valid.
Setting MERVAL to logic “1” allows the message to be also valid if the status word is followed by no data words (e.g. illegal command).</td></tr>
<tr><td>5</td><td>BUSYVAL</td><td>R/W</td><td>0</td><td colspan="4">When an RT responds to a valid message with the Busy bit bit set in the status word, the requested number of data words must follow the status word in order for the response to be valid.
Setting BUSYVAL to logic “1” allows the message to be also valid if the status word is followed with no data words.</td></tr>
<tr><td>4</td><td>MTGAP</td><td>R/W</td><td>0</td><td colspan="4">When in MT mode, this bit allows an additional 20µs to be added to the gap time of consecutive messages when the second message is received on the alternate bus.
Logic “0”: Add 20µs to gap time, even if messages overlap.
Logic “1”: Gap time will remain unchanged.</td></tr>
<tr><td>3</td><td>RTLATEN</td><td>R/W</td><td>0</td><td colspan="4">When set to logic “1”, RTLATEN enables latching of the RT address and parity, provided the input signal RT_AD_LAT is also logic “1”.
When RTLATEN is logic “0”, the RT address and parity will not be latched.
For a more detailed discussion on Latching the RT Address, see Section “4.1. Latching the RT Address and Parity”.</td></tr>
<tr><td rowspan="10">2 − 0
(LSB)</td><td rowspan="10">TEST[2:0]</td><td rowspan="10">R/W</td><td rowspan="10">0</td><td colspan="4">The TEST[2:0] bits are used to set hardware and protocol test conditions:</td></tr>
<tr><td>TEST2</td><td>TEST1</td><td>TEST0</td><td>Description</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Normal Operation.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Test Decoder.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Test Encoder.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Test Protocol.</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Test failsale timer.</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Test Registers.</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Reserved.</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Not supported.</td></tr>
</table>

2.12. Configuration Register #5, Read/Write 0x0009

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th colspan="3">Bit Description</th></tr>
<tr><td>15 (MSB)</td><td>CLKSEL</td><td>R</td><td>0</td><td colspan="3">This Read-Only bit simply returns the value of CLKSEL0, bit 0 of Configuration Register #6.</td></tr>
<tr><td>14</td><td>SNGLEND</td><td>R</td><td>0</td><td colspan="3">This bit reflects the state of the $\overline{\text{SNGL\_END}}$ input signal. See the section Signal Descriptions.</td></tr>
<tr><td>13</td><td>TXINHA</td><td>R</td><td>0</td><td colspan="3">TXINHA will be logic “1” when the TX_INH_A input signal is logic “1”, indicating that transmission on Bus A has been inhibited.</td></tr>
<tr><td>12</td><td>TXINHB</td><td>R</td><td>0</td><td colspan="3">TXINHB will be logic “1” when the TX_INH_B input signal is logic “1”, indicating that transmission on Bus B has been inhibited.</td></tr>
<tr><td>11</td><td>ZEROXEN</td><td>R/W</td><td>0</td><td colspan="3">Setting ZEROXEN to logic “0” will cause the decoder to sample both edges of the clock input.</td></tr>
<tr><td rowspan="6">10 – 9</td><td rowspan="6">RTRTTO[1:0]</td><td rowspan="6">R/W</td><td rowspan="6">0</td><td colspan="3">These two bits set the device RT-to-RT response timeout as follows:</td></tr>
<tr><th>RTRTTO1</th><th>RTRTTO0</th><th>RT-to-RT Response Timeout</th></tr>
<tr><td>0</td><td>0</td><td>18.5 µs</td></tr>
<tr><td>0</td><td>1</td><td>22.5 µs</td></tr>
<tr><td>1</td><td>0</td><td>50.5 µs</td></tr>
<tr><td>1</td><td>1</td><td>130 µs</td></tr>
<tr><td>8</td><td>GTEN</td><td>R/W</td><td>0</td><td colspan="3">If GTEN is set to logic “0”, the device will not check for a minimum gap time between messages.
If GTEN is set to logic “1”, the device will check for a minimum gap time between messages of 2µs. Violating this minimum time will result in the message being invalid.</td></tr>
<tr><td>7</td><td>BCSTDIS</td><td>R/W</td><td>0</td><td colspan="3">If BCSTDIS is set to logic “1”, the device will not recognise subaddress 31 as a Broadcast Command.
If BCSTDIS is set to logic “0”, the device will recognise subaddress 31 as a Broadcast Command.</td></tr>
<tr><td>6</td><td>RTADLAT</td><td>R</td><td>0</td><td colspan="3">This bit reflects the state of the RT_AD_LAT input signal. See the section Signal Descriptions.</td></tr>
<tr><td>5 – 0 (LSB)</td><td>RTAD[4:0]
RTADP (LSB)</td><td>R/W</td><td>0</td><td colspan="3">Writing these lower 6 bits via data lines D5 – D0 provide a mechanism to set the RT Address and Parity bit (LSB) via software.
For a more detailed discussion on Latching the RT Address, see Section “4.1. Latching the RT Address and Parity”.</td></tr>
</table>

2.13. Test Mode Register 1, ETest Register, Read/Write 0x0011

This register configures Encoder test functions. See Section “5.6. Channel A-to-B Wraparound Self-Test” in “Built-In Self-Test (BIST)” for more detailed information.

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	E_CHA	R/W	0	Set Encoder Channel Writing logic “0” sets Channel B. Writing logic “1” to sets Channel A. This bit will read back the inverse value of what was written to it.
14	EVNPAR	R	0	Even Parity RAM Test This bit reads logic “0” by default. **In Register Test Mode** (“Configuration Register #4, Read/Write 0x0008”, bits [2:0] = 101) setting this bit to logic “1” enables Even Parity RAM test.
13	E_TXENA	R/W	0	Encoder Transmit Enable Setting this bit to logic “1” enables encoder transmission
12	E_ENCENA	R/W	0	Encoder Enable Setting this bit to logic “1” enables the encoder
11	E_SYNC	R/W	0	Command/Status Sync Byte Setting this bit to logic “1” results in command/status word sync Setting this bit to logic “0” results in data word sync
10	E_STAT	R/W	0	This bit will read logic “1” if the encoder test in not running. Setting this bit to logic “1” will cause the transmitted encoder test message to be received on the same and alternate bus decoders. Setting this bit to logic “0” will cause the transmitted encoder test message to be received only on the alternate bus decoder.
9	Not used	R	1	This read-only bit has no function in Encoder Test Mode and reads logic “1”.
8 – 6	Not used	R	0	These read-only bits have no function in Encoder Test Mode and read logic “0”.
5	BIT15	R	0	This bit reads back the value of bit 15 and shows which Encoder Channel is set Read logic “0” = Channel B Read logic “1” = Channel A
4	Not used	R	0	This read-only bit has no function in Encoder Test Mode and reads logic “0”.
3	E_BUS	R	0	This bit reads logic “1” if an Encoder Test is Active on Bus A This bit reads logic “0” if an Encoder Test is Active on Bus B

Bit No.	Mnemonic	R/W	Reset	Bit Description
2	Not used	R	0	This read-only bit has no function in Encoder Test Mode and reads logic “0”.
1	TBUSYA	R	0	This Active Low status bit reads logic “0” if there is transmit activity on Bus A.
0	TBUSYB	R	0	This Active Low status bit reads logic “0” if there is transmit activity on Bus B.

2.14. RT/Monitor Data Stack Address Register, Read/Write 0x000A

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0 (LSB)	R/W	0	This register contains the current value of the Data Stack pointer, either RT Data stack or Word Monitor Data Stack, depending on the mode of operation.

2.15. BC Frame Time Remaining Register, Read Only 0x000B

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0 (LSB)	R	0	In BC Mode, this register contains the value of the time remaining in the BC frame. The resolution is 100μs/LSB, with a maximum value of 6.5535s.

2.16. BC Message Time Remaining Register, Read Only 0x000C

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0 (LSB)	R	0	In BC Mode, this register contains the current value of the time-to-next message timer. The resolution is 1μs/LSB, with a maximum value of 65.535ms.

2.17. Non-Enhanced BC Frame Time / Enhanced BC Initial Instruction Pointer / RT Last Command / MT Trigger Register, Read/Write 0x000D

<table>
<tr><th>Bit No.</th><th>R/W</th><th>Reset</th><th colspan="2">Bit Description</th></tr>
<tr><td rowspan="6">15 (MSB) − 0 (LSB)</td><td rowspan="6">R/W</td><td rowspan="6">0</td><td colspan="2">The value of this register depends of the mode of operation as follows:</td></tr>
<tr><td>Mode of Operation</td><td>Register Function</td></tr>
<tr><td>Non-Enhanced BC</td><td>Used to program the BC frame time</td></tr>
<tr><td>Enhanced BC</td><td>Used to program the initial value of the BC instruction list pointer</td></tr>
<tr><td>RT</td><td>Used to store the last command processed by the RT.</td></tr>
<tr><td>Word Monitor</td><td>Used to store the value of the word which will initiate a monitor start if a valid received word matches it.</td></tr>
</table>

2.18. RT Status Word Register, Read Only 0x000E

This register contains the current value of the device RT Status Word. This includes the Alternate RT Status Word, where all lower 11 bits are all programmable by the host.

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 11	R	0	Logic “0”
10	R	0	Message Error Status Bit
9	R	0	Instrumentation Status Bit
8	R	0	Service Request Status Bit
7 − 5	R	0	Reserved bits
4	R	0	Broadcast Command Received Status Bit
3	R	0	Busy Status Bit
2	R	0	Subsystem Flag Status Bit
1	R	0	Dynamic Bus Control Acceptance Status Bit
0 (LSB)	R	0	Terminal Flag Status Bit

2.19. RT BIT Word Register, Read Only 0x000F

This register's bits will read logic "1" to reflect errors flagged by the device. The content of this register will be transmitted to the BC following a "Transmit BIT Word" mode command. It may also be read by the host.

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	TXTO	R	0	Transmitter Timed Out. The transmitter timeout of 668µs was exceeded.
14	LBFB	R	0	Loopback Test Failure B. A loopback failure occurred on Bus B.
13	LBFA	R	0	Loopback Test Failure A. A loopback failure occurred on Bus A.
12	HSF	R	0	Transparent Mode Handshake Failure.
11	TXSDB	R	0	Transmitter Shutdown B. A Transmitter Shutdown mode command was received on Bus A. This mode command shuts down the transmitter of the inactive bus.
10	TXSDA	R	0	Transmitter Shutdown A. A Transmitter Shutdown mode command was received on Bus B. This mode command shuts down the transmitter of the inactive bus.
9	TFINH	R	0	Terminal Flag Inhibited. An Inhibit Terminal Flag mode command was received.
8	BITF	R	0	BIT Test Fail. The device failed its internal Built-In-Test routine.
7	DWCH	R	0	Data Word Count High. The number of data words received in the last message was higher than expected.
6	DWCL	R	0	Data Word Count Low. The number of data words received in the last message was lower than expected.
5	SNYCF	R	0	Incorrect Sync Received. A command sync bit was detected in a data word.
4	INVW	R	0	Invalid Word Received
3	RTRTE	R	0	RT−to−RT Gap / Sync / Address Error. If the device is the receiving RT in an RT-to-RT transfer, this bit will be set if there is a gap time error (gap less than 2µs), incorrect sync or format error, or incorrect RT address.

Bit No.	Mnemonic	R/W	Reset	Bit Description
2	RTRTTO	R	0	RT−to−RT Timeout Error. This bit will be set if the allowed RT-to-RT response time is exceeded. The RT-to-RT response timeout is programmed by setting the RTRT-TO[1:0] bits [10:9] in Configuration Register #5.
1	RTRTCWE	R	0	RT−to−RT Command Word Error . If the device is the receiving RT in an RT-to-RT transfer, this bit will be set if there is an error in the Transmit Command Word, e.g. T/$\overline{R}$ bit is not logic “1”.
0 (LSB)	RXCWE	R	0	Received Command Word Error. This bit will be set if there is an error in a received Command Word

2.20. Configuration Register #6, Read/Write 0x0018

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th colspan="4">Bit Description</th></tr>
<tr><td>15 (MSB)</td><td>ENHBC</td><td>R/W</td><td>0</td><td colspan="4">Setting ENHBC to logic “1” puts the device in Enhanced BC Mode operation.</td></tr>
<tr><td>14</td><td>ENHCPU</td><td>R/W</td><td>0</td><td colspan="4">Setting ENHCPU to logic “1” reduces the wait time for the host to access the bus if a message is in progress. If ENHCPU = logic “0”, the host has to wait until the end of the entire message sequence (approximately 3.6μs for a 20MHz clock).</td></tr>
<tr><td>13</td><td>INCSTK</td><td>R/W</td><td>0</td><td colspan="4">In MT or RT modes, setting INCSTK to logic “1” will cause the command stack pointer to be incremented by 4 at EOM instead of SOM.</td></tr>
<tr><td>12</td><td>CIRCEN</td><td>R/W</td><td>0</td><td colspan="4">Setting CIRCEN to logic “1” enables the RT global circular buffer.</td></tr>
<tr><td rowspan="10">11 – 9</td><td rowspan="10">CIRSZE[2:0]</td><td rowspan="10">R/W</td><td rowspan="10">0</td><td colspan="4">These bits are use to define the size of the global circular buffer as follows:</td></tr>
<tr><th>CIRSZE2</th><th>CIRSZE1</th><th>CIRSZE0</th><th>Global Circular Buffer Size</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Circular buffering not enabled</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>128 words</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>256 words</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>512 words</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1024 words</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>2048 words</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>4096 words</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>8192 words</td></tr>
<tr><td>8</td><td>NOINVMSG</td><td>R/W</td><td>0</td><td colspan="4">If NOINVMSG is set to logic “1” then invalid messages which result in interrupts will not result in any update to the Interrupt Status Queue.</td></tr>
<tr><td>7</td><td>NOVALMSG</td><td>R/W</td><td>0</td><td colspan="4">If NOVALMSG is set to logic “1” then valid messages which result in interrupts will not result in any update to the Interrupt Status Queue.</td></tr>
<tr><td>6</td><td>INTQEN</td><td>R/W</td><td>0</td><td colspan="4">Setting this bit to logic “1” will enable the Interrupt Status Queue.</td></tr>
</table>

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th colspan="3">Bit Description</th></tr>
<tr><td>5</td><td>RTADSRC</td><td>R/W</td><td>0</td><td colspan="3">If RTADSRC is logic “0”, then the source of the RT address and parity will be come from the input signals RTAD[4:0] and RTADP respectively.
If RTADSRC is logic “1”, then the source of the RT address and parity will be come from bits 5 − 0 in Configuration Register #5.
For a more detailed discussion on Latching the RT Address, see Section “4.1. Latching the RT Address and Parity”.</td></tr>
<tr><td>4</td><td>ENHMT</td><td>R/W</td><td>0</td><td colspan="3">This bit affects operation when operating in combined RT/MT Mode. Setting ENHMT to logic “1” results in all command and data words being stored by the MT, including the RT status words.</td></tr>
<tr><td>3</td><td>-</td><td>R/W</td><td>0</td><td colspan="3">Reserved</td></tr>
<tr><td>2</td><td>64WORD</td><td>R/W</td><td>0</td><td colspan="3">Setting this bit to logic “1” expands the device internal register address space. As this accesses unavailable test registers, it is recommended to program this bit to logic “0”.</td></tr>
<tr><td rowspan="6">1 − 0 (LSB)</td><td rowspan="6">CLKSEL[1:0]</td><td rowspan="6">R/W</td><td rowspan="6">0</td><td colspan="3">These two bits select the Clock Frequency according to the table below.</td></tr>
<tr><td>CLKSEL1</td><td>CLKSEL0</td><td>Clock Frequency (MHz)</td></tr>
<tr><td>0</td><td>0</td><td>50</td></tr>
<tr><td>0</td><td>1</td><td>16</td></tr>
<tr><td>1</td><td>0</td><td>20</td></tr>
<tr><td>1</td><td>1</td><td>40</td></tr>
</table>

2.21. Configuration Register #7, Read/Write 0x0019

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB) − 10	MEMADR	R/W	0	Memory Management Base Address, bits[15 − 10] respectively.
9 − 5	-	R/W	0	Reserved.
4	RTOFF	R/W	0	Setting this bit to logic “1” will enable the RT to go offline upon receipt of an Initiate Self-Test mode command. The host will then be able to run the built-in selt-test.
3	1553RT	R/W	0	Setting this bit to logic “1” will increase the maximum time from when a host requests access to when access is granted during a DMA transfer frmo 8µs to 10µs.
2	ENHTT	R/W	0	This bit affects the functionality of a Synchronize With Data Mode Command. In RT Mode, if SYNCDAT bit 5 in Configuration Register #5 is logic “1”, then the data word in a Synchronize with data mode command will be loaded into the time tag register. If ENHTT is also logic “1”, then this will only happen if the LSB is “0”. In BC Mode, if SYNCDAT bit 5 in Configuration Register #5 is logic “1” and TXTTMC17 bit 15 in BC Control Word is logic “1” and ENHTT is also logic “1”, then the data word for a Synchronize with data mode command will come from the time tag register.
1	ENBCWDT	R/W	0	Setting this bit to logic “1” enables an interrupt to be generated when the BC Frame Timer expires (BCEOF will be set in the Interrupt Status Register and the interrupt will be generated if not masked by bit 3 in Interrupt Enable Register).
0 (LSB)	MCRST	R/W	0	This bit sets the functionality of the shared $\overline{\text{INCMD}}$ / $\overline{\text{MCRST}}$ digital output. If logic “0”, the output is $\overline{\text{INCMD}}$. If logic “1”, the output is $\overline{\text{MCRST}}$. See section Pin Diagrams.

2.22. BC Condition Code Register, Read Only 0x001B

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th colspan="3">Bit Description</th></tr>
<tr><td>15 (MSB)</td><td>ENHBC</td><td>R</td><td>0</td><td colspan="3">This bit is always logic “1” in Enhanced BC Mode.</td></tr>
<tr><td rowspan="6">14 − 13</td><td rowspan="6">RETRY[1:0]</td><td rowspan="6">R</td><td rowspan="6">0</td><td colspan="3">These bits indicate the number of retries of the most recent message as follows:</td></tr>
<tr><th>RETRY1</th><th>RETRY0</th><th>Number of Retries</th></tr>
<tr><td>0</td><td>0</td><td>None</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>Not Used</td></tr>
<tr><td>1</td><td>1</td><td>2</td></tr>
<tr><td>12</td><td>BADMSG</td><td>R</td><td>0</td><td colspan="3">This message will be logic “1” if the previous message was unsuccessful, i.e. contained errors, failed loopback or failed to elicit a response.</td></tr>
<tr><td>11</td><td>RTSTAT</td><td>R</td><td>0</td><td colspan="3">This bit will be set if any of the RT Status Word bits are set (provided they are unmasked in the BC Control Word).</td></tr>
<tr><td>10</td><td>GOODMSG</td><td>R</td><td>0</td><td colspan="3">This bit will be set to logic “1” if the previous message was error free. It will be set to zero following an invalid message.</td></tr>
<tr><td>9</td><td>FORMERR</td><td>R</td><td>0</td><td colspan="3">The bit will be set if the previous RT response had a 1553 Format Error.</td></tr>
<tr><td>8</td><td>NORESP</td><td>R</td><td>0</td><td colspan="3">This bit will be set if the BC receives no response or if the maximum response time has been exceeded.</td></tr>
<tr><td>7 − 2</td><td>GPFLAG[7:2]</td><td>R</td><td>0</td><td colspan="3">General Purpose Flags bits[7 − 2] respectively. These bits may be re-purposed for use by the host and set/reset by the BC FLG Instruction.</td></tr>
<tr><td>1</td><td>GPFLAG1</td><td>R</td><td>0</td><td colspan="3">General Purpose Flag 1. This flag may also be used as an “equal to” flag following BC compare instructions.</td></tr>
<tr><td>0 (LSB)</td><td>GPFLAG0</td><td>R</td><td>0</td><td colspan="3">General Purpose Flag 0. This flag may also be used as a “less than” flag following BC compare instructions.</td></tr>
</table>

2.23. BC General Purpose Flag Register, Write Only 0x001B

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 8	W	0	Clear General Purpose Flag, bits[7 − 0] respectively.
7 − 0 (LSB)	W	0	Set General Purpose Flag, bits[7 − 0] respectively.

2.24. BIT Test Status Flag Register, Read Only 0x001C

The bits in this read-only register will be set when the corresponding conditions below have occurred (except for logic “0” bits).

Bit No.	R/W	Reset	Bit Description
15 (MSB)	R	0	Protocol Built-In Test Complete
14	R	0	Protocol Built-In Test In-Progress
13	R	0	Protocol Built-In Test Passed
12	R	0	Protocol Built-In Test Abort
11	R	0	Protocol Built-In Test Complete / In-Progress
10 − 8	R	0	These bits always read Logic “0”
7	R	0	RAM Built-In Test Complete
6	R	0	RAM Built-In Test In-Progress
5	R	0	RAM Built-In Test Passed
4 − 0 (LSB)	R	0	These bits always read Logic “0”

2.25. Interrupt Enable Register #2, Read/Write 0x001D

Setting a respective bit below to logic “1” will cause an interrupt to be generated when the corresponding event occurs. The equivalent bit in Interrupt Status Register #2 will also be set to logic “1” regardless of whether the enable bit is set or not. Setting a respective bit below to logic “0” will disable (mask) the interrupt.

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	–	R/W	0	Not Used
14	BCOPER	R/W	0	Set BCOPER to logic “1” to generate an interrupt when a parity error is detected in an Enhanced BC instruction.
13	ILLCMD	R/W	0	In RT Mode, set ILLCMD to logic “1” to generate an interrupt when an illegalized command is received. In Message Monitor Mode, set this bit to logic “1” to generate an interrupt when a message is received and stored by the monitor.
12	QUERO	R/W	0	In Enhanced BC Mode, set this bit to logic “1” to generate an interrupt when the General Purpose Queue rolls over. In RT and MT modes, set this bit to logic “1” to generate an interrupt when the Interrupt Status Queue rolls over.
11	STKERR	R/W	0	In Enhanced BC Mode, set this bit to logic “1” to generate an interrupt when the BC Call Stack overflows or underflows.
10	BCILL	R/W	0	Set BCILL to logic “1” to generate an interrupt when the Enhanced BC fetches an illegal op code.
9	RTSTK50	R/W	0	Set RTSTK50 to logic “1” to generate an interrupt when the RT Command Stack is 50% full.
8	RTCIR50	R/W	0	Set RTCIR50 to logic “1” to generate an interrupt when the RT Circular Buffer is 50% full.
7	MTSTK50	R/W	0	Set MTSTK50 to logic “1” to generate an interrupt when the MT Command Stack is 50% full.
6	MTDT50	R/W	0	Set MTDT50 to logic “1” to generate an interrupt when the MT Data Stack is 50% full.
5 − 2	BCIRQ[3:0]	R/W	0	Set BCIRQ[3:0] to logic “1” to generate an interrupt when the Enhanced BC issues an IRQ instruction.
1	BIST	R/W	0	Set BIST to logic “1” to generate an interrupt when the devices completes a built-in self-test.
0 (LSB)	–	R/W	0	Not Used

2.26. Interrupt Status Register #2, Read Only 0x001E

The bits in this register will be set when the respective event occurs, regardless of whether the interrupt is enabled (equivalent bit set in the Interrupt Enable Register #2) or not.

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	MSTINT	R	0	MSTINT will be logic "1" when one or more of the interrupts below is pending.
14	BCOPER	R	0	BCOPER will be set to logic "1" when a parity error is detected in an Enhanced BC instruction.
13	ILLCMD	R	0	In RT Mode, ILLCMD will be set to logic "1" when an illegalized command is received. In Message Monitor Mode, this bit is set to logic "1" when a message is received and stored by the monitor.
12	QUERO	R	0	In Enhanced BC Mode, QUERO will be set to logic "1" when the General Purpose Queue rolls over. In RT and MT modes, this bit will be set to logic "1" when the Interrupt Status Queue rolls over.
11	STKERR	R	0	In Enhanced BC Mode, STKERR will be set to logic "1" when the BC Call Stack overflows or underflows.
10	BCILL	R	0	BCILL will be set to logic "1" when the Enhanced BC fetches an illegal op code
9	RTSTK50	R	0	RTSTK50 will be set to logic "1" when the RT Command Stack is 50% full.
8	RTCIR50	R	0	RTCIR50 will be set to logic "1" when the RT Circular Buffer is 50% full.
7	MTSTK50	R	0	MTSTK50 will be set to logic "1" when the MT Command Stack is 50% full.
6	MTDT50	R	0	MTDT50 will be set to logic "1" when the MT Data Stack is 50% full.
5 − 2	BCIRQ[3:0]	R	0	These bits will be change when the Enhanced BC issues an IRQ instruction. The value of these bits will reflect the value of the 4 LSBs of the IRQ parameter respectively.
1	BIST	R	0	Built-In Self-Test Complete. BIST will be set to logic "1" when a protocol self-test or RAM self-test is completed.
0 (LSB)	INTSTAT1	R	0	INTSTAT1 will be set to logic "1" when one or more bits are set in Interrupt Status Register #1.

2.27. BC General Purpose Queue Pointer Register / RT, MT Interrupt Status Queue Pointer Register, Read/Write 0x001F

In Enhanced BC mode, this register contains the pointer for the General Purpose Queue. In RT and Message Monitor modes, it contains the pointer for the Interrupt Status Queue. Bits 15 − 6 contain the base address and bits 5 − 0 contain the address of the next data location.

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 6	R/W	0	Queue Pointer Base Address, bits[15 − 6] respectively.
5 − 0 (LSB)	R/W	0	Queue Pointer Address, bits[5 − 0] respectively.

2.28. BC Block Status Word

The Block Status Word in the Message Control / Status Block provides information regarding message status (in process or completed), the bus it was transmitted on, whether errors occurred during the message, and the type of occurring errors. This word is written into RAM by the device after message completion. Because it resides in RAM, the host has read-write access, although this word is usually treated as read-only by the host.

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	EOM	R/W	0	End of Message. This bit is set upon completion of a BC message, whether or not errors occurred.
14	SOM	R/W	0	Start of Message. This bit is set at the start of a BC message and cleared at the end of the message.
13	BID	R/W	0	Bus ID (Bus B / $\overline{\text{Bus A}}$). This bit is logic “1” if the BC message was transacted on Bus B. This bIt is logic “0” if the BC message was transacted on Bus A.
12	EF	R/W	0	This bit acts as an Error Flag. If EF is logic “1” and some/all of bits 10, 9 or 8 are also set, it is an indication that one or more of those respective errors occurred in the current message. If EF is logic “1” and all of bits 10, 9 and 8 are zero, then a handshake failure has occurred (applies only to transparent mode).
11	STATSET	R/W	0	Status Set. This bit is not affected by the values of mask bits 14-9 in the BC Control Word for the message. This bit is logic “1” when the received RT Status Word contains an unexpected bit value in the bit range 10 − 0. The expected value is usually logic “0”, except when broadcast is enabled.

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Bit Description</th></tr>
<tr><td>10</td><td>FE</td><td>R/W</td><td>0</td><td>Format Error.

This bit is logic “1” when a received RT response violates MIL-STD-1553 message protocol. This includes sync, word count, encoding, bit count or parity errors.</td></tr>
<tr><td>9</td><td>TOER</td><td>R/W</td><td>0</td><td>No Response Timeout Error.

This bit is logic “1” when a receiving RT responded later than the RT-to-RT Response Timeout interval specified by bits RTRTTO[10 − 9] in Configuration Register #5.</td></tr>
<tr><td>8</td><td>LBE</td><td>R/W</td><td>0</td><td>Loopback Error.

Each word transmitted by the BC is looped back to the receiver and checked for 1553 validity (sync, encoding, bit count and/or parity error). In addition, for each message transacted, the received image for the last word transmitted by the BC is evaluated for data match.

This bit is logic “1” when the received version for one or more words transmitted by the BC fails 1553 “word validity” criteria, and/or the received version for the last word transmitted by the BC does not match the transmitted Manchester II word.</td></tr>
<tr><td>7</td><td>MSTATSET</td><td>R/W</td><td>0</td><td>Masked Status Set.

This bit is logic “1” when one or more of the mask bits 14-9 in the BC Control Word is logic “0” and the corresponding bit is logic “1” in the received RT Status Word.</td></tr>
<tr><td>6 − 5</td><td>RETRY[1:0]</td><td>R/W</td><td>0</td><td>These two bits indicate the number of times a message was retried:
<table><tr><th>RETRY1</th><th>RETRY0</th><th>Number of Retries</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>2</td></tr><tr><td>1</td><td>1</td><td>2</td></tr></table></td></tr>
<tr><td>4</td><td>GDB</td><td>R/W</td><td>0</td><td>Good Transmit Data Block Transfer.

This bit is set to logic “1” upon successful completion of an error-free RT-to-BC message, RT-to-RT message, or transmit mode code message with data. This bit always resets to logic 0 for any BC-to-RT message, mode code message without data, or any incomplete or invalid message.</td></tr>
</table>

Bit No.	Mnemonic	R/W	Reset	Bit Description
3	WAG	R/W	0	Wrong RT Address and/or No Gap. This bit is logic 1 when one or both of the following conditions occur: • the RT address field within a received RT Status Word does not match the RT address field in the Command Word transmitted by the BC or • the GTEN Gap Check Enable bit 8 of Configuration Register #5 is set and the RT responds with response time less than 4 µs per MIL-STD-1553B, mid-parity bit to mid-sync, (2 µs bus “dead time”).
2	LE	R/W	0	Word Count (Length) Error. This bit is logic 1 when an RT-to-BC message, RT-to-RT message, or transmit mode code message with data is transacted with the wrong number of data words. This bit always resets to logic 0 for BC-to-RT messages, receive mode code messages, or transmit mode code messages without data.
1	SE	R/W	0	Sync Error. This bit is logic 1 when an RT responds with Data Sync in its Status Word, or with Command/Status Sync in a Data Word.
0 (LSB)	IWE	R/W	0	Invalid Word Error. This bit is logic 1 when an RT response in one or more words having at least one of the following errors: sync encoding error, Manchester II encoding error, bit count error, parity error.

2.29. RT and MT Block Status Word

The following block status word applies to both RT and Message Monitor Modes.

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	EOM	R/W	0	End of Message. This bit is set upon completion of an RT message, whether or not errors occurred.
14	SOM	R/W	0	Start of Message. This bit is set at the start of an RT message and cleared at the end of the message.
13	BID	R/W	0	Bus ID (Bus B / $\overline{\text{Bus A}}$). This bit is logic “1” if the RT message was transacted on Bus B. This bIt is logic “0” if the RT message was transacted on Bus A.
12	EF	R/W	0	This bit acts as an Error Flag. If EF is logic “1” and some/all of bits 10, 9 or 8 (10 and 9 in Message Monitor Mode) are also set, it is an indication that one or more of those respective errors occurred in the current message. If EF is logic “1” and all of bits 10, 9 and 8 (10 and 9 in Message Monitor Mode) are zero, then a handshake failure has occurred (applies only to transparent mode).
11	RTRTRX	R/W	0	This bit will be set in the RT Block Status Word if the device is the receiving RT in an RT-to-RT transfer. In Message Monitor Mode, this bit will be set to indicate the message was an RT-to-RT transfer.
10	FE	R/W	0	Format Error. This bit is logic “1” when a received RT response violates MIL-STD-1553 message protocol. This includes sync, word count, encoding, bit count or parity errors.
9	TOER	R/W	0	No Response Timeout Error. This bit is logic “1” when the device is the receiving RT in an RT-to-RT transfer and the transmitting RT failed to respond, or responded later than the RT-to-RT Response Timeout interval specified by bits RTRTTO[10 − 9] in Configuration Register #5.

Bit No.	Mnemonic	R/W	Reset	Bit Description
8	LBE	R/W	0	Loopback Error. In RT Mode, this bit will be logic "1" following a loopback error, i.e. when the received version of a transmitted word fails 1553 "word validity" criteria, and/or the received version of the last word transmitted does not match the transmitted Manchester II word. In Message Monitor Mode, this bit will be logic "1" following receipt of a valid message. It will be logic "0" if the message was invalid.
7	CIRRO	R/W	0	CIRRO will be set to logic "1" if the enabled global circular buffer rolls over. This will happen if the upper boundary of the circular buffer is exceeded. If OVINV bit 11 of Configuration register #2 is set to logic "1", the roll over will only occur following receipt of a valid message. Invalid messages will be overwritten and roll over will not occur until the next valid message. In Message Monitor Mode, the size of the circular buffer is set by bits MTDATA[10 − 8] in Configuration Register #3.
6	ILLCMD	R/W	0	In RT Mode, ILLCMD will be set to logic "1" when an illegal command is received.
5	LE	R/W	0	Word Count (Length) Error. This bit is logic 1 when an RT-to-BC message, RT-to-RT message, or transmit mode code message with data is transacted with the wrong number of data words.
4	SE	R/W	0	Sync Error. This bit is logic 1 when an RT responds with Data Sync in its Status Word, or with Command/Status Sync in a Data Word.
3	IWE	R/W	0	Invalid Word Error. This bit is logic 1 when an RT response in one or more words having at least one of the following errors: sync encoding error, Manchester II encoding error, bit count error, parity error.
2	RTRTERR	R/W	0	This bit is set if one of the following occurs during an RT-to-RT transfer: • the RT address of the responding RT does not match the RT address field in the Command Word • the GTEN Gap Check Enable bit 8 of Configuration Register #5 is set and the RT responds with response time less than 4 µs per MIL-STD-1553B, mid-parity bit to mid-sync, (2 µs bus "dead time") • the responding RT had an invalid status word or wrong sync bit.
1	RTRTERR2	R/W	0	This bit is set if the second command word in an RT-to-RT transfer had an error (e.g. wrong T/$\overline{R}$ bit).

Bit No.	Mnemonic	R/W	Reset	Bit Description
0 (LSB)	CWERR	R/W	0	This bit is set if a received Command Word is undefined (violates MIL-STD-1553 rules), e.g. if broadcast is enabled (BCSTDIS bit 7 in Configuration Register #5 is set to logic "0") and a mode command not allowed to be broadcast under 1553 rules (e.g. Transmit Last Command) is sent to subaddress 31.

2.30. Word Monitor Identification Word

The Word Monitor Information Word gives information about the received words stored during Word Monitor Mode operation.

Bit No.	Mnemonic	Bit Description
15 (MSB) − 8	GT[7:0]	Gap Time, bits 7 − 0. If CTDATA, bit 1 is logic "0", then these bits will show the gap time between the start of the current word and the end of the previous word. The resolution is 0.5 μs/LSB, up to a max of 127.5 μs.
7	WF	Word Flag, always set to logic "1".
6	RTCMD	If RTCMD is logic "0", then the received word was a valid RT command (correct sync, RT Address and Parity). Otherwise, RTCMD will be logic "1".
5	BCST	If BCST is logic "0", then the received word was a valid broadcast command with RT address = 31. Otherwise, BCST will be logic "1".
4	ERR	This bit will be set to logic "1" if the received word contained an error.
3	SYNC	If SYNC = logic "1", then the received word contained a command sync. If SYNC = logic "0", then the received word contained a data sync.
2	BUSAB	If BUSAB = logic "0", then the word was received on Bus A. If BUSAB = logic "1", then the word was received on Bus B.
1	CTDATA	If CTDATA is logic "1", then previous and next message is contiguous and the gap time bits GT[7:0] above are not used. If CTDATA is logic "0", then the gap time is stored in bits 15 − 8 above.
0 (LSB)	MCODE	If MCODE is logic "0", then the received word was a valid mode code command.

2.31. RT/MT Interrupt Status Queue Word

In Enhanced RT or MT Modes, or combined RT/MT Mode, both the RT and MT have the capability to store interrupt information in the Interrupt Status Queue. A two-word entry is written to the Interrupt Status Queue every time an interrupt event occurs. The first word is the Status Queue Word (see Table 7 and Table 8 below), which describe what event(s) caused the interrupt. Bit 0 will indicate if the interrupt was a message interrupt (bit 0 = logic “1”) or a non-message interrupt (bit 0 = logic “0”) event. A logic “1” value on any of the other bits indicates that respective interrupt event took place.

The second word stored in the status queue will be a parameter word, indicating where the interrupt came from, e.g. in the case of a Message Interrupt Event, the parameter word will be a pointer to the relevant Block Status Word in the RT or MT descriptor stack.

Table 7. RT/Monitor Interrupt Status Queue Word for Message Interrupt Events

Bit No.	Message Interrupt Event	Parameter Word
15 (MSB)	RT transmitter watchdog timer has timed out.	RT Block Status Word pointer
14	In RT Mode, this bit is set when an illegalized command has been received. In MT Mode, this bit is set when a valid message is received. **Note:** Bit 7, NOVALMSG of Configuration Register #6 must be logic “0” or this bit will not be set when a valid message is received.	RT/MT Block Status Word pointer
13	The Monitor Data Stack is half-full.	MT Block Status Word pointer
12	The Monitor Data Stack is full and has rolled over.	MT Block Status Word pointer
11	The RT Circular Buffer is half full.	RT Block Status Word pointer
10	The RT Circular Buffer is full and has rolled over.	RT Block Status Word pointer
9	The Monitor Command Stack is half-full.	MT Block Status Word pointer
8	The Monitor Command Stack is full and has rolled over.	MT Block Status Word pointer
7	The RT Command Stack is half-full.	RT Block Status Word pointer
6	The RT Command Stack is full and has rolled over.	RT Block Status Word pointer
5	A Handshake Failure occured between the device and external RAM in Transparent Mode.	RT Block Status Word pointer
4	A 1553 Message Error, loopback failure or response timeout was detected	RT/MT Block Status Word pointer
3	A Mode Command has been received. **Note:** The mode command must have its interrupt enabled in the Mode Command Interrupt Enable Lookup Table at addresses 0x108 to 0x10F.	RT Block Status Word pointer

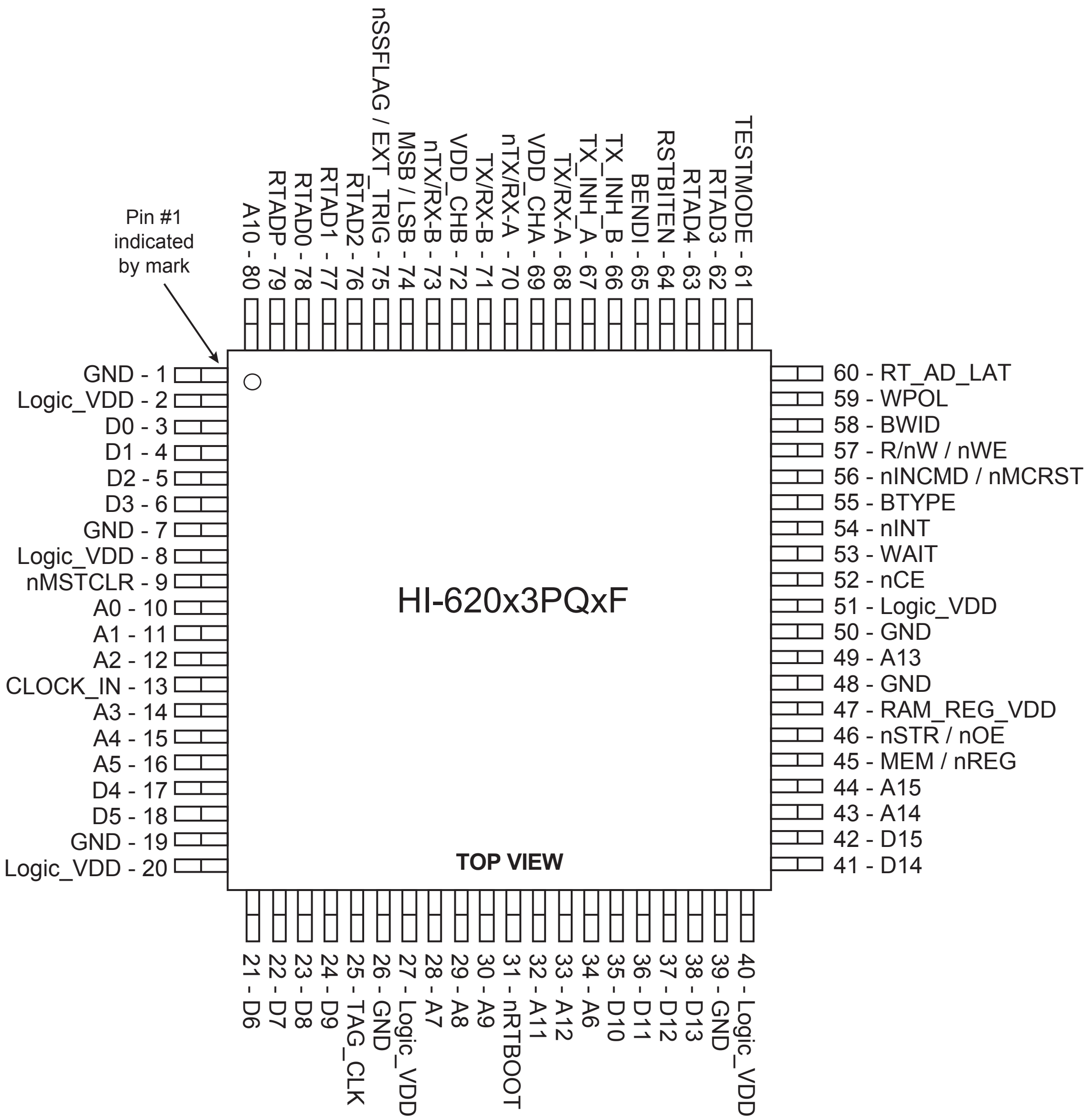
Bit No.	Message Interrupt Event	Parameter Word
2	An EOM occurred in a specific RT Subaddress Control Word. **Note:** The RT must be in Enhanced Memory Management Mode and the appropriate EOM interrupt bit (TXEOM, RXEOM or BCSTEOM) must be set in the RT Subaddress Control Word Register.	RT Block Status Word pointer
1	A message was completed (EOM).	RT/MT Block Status Word pointer
0 (LSB)	Logic “1”.	N/A.

Table 8. RT/Monitor Interrupt Status Queue Word for non-Message Interrupt Events

A logic “1” value on any of the bits indicates that respective interrupt event took place.

Bit No.	Non-Message Interrupt Event	Parameter Word
15 (MSB) − 5	No function.	No function.
4	The Time Tag Register value rolled over.	0x0000
3	An RT Address Parity Error occured.	0x0000
2	A Protocol Self-Test was completed.	0x0000
1	A RAM Parity Error occurred.	Address location where parity error occurred.
0 (LSB)	Logic “0”.	N/A.

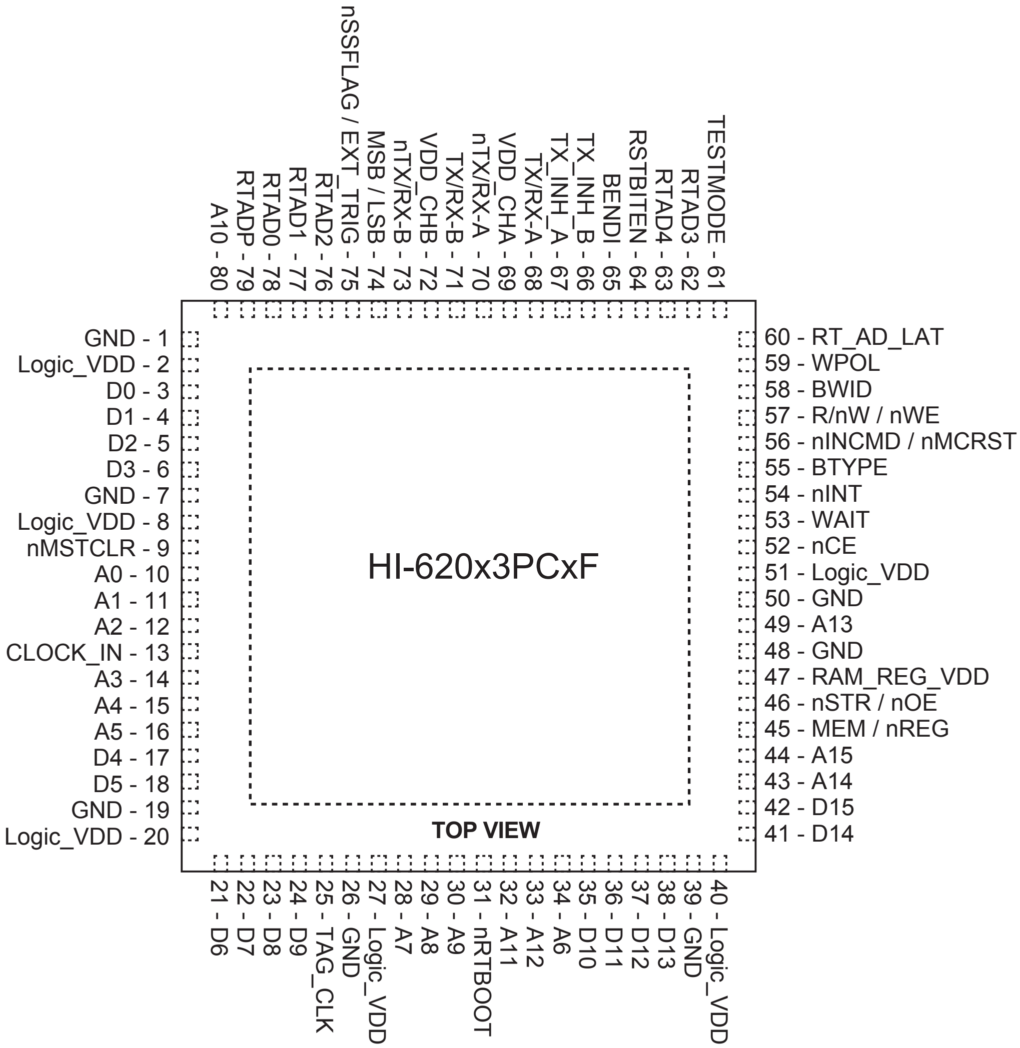
3. PIN DIAGRAMS



Notes:
1. Prefix “n” denotes an inverted or negative signal, e.g. nMSTCLR = $\overline{\text{MSTCLR}}$, etc.

Figure 1. HI-620x3PQxF PQFP Package Pinout

Pin Diagrams



Notes:

1. Prefix "n" denotes an inverted or negative signal, e.g. nMSTCLR = $\overline{\text{MSTCLR}}$, etc.

Figure 2. HI-620x3PCxF QFN Package Pinout

4. SIGNAL AND PIN DESCRIPTIONS

Table 9. Power and Ground

Signal Name	Function	Description
VDD_CHA	Power Supply	+3.3V DC power supply for bus transceiver, Channel A
VDD_CHB	Power Supply	+3.3V DC power supply for bus transceiver, Channel B
Logic_VDD	Power Supply	+3.3V DC power supply for digital logic
GND	Power Supply	Power supply ground
RAM_REG_VDD	Power Supply	+ 3.3 Volt power for internal RAM voltage regulator

Table 10. MIL-STD-1553 Isolation Transformer Connections

Signal Name	Function	Description
TX/RX-A	Analog I/O	Bi-directional Bus A interface to external MIL-STD-1553 isolation transformer. Observe positive / negative polarity.
$\overline{\text{TX/RX-A}}$	Analog I/O	
TX/RX-B	Analog I/O	Bi-directional Bus B interface to external MIL-STD-1553 isolation transformer. Observe positive / negative polarity.
$\overline{\text{TX/RX-B}}$	Analog I/O	

Table 11. Host Interface

Signal Name	Function	Description
D15 (MSB) − D0 (LSB)	Data inputs or Data outputs 50 kΩ Pull-Up when inputs	Bi-directional data bus for host read/write operations on registers and RAM.
A15 (MSB) − A0 (LSB)	Digital inputs 50 kΩ Pull-Up	Address bus for host read/write operations on registers and RAM.
$\overline{\text{CE}}$	Digital Input 50 kΩ Pull-Up	Chip Enable, active low. When asserted, this pin enables host read or write accesses to device RAM or registers. This pin is normally connected to a Chip Select output from the host's bus interface and is used by the host to select the device for a transfer to/from either RAM or registers.
BWID	Digital Input 50 kΩ Pull-Up	Configuration pin for host bus width. High selects 16-bit bus width, low selects 8-bit bus width.
BTYPE	Digital Input 50 kΩ Pull-Up	Configuration pin for host bus read/write control signal style. High selects "Intel style" using separate read strobe $\overline{\text{OE}}$ (output enable) and write strobe $\overline{\text{WE}}$. Low selects "Motorola style" using single active-low read/write strobe $\overline{\text{STR}}$ and read/write select signal, R/$\overline{\text{W}}$.
R/$\overline{\text{W}}$ / $\overline{\text{WE}}$	Digital Input 50 kΩ Pull-Up	Read / $\overline{\text{Write}}$. Read/write direction signal R/$\overline{\text{W}}$ when BTYPE pin is low. Active-low Write Enable $\overline{\text{WE}}$ when BTYPE pin is high. Used for host read or write accesses to device RAM or registers. This pin or the $\overline{\text{CE}}$ pin should be high during all address transitions.
$\overline{\text{STR}}$ / $\overline{\text{OE}}$	Digital Input 50 kΩ Pull-Up	Active-low common read/write strobe $\overline{\text{STR}}$ when BTYPE pin is low. Active-low Output Enable $\overline{\text{OE}}$ when BTYPE pin is high. Used for host read or write accesses to device RAM or registers.
WPOL	Digital Input 50 kΩ Pull-Up	Configuration pin for WAIT output polarity. When the WPOL pin is low, the "wait" output is active low ($\overline{\text{WAIT}}$). When WPOL is high, the "wait" output is active high (WAIT).
WAIT / $\overline{\text{WAIT}}$	Digital Output	Host bus read cycle WAIT or $\overline{\text{WAIT}}$ output. The WPOL input pin sets the output polarity for this "wait" output. RAM Read cycles are slower than write cycles, but prefetching speeds up data availability for multi-word sequential address read cycles. For every new RAM read cycle, the device asserts WAIT. Connected to the processor WAIT or $\overline{\text{WAIT}}$ input, this action inserts one or more processor wait states (depending on processor clock frequency) while the HI-6200 fetches the **first** word. After reading each HI-6200 RAM address, the device prefetches and retains data from the next address. If the next bus access reads that sequential address, the data is ready without WAIT assertion. Thus WAIT assertion only occurs for the first word read. **NOTE:** Register reads don't use prefetch therefore will have a WAIT cycle during every address read, whether sequential or not.

Signal Name	Function	Description
MSB / LSB	Digital Input 50 kΩ Pull-Up	Most Significant Byte/Least Significant Byte. For 8-bit bus width, the input signal (MSB / LSB) is used to indicate which byte of the 16-bit word is currently being transferred (MSB or LSB). The logic sense of MSB / LSB is controlled by the BENDI input (see BENDI pin description and Table 1). If BENDI is connected to logic “0”, MSB / LSB should be asserted low (logic “0”) to indicate the transfer of the least significant byte and high (logic “1”) to indicate the transfer of the most significant byte. If BENDI is connected to logic “1”, MSB / LSB should be asserted low (logic “0”) to indicate the transfer of the most significant byte and high (logic “1”) to indicate the transfer of the least significant byte. See Table 1. MSB / LSB is “Don’t Care” for 16-bit bus width.
BENDI	Digital Input 50 kΩ Pull-Up	Big Endian Configuration Pin. The BENDI pin works in conjunction with the MSB / LSB and BWID pins to determine the “endianness” or byte order of 16-bit word transfers to the HI-6200. Table 1 below summarizes the interoperability of the three pins.
MEM / $\overline{REG}$	Digital Input 50 kΩ Pull-Up	Memory or Register. Selects between memory access (MEM / $\overline{REG}$ = "1") or register access (MEM / $\overline{REG}$ = "0"). Usually connected to either a CPU address line or address decoder output.

Table 12. BENDI Pin Functionality

The BENDI and MSB / LSB pins are used as outlined below to set the order for byte accesses when transacting 16-bit words on 16-bit or 8-bit host busses.

BENDI	BWID	MSB / LSB	WR		RD	
			µP/HI-6200 Data Bus Pins	HI-6200 internal RAM or Register 16-bit Word	HI-6200 internal RAM or Register 16-bit Word	µP/HI-6200 Data Bus Pins
0	0	0	D[7:0]	Bits[7:0]	Bits[7:0]	D[7:0]
0	0	1	D[7:0]	Bits[15:8]	Bits[15:8]	D[7:0]
0	1	X	D[15:0]	Bits[7:0], Bits[15:8]	Bits[7:0], Bits[15:8]	D[15:0]
1	0	0	D[7:0]	Bits[15:8]	Bits[15:8]	D[7:0]
1	0	1	D[7:0]	Bits[7:0]	Bits[7:0]	D[7:0]
1	1	X	D[15:0]	Bits[15:8], Bits[7:0]	Bits[15:8], Bits[7:0]	D[15:0]

Table 13. RT Address

<table>
<tr><th>Signal Name</th><th>Function</th><th colspan="2">Description</th></tr>
<tr><td>RTAD4 (MSB)</td><td>Digital Input
50 kΩ Pull-Up</td><td colspan="2" rowspan="5">RT Address Input signals.
NOTE: The RT address and parity may be programmed by software if bit 5 of Configuration Register #6 (RTADSRC) is set to logic "1". In this case, the RT Address and Parity are provided by the Host via data lines D5 − D0 and RTAD4:0 (and RTADP below) are not used.</td></tr>
<tr><td>RTAD3</td><td>Digital Input
50 kΩ Pull-Up</td></tr>
<tr><td>RTAD2</td><td>Digital Input
50 kΩ Pull-Up</td></tr>
<tr><td>RTAD1</td><td>Digital Input
50 kΩ Pull-Up</td></tr>
<tr><td>RTAD0 (LSB)</td><td>Digital Input
50 kΩ Pull-Up</td></tr>
<tr><td>RTADP</td><td>Digital Input
50 kΩ Pull-Up</td><td colspan="2">Remote Terminal Address Parity.
Used to provide odd parity for the RT address on RTAD[4:0].</td></tr>
<tr><td rowspan="5">RT_AD_LAT</td><td rowspan="5">Digital Input
50 kΩ Pull-Up</td><td colspan="2">RT Address Latch.
This input signal is used to control how the RT address is latched internally. If RT_AD_LAT is logic "0", then the RT address and parity will simply track RTAD4:0 and RTADP inputs.
If RT_AD_LAT transitions from logic "0" to logic "1", the values on RTAD4:0 and RTADP will then be latched on the rising edge of RT_AD_LAT.
If RT_AD_LAT is connected to logic "1", then the RT address is latched under software control, and depends on the value of bit 5 of Configuration Register #6 (RTADSRC) as follows:</td></tr>
<tr><td>RTADSRC bit 5 value</td><td>RT Address latch control when RT_AD_LAT = 1</td></tr>
<tr><td>Logic "0" (Default)</td><td>The RT address and parity will be latched directly from the RTAD4:0 and RTADP input signals by writing Configuration Register #5.</td></tr>
<tr><td>Logic "1"</td><td>RT address parity will be provided by the host by writing via the data bus inputs D5 − D1 for the address and D0 for parity.
Note: Bit 3 of Configuration Register #4 (RTLATEN) must be written logic "1" while the RT address and parity are written via D5 − D0 to the lower 6 bits of Configuration Register #5 (RTAD[4:0] and RTADP (LSB)).</td></tr>
<tr><td colspan="2">For a more detailed discussion on Latching the RT Address, see Section “4.1. Latching the RT Address and Parity”.</td></tr>
</table>

Table 14. Other Signals

<table>
<tr><th>Signal Name</th><th>Function</th><th colspan="2">Description</th></tr>
<tr><td rowspan="2">$\overline{INCMD}$

or

$\overline{MCRST}$</td><td rowspan="2">Digital Output

or

Digital Output</td><td colspan="2">The function of this signal depends on the value of bit 0, Configuration Register #7 (MCRST). If MCRST is logic "0", this signal functions as the output $\overline{INCMD}$.
$\overline{INCMD}$ is asserted low whenever a message is in progress.
In Word Monitor mode, $\overline{INCMD}$ remains low while the mode is active.</td></tr>
<tr><td colspan="2">If MCRST is logic "0", this signal functions as the output $\overline{MCRST}$.
When in RT mode, this output will be asserted low for two clock cycles when a Reset Remote Terminal mode command is received.</td></tr>
<tr><td rowspan="9">$\overline{SSFLAG}$

or

EXT_TRIG</td><td rowspan="9">Digital Input
50 kΩ Pull-Up

or

Digital Input
50 kΩ Pull-Up</td><td colspan="2">Subsystem Flag (RT) or External Trigger input.
In RT mode, this signal functions as $\overline{SSFLAG}$. If asserted (logic “0”), the Subsystem Flag bit will be set in the transmitted RT Status Word.
In BC or MT modes, this signal functions as an External Trigger as follows:</td></tr>
<tr><td colspan="2">BC Mode</td></tr>
<tr><td>Non-Enhanced Mode (Legacy)</td><td>No function.</td></tr>
<tr><td>Enhanced Mode (Legacy)</td><td>If the external trigger is enabled by setting bit 7 in Configuration Register #1, a low-to-high transition on EXT_TRIG will initiate a BC Start.</td></tr>
<tr><td>Enhanced Mode</td><td>When a Wait for External Trigger (WTG) instruction is executed, the BC will wait for a low-to-high transition on EXT_TRIG before executing the next instruction.</td></tr>
<tr><td colspan="2">MT Mode</td></tr>
<tr><td>Word Monitor</td><td>If the external trigger is enabled by setting bit 7 in Configuration Register #1, a low-to-high transition on EXT_TRIG will start monitor operation.</td></tr>
<tr><td>Message Monitor</td><td>No effect.</td></tr>
<tr><td colspan="2" style="display:none"></td></tr>
<tr><td>$\overline{INT}$</td><td>Digital Output</td><td colspan="2">Interrupt Request.
If Configuration Register #2, bit 3 LEVEL is logic “0”, the interrupt request output on $\overline{INT}$ will be a negative pulse of about 500 ns.
If LEVEL is logic “1”, the interrupt request output on $\overline{INT}$ will be a LOW continuous level. To clear the interrupt, one of following events should occur:
1. Logic “1” should be written to bit 2 of the Start/Reset Register (INTRST); or
2. If bit 4 of Configuration Register #2 (CLRSTAT) is logic “1”, then reading the Interrupt Status Register will clear $\overline{INT}$. NOTE: In cases where both Interrupt Status Registers #1 and #2 have bits set, both registers must be read in order to clear $\overline{INT}$.</td></tr>
<tr><td>CLOCK_IN</td><td>Digital Input</td><td colspan="2">50 MHz, 40 MHz, 20 MHz, or 16 MHz clock input.</td></tr>
</table>

Signal Name	Function	Description
TX_INH_A	Digital Input 50 kΩ Pull-Up	Transmit inhibit inputs for Bus A and Bus B, active high. These two inputs enable (logic “0”) or inhibit (logic “1”) transmit on Bus A or Bus B, affecting behavior for all enabled 1553 devices.
TX_INH_B	Digital Input 50 kΩ Pull-Up	
$\overline{\text{MSTCLR}}$	Digital Input 50 kΩ Pull-Up	Master Reset, active low.
RSTBITEN	Digital Input 50 kΩ Pull-Up	If this input is set to logic “1”, the Built-In-Self-Test feature will be enabled and run automatically after power up following a hardware reset. See “Built-In Self-Test (BIST)” and **Note 1** below regarding power-up times. If this input is set to logic “0”, automatic BIST is disabled.
$\overline{\text{RTBOOT}}$	Digital Input 50 kΩ Pull-Up	If $\overline{\text{RTBOOT}}$ is logic “0”, MIL-STD-1760 operation is enabled (the RT will initialize with the busy bit set in the RT Status Word). If $\overline{\text{RTBOOT}}$ is logic “1”, the device will initialize in Idle mode for an RT-only device, or in BC mode for a BC/RT/MT device.
TAG_CLK	Digital Input 50 kΩ Pull-Up	Time Tag Clock. This optional clock input may be used to increment the Time Tag Register. It is enabled by setting Bits 7, 8 and 9 of Configuration Register #2 (TTRES[9:7]) to [111].
TESTMODE	Digital Input 50 kΩ Pull-Down	Factory test pin. **DO NOT CONNECT.**

Note 1: Power-up Time. The total time required for power-up will depend on whether the user initiates self-test or not. See “Table 15. User-initiated self-test times as a function of clock frequency.”

4.1. Latching the RT Address and Parity

The RT address and parity may be latched from two sources, the input signals RTAD[4:0] and RTADP, or data inputs D5 – D0 (D5 – D1 for RT address and D0 for parity) by writing “Configuration Register #5, Read/Write 0x0009”. Numerous methods are available to latch the RT address and parity via hardware or software depending on combinations of the input signal RT_AD_LAT, RTLATEN bit 3 of “Configuration Register #4, Read/Write 0x0008” and RTADSRC bit 5 of “Configuration Register #6, Read/Write 0x0018”.

4.1.1. Latching the RT Address and parity from input signals RTAD[4:0] and RTADP

- The source of the RT address and parity must be defined as the input signals RTAD[4:0] and RTADP by setting RTADSRC bit 5 of “Configuration Register #6, Read/Write 0x0018” to logic “0”.
- If the input RT_AD_LAT is logic “0”, then the RT address and parity will continuously track the input signals (not latched).
- The RT address and parity may be latched under **hardware control** by transitioning the RT_AD_LAT input from logic “0” to logic “1”.
- **To latch the RT address and parity under software control from the input signals RTAD[4:0] and RTADP;**

- The input signal RT_AD_LAT **must** be connected to logic “1” or left floating (Internal pull-up).
- Program the device for ENHANCED MODE, by writing logic “1” to ENHANC bit 15 of “Configuration Register #3, Read/Write 0x0007”.
- Enable latched mode by setting RTLATEN bit 3 of “Configuration Register #4, Read/Write 0x0008” to logic “1”.
- The RT address and parity will be latched from the input signals when the host writes to “Configuration Register #5, Read/Write 0x0009”. For this write operation, the values of the data inputs D5 – D0 are “don’t care” since the RT address and parity will be latched from the RTAD[4:0] and RTADP input signals. The latched values may be read at any time from bits[5:0] of “Configuration Register #5, Read/Write 0x0009”.
- To prevent an erroneous change in the RT address via a subsequent write to “Configuration Register #5, Read/Write 0x0009”, bit 3, RTLATEN, of “Configuration Register #4, Read/Write 0x0008” should be programmed to logic “0”.

4.1.2. Latching the RT Address and parity under software control from data inputs D5 – D0 by writing “Configuration Register #5, Read/Write 0x0009”

- The input signal RT_AD_LAT **must** be connected to logic “1” or left floating (Internal pull-up).
    - **NOTE:** If RT_AD_LAT is logic “1” and is then forced to logic “0”, the RT address will revert to tracking the input signals RTAD[4:0] and RTADP and not be software programmable.
- Program the device for ENHANCED MODE, by writing logic “1” to ENHANC bit 15 of “Configuration Register #3, Read/Write 0x0007”.
- The source of the RT address and parity must be defined as the data inputs D5 – D0 by setting RTADSRC bit 5 of “Configuration Register #6, Read/Write 0x0018” to logic “1”.
- Set RTLATEN bit 3 of “Configuration Register #4, Read/Write 0x0008” to logic “1”.
- Write the value of the RT address (bits 5-1) and parity (bit 0) via D5 – D1 and D0 respectively to the lower six bits of “Configuration Register #5, Read/Write 0x0009”. The latched values may be read back any time from bits[5:0] of “Configuration Register #5, Read/Write 0x0009”.
- To prevent an erroneous change in the RT address via a subsequent write to “Configuration Register #5, Read/Write 0x0009”, bit 3, RTLATEN, of “Configuration Register #4, Read/Write 0x0008” should be programmed to logic “0”.

Note: The state of the RT_AD_LAT pin may be checked by the host by reading bit 6, RTADLAT, of “Configuration Register #5, Read/Write 0x0009”.

5. BUILT-IN SELF-TEST (BIST)

The HI-6200 has two built-in self-test modes, a Protocol Self-Test and a RAM Self-Test. RAM Self-Test is initiated by setting bit 9, RAMST in “Start/Reset Register, Write Only 0x0003”. Protocol and RAM self-test are performed separately and test times need to be taken into account when calculating total power-up time. The total time required for power-up will depend on whether the user initiates self-test or not. See “Table 15. User-initiated self-test times as a function of clock frequency.”

Table 15. User-initiated self-test times as a function of clock frequency.

User-initiated self-test	Test Time as a function of Clock Frequency			
	50 MHz	40 MHz	20 MHz	16 MHz
No Self-Test	80 ns	100 ns	200 ns	250 ns
Protocol Self-Test	0.6 ms	0.8 ms	1.6 ms	2.0 ms
RAM Self-Test	13.1 ms	16.4 ms	32.8 ms	41 ms

5.1. Protocol Self-Test

5.1.1. Automatic Power-On Protocol Self-Test

The protocol self-test will run automatically after power up following a hardware reset if the RSTBITEN input pin is set to logic “1”. The protocol self-test uses internal BIST scan chains to perform a comprehensive test of the registers, Manchester encoder/decoders, protocol logic and internal protocol state machines, and memory manager. The test time is 32,000 clocks and the total duration depends on the system clock frequency as shown in Table 15 above. Registers are temporarily stored in memory and restored following the protocol self-test. The host should not perform a register or memory write cycle during this test. To determine when the power-up protocol self-test has been completed, the host may poll the value of the “BIT Test Status Flag Register, Read Only 0x001C”. A host read to address 0x001C will read out the BIT register, other registers will result in 0x0000. A write during the Protocol test will abort the test.

5.1.2. User-Initiated Protocol Self-Test

This test operates the same as automatic protocol self-test, but is initiated by the host at any time by setting bit 7, PROST in “Start/Reset Register, Write Only 0x0003”.

5.2. User-Initiated RAM Self-Test

The RAM Self-Test is initiated by the host by setting bit 9, RAMST in “Start/Reset Register, Write Only 0x0003”. Completion time depends on the system clock frequency as shown in Table 15 above. The built-in RAM self-test consists of writing and then reading/verifying the walking pattern “data = address,” followed by the walking pattern “data = address inverted.” At the end of the test, the data test pattern is left resident in the RAM. Unlike the protocol self-test, the RAM test is “destructive” of system data stored in RAM. As a result, following the RAM self-test, regardless of whether the test passes or fails, the data in shared RAM is not automatically restored to its previous values. RAM BIST will allow host read/writes to Registers during test but not the RAM. Writing a logic “1” to bit 0 or bit 10 in register “Start/Reset Register, Write Only 0x0003” will abort the RAM BIST test.

Note that the device shared RAM supports error correcting code (ECC RAM) and will automatically correct any single bit errors and can detect double bit errors. If a double bit error is detected the host is notified via an interrupt, RAMPE, bit 14, of “Interrupt Status Register #1, Read Only 0x0006”.

5.3. BC/RT Continuous Online Loopback Test

The device automatically performs an online loop test for every message transmitted by the BC or non-broadcast message transmitted by the RT. Received versions of all words transmitted by the BC or RT are checked for validity (Sync, Manchester Encoding, bit count, parity) and there is a bit-by-bit comparison performed on the received version of the last transmitted word. If either of these tests fail, the loop test is considered to have failed and the user may be notified via an interrupt.

5.4. BC Offline Loopback Test

In addition to the online loopback test, the device includes capability for performing an offline loopback test. For any individual message, the BC offline loopback test may be activated by setting SELFTST, bit 6 of the “BC Control Word Register, Read/Write 0x0004”, to logic “1.” This test involves the “transmission” of an internal message in which the serial output of the Manchester encoder is routed to the input of the Manchester decoder. For this test, no message is transmitted on the external 1553 bus. A failure of this loop test would indicate a failure of the Manchester encoder or decoder parallel or serial data paths, or the BC state machine logic. Similar to the online loopback test, the result of this test is host accessible by means of the message’s block status word, the BC loopback word (stored in RAM), and/or “Interrupt Status Register #1, Read Only 0x0006”.

5.5. Transmitter Watchdog (Failsafe) Time Test

The purpose of the transmitter watchdog timer is to mitigate against a “babbling” Manchester encoder by automatically shutting down the channel A or channel B transmitter. The watchdog timer logic operates independently of the Manchester encoder logic. Specifically, its purpose is to automatically shut down the active encoder and transmitter if it attempts to transmit for longer than 660.5 µs. The longest valid MIL-STD-1553 transmission is 660 µs. To test the transmitter watchdog timer, it is necessary to induce a timeout condition, which will not occur under normal operation.

To induce a transmitter timeout condition, the host sets the lower three bits, TEST[2:0] of “Configuration Register #4, Read/Write 0x0008” to a value of 4 (100). This configures the device for “Test Failsafe Timer” test mode. When this is done, the device will transmit until a time-out condition occurs for every BC or RT transmission regardless of the message’s correct word count. That is, for every BC message or every RT response, the active bus will transmit until the watchdog timer terminates the transmission. This will occur following a transmission of approximately 660.5 µs. To resume correct BC, RT, or Monitor operation following this test, the host should select “NORMAL OPERATION” mode by programming the lower three bits of “Configuration Register #4, Read/Write 0x0008” to a value of 000.

5.6. Channel A-to-B Wraparound Self-Test

This self-test mode is only available on device versions with BC/RT/MT capability.

This test provides a method to exercise the Channel A and Channel B front end circuitry, including the respective transceivers and isolation transformers. This test involves the simultaneous use of the Word Monitor Mode and Test Mode. Note that this test is not possible for RT-only device versions, since these don’t provide the Word Monitor function. Also note that a valid RT-ADDRESS/PARITY BIT combination must be supplied otherwise Bit #6 RTCMD of the “Word Monitor Identification Word” will indicate a fault condition.

In order to perform this test, there needs be a wraparound connection between the 1553 A and B bus channels. This connection must include a termination resistor connected between the BUSA/B and $\overline{\text{BUSA/B}}$ wires. Assuming that the transformer-coupled (stub-coupled) taps (usually the inner taps) of the isolation transformers are used, the value of this resistor should be 78 ohms. If the outer (direct coupled) taps are used -- which are required to include 55 ohm series resistors in each leg – then the value of the termination resistor should be 39 ohms.

The software programming steps required to perform the wraparound test are as follows:

1. Program the device for ENHANCED MODE, by writing logic “1” to ENHANC bit 15 of “Configuration Register #3, Read/Write 0x0007”.
2. Program the device for Encoder Test Mode, by writing the lower three bits of “Configuration Register #4, Read/Write 0x0008” to a value of 010.
3. Program the device for Word Monitor Mode by programming “Configuration Register #1, Read/Write 0x0001” to a value of x4000. Initialize the value of the Monitor Stack Pointer (shared RAM address x0100) to a known value – a value of 0000 is suggested. Then, to start the Word Monitor, write a value of logic “1” to BCMTSTRT of the “Start/Reset Register, Write Only 0x0003”.
4. Write the 16-bit data pattern for the 1553 “command,” “status,” or “data” word to be transmitted to the “MT Trigger Word Register (see “Non-Enhanced BC Frame Time / Enhanced BC Initial Instruction Pointer / RT Last Command / MT Trigger Register, Read/Write 0x000D”).
5. “Test Mode Register 1, ETest Register, Read/Write 0x0011”, is written with the following values to configure the encoder test functions as follows:

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	E_CHA	R/W	0	Set Encoder Channel Write logic “0” to set Channel B. Write logic “1” to set Channel A. This bit will read back the inverse value of what was written to it.
14	EVNPAR	R	0	Write logic “0”. Note: This bit reads logic “0”. In Register Test Mode (“Configuration Register #4, Read/Write 0x0008”, bits [2:0] = 101) writing “1” to this bit enables Even Parity RAM test.
13	E_TXENA	R/W	0	Encoder Transmit Enable Write logic “1” to enable encoder transmission
12	E_ENCENA	R/W	0	Encoder Enable Write logic “1” to enable the encoder
11	E_SYNC	R/W	0	Command/Status Sync Byte Write logic “1” for command/status word sync Write logic “0” for data word sync
10	E_STAT	R/W	0	This bit will read logic “1” if the encoder test in not running. Writing logic “1” to this bit will cause the transmitted encoder test message to be received on the same and alternative bus decoders. If this bit is logic “0,” the transmitted encoder test message will be received only on the alternate bus decoder.
9	Not used	R	1	This read-only bit has no function in Encoder Test Mode and reads logic “1”.
8 – 6	Not used	R	0	These read-only bits have no function in Encoder Test Mode and read logic “0”.

Bit No.	Mnemonic	R/W	Reset	Bit Description
5	BIT15	R	0	This bit reads back the value of bit 15 and shows which Encoder Channel is set Read logic “0” = Channel B Read logic “1” = Channel A
4	Not used	R	0	This read-only bit has no function in Encoder Test Mode and reads logic “0”.
3	E_BUS	R	0	This bit reads logic “1” if an Encoder Test is Active on Bus A This bit reads logic “0” if an Encoder Test is Active on Bus B
2	Not used	R	0	This read-only bit has no function in Encoder Test Mode and reads logic “0”.
1	TBUSYA	R	0	Bus A Busy, active low status bit. In Encoder Test Mode this bit reads logic “1” when there is no transmit activity on Bus A. This bit will read logic “0” if there is transmit activity on Bus A.
0	TBUSYB	R	0	Bus B Busy, active low status bit. In Encoder Test Mode this bit reads logic “1” when there is no transmit activity on Bus B. This bit will read logic “0” if there is transmit activity on Bus B.

This write operation will cause the word with data from step 4 and sync type defined by bit 11 to be transmitted on the 1553 bus specified by bit 15. The same word will repeatedly transmit until the encoder is disabled (write logic “0” to E_ENCENA) or the watchdog timer times out at 660 µs.

6. Immediately after step 5, depending on which bus the word was transmitted on, poll bit 1 or bit 0 of ETEST Register 0x0011 to determine transmit activity status. A logic “0” indicates transmit activity.

   Some time after step 5 (immediately, in the case of the first word transmitted by the BC or an RT), the respective TBUSY bit (A or B) will transition from logic “1” to logic “0”, indicating transmit activity on the respective bus. It will stay at logic “0” for approximately 4 µs of the 20 µs total test word time. If it is desired to transmit a subsequent **different** contiguous word, then steps 4, 5, and 6 must be repeated for that next word **before** the respective TBUSY bit transitions back to logic “1”, i.e. during the 4 µs interval while TBUSY is logic “0”.

   Following the loading of the last test word to be sent, transmission must be halted by disabling the respective encoder. Writing logic “0” to bit 12 (E_ENCENA) will shut down the respective encoder (and therefore the respective 1553 transmitter) at the end of the current word.

7. To verify that data was correctly transmitted from Channel A to Channel B (or visa versa), it is necessary to read the words received by the device Word Monitor. For each word transmitted on either channel, it is possible to read the received version of the data, along with the respective Monitor Tag (ID) word. That is, assuming that bit 10 of the “ETEST” register was assigned a value of logic “1,” there should be a total of four (4) words stored in the Word Monitor RAM, starting at the monitor stack pointer address (e.g., 0000) for each word transmitted. These are, for each word transmitted:

   i. Word Data (CHANNEL A(B)) – The 16-bit word data written in step (4).

   ii. Tag Word (ID Word). This will indicate bus channel, word validity, command/status, data sync type, some timing information and other bits for the first received version of the transmitted word. This word will usually indicate the most recent bus channel transmitted (A or B). However, it’s theoretically possible for the test word to be received on the alternate (non-transmitting) channel first.

iii. Word Data (CHANNEL B(A)) – Like step (i), verify that this word matches the 16-bit word data written in step (4).

iv. Tag Word (ID Word). --- This word should be the same pattern as read in step (ii), except that it will indicate the alternate bus channel from the word represented by verification steps (i) and (ii). In addition, the timing information may be different.

6. HOST INTERFACE

The HI-6200 uses a parallel bus interface for communications with the host. Host interface to registers and RAM is enabled through the Chip Enable ($\overline{CE}$) pin, and accessed via 16-bit data bus and several host-originated control signals described below. Timing is identical for register operations and RAM operations via the host bus interface, with the exception that RAM read operations are sped up by prefetching, which eliminates WAIT states during sequential RAM address reads (see below).

The bus interface is compatible with the two prevalent host bus control signal methods: “Intel style” interface, characterized by separate strobes for read and write operations ($\overline{OE}$ and $\overline{WE}$), and “Motorola style” interface, characterized by a single read/write strobe ($\overline{STR}$) and a data direction signal (R/$\overline{W}$). Bus control style is selected using the BTYPE configuration pin, which sets the function of two other input pins to serve as either $\overline{OE}$ and $\overline{WE}$, or $\overline{STR}$ and R/$\overline{W}$.

The BWID configuration pin selects either 8- or 16-bit bus widths. When the BWID pin is connected to ground (logic “0”), 8-bit mode is selected; two bytes are sequentially transferred for each 16-bit word operation and all transacted data uses bus data pins D7:0 (bus data pins D15:8 are not used). The BENDI and MSB / LSB pins are used in conjunction with each other to define the byte order. When the BWID pin is connected high or left unconnected, 16-bit bus width is used and data is transacted on bus data pins D15:0. For 16-bit bus operation, the MSB/LSB pin is “Don’t Care” and byte order is defined by the BENDI pin. The interoperability of BWID, BENDI and MSB / LSB pins is outlined in detail in section “Table 12. BENDI Pin Functionality”.

6.1. Bus Wait States and Data Prefetch for RAM Reads

The HI-6200 has a WAIT output pin that tells the host to add wait states when additional access time is needed during bus read cycles. For compatibility with different host processors, the state of the WPOL input pin sets the WAIT output as active high or active low. The WAIT output can be ignored when the host processor read cycle time is always slow enough to work with the HI-6200 bus. When using faster host processors, cycle time is sometimes slowed down by configuring the processor to add one or more wait states during every read or write cycle, but slow-down affects all cycles, even when unnecessary.

Data prefetch is a technique used by the HI-6200 to speed up host multi-word read access to RAM by eliminating wait states. Prefetching occurs when HI-6200 logic requests data before it is actually needed. Because RAM locations are often read sequentially, performance improves when data is prefetched in address sequence order. For every host read cycle, the device first reads the addressed location, then prefetches the following address, to speed up access in the likely event that the following word will be read next.

For the HI-6200, WAIT is always asserted for the first word fetched in any RAM read sequence. The first read cycle has a long access time because there is no prefetch. This may be the first byte read in 8-bit mode, or the first word read in 16-bit mode. After each word (or byte) is fetched for a read operation, the next word (or byte) is prefetched to speed-up the read cycle time when sequential address read sequences occur. After the first word read, the following words read in sequence are accessed without WAIT, resulting in faster overall multi-word read timing. As long as bytes or words are read in address order, additional wait states are unnecessary.

For fastest read access under all conditions, the user can set host processor bus timing (by adjusting processor wait states for the chip select assigned to the HI-6200) to match the faster read cycle time for prefetched data, while the HI-6200 WAIT output adds one or more additional wait states for the slower initial read cycle.

NOTE: Register reads don’t use prefetch therefore will have a WAIT cycle during every address read.

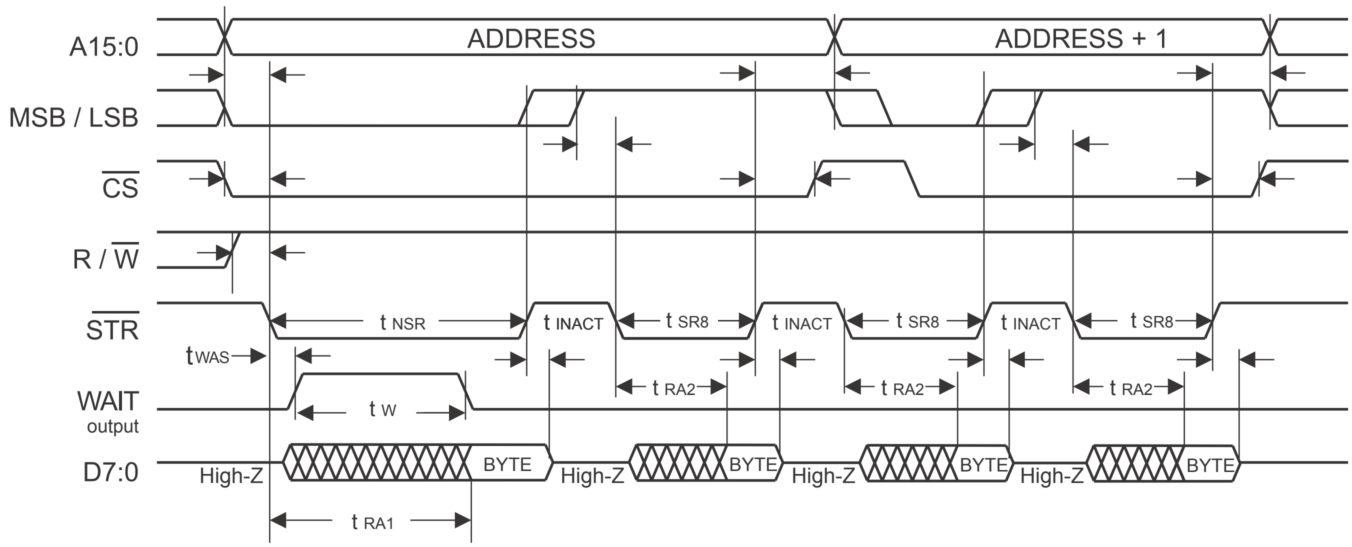
Timing diagrams for host read and write operations are shown in the following pages. Separate diagrams show “Intel style” and “Motorola style” control interfaces.

6.2. Host RAM Read Operation Timing

After the first byte is read, prefetch allows faster access times for successive reads, as long as read addresses are sequential. WAIT is always asserted during the first read cycle and is never asserted for successive read cycles to sequential addresses. This allows the default host bus configuration for the HI-6200 chip select to match the timing characteristics of the faster successive cycles, while the slower initial cycle is handled on a WAIT-controlled exception basis. WAIT can be optionally inverted using the WPOL pin.

Host RAM read operations for 8-bit bus width (Figure 3) and 16-bit bus width (Figure 4) using "Motorola style" bus control (pin BTYPE =0) are shown below. See for timing parameter values.

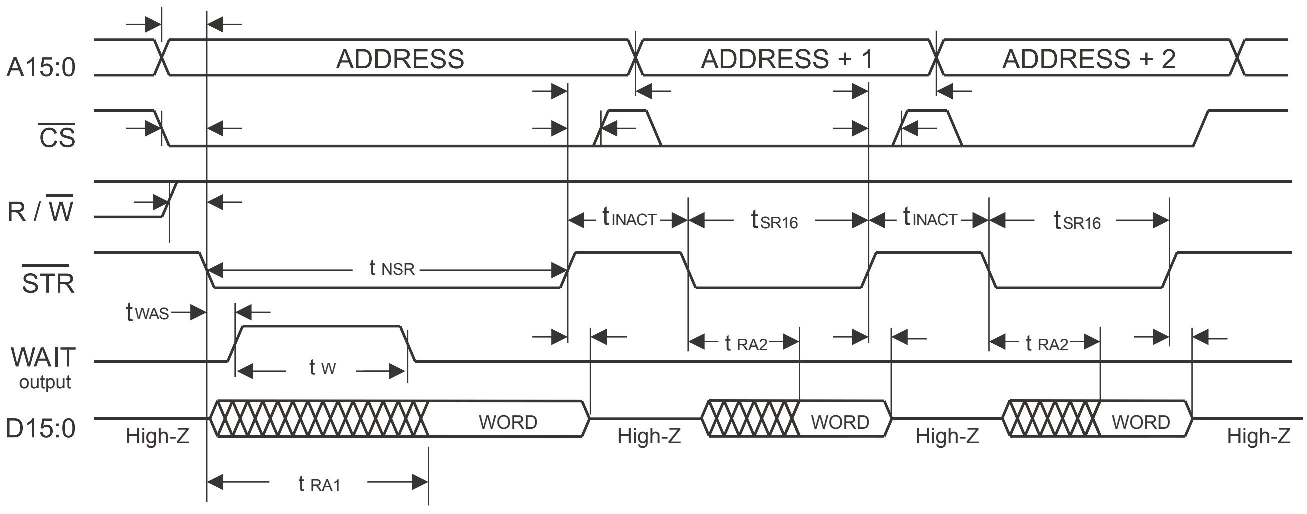
showing two successive 16-bit words (4 bytes) read from sequential addresses



All timing intervals equal 0 ns MIN unless otherwise indicated.

Figure 3. Host Read for 8-bit bus width using "Motorola style" bus control (pin BTYPE = 0).

showing a three word read access from sequential addresses



All timing intervals equal 0 ns MIN unless otherwise indicated.

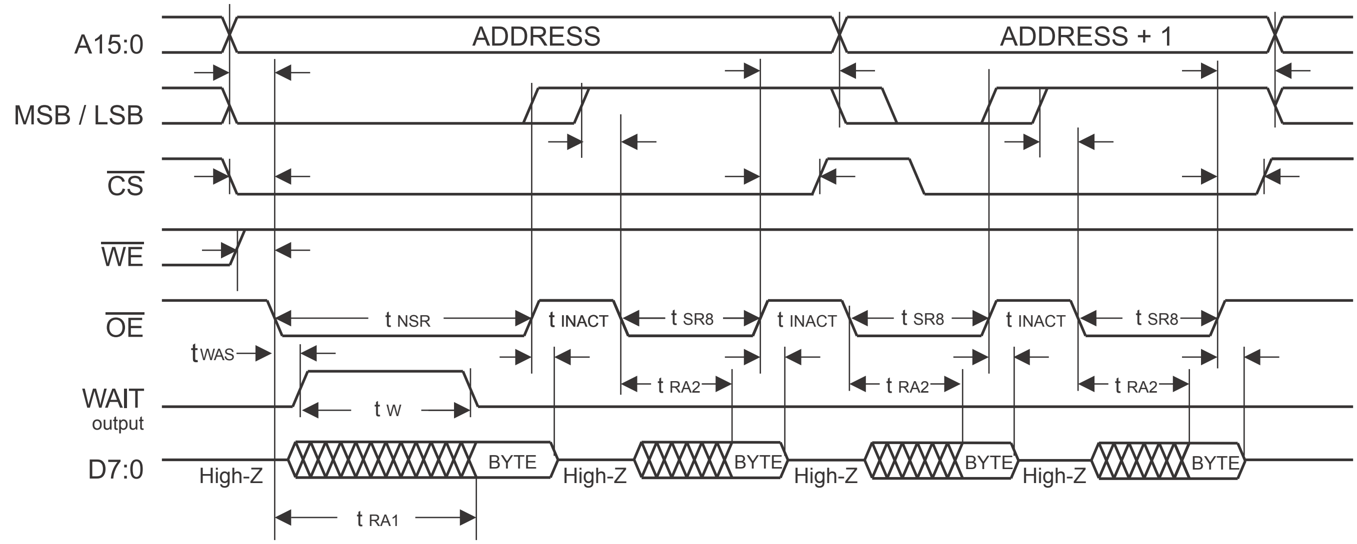
After first byte or word is read, prefetch allows faster access times for successive reads, as long as read addresses are sequential.

Figure 4. Host Read for 16-bit bus width using “Motorola style” bus control (pin BTYPE = 0).

Host Interface

The following figures show host RAM read operations for 8-bit bus width (Figure 5) and 16-bit bus width (Figure 6) using “Intel style” bus control (pin BTYPE =1).

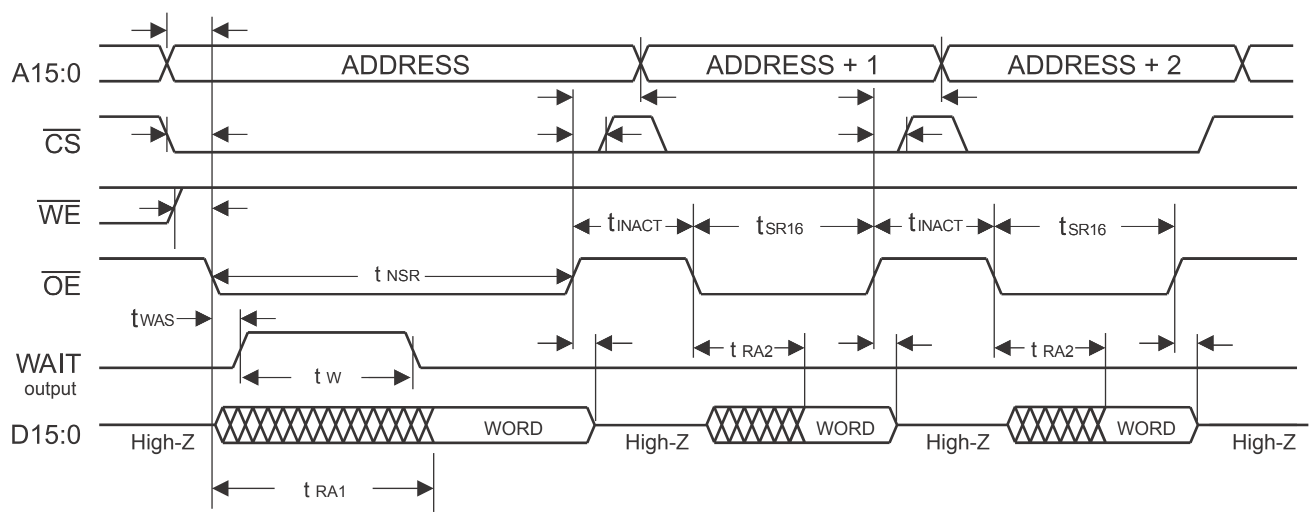
showing two successive 16-bit words (4 bytes) read from sequential addresses



All timing intervals equal 0 ns MIN unless otherwise indicated.

Figure 5. Host Read for 8-bit bus width using “Intel style” bus control (pin BTYPE = 1).

showing a three word read access from sequential addresses



All timing intervals equal 0 ns MIN unless otherwise indicated.

After first byte or word is read, prefetch allows faster access times for successive reads, as long as read addresses are sequential.

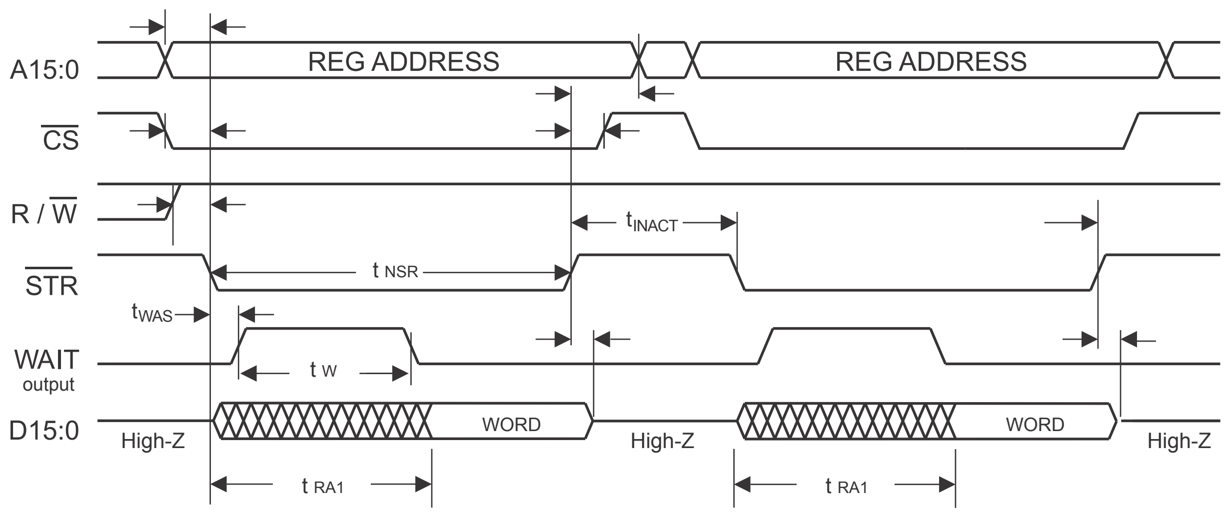
Figure 6. Host Read for 16-bit bus width using “Intel style” bus control (pin BTYPE = 1).

6.3. Host Register Read Operation Timing

Host register read operations are identical to RAM read operations with the exception that there is no prefetching for sequential address reads and therefore every address read will have a WAIT cycle. This is shown below in Figure 7 and Figure 8 for "Motorola style" and "Intel style" bus control respectively.

When using 8-bit bus width, all register reads behave in a similar fashion to their respective RAM reads, except all register read accesses have a WAIT cycle for each address that is read.

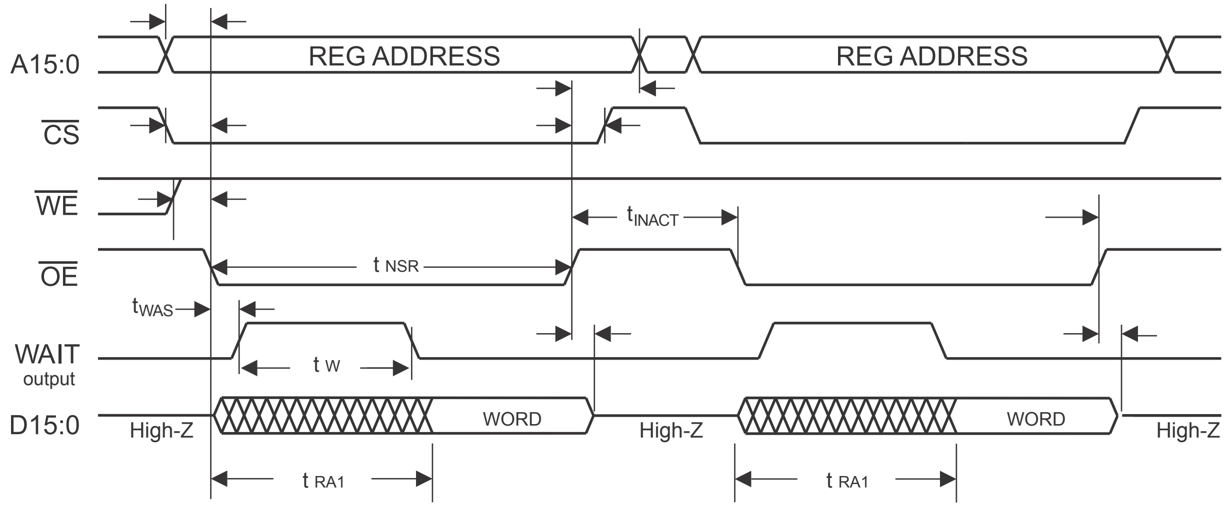
Showing two 16-bit words read from sequential or non-sequential Register addresses



All timing intervals equal 0 ns MIN unless otherwise indicated.

Figure 7. Host sequential (or non-sequential) Register Read for 16-bit bus width using "Motorola style" bus control.

Showing two 16-bit words read from sequential or non-sequential Register addresses



All timing intervals equal 0 ns MIN unless otherwise indicated.

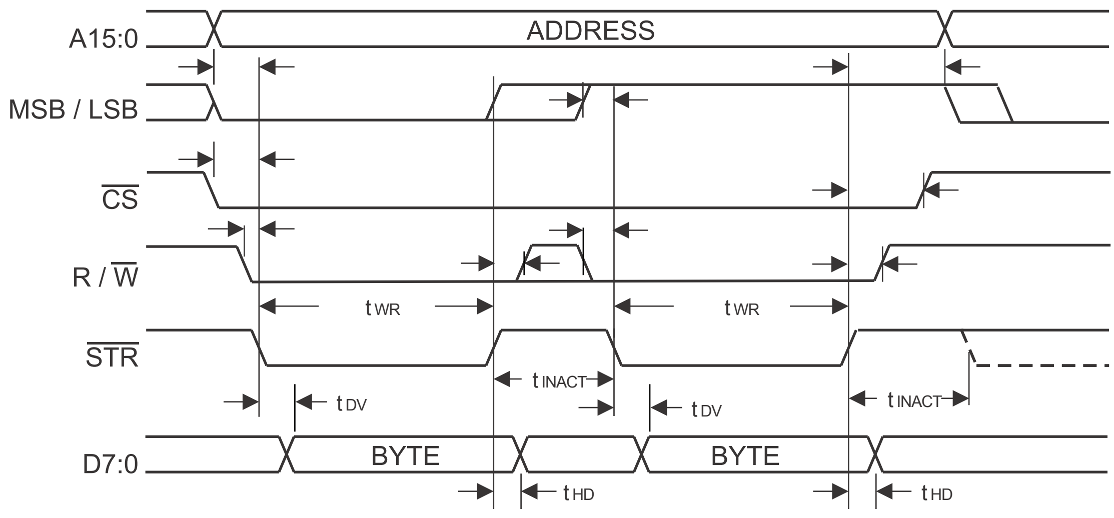
Figure 8. Host sequential (or non-sequential) Register Read for 16-bit bus width using “Intel style” bus control.

6.4. Host RAM and Register Write Operation Timing

Host RAM and register write operations behave exactly the same via the host bus interface.

Figure 9 and Figure 10 show examples of host RAM and register write operations for 8-bit bus width and 16-bit bus width "Motorola style" bus control (pin BTYPE =0) are shown below.

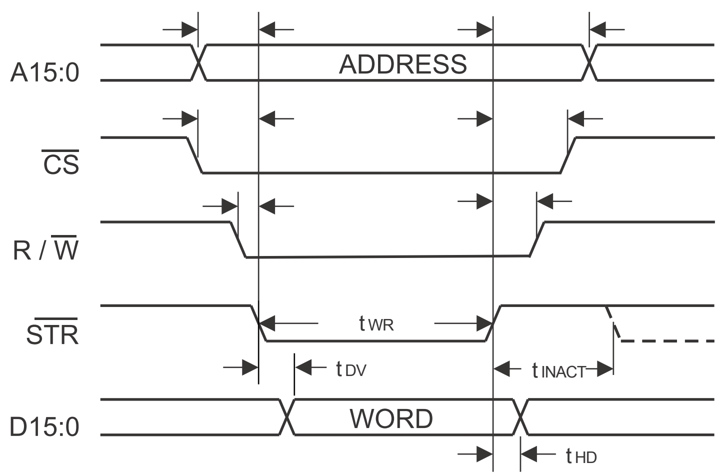
showing 2 bytes written for a single 16-bit word



All timing intervals equal 0 ns MIN unless otherwise indicated.
The WAIT output is inactive during write access

Figure 9. Host Write for 8-bit bus width using "Motorola style" bus control (pin BTYPE = 0).

showing a one-word write cycle. Successive writes to sequential addresses have same timing.



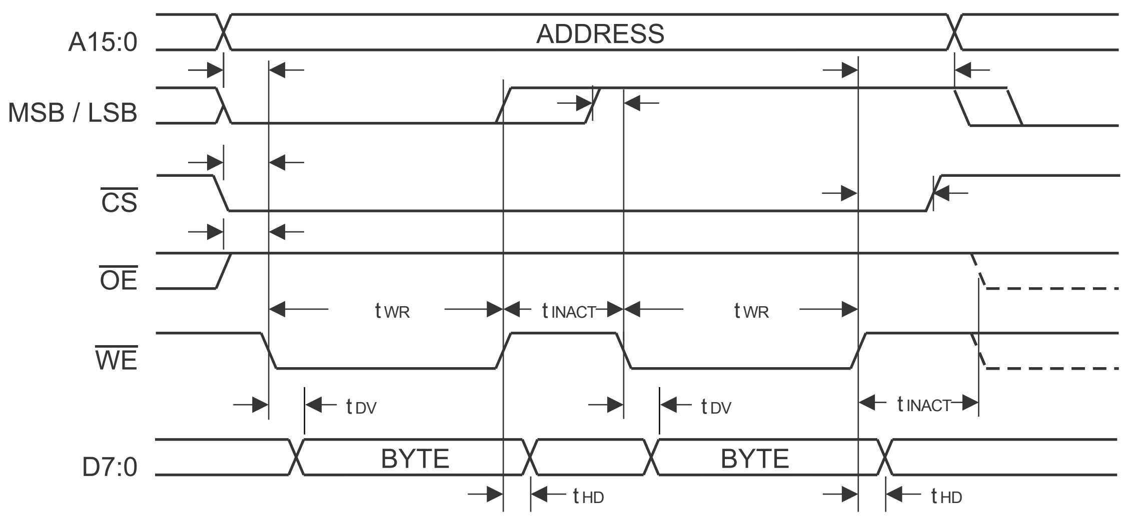
All timing intervals equal 0 ns MIN unless otherwise indicated.
The WAIT output is inactive during write access

Figure 10. Host Write for 16-bit bus width using "Motorola style" bus control (pin BTYPE = 0).

Host Interface

The following figures show host RAM and register write operations for 8-bit bus width (Figure 11) and 16-bit bus width (Figure 12) using “Intel style” bus control (pin BTYPE =1).

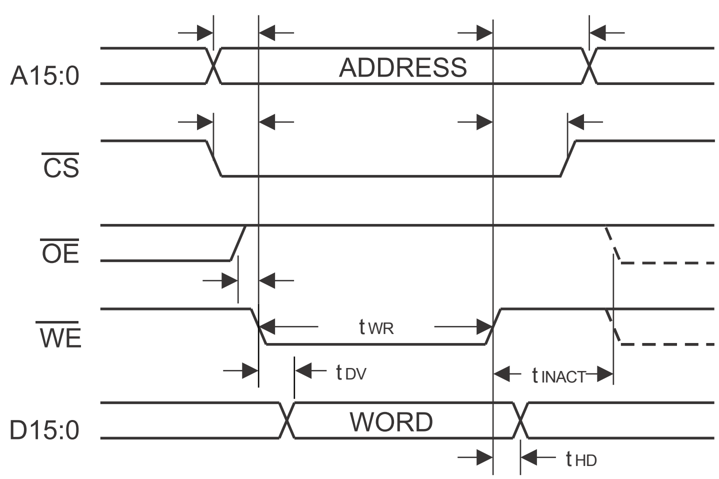
showing 2 bytes written for a single 16-bit word



All timing intervals equal 0 ns MIN unless otherwise indicated.
The WAIT output is inactive during write access

Figure 11. Host Write for 8-bit bus width using “Intel style” bus control (pin BTYPE = 1).

showing a one-word write cycle. Successive writes to sequential addresses have same timing.



All timing intervals equal 0 ns MIN unless otherwise indicated.
The WAIT output is inactive during write access

Figure 12. Host Write for 16-bit bus width using “Intel style” bus control (pin BTYPE = 1).

Table 16. Host Bus Interface Timing

Parameters	Symbol	Limits			Units
		Min	Typ	Max	
WRITE TIMING					
Write strobe (@ 50 MHz)	t_{WR}	55	-	-	ns
(@ 40 MHz)		68	-	-	ns
(@ 20 MHz)		130	-	-	ns
(@ 16 MHz)		162	-	-	ns
Write inactive time (@ 50 MHz)	t_{INACT}	25	-	-	ns
(@ 40 MHz)		30	-	-	ns
(@ 20 MHz)		55	-	-	ns
(@ 16 MHz)		68	-	-	ns
Write data available	t_{DV}	-	-	20	ns
Write cycle, t_{WR} + t_{INACT} (@ 50 MHz)	-	80	-	-	ns
(@ 40 MHz)		98	-	-	ns
(@ 20 MHz)		185	-	-	ns
(@ 16 MHz)		230	-	-	ns
READ TIMING					
Wait assertion time	t_{WAS}	-	-	20	ns
Wait time (@ 50 MHz)	t_W	-	-	110	ns
(@ 40 MHz)		-	-	138	ns
(@ 20 MHz)		-	-	275	ns
(@ 16 MHz)		-	-	344	ns
Read strobe, sequential RAM address, 8-bit bus mode (@ 50 MHz)	t_{SR8}	55	-	-	ns
(@ 40 MHz)		68	-	-	ns
(@ 20 MHz)		130	-	-	ns
(@ 16 MHz)		162	-	-	ns
Read strobe, sequential RAM address, 16-bit bus mode (@ 50 MHz)	t_{SR16}	55	-	-	ns
(@ 40 MHz)		68	-	-	ns
(@ 20 MHz)		130	-	-	ns
(@ 16 MHz)		162	-	-	ns
Read strobe, non-sequential address (@ 50 MHz)	t_{NSR}	130	-	-	ns
(@ 40 MHz)		163	-	-	ns
(@ 20 MHz)		325	-	-	ns
(@ 16 MHz)		407	-	-	ns

Parameters	Symbol	Limits			Units
		Min	Typ	Max	
Read inactive time (@ 50 MHz)	t_{INACT}	25	-	-	ns
(@ 40 MHz)		30	-	-	ns
(@ 20 MHz)		55	-	-	ns
(@ 16 MHz)		68	-	-	ns
Read access time1 (@ 50 MHz)	t_{RA1}	-	-	130	ns
(@ 40 MHz)		-	-	163	ns
(@ 20 MHz)		-	-	325	ns
(@ 16 MHz)		-	-	407	ns
Read access time2 (@ 50 MHz)	t_{RA2}	-	-	55	ns
(@ 40 MHz)		-	-	68	ns
(@ 20 MHz)		-	-	130	ns
(@ 16 MHz)		-	-	162	ns
Read cycles in 8-bit bus mode (see note below)					
Read cycle, sequential address, 16-bit word, 8-bit bus mode, $t_{SR8} + t_{INACT} + t_{SR8} + t_{INACT}$ (@ 50 MHz)	-	160	-	-	ns
(@ 40 MHz)		196	-	-	ns
(@ 20 MHz)		370	-	-	ns
(@ 16 MHz)		460	-	-	ns
Read cycle, non-sequential address, 8-bit bus mode, $t_{WAS} + t_W + t_{INACT} + t_{SR8}$ (@ 50 MHz)	-	-	-	210	ns
(@ 40 MHz)		-	-	256	ns
(@ 20 MHz)		-	-	480	ns
(@ 16 MHz)		-	-	594	ns
Read cycles in 16-bit bus mode (see note below)					
Read cycle, sequential address, 16-bit bus mode, $t_{SR16} + t_{INACT}$ (@ 50 MHz)	-	80	-	-	ns
(@ 40 MHz)		98	-	-	ns
(@ 20 MHz)		185	-	-	ns
(@ 16 MHz)		230	-	-	ns
Read cycle, non-sequential address, 16-bit bus mode, $t_{WAS} + t_W$ (@ 50 MHz)	-	-	-	130	ns
(@ 40 MHz)		-	-	158	ns
(@ 20 MHz)		-	-	295	ns
(@ 16 MHz)		-	-	364	ns

NOTE: When reading a series of sequential RAM addresses, the read cycle for the first word (or byte) location is always longer because the HI-6200 asserts the WAIT output. As long as sequential addresses are then read, automatic prefetch speeds up read access for following words (or bytes) since these occur without WAIT assertion. When reading register addresses, the WAIT output is asserted for each address, whether sequential or not.

7. ELECTRICAL CHARACTERISTICS

7.1. Absolute Maximum Ratings

Supply voltages	Logic	-0.3 V to +6.0 V
	Transceivers	-0.3 V to +6.0 V
Logic input voltage range		-0.3 V to +6.0 V
Receiver differential voltage		10 Vp-p
Solder Temperature (reflow)		260°C
Junction Temperature		175°C
Storage Temperature		-65°C to +150°C

7.2. Recommended Operating Conditions

Parameters		Limits			Unit
		Min	Typ	Max	
Supply Voltages	Logic	3.15	3.3	5.5	V
	3.3V Transceivers	3.15	3.3	3.46	V
	5.0V Transceivers (HI-62025 only)	4.75	5.0	5.25	V
Temperature Range	Industrial	-40		85	°C
	Extended	-55		125	°C

7.3. DC Electrical Characteristics

Unless otherwise stated, V_{DD} = 3.3V, GND = 0V, T_A = Operating Temperature Range

Parameters		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Power Supply							
Operating Supply Voltages	Logic	V_{Logic}		3.15	3.3	5.5	V
	3.3V Transceivers	V_{DD}		3.15	3.3	3.46	V
	5.0V Transceivers (HI-62025 only)	V_{DD}		4.75	5.0	5.25	V
Power Supply Current (Isolation Transformer ratio of 1:2.07 for MIL-STD-1553 only Compliant Application) See Note 1	V_{LOGIC} = 3.3V = V_{DD}	I_{CC1}	Not Transmitting	-	40	50	mA
		I_{CC2}	Continuous supply current while one bus transmits @ 50% duty cycle	-	390	460	mA
		I_{CC23}	Continuous supply current while one bus transmits @ 100% duty cycle	-	745	885	mA
Power Dissipation (Isolation Transformer ratio of 1:2.07 for MIL-STD-1553 only Compliant Application) See Note 2	V_{LOGIC} = 3.3V = V_{DD}	PD_1	Not Transmitting	-	132	175	mW
		PD_2	Transmit one bus @ 50% duty cycle	-	305	395	mW
		PD_3	Transmit one bus @ 100% duty cycle	-	540	765	mW
Power Supply Current (Isolation Transformer ratio of 1:2.5 for MIL-STD-1760/1553 Compliant Application) See Note 1	V_{LOGIC} = 3.3V = V_{DD}	I_{CC1}	Not Transmitting	-	40	50	mA
		I_{CC2}	Continuous supply current while one bus transmits @ 50% duty cycle	-	450	530	mA
		I_{CC23}	Continuous supply current while one bus transmits @ 100% duty cycle	-	875	1040	mA
Power Dissipation (Isolation Transformer ratio of 1:2.5 for MIL-STD-1760/1553 Compliant Application) See Note 3	V_{LOGIC} = 3.3V = V_{DD}	PD_1	Not Transmitting	-	132	175	mW
		PD_2	Transmit one bus @ 50% duty cycle	-	520	700	mW
		PD_3	Transmit one bus @ 100% duty cycle	-	960	1300	mW
Power Supply Current (HI-62025 only) (Isolation Transformer ratio of 1:2.5 for MIL-STD-1760/1553 Compliant Application) See Note 1	V_{LOGIC} = 3.3V V_{DD} = 5.0V	I_{CC1}	Not Transmitting	-	40	50	mA
		I_{CC2}	Continuous supply current while one bus transmits @ 50% duty cycle	-	295	330	mA
		I_{CC23}	Continuous supply current while one bus transmits @ 100% duty cycle	-	560	600	mA

Parameters		Symbol	Conditions	Limits Min	Limits Typ	Limits Max	Unit
Power Dissipation (HI-62025 only) (Isolation Transformer ratio of 1:2.5 for MIL-STD-1760/1553 Compliant Application) See Note 4	V_{LOGIC} = 3.3V V_{DD} = 5.0V	PD_1	Not Transmitting	-	200	265	mW
		PD_2	Transmit one bus @ 50% duty cycle	-	1.0	1.1	W
		PD_3	Transmit one bus @ 100% duty cycle	-	1.45	1.55	W
Logic							
Input Voltage (High)		V_{IH}	All digital inputs, except CLK_{IN}	2.1	-	-	V
			CLK_{IN}	0.8			V_{DD}
Input Voltage (Low)		V_{IL}	All digital inputs, except CLK_{IN}	-	-	0.7	V
			CLK_{IN}			0.2	V_{DD}
Schmidt Trigger Hysteresis		V_{HYST}	All digital inputs, except CLK_{IN} V_{LOGIC} = 3.6V or 5.25V	0.2			V
Input Current (High)		I_{IH}	All digital inputs, except CLK_{IN} V_{LOGIC} = 3.6V or 5.25V, V_{IH} = 2.5V	-100	-	-10	µA
			CLK_{IN}	-10	-	10	µA
Input Current (Low)		I_{IL}	All digital inputs, except CLK_{IN} V_{LOGIC} = 3.6V or 5.25V, V_{IL} = 0V	-100	-	-20	µA
			CLK_{IN}	-10	-	10	µA
Output Voltage (High)		V_{OH}	V_{LOGIC} = 3.15V or 4.5V, V_{IH} = 2.7V, V_{IL} = 0.2V, I_{OH} = max	2.4	-	-	V
Output Voltage (Low)		V_{OL}	V_{LOGIC} = 3.15V or 4.5V, V_{IH} = 2.7V, V_{IL} = 0.2V, I_{OL} = max	-	-	0.5	V
Output Current (High)		I_{OH}	V_{LOGIC} = 3.15V	-	-	-2.2	mA
			V_{LOGIC} = 4.5V	-	-	-3.4	mA
Output Current (Low)		I_{OL}	V_{LOGIC} = 3.15V	2.2	-	-	mA
			V_{LOGIC} = 4.5V	3.4	-	-	mA
RECEIVER (Measured at Point "AD" in Table 1 unless otherwise specified)							
Input Resistance		R_{IN}	Differential	20	-	-	kΩ
Input Capacitance		C_{IN}	Differential	-	-	5	pF
Common Mode Rejection Ratio		CMRR		40	-	-	dB
Input Level		V_{IN}	Differential	-	-	9	Vp-p
Input Common Mode Voltage		V_{ICM}		-10	-	+10	V-pk

Electrical Characteristics

Parameters		Symbol	Conditions	Limits Min	Limits Typ	Limits Max	Unit
Threshold Voltage (Direct-Coupled)	Detect	V_{THD}	1 MHz Sine Wave (Measured at Point “AD“ in Table 1)	1.2	-	20.0	Vp-p
	No Detect	V_{THND}		-	-	0.28	Vp-p
Threshold Voltage (Transformer-Coupled)	Detect	V_{THD}	1 MHz Sine Wave (Measured at Point “AT“ in 2.2)	0.86	-	14.0	Vp-p
	No Detect	V_{THND}		-	-	0.2	Vp-p
TRANSMITTER (Measured at Point “AD” in Table 1 unless otherwise specified)							
Output Voltage	Direct Coupled	V_{OUT}	35Ω Load	6.0	7.2	9.0	Vp-p
	Transformer Coupled	V_{OUT}	70Ω Load (Measured at Point “AT“ in 2.2)	20.0	21.5	27.0	Vp-p
Output Noise		V_{ON}	Differential, inhibited	-	-	14.0	mV_{RMS}
Output Dynamic Offset Voltage	Direct Coupled	V_{DYN}	35Ω Load	-90	-	90	mV
	Transformer Coupled	V_{DYN}	70Ω Load (Measured at Point “AT“ in 2.2)	-250	-	250	mVp
Rise/Fall Time		$t_{r/f}$		100	150	300	ns
Output Resistance		R_{OUT}	Differential, not transmitting	10	-	-	kΩ
Output Capacitance		C_{OUT}	1 MHz sine wave	-	-	15	pF
Clock Input							
Frequency	(Default)	CLK_{IN}			50.0		MHz
	(option)				40.0		MHz
	(option)				20.0		MHz
	(option)				16.0		MHz
Master Reset ($\overline{\text{MSTCLR}}$) Timing							
Minimum $\overline{\text{MSTCLR}}$ pulsewidth for Master Reset		t_{MR}	Rise Time < 10µs	100			ns
MIL-STD-1553 Message Timing							
Completion of CPU write (BC Start) to Start of First Message for non-Enhanced BC Mode				2.5			µs
BC intermessage gap time (typical value; may be lengthened under software control to 65.535 ms)			non-Enhanced BC Mode		9.5		µs
			Enhanced BC Mode		10.5		µs
BC/RT/MT Response Timeout (Software programmable, 4 options)			18.5 nominal	17.5	18.0	19.5	µs
			22.5 nominal	21.5	22.5	23.5	µs
			50.5 nominal	49.5	50.5	51.5	µs
			128.0 nominal	127.0	129.5	131.0	µs
RT Response Time (mid-parity to mid-sync)				4		7	µs
Transmitter Watchdog Timeout					660.5		µs

Note 1: In actual use, the highest practical transmit duty cycle is 96%, occurring when a Remote Terminal responds to a series of 32 data word transmit commands (RT to BC) repeating with minimum intermessage gap of 4µs (2µs dead time) and typical RT response delay of 5µs.

Note 2: While one bus continuously transmits, the power delivered by the 3.3V power supply is 3.3V × 745mA typical = 2.46W. Of this, 540mW is dissipated in the device, the remainder in the load.

Note 3: While one bus continuously transmits, the power delivered by the 3.3V power supply is 3.3V × 875mA typical = 2.89W. Of this, 960mW is dissipated in the device, the remainder in the load.

Note 4: While one bus continuously transmits, the power delivered by the 5.0V power supply is 5.0V × 560mA typical = 2.80W. Of this, 1.45W is dissipated in the device, the remainder in the load.

7.4. MIL-STD-1553/1760 Bus Interface

MIL-STD-1553 integrated circuits commonly meet both MIL-STD-1553 and MIL-STD-1760 requirements. One of the main electrical differences between MIL-STD-1760 and MIL-STD-1553 is the minimum transmit voltage amplitude. For transformer coupled stub connections, MIL-STD-1760 requires amplitudes between 20 Vp-p and 27 Vp-p. By contrast, MIL-STD-1553 requires a lower 18 Vp-p to 27 Vp-p.

The HI-6200 family of devices support both MIL-STD-1760 and MIL-STD-1553 bus amplitude by default when paired with a 1:2.5 turns ratio isolation transformer, as shown in Figure 13 below.

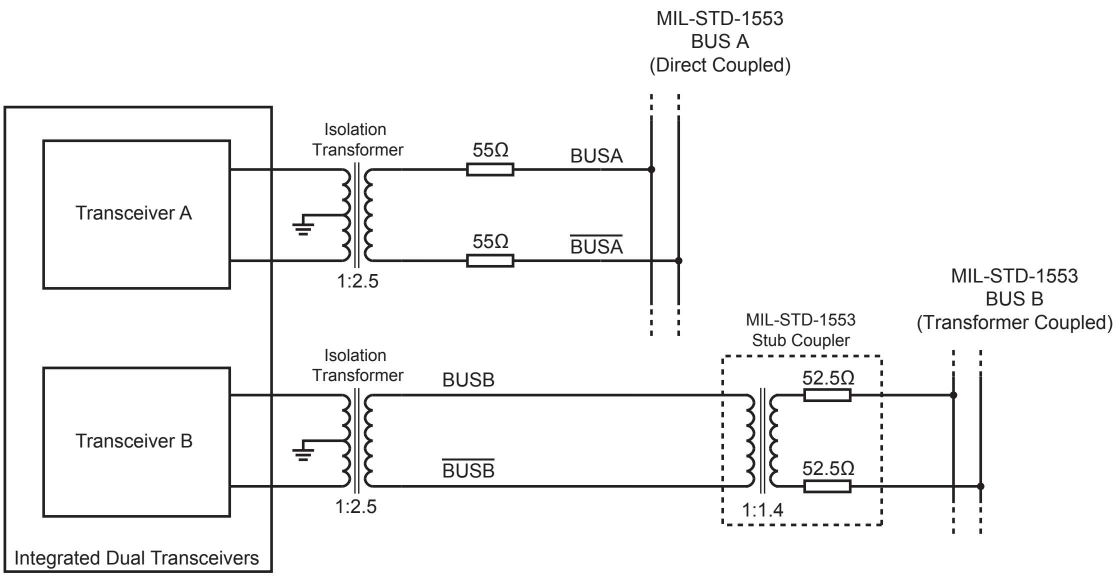


Figure 13. 3.3V Transceivers, MIL-STD-1760/1553 Transmit Amplitude

7.4.1. MIL-STD-1553 Bus Interface

Supporting a higher minimum transmit amplitude to meet both MIL-STD-1760 and MIL-STD-1553 requirements has the effect of higher power consumption and power dissipation. If the requirement is to support the lower MIL-STD-1553B voltage amplitude of 18 Vp-p only, then the HI-6200 may be paired with a 1:2.07 turns ratio isolation transformer as shown in Figure 14 below. The lower turns ratio will result in a lower transmit amplitude and thus lower power consumption and dissipation. See “DC Electrical Characteristics” above.

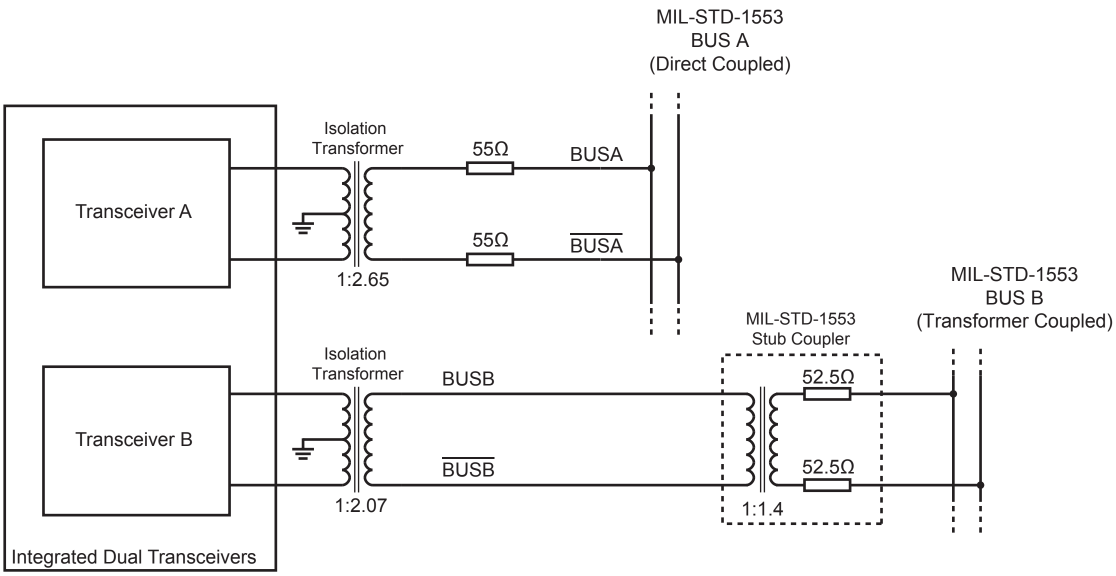


Figure 14. 3.3V Transceivers, MIL-STD-1553 Transmit Amplitude

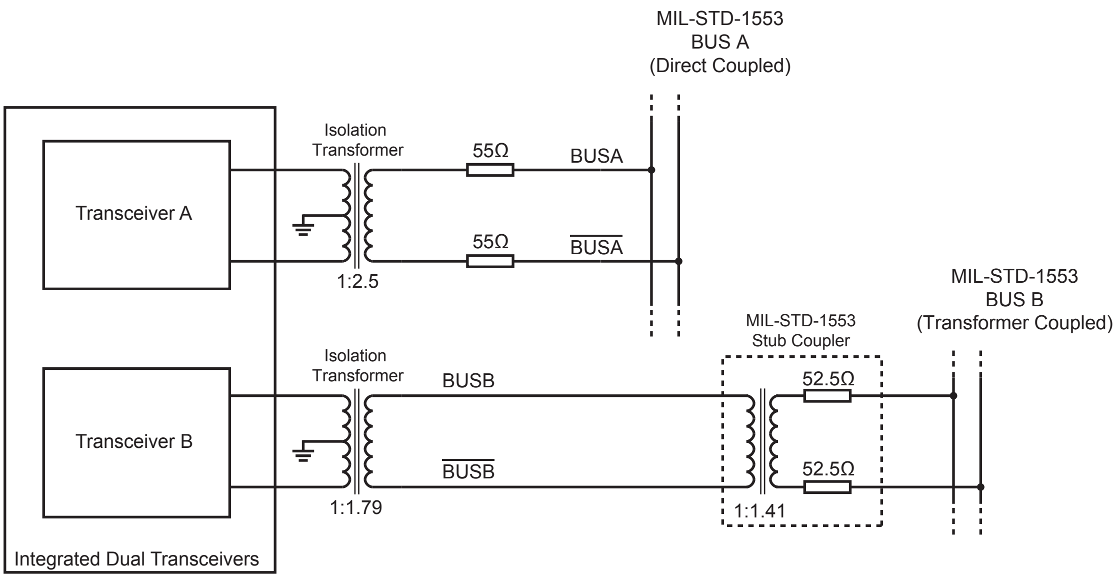


Figure 15. 5.0V Transceivers (HI-62025 only), MIL-STD-1760/1553 Transmit Amplitude

7.4.2. Recommended MIL-STD-1553 Transformers

Holt recommends Premier Magnetics transformers as offering the best combination of electrical performance, low cost and small footprint.

Manufacturer	Part Number	Number of Cores	Turns Ratio(s)	Form Factor	Dimensions (LxWxH) Temperature
Premier Magnetics	PM-DB2798S	Single	1:1.79 / 1:2.5	Surface Mount	10.16 x 10.16 x 4.699 mm
Premier Magnetics	PM-DB2762	Dual	1:2.5	Surface Mount	10.16 x 10.16 x 8.128 mm
Premier Magnetics	PM-DB2776	Dual	1:1.79 / 1:2.5	Surface Mount	17.145 x 10.16 x 4.699 mm
Premier Magnetics	PM-DB27501S	Single	1:2.65 / 1:2.07	Surface Mount	10.16 x 10.16 x 4.699 mm
Premier Magnetics	PM-DB2779	Dual	1:2.65 / 1:2.07	Surface Mount	17.145 x 10.16 x 4.699 mm
Premier Magnetics	PM-DB2771	Dual	1:2.07	Surface Mount	10.16 x 10.16 x 8.128 mm

7.5. MIL-STD-1553 Test Circuits

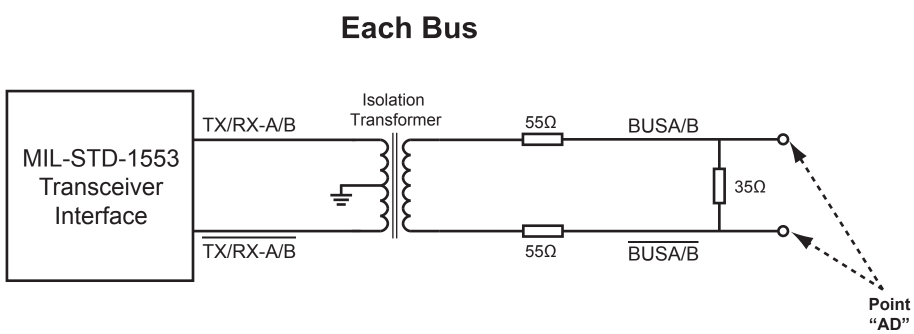


Figure 16. MIL-STD-1553 Direct Coupled Test Circuits

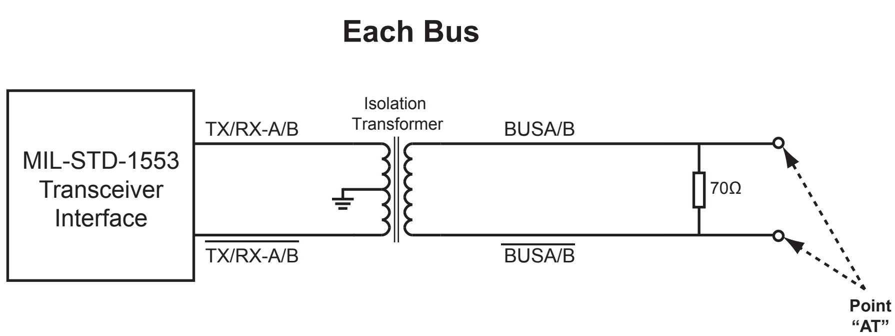


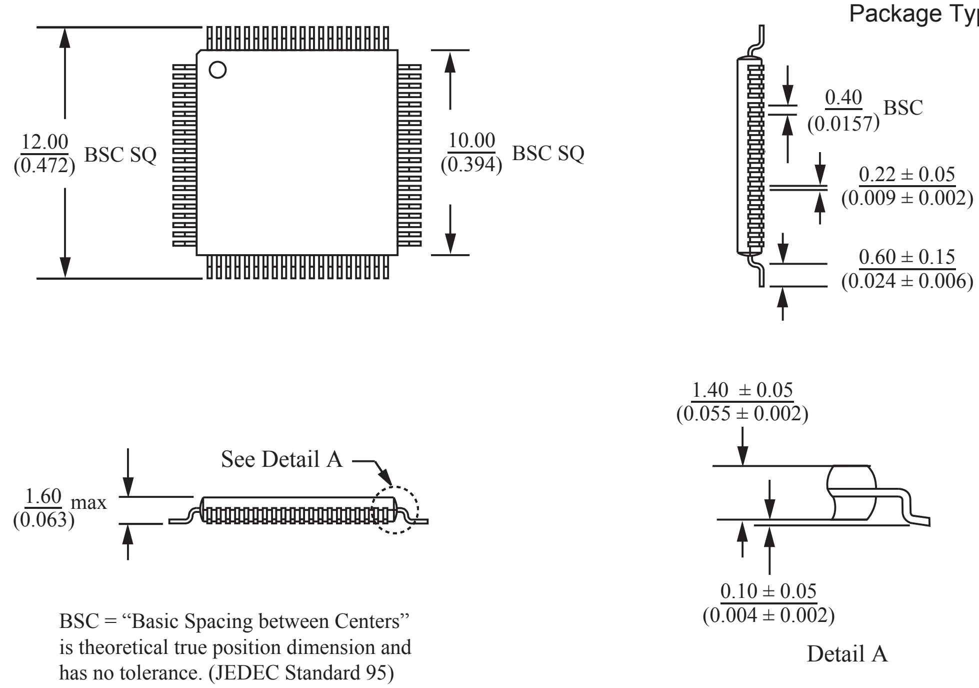
Figure 17. MIL-STD-1553 Transformer Coupled Test Circuits

8. PACKAGE DIMENSIONS

80-PIN PLASTIC QUAD FLAT PACK (PQFP)

millimeters (inches)

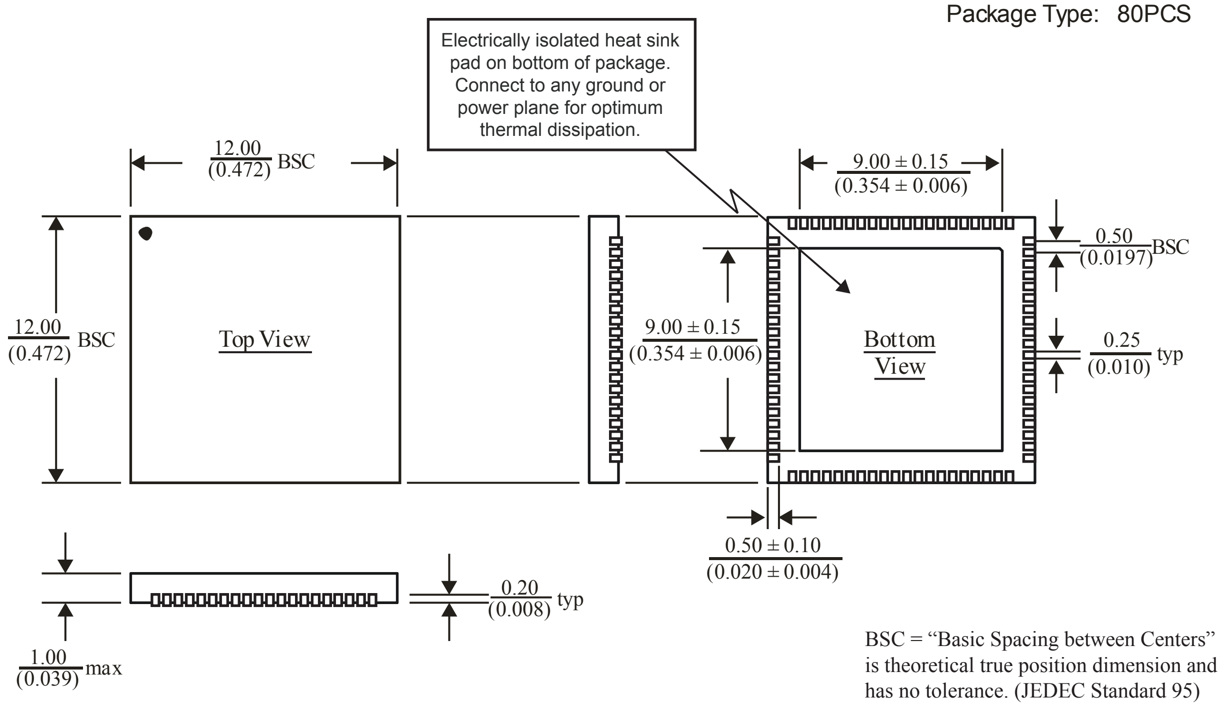
Package Type: 80PTQS



80-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

millimeters (inches)

Package Type: 80PCS



9. ORDERING INFORMATION

HI - 620 x 3 Px x x

Blank	=	Leaded, non-RoHS compliant
F	=	RoHS Compliant
I	=	−40°C to +85°C
T	=	−55°C to +125°C
PC	=	80-pin plastic QFN package, 12mm x 12mm x 1mm
PQ	=	80-pin plastic QFP package, 12mm x 12mm x 1.6mm
3	=	3.3V Transceiver supply voltage
0	=	BC/MT/RT, 64K x 16 bit word ECC RAM
2	=	RT only, 64K x 16 bit word ECC RAM

HI - 620 2 5 PQ x x

Blank	=	Leaded, non-RoHS compliant
F	=	RoHS Compliant
I	=	−40°C to +85°C
T	=	−55°C to +125°C
PQ	=	80-pin plastic QFP package, 12mm x 12mm x 1.6mm
5	=	5.0V Transceiver supply voltage
2	=	RT only, 64K x 16 bit word ECC RAM

10. REVISION HISTORY

Revision	Date	Description of Change
DS6200, Rev. New	05/10/18	Initial Release
A	07/02/18	Correct typo in ordering information
B	10/03/18	Add additional notes regarding ECC RAM feature. Correct numerous typos.
C	12/18/18	Update transformer ratios for direct and transformer coupled bus interfaces to 1:2.5. Add additional parameters t_{DV}, T_{RA1} and T_{RA2} to Table 14, “Host Bus Interface Timing”. Update timing diagrams in Figures 1 – 10.
D	01/17/19	Add Table to indicate Self-Test times and clarify total Power-up time. Update Host Bus Interface Timing parameter table to reflect clock frequency options.
E	05/20/19	Add package photos to title page. Add minor clarification to RTBOOT signal description (enables MIL-STD-1760 operation). Correct name of A0 signal.
F	11/14/19	Add more detail to register definitions and block diagram. Add pin diagrams, clarify pin descriptions. Update Logic Supply and Transceiver Supply voltage minimum to 3.15V Other minor updates and corrections.
G	05/01/2020	Update Power Supply Current and Power Dissipation parameters in “DC Electrical Characteristics” table for 3.3V devices. Add HI-62025 (5V transceiver option) to the datasheet and update all Electrical Characteristics to reflect this. Update dimensions of QFN package (80PCS).
H	08/12/2020	Correct typos in timing diagram labels.
J	11/06/2020	Add Supply Current and Power Dissipation numbers for 1:2.07 turns ratio isolation transformer to Electrical Characteristics.
K	07/14/2021	Correct typo in description of RAMST, bit 9, register 0x0003. Clarify description of BIST, bit 1, register 0x001E. Add timing parameters for $\overline{\text{MSTCLR}}$ to Electrical Characteristics.
L	10/07/2021	Correct errors in description of buffering modes in “RT Subaddress Control Word Register 0x0004”
M	12/09/2021	Clarify description of buffering modes in “RT Subaddress Control Word Register 0x0004”

Revision	Date	Description of Change
N	06/07/2023	Add hyperlinks to “Table 1. Register Summary”. Clarify operation of Monitor Active (MACT) bit 0 in “Table 6. Configuration Register #1, Enhanced Monitor Mode.” Add hysteresis value for digital inputs in “DC Electrical Characteristics” table. Add description for “Test Mode Register 1, ETest Register, Read/Write 0x0011”. Add new section on “Built-In Self-Test (BIST)”. Clarify description of bit 10 (256RO), in “Configuration Register #2, Read/Write 0x0002”. Correct typo in description of “BC Frame Time Remaining Register, Read Only 0x000B”.
P	01/22/2024	Add section on “Latching the RT Address and Parity”. Add pull-up/down values for digital inputs in “Signal and Pin Descriptions”.