MOSFET – P-Channel, POWERTRENCH®

-20 V, -18 A, 8.0 mΩ

FDMC510P

V_{DS}	$r_{DS(on)}$ MAX	I_D MAX
−20 V	8 mΩ @ −4.5 V	−18 A
	9.8 mΩ @ −2.5 V	
	13 mΩ @ −1.8 V	
	17 mΩ @ −1.5 V	

General Description

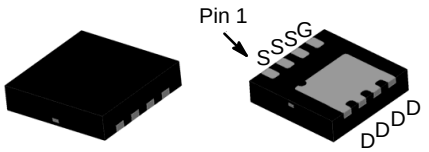
This P−Channel MOSFET is produce using **onsemi**'s advanced POWERTRENCH® process that has been optimized for $r_{DS(ON)}$, switching performance and ruggedness.

Features

- Max $r_{DS(on)}$ = 8.0 mΩ at V_{GS} = −4.5 V, I_D = −12 A
- Max $r_{DS(on)}$ = 9.8 mΩ at V_{GS} = −2.5 V, I_D = −10 A
- Max $r_{DS(on)}$ = 13 mΩ at V_{GS} = −1.8 V, I_D = −9.3 A
- Max $r_{DS(on)}$ = 17 mΩ at V_{GS} = −1.5 V, I_D = −8.3 A
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- 100% UIL Tested
- HBM ESD Capability Level >2 kV Typical (Note 4)
- This Device is Pb−Free, Halide Free and is RoHS Compliant

Applications

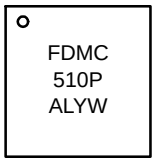
- Battery Management
- Load Switch



Top Bottom

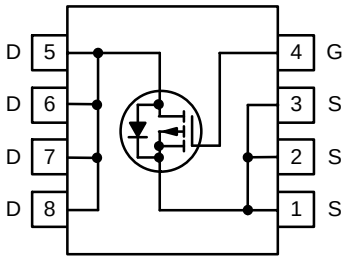
WDFN8 3.3x3.3, 0.65P
(MLP 3.3x3.3)
CASE 511DH

MARKING DIAGRAM



FDMC510P = Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week

PIN ASSIGNMENT



P−Channel MOSFET

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

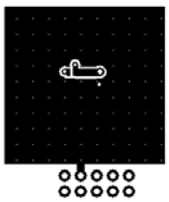
Symbol	Parameter			Ratings	Unit
V_{DS}	Drain to Source Voltage			−20	V
V_{GS}	Gate to Source Voltage			±8	V
I_D	Drain Current	Continuous	T_C = 25°C	−18	A
		Continuous (Note 1a)	T_A = 25°C	−12	
		Pulsed		−50	
E_{AS}	Single Pulse Avalanche Energy			37	mJ
P_D	Power Dissipation		T_C = 25°C	41	W
	Power Dissipation (Note 1a)		T_A = 25°C	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			−55 to + 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a. 53°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 125°C/W when mounted on a minimum pad of 2 oz copper

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = −250 μA, V_{GS} = 0 V	−20	−	−	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = −250 μA, referenced to 25°C	−	−12	−	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −16 V, V_{GS} = 0 V	−	−	−1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8 V, V_{DS} = 0 V	−	−	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = −250 μA	−0.4	−0.5	−1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = −250 μA, referenced to 25°C	−	3	−	mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = −4.5 V, I_D = −12 A	−	6.4	8.0	mΩ
		V_{GS} = −2.5 V, I_D = −10 A	−	7.6	9.8	
		V_{GS} = −1.8 V, I_D = −9.3 A	−	9.2	13	
		V_{GS} = −1.5 V, I_D = −8.3 A	−	11	17	
		V_{GS} = −4.5 V, I_D = −12 A, T_J = 125°C	−	8.5	12	
g_{FS}	Forward Transconductance	V_{DS} = −5 V, I_D = −12 A	−	75	−	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 MHz	−	5910	7860	pF
C_{oss}	Output Capacitance		−	840	1120	pF
C_{rss}	Reverse Transfer Capacitance		−	738	1110	pF
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = −10 V, I_D = −12 A, V_{GS} = −4.5 V, R_{GEN} = 6 Ω	−	15	27	ns
t_r	Rise Time		−	34	55	ns
$t_{d(off)}$	Turn−Off Delay Time		−	338	540	ns
t_f	Fall Time		−	170	272	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to −4.5 V, V_{DD} = −10 V, I_D = −12 A	−	83	116	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to −2.5 V, V_{DD} = −10 V, I_D = −12 A	−	50	70	nC
Q_{gs}	Gate to Source Charge	V_{DD} = −10 V, I_D = −12 A	−	6.3	−	nC
Q_{gd}	Gate to Drain “Miller” Charge		−	20.4	−	nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = −12 A (Note 2)	−	−0.70	−1.3	V
		V_{GS} = 0 V, I_S = −2 A (Note 2)	−	−0.53	−1.2	
t_{rr}	Reverse Recovery Time	I_F = −12 A, di/dt = 100 A/μs	−	35	57	ns
Q_{rr}	Reverse Recovery Charge		−	20	32	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting T_J = 25°C; P−Ch: L = 3 mH, I_{AS} = −5 A, VDD = −20 V, V_{GS} = −4.5 V.
4. No gate overvoltage rating is implied.

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TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

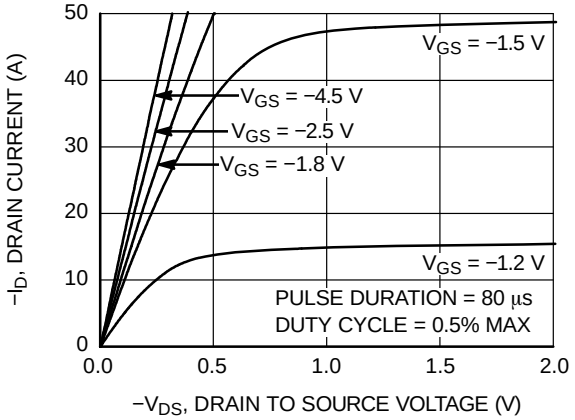


Figure 1. On Region Characteristics

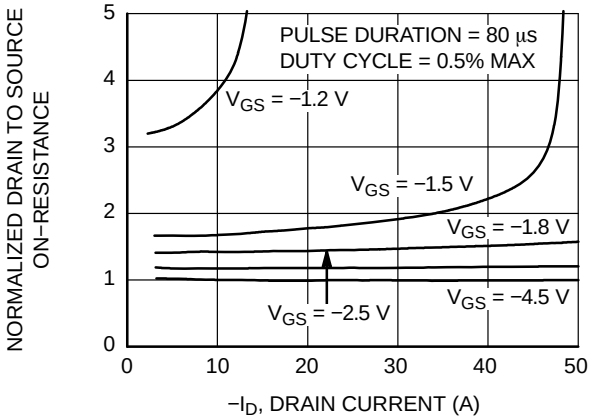


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

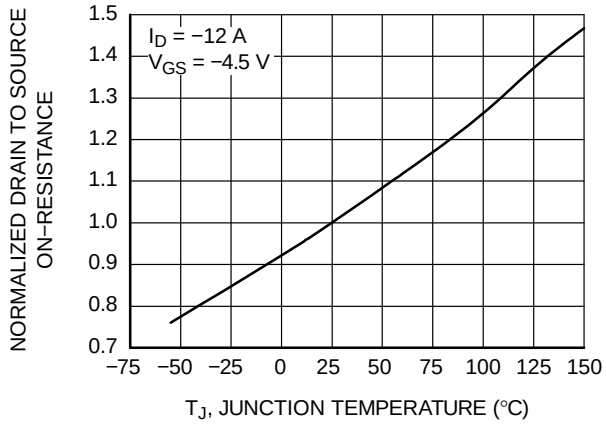


Figure 3. Normalized On Resistance vs. Junction Temperature

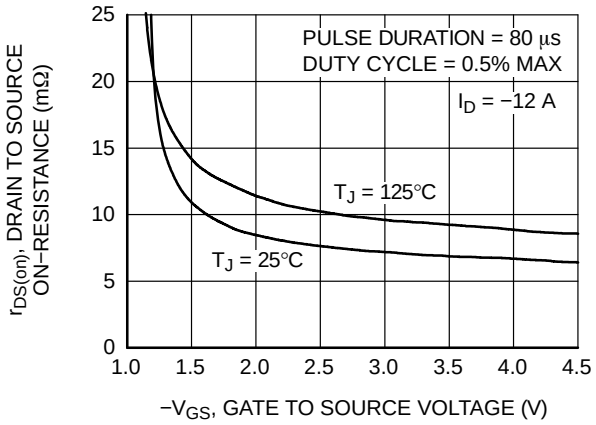


Figure 4. On−Resistance vs. Gate to Source Voltage

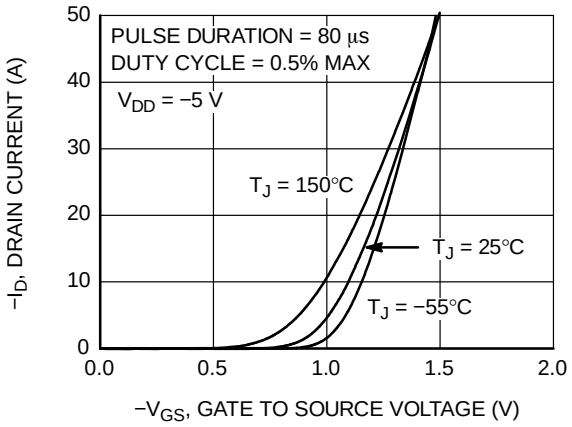


Figure 5. Transfer Characteristics

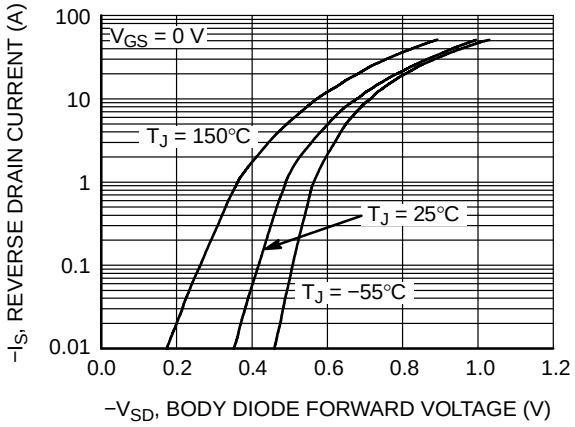


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

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TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

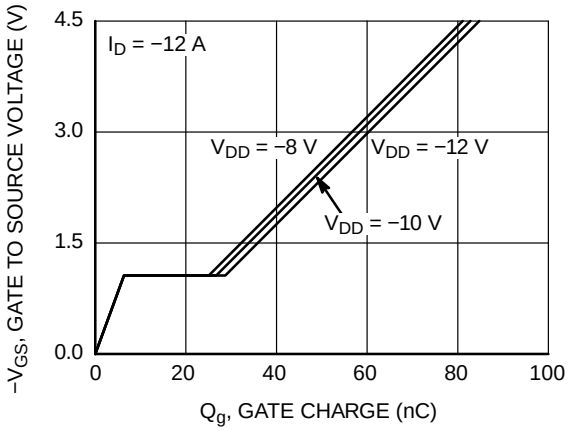


Figure 7. Gate Charge Characteristics

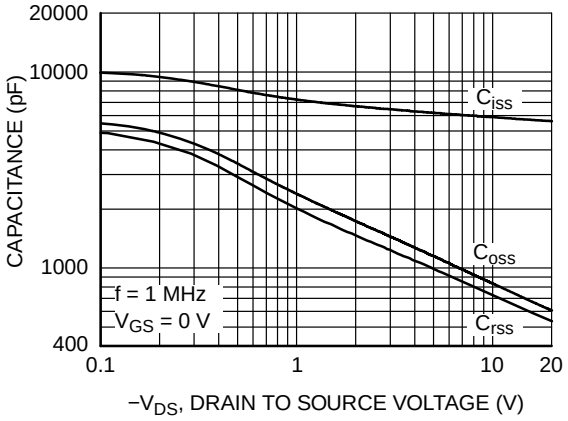


Figure 8. Capacitance vs. Drain to Source Voltage

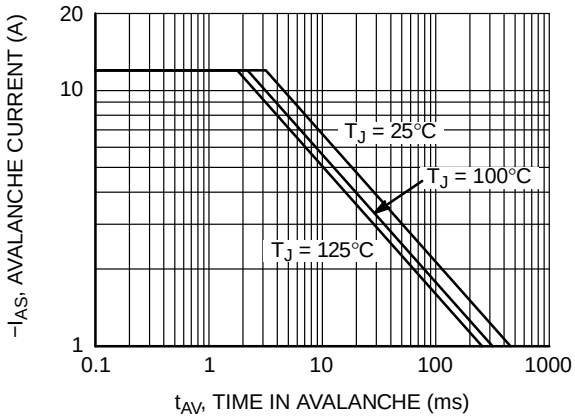


Figure 9. Unclamped Inductive Switching Capability

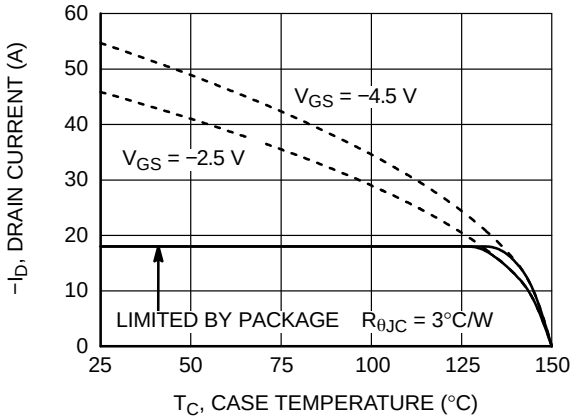


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

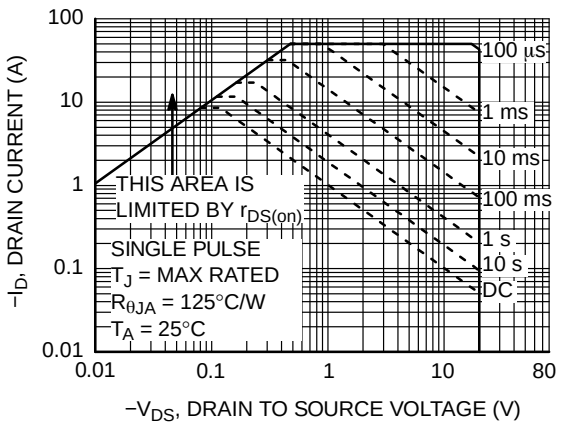


Figure 11. Forward Bias Safe Operating Area

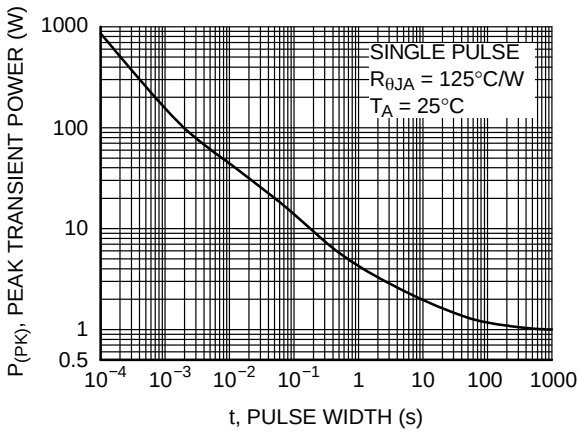


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

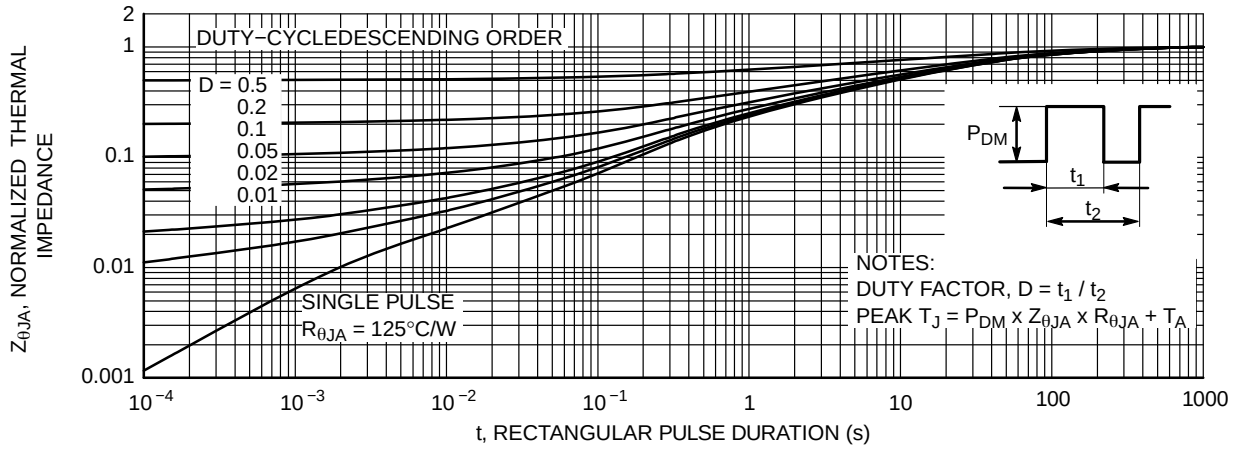


Figure 13. Transient Thermal Response Curve

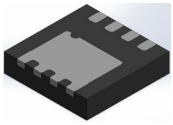
PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping†
FDMC510P	FDMC510P	WDFN8 3.3x3.3, 0.65P (MLP 3.3x3.3) (Pb−Free and Halide Free)	13”	12 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

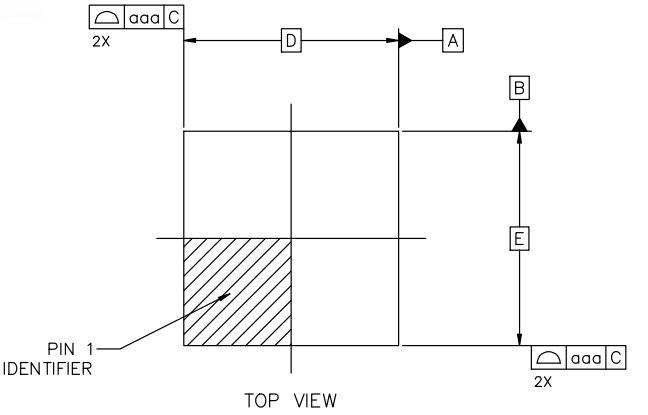
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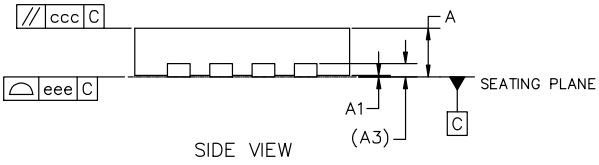


WDFN−8 3.30x3.30x0.75, 0.65P
CASE 511DH
ISSUE A

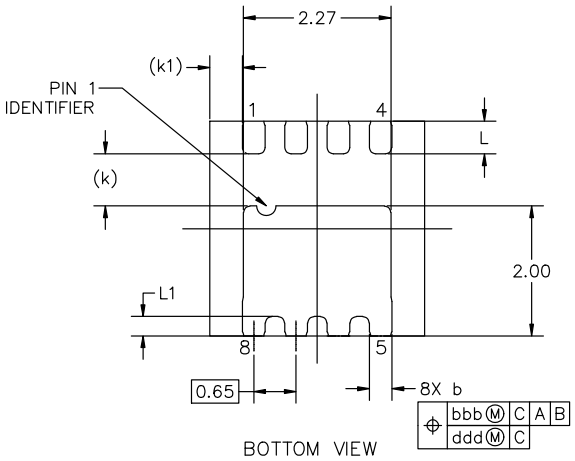
DATE 04 DEC 2025



TOP VIEW



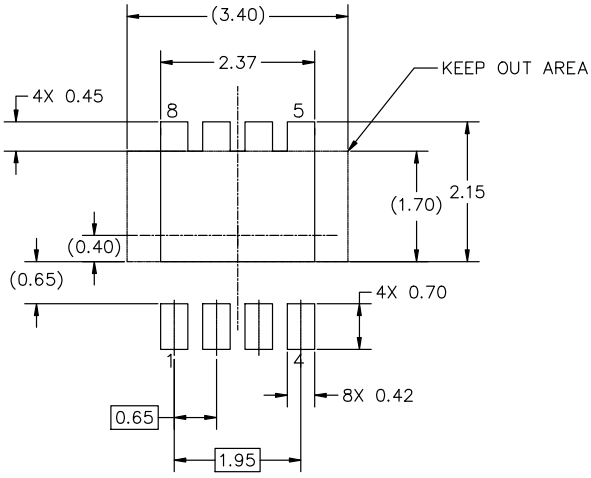
SIDE VIEW



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.025	0.05
A3		0.20 REF	
b	0.30	0.35	0.40
D		3.30 BSC	
D2	2.22	2.27	2.32
E		3.30 BSC	
E2	1.95	2.00	2.05
e		0.65 BSC	
k		0.80 REF	
k1		0.50 REF	
L	0.45	0.50	0.55
L1	0.25	0.30	0.35
TOLERANCE FORM & POSITION			
aaa		0.05	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques reference manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WDFN−8 3.30x3.30x0.75, 0.65P**	**PAGE 1 OF 1**

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