

NCS7101, NCV7101

Operational Amplifier, Rail-to-Rail, 1.8 V

The NCS7101 operational amplifier provides rail-to-rail operation on both the input and output. The output can swing within 50 mV of each rail. This rail-to-rail operation enables the user to make full use of the entire supply voltage range available. It is designed to work at very low supply voltages (1.8 V and ground), yet can operate with a supply of up to 10 V and ground. The NCS7101 is available in the space saving SOT-23-5 package with two industry standard pinouts.

Features

- Low Voltage, Single Supply Operation (1.8 V and Ground to 10 V and Ground)
- 1.0 pA Input Bias Current
- Unity Gain Bandwidth of 1.0 MHz at 5.0 V, 0.9 MHz at 1.8 V
- Output Voltage Swings Within 50 mV of Both Rails @ 1.8 V
- No Phase Reversal on the Output for Over-Driven Input Signals
- Input Offset Trimmed to 1.0 mV
- Low Supply Current ($I_D = 1.0$ mA)
- Works Down to Two Discharged NiCd Battery Cells
- ESD Protected Inputs Up to 2.0 kV
- These Devices are Pb-Free and are RoHS Compliant
- AEC-Q100 Qualified and PPAP Capable
- *NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements

Typical Applications

- Dual NiCd/NiMH Cell Powered Systems
- Portable Communication Devices
- Low Voltage Active Filters
- Power Supply Monitor and Control
- Interface to DSP

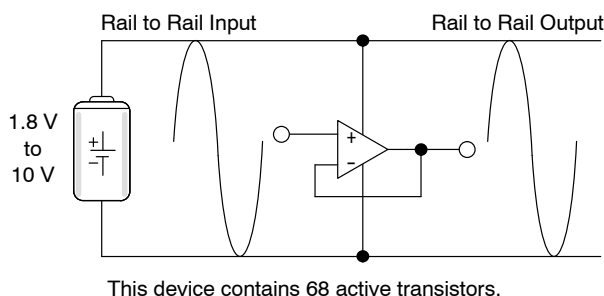


Figure 1. Typical Application



ON Semiconductor®

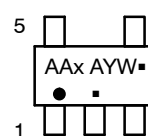
<http://onsemi.com>

LOW VOLTAGE RAIL-TO-RAIL OPERATIONAL AMPLIFIER



CASE 483
SOT-23-5
SN SUFFIX

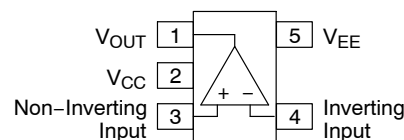
MARKING DIAGRAM



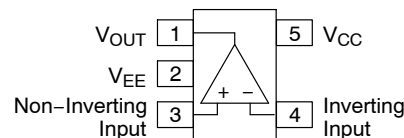
x = C for SN1
D for SN2
A = Assembly Location
Y = Year
W = Work Week
■ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



Style 1 Pin Out (SN1T1)



Style 2 Pin Out (SN2T1)

ORDERING INFORMATION

Device	Package	Shipping†
NCS7101SN1T1G	SOT-23-5 (Pb-Free)	3000 Tape & Reel (7 inch Reel)
NCV7101SN1T1G*		
NCS7101SN2T1G		
NCV7101SN2T1G*		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCS7101, NCV7101

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	10	V
Input Differential Voltage Range (Note 1)	V_{IDR}	$V_{EE} - 300 \text{ mV}$ to 10 V	V
Input Common Mode Voltage Range (Note 1)	V_{ICR}	$V_{EE} - 300 \text{ mV}$ to 10 V	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Junction Temperature	T_J	150	°C
Power Dissipation and Thermal Characteristics – SOT-23-5 Package			
Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	220	°C/W
Power Dissipation @ $T_A = 70^\circ\text{C}$	P_D	364	mW
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Ambient Temperature Range	T_A	-40 to +85 -40 to +125	°C
ESD Protection at any Pin Human Body Model (Note 3)	V_{ESD}	2000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Either or both inputs should not exceed the range of $V_{EE} - 300 \text{ mV}$ to $V_{EE} + 10 \text{ V}$.
2. Maximum package power dissipation limits must be observed to ensure that the maximum junction temperature is not exceeded.
 $T_J = T_A + (P_D R_{\theta JA})$
3. ESD data available upon request.

NCS7101, NCV7101

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = 2.5\text{ V}$, $V_{EE} = -2.5\text{ V}$, $V_{CM} = V_O = 0$, R_L to GND, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage $V_{CC} = 0.9\text{ V}$, $V_{EE} = -0.9\text{ V}$ $T_A = 25^\circ\text{C}$ $T_A = T_{Low}$ to T_{High} $V_{CC} = 2.5\text{ V}$, $V_{EE} = -2.5\text{ V}$ $T_A = 25^\circ\text{C}$ $T_A = T_{Low}$ to T_{High} $V_{CC} = 5.0\text{ V}$, $V_{EE} = -5.0\text{ V}$ $T_A = 25^\circ\text{C}$ $T_A = T_{Low}$ to T_{High}	V_{IO}	-7.0 -9.0 -7.0 -9.0 -7.0 -9.0	0.6 - 0.6 - 0.6 -	7.0 9.0 7.0 9.0 7.0 9.0	mV
Input Offset Voltage Temperature Coefficient ($R_S = 50$) $T_A = -40^\circ\text{C}$ to 125°C	$\Delta V_{IO}/\Delta T$	-	8.0	-	$\mu\text{V}/^\circ\text{C}$
Input Bias Current ($V_{CC} = 1.8\text{ V}$ to 10 V)	$ I_{IB} $	-	1.0	-	pA
Common Mode Input Voltage Range	V_{ICR}	V_{EE}	-	V_{CC}	V
Large Signal Voltage Gain $V_{CC} = 5.0\text{ V}$, $V_{EE} = -5.0\text{ V}$ $R_L = 10\text{ k}\Omega$ $R_L = 2.0\text{ k}\Omega$	A_{VOL}	16 16	50 30	- -	kV/V
Output Voltage Swing, High ($V_{ID} = \pm 0.2\text{ V}$) $V_{CC} = 0.9\text{ V}$, $V_{EE} = -0.9\text{ V}$ ($T_A = 25^\circ\text{C}$) $R_L = 10\text{ k}$ $R_L = 2.0\text{ k}$ $T_A = T_{Low}$ to T_{High} $R_L = 10\text{ k}$ $R_L = 2.0\text{ k}$ $V_{CC} = 2.5\text{ V}$, $V_{EE} = -2.5\text{ V}$ ($T_A = 25^\circ\text{C}$) $R_L = 600$ $R_L = 2.0\text{ k}$ $T_A = T_{Low}$ to T_{High} $R_L = 600$ $R_L = 2.0\text{ k}$ $V_{CC} = 5.0\text{ V}$, $V_{EE} = -5.0\text{ V}$ ($T_A = 25^\circ\text{C}$) $R_L = 600$ $R_L = 2.0\text{ k}$ $T_A = T_{Low}$ to T_{High} $R_L = 600$ $R_L = 2.0\text{ k}$	V_{OH}	0.85 0.80 0.85 0.79 2.10 2.35 2.00 2.40 4.40 4.80 4.40 4.80	0.88 0.82 - - 2.21 2.44 - - 4.60 4.88 - -	- - - - - - - - - - - -	V
Output Voltage Swing, Low ($V_{ID} = \pm 0.2\text{ V}$) $V_{CC} = 0.9\text{ V}$, $V_{EE} = -0.9\text{ V}$ ($T_A = 25^\circ\text{C}$) $R_L = 10\text{ k}$ $R_L = 2.0\text{ k}$ $T_A = T_{Low}$ to T_{High} $R_L = 10\text{ k}$ $R_L = 2.0\text{ k}$ $V_{CC} = 2.5\text{ V}$, $V_{EE} = -2.5\text{ V}$ ($T_A = 25^\circ\text{C}$) $R_L = 600$ $R_L = 2.0\text{ k}$ $T_A = T_{Low}$ to T_{High} $R_L = 600$ $R_L = 2.0\text{ k}$ $V_{CC} = 5.0\text{ V}$, $V_{EE} = -5.0\text{ V}$ ($T_A = 25^\circ\text{C}$) $R_L = 600$ $R_L = 2.0\text{ k}$ $T_A = T_{Low}$ to T_{High} $R_L = 600$ $R_L = 2.0\text{ k}$	V_{OL}	- - - - - - - - - - - -	-0.88 -0.82 - - -2.22 -2.38 - - -4.66 -4.88 - -	-0.85 -0.80 -0.85 -0.78 -2.10 -2.35 -2.00 -2.30 -4.40 -4.80 -4.35 -4.80	V
Common Mode Rejection Ratio $V_{in} = 0$ to 10 V $V_{in} = 0$ to 5.0 V	CMRR	65 60	- -	- -	dB

NCS7101, NCV7101

DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = 2.5\text{ V}$, $V_{EE} = -2.5\text{ V}$, $V_{CM} = V_O = 0$, R_L to GND, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply Rejection Ratio $V_{CC}/V_{EE} = 10\text{ V/Ground}$, $\Delta V_S = 2.5\text{ V}$	PSRR	65	–	–	dB
Output Short Circuit Current ($V_{in}\text{ Diff} = \pm 1.0\text{ V}$) $V_{CC} = +0.9\text{ V}$, $V_{EE} = -0.9\text{ V}$ Source Sink $V_{CC} = +2.5\text{ V}$, $V_{EE} = -2.5\text{ V}$ Source Sink $V_{CC} = 5.0\text{ V}$, $V_{EE} = -5.0\text{ V}$ Source Sink	I_{SC}	– – 20 –60 50 –140	3.0 –3.0 25 –25 72 –72	– – 60 –20 140 –50	mA
Power Supply Current ($V_O = 0\text{ V}$) $V_{CC} = +0.9\text{ V}$, $V_{EE} = -0.9\text{ V}$ $T_A = 25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to 85°C $T_A = -40^\circ\text{C}$ to 125°C $V_{CC} = +2.5\text{ V}$, $V_{EE} = -2.5\text{ V}$ $T_A = 25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to 85°C $T_A = -40^\circ\text{C}$ to 125°C $V_{CC} = 5.0\text{ V}$, $V_{EE} = -5.0\text{ V}$ $T_A = 25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to 85°C $T_A = -40^\circ\text{C}$ to 125°C	I_D	– – – – – – – – – – – –	0.97 – – 1.05 – – 1.13 – – – – –	1.20 1.30 1.60 1.30 1.40 1.70 1.40 1.50 1.80	mA

AC ELECTRICAL CHARACTERISTICS

($V_{CC} = 2.5\text{ V}$, $V_{EE} = -2.5\text{ V}$, $V_{CM} = V_O = 0$, R_L to GND, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate ($V_O = -2.0$ to 2.0 V , $R_L = 2.0\text{ k}\Omega$, $A_V = 1.0$)	SR	0.7	1.2	3.0	V/ μs
Gain Bandwidth Product ($V_{CC} = 10\text{ V}$)	GBW	0.5	1.0	3.0	MHz
Gain Margin ($R_L = 10\text{ k}$, $C_L = 5.0\text{ pF}$)	A_m	–	6.5	–	dB
Phase Margin ($R_L = 10\text{ k}$, $C_L = 5.0\text{ pF}$)	ϕ_m	–	60	–	Deg
Power Bandwidth ($V_O = 4.0\text{ Vpp}$, $R_L = 2.0\text{ k}\Omega$, $\text{THD} \leq 1.0\%$)	BW_P	–	130	–	kHz
Total Harmonic Distortion ($V_O = 4.0\text{ Vpp}$, $R_L = 2.0\text{ k}\Omega$, $A_V = 1.0$) $f = 1.0\text{ kHz}$ $f = 10\text{ kHz}$	THD	– –	0.02 0.2	– –	%
Differential Input Resistance ($V_{CM} = 0\text{ V}$)	R_{in}	–	> 1.0	–	tera Ω
Differential Input Capacitance ($V_{CM} = 0\text{ V}$)	C_{in}	–	2.0	–	pF
Equivalent Input Noise Voltage (Freq = 1.0 kHz)	e_n	–	140	–	nV/ $\sqrt{\text{Hz}}$

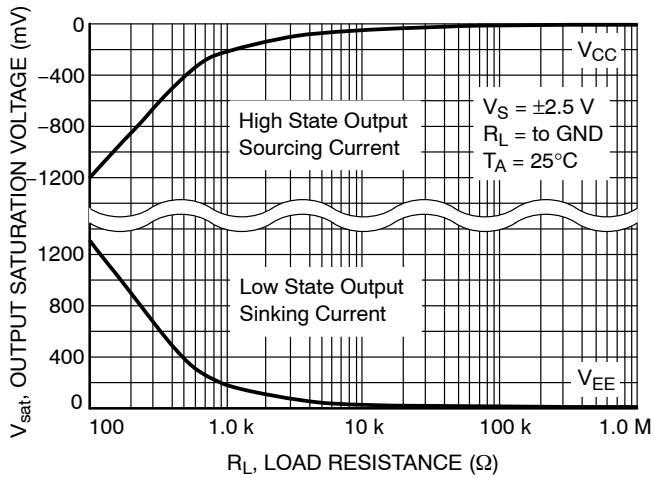


Figure 2. Output Saturation Voltage versus Load Resistance

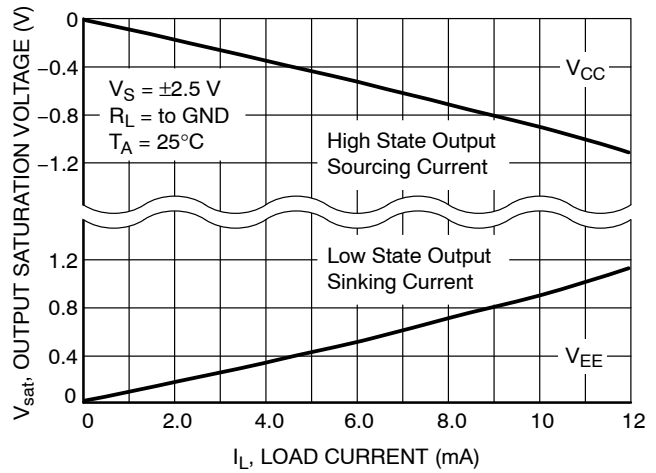


Figure 3. Output Saturation Voltage versus Load Current

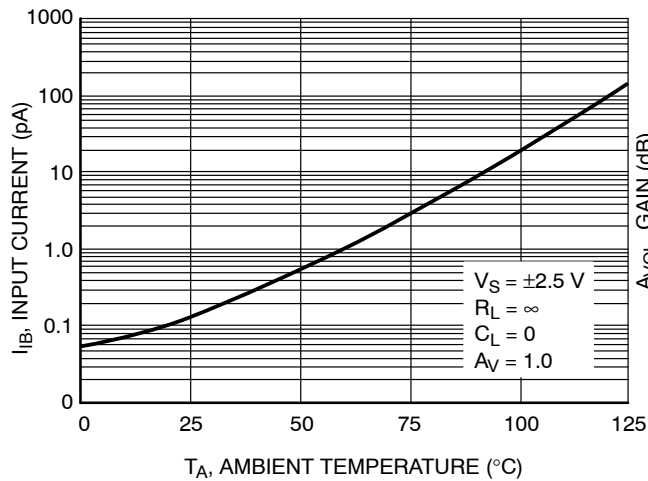


Figure 4. Input Bias Current versus Temperature

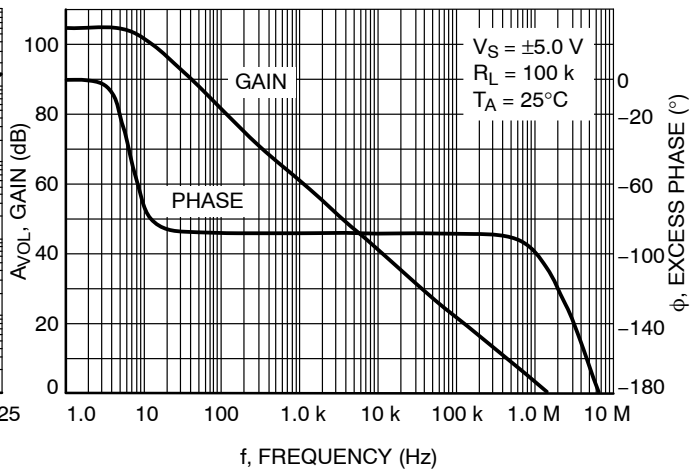


Figure 5. Gain and Phase versus Frequency

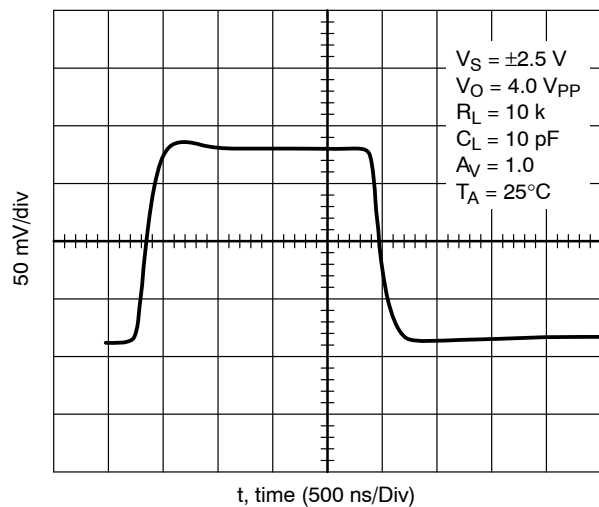


Figure 6. Transient Response

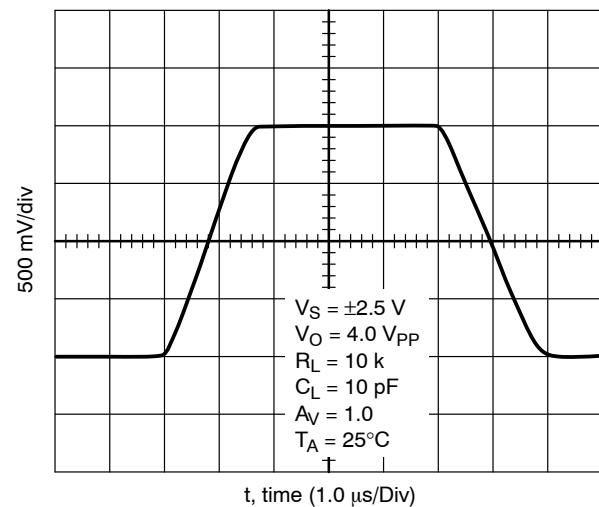


Figure 7. Slew Rate

NCS7101, NCV7101

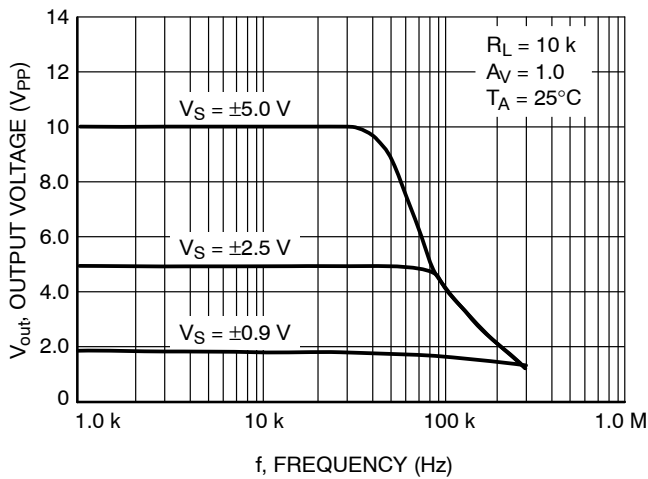


Figure 8. Output Voltage versus Frequency

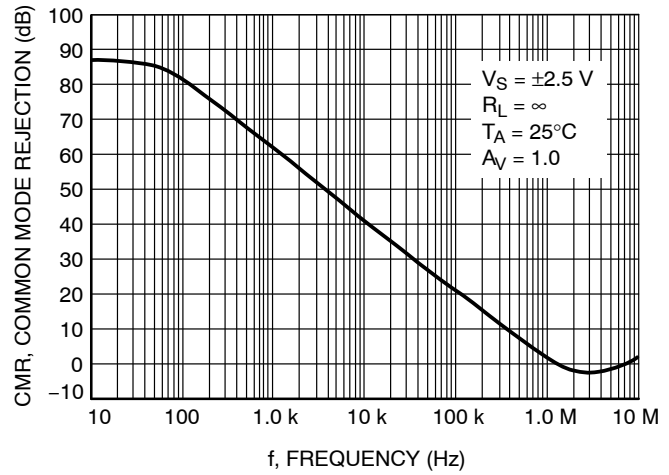


Figure 9. Common Mode Rejection versus Frequency

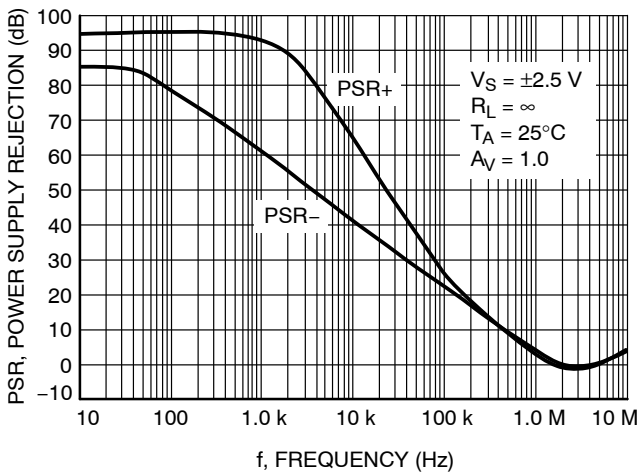


Figure 10. Power Supply Rejection versus Frequency

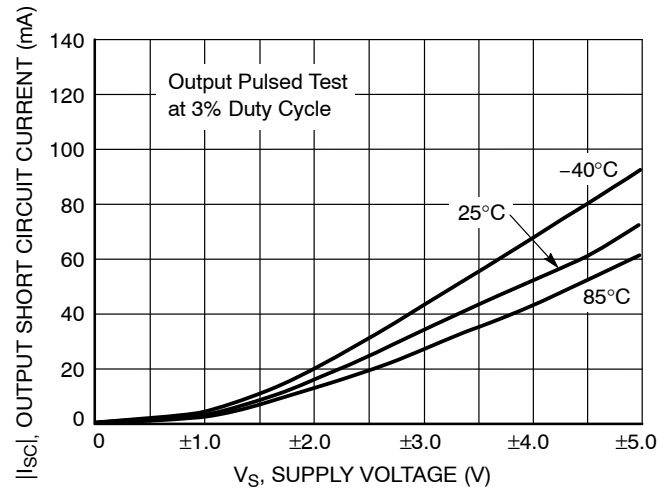


Figure 11. Output Short Circuit Sinking Current versus Supply Voltage

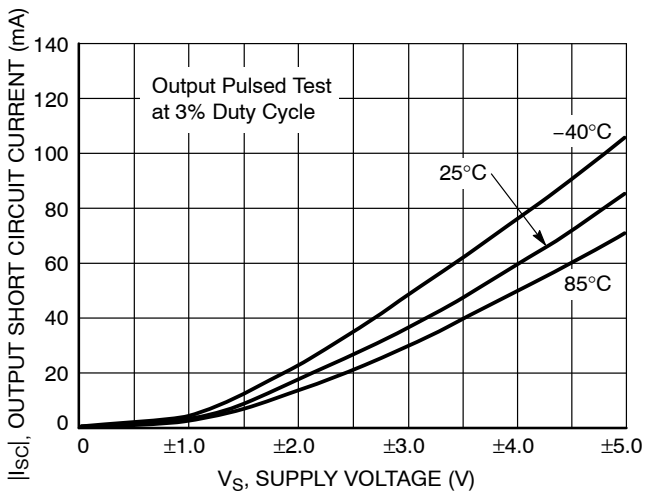


Figure 12. Output Short Circuit Sourcing Current versus Supply Voltage

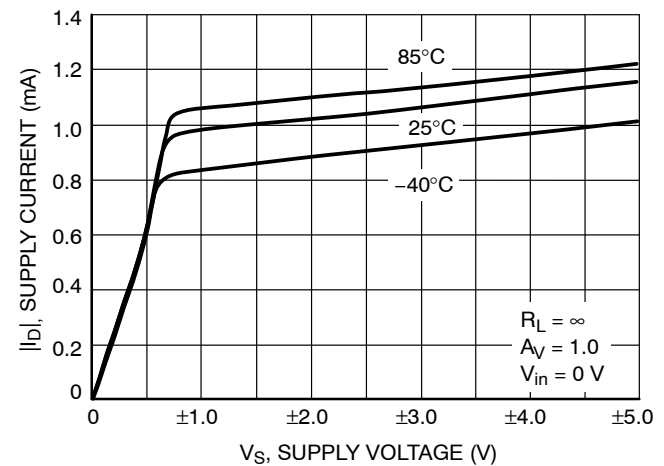


Figure 13. Supply Current versus Supply Voltage with No Load

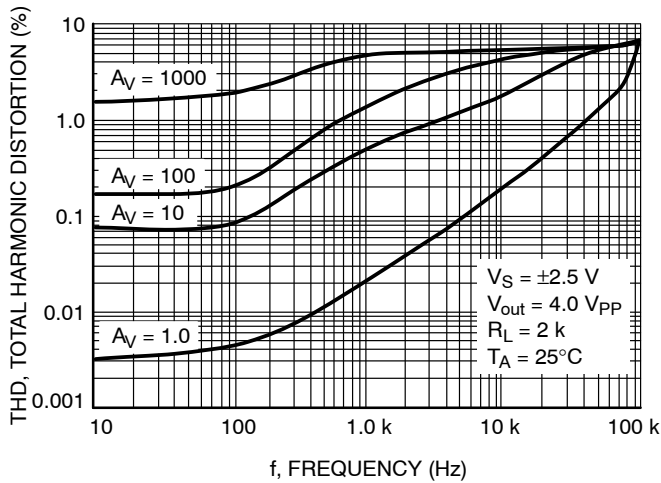


Figure 14. Total Harmonic Distortion versus Frequency with 5.0 V Supply

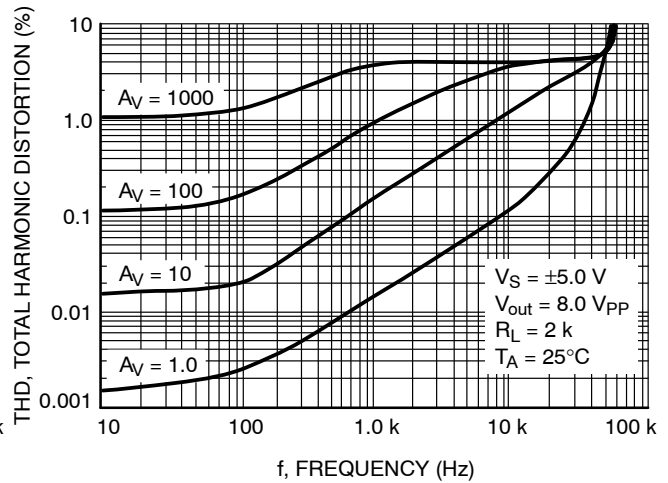


Figure 15. Total Harmonic Distortion versus Frequency with 10 V Supply

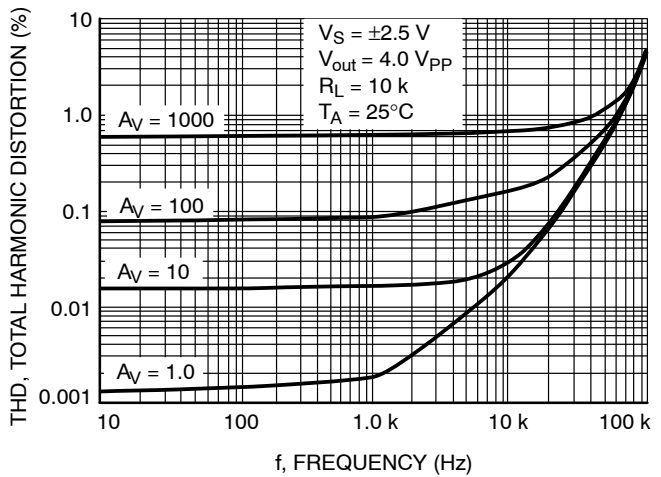


Figure 16. Total Harmonic Distortion versus Frequency with 5.0 V Supply

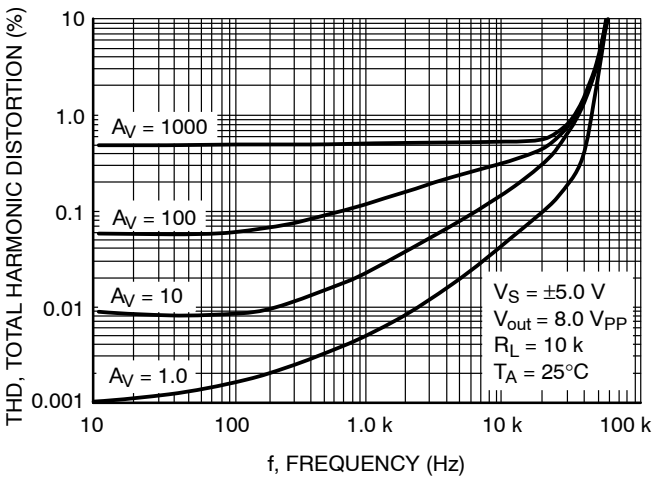


Figure 17. Total Harmonic Distortion versus Frequency with 10 V Supply

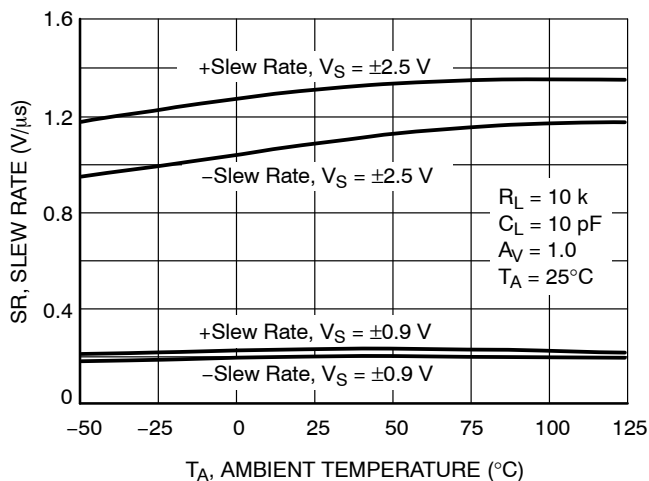


Figure 18. Slew Rate versus Temperature (Avg.)

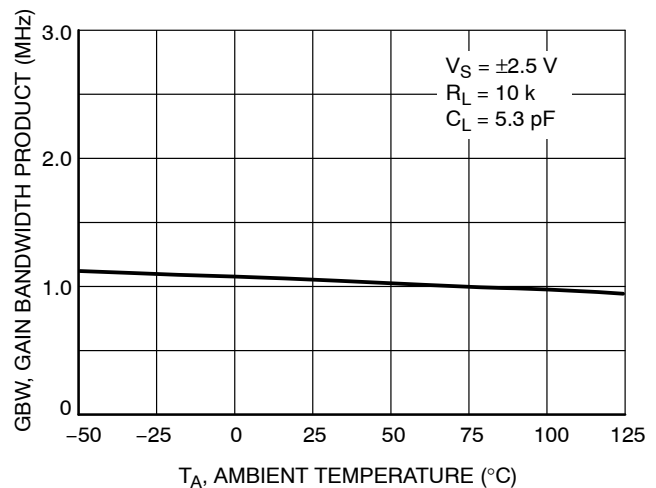


Figure 19. Gain Bandwidth Product versus Temperature

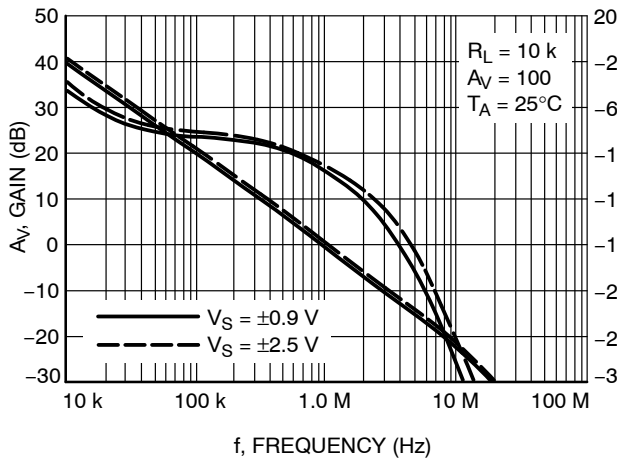


Figure 20. Voltage Gain and Phase versus Frequency

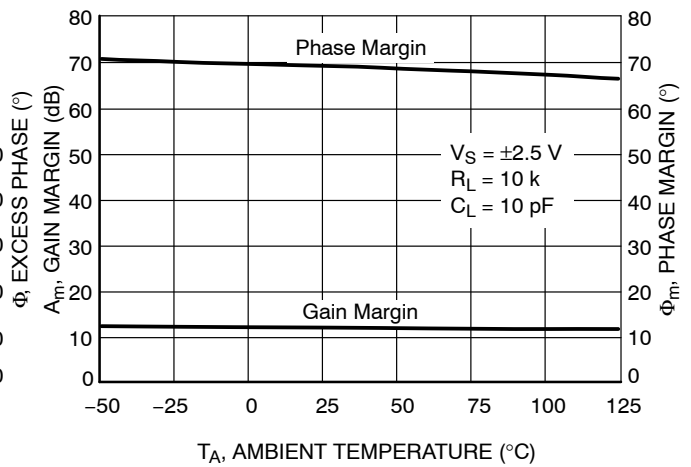


Figure 21. Gain and Phase Margin versus Temperature

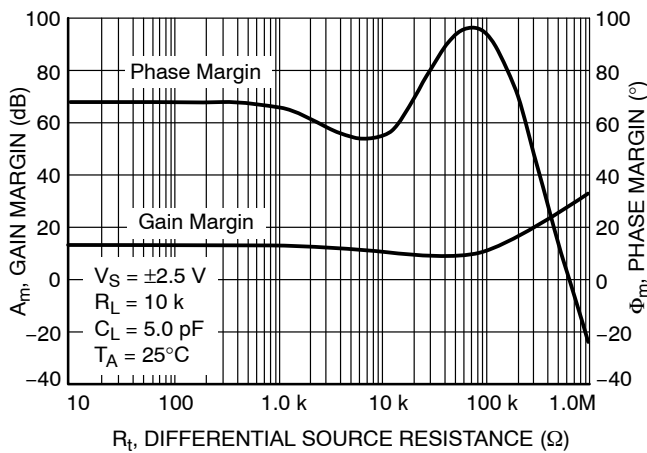


Figure 22. Gain and Phase Margin versus Differential Source Resistance

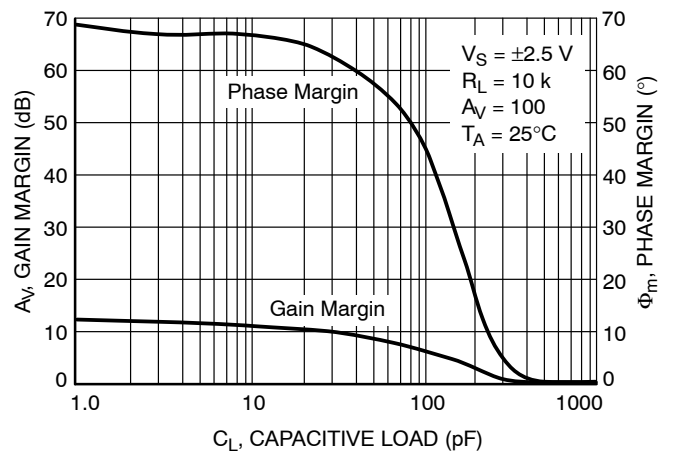


Figure 23. Gain and Phase Margin versus Output Load Capacitance

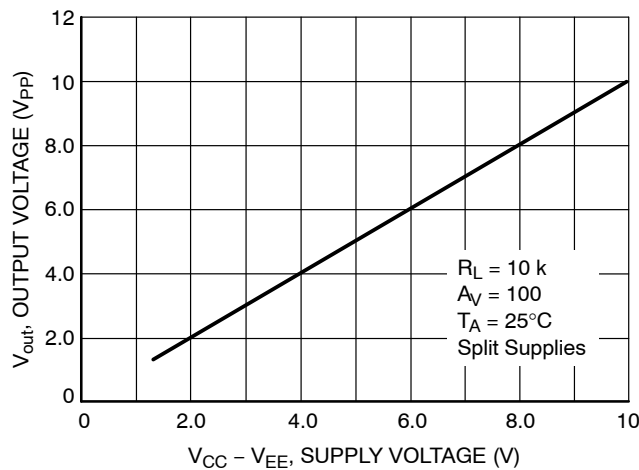


Figure 24. Output Voltage Swing versus Supply Voltage

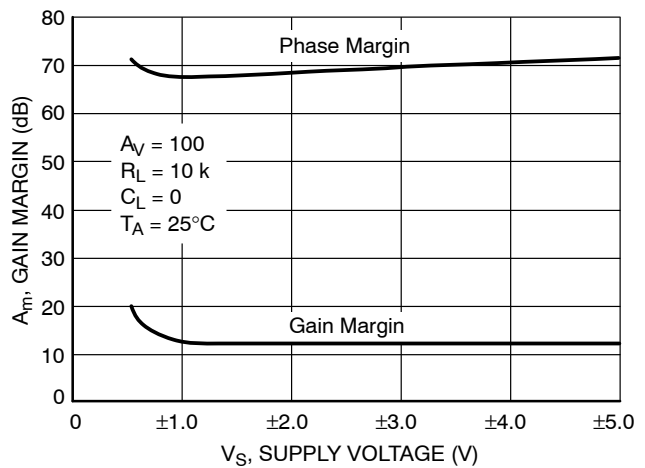


Figure 25. Gain and Phase Margin versus Supply Voltage

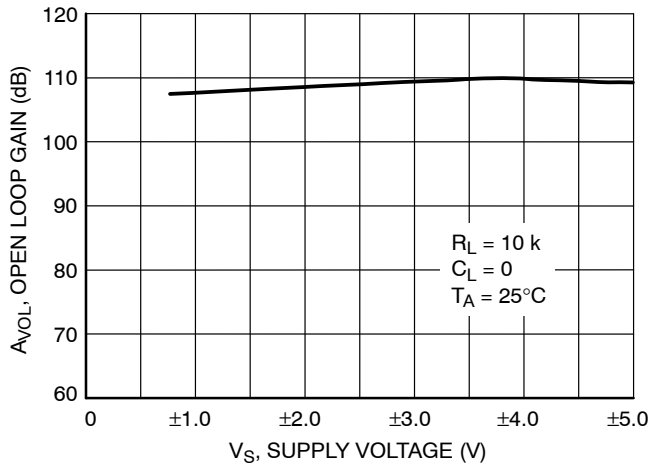


Figure 26. Open Loop Voltage Gain versus Supply Voltage (Split Supplies)

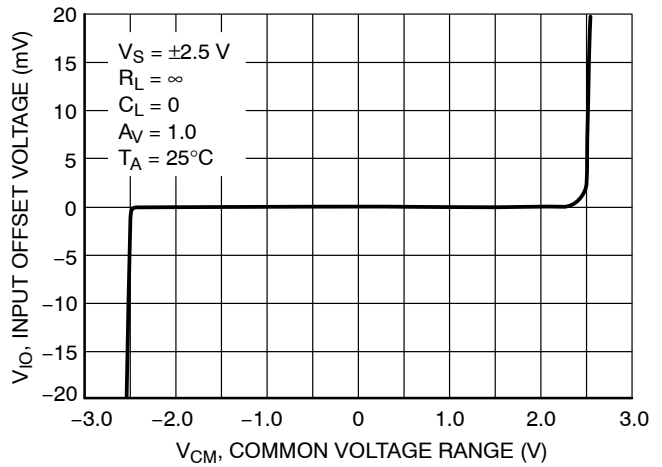


Figure 27. Input Offset Voltage versus Common Mode Input Voltage Range, $V_S = \pm 2.5\text{ V}$

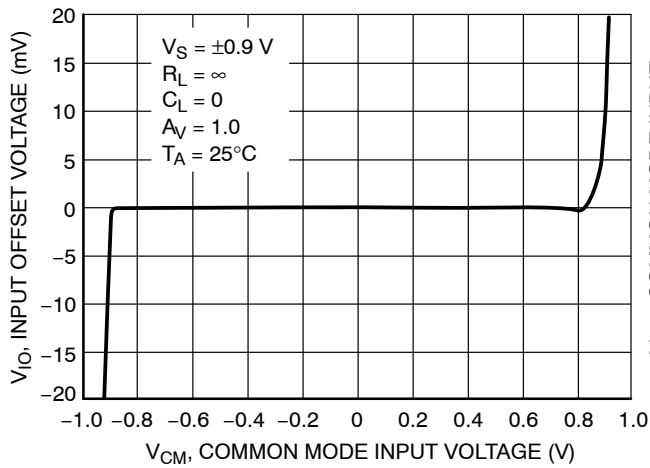


Figure 28. Input Offset Voltage versus Common Mode Input Voltage Range, $V_S = \pm 0.9\text{ V}$

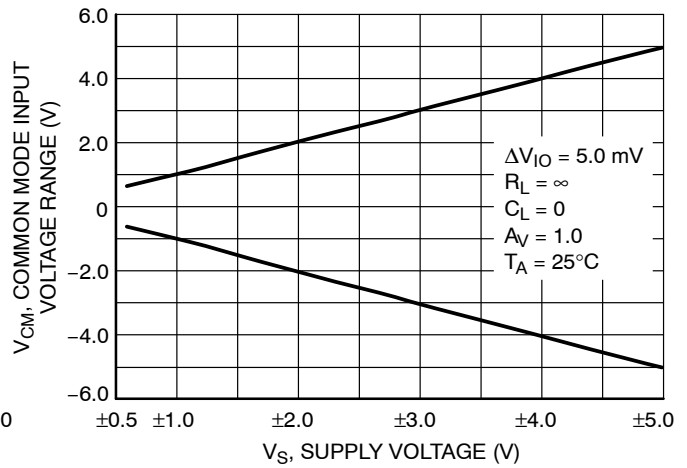


Figure 29. Common-Mode Input Voltage Range versus Power Supply Voltage

APPLICATION INFORMATION AND OPERATING DESCRIPTION

GENERAL INFORMATION

The NCS7101 is a rail-to-rail input, rail-to-rail output operational amplifier that features guaranteed 1.8 volt operation. This feature is achieved with the use of a modified analog CMOS process that allows the implementation of depletion MOSFET devices. The amplifier has a 1.0 MHz gain bandwidth product, 1.2 V/ μ s slew rate and is operational over a power supply range less than 1.8 V to as high as 10 V.

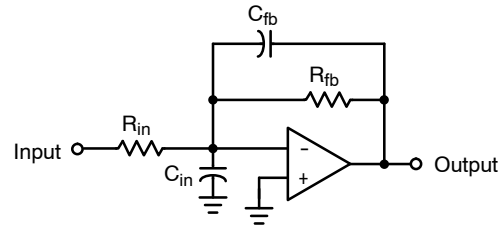
Inputs

The input topology of this device series is unconventional when compared to most low voltage operational amplifiers. It consists of an N-channel depletion mode differential transistor pair that drives a folded cascode stage and current mirror. This configuration extends the input common mode voltage range to encompass the V_{EE} and V_{CC} power supply rails, even when powered from a combined total of less than 1.8 volts. Figures 27 and 28 show the input common mode voltage range versus power supply voltage.

The differential input stage is laser trimmed in order to minimize offset voltage. The N-channel depletion mode MOSFET input stage exhibits an extremely low input bias current of less than 40 pA. The input bias current versus temperature is shown in Figure 4. Either one or both inputs can be biased as low as V_{EE} minus 300 mV to as high as 10 V without causing damage to the device. If the input common mode voltage range is exceeded, the output will not display a phase reversal but it may latch in the appropriate high or low state. The device can then be reset by removing and reapplying power. If the maximum input positive or negative voltage ratings are to be exceeded, a series resistor must be used to limit the input current to less than 2.0 mA.

The ultra low input bias current of the NCS7101 allows the use of extremely high value source and feedback resistor without reducing the amplifier's gain accuracy. These high value resistors, in conjunction with the device input and printed circuit board parasitic capacitances C_{in} , will add an additional pole to the single pole amplifier shown in Figure 30. If low enough in frequency, this additional pole can reduce the phase margin and significantly increase the output settling time. The effects of C_{in} can be canceled by placing a zero into the feedback loop. This is accomplished with the addition of capacitor C_{fb} . An approximate value for C_{fb} can be calculated by:

$$C_{fb} = \frac{R_{in} \times C_{in}}{R_{fb}}$$



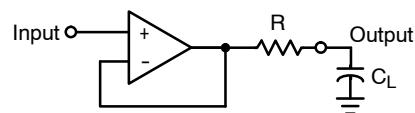
C_{in} = Input and printed circuit board capacitance

Figure 30. Input Capacitance Pole Cancellation

Output

The output stage consists of complementary P and N channel devices connected to provide rail-to-rail output drive. With a 2.0 k load, the output can swing within 100 mV of either rail. It is also capable of supplying over 95 mA when powered from 10 V and 3.0 mA when powered from 1.8 V.

When connected as a unity gain follower, the NCS7101 can directly drive capacitive loads in excess of 390 pF at room temperature without oscillating but with significantly reduced phase margin. The unity gain follower configuration exhibits the highest bandwidth and is most prone to oscillations when driving a high value capacitive load. The capacitive load in combination with the amplifier's output impedance, creates a phase lag that can result in an under-damped pulse response or a continuous oscillation. Figure 32 shows the effect of driving a large capacitive load in a voltage follower type of setup. When driving capacitive loads exceeding 390 pF, it is recommended to place a low value isolation resistor between the output of the op amp and the load, as shown in Figure 31. The series resistor isolates the capacitive load from the output and enhances the phase margin. Refer to Figure 33. Larger values of R will result in a cleaner output waveform but excessively large values will degrade the large signal rise and fall time and reduce the output's amplitude. Depending upon the capacitor characteristics, the isolation resistor value will typically be between 50 to 500 ohms. The output drive capability for resistive and capacitive loads is shown in Figures 2, 3, and 23.



Isolation resistor R = 50 to 500

Figure 31. Capacitance Load Isolation

Note that the lowest phase margin is observed at cold temperature and low supply voltage.

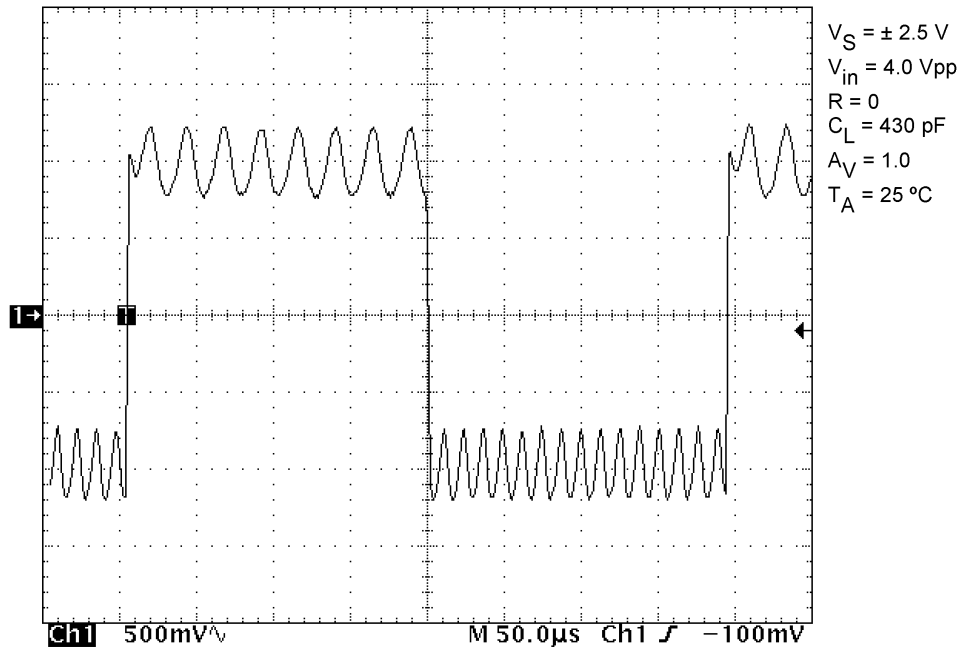


Figure 32. Small Signal Transient Response with Large Capacitive Load

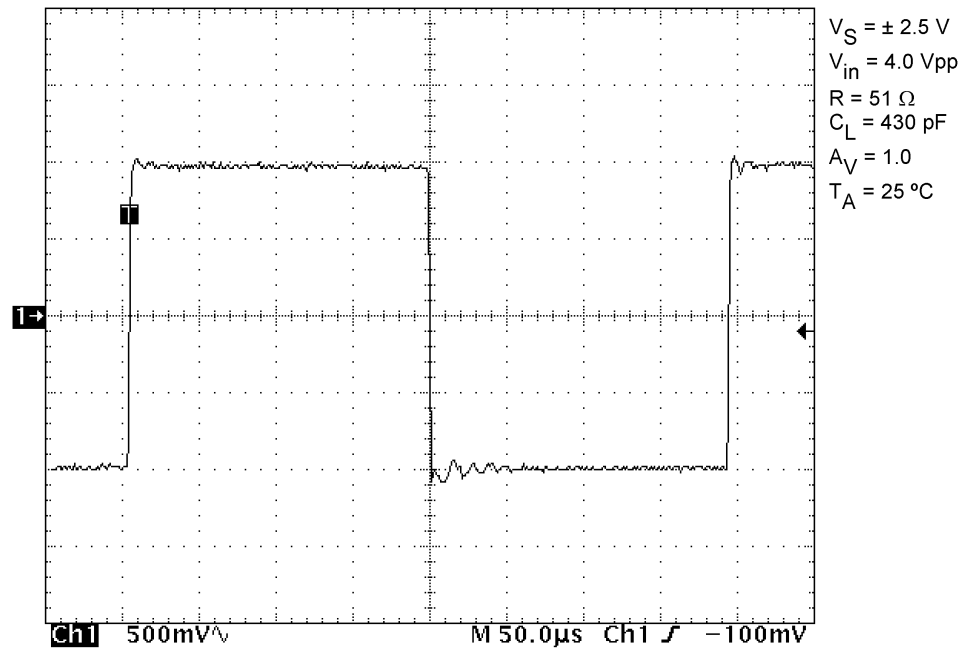


Figure 33. Small Signal Transient Response with Large Capacitive Load and Isolation Resistor.

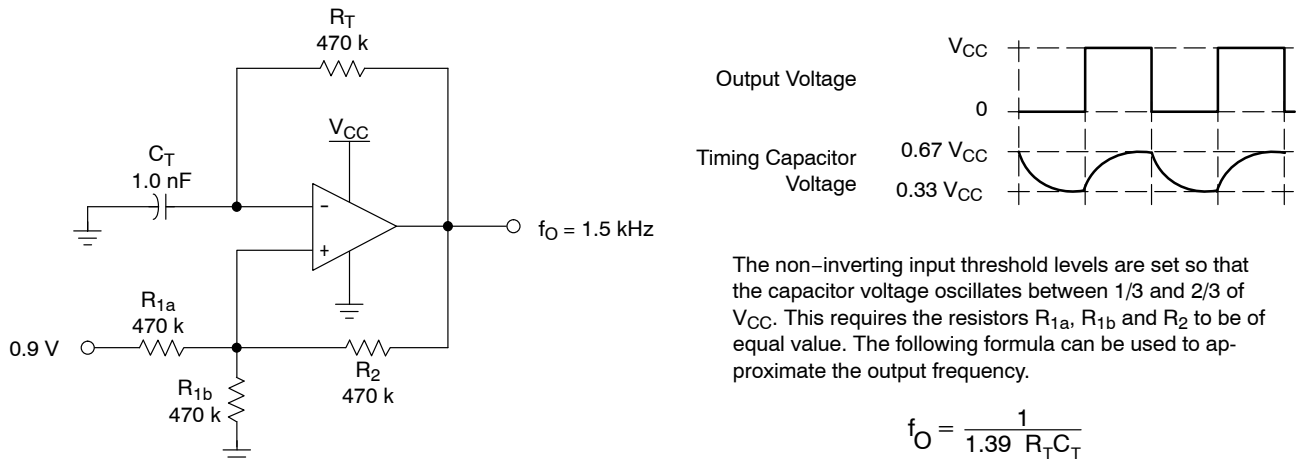


Figure 34. Square Wave Oscillator

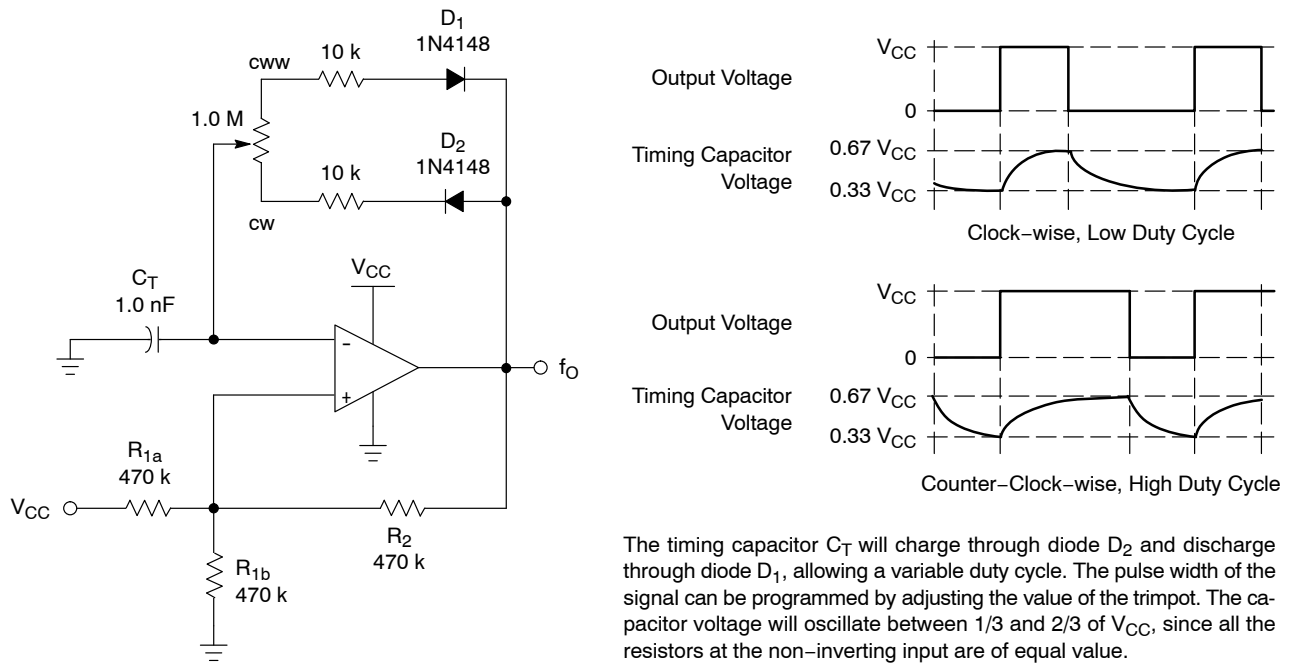


Figure 35. Variable Duty Cycle Pulse Generator

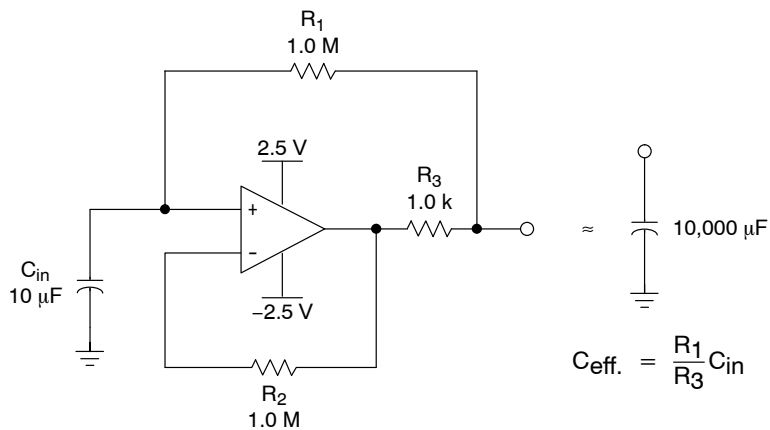


Figure 36. Positive Capacitance Multiplier

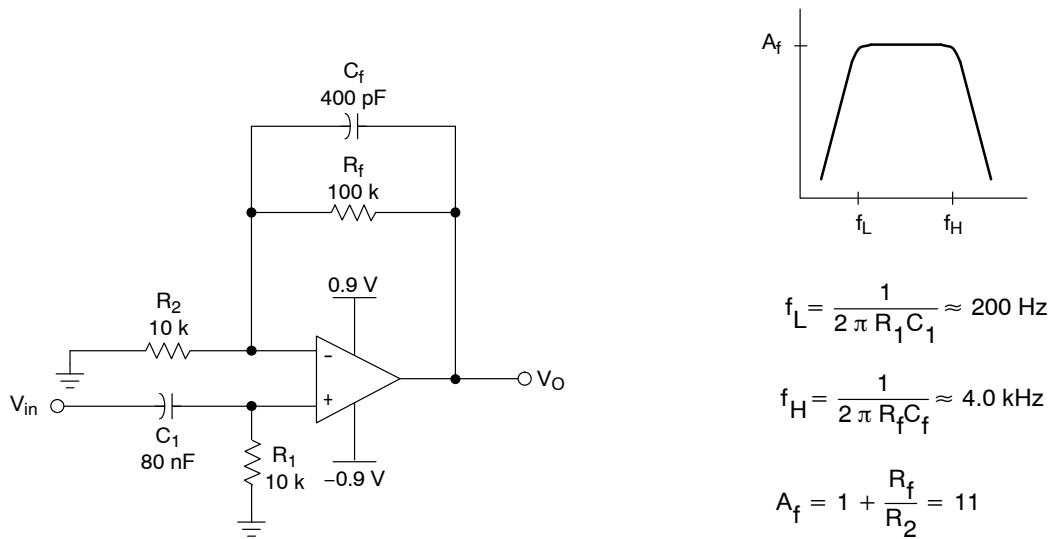


Figure 37. Voice Band Filter

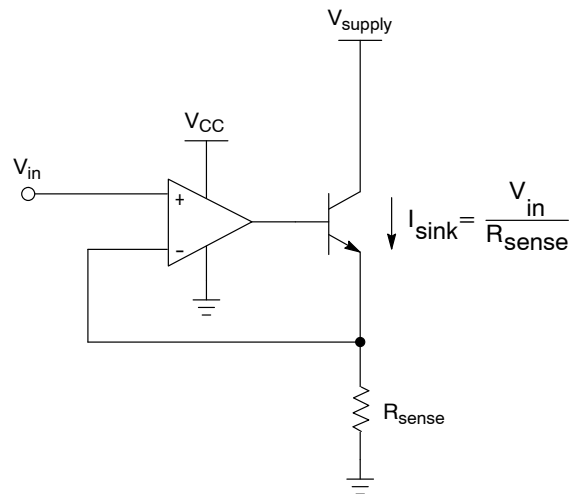
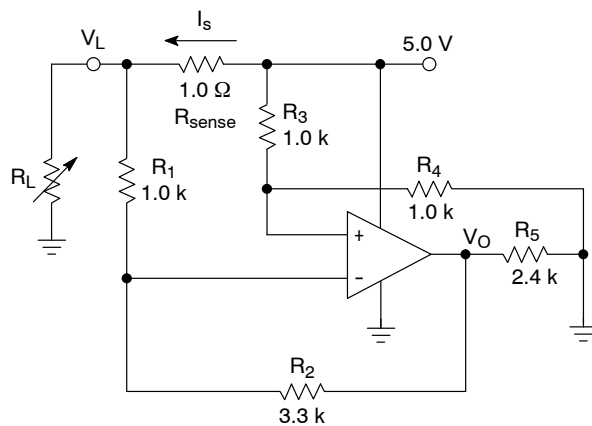


Figure 38. High Compliance Current Sink



I _s	V _O
1.00 A	67.93 mV
0.50 A	78.67 mV

For best performance, use low tolerance resistors.

Figure 39. High Side Current Sense

NCS7101, NCV7101

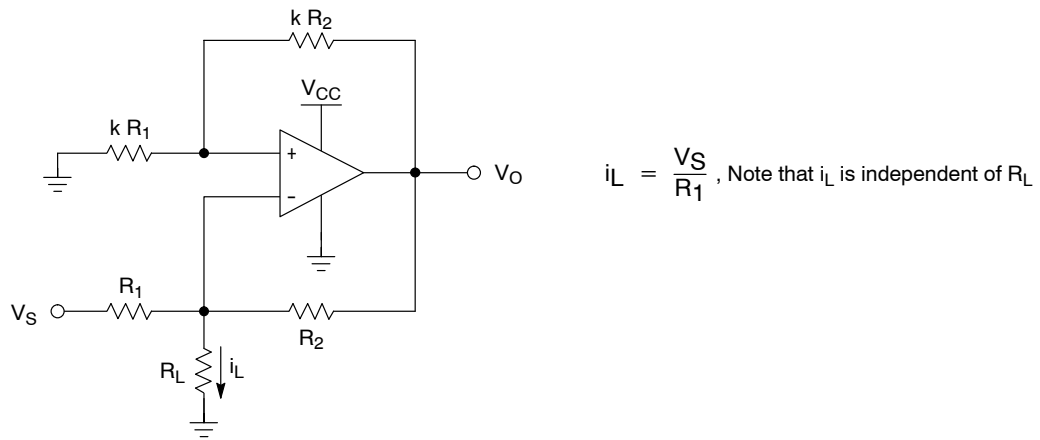


Figure 40. Current Source

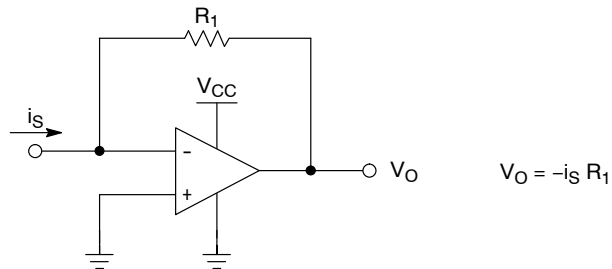


Figure 41. Current to Voltage Converter

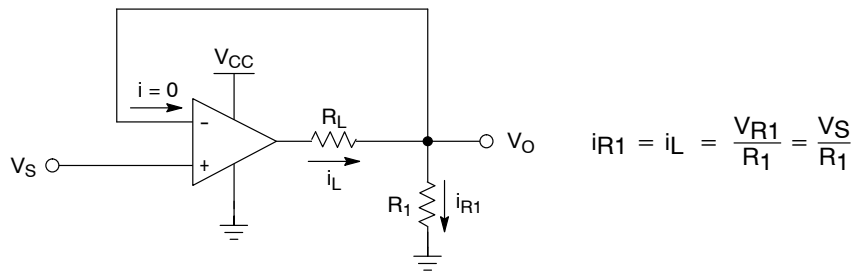
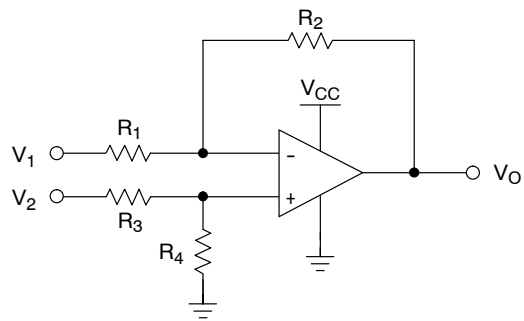


Figure 42. Voltage to Current Converter

NCS7101, NCV7101

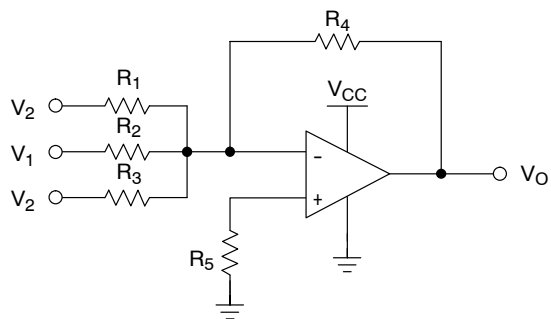


$$V_O = V_2 \left[\frac{R_4}{R_3 + R_4} \right] \left[\frac{R_2}{R_1} + 1 \right] - V_1 \frac{R_2}{R_1}$$

If $R_1 = R_3$, and $R_2 = R_4$, the equation simplifies to:

$$V_O = (V_2 - V_1) \frac{R_2}{R_1}$$

Figure 43. Differential Amplifier



$$V_O = -R_2 \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right]$$

To minimize input offset current take:
 $R_5 = R_1 // R_2 // R_3 // R_4$

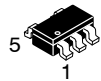
Figure 44. Summing Amplifier

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

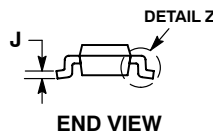
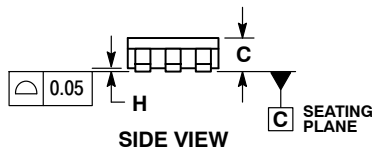
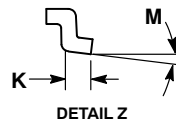
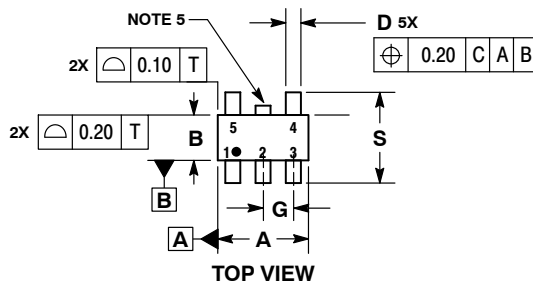
ON



SCALE 2:1

TSOP-5 CASE 483 ISSUE N

DATE 12 AUG 2020

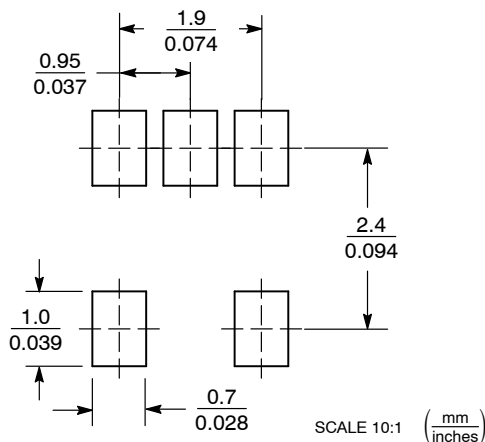


NOTES:

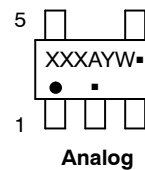
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

DIM	MILLIMETERS	
	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0°	10°
S	2.50	3.00

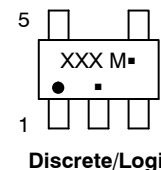
SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



Analog



Discrete/Logic

XXX = Specific Device Code
 A = Assembly Location
 Y = Year
 W = Work Week
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98ARB18753C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TSOP-5	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative

