

MOSFET

OptiMOS™3 Power-MOSFET, 60 V

Features

- Optimized technology for DC/DC converters
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Superior thermal resistance
- Dual sided cooling
- low parasitic inductance
- Low profile (<0.7mm)
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant

Product validation

Fully qualified according to JEDEC for Industrial Applications

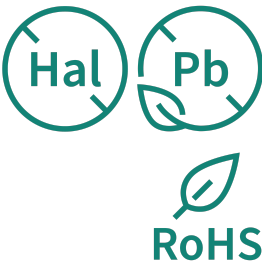
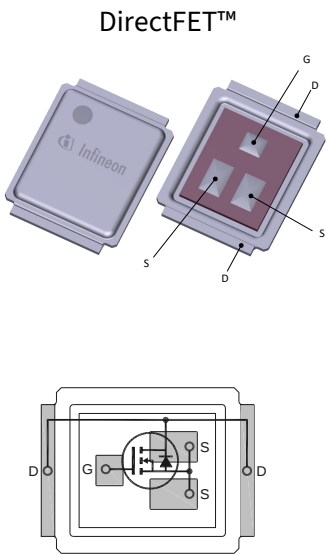


Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	2.8	mΩ
I_D	90	A

Type / Ordering code	Package	Marking	Related links
BSB028N06NN3 G	MG-WDSO5-5	0106	-



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1 Maximum ratings

at $T_j=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	90 85 22	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=58\text{ K/W}^{1)}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	360	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse	E_{AS}	-	-	590	mJ	$I_D=30\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	78 2.2	W -	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=58\text{ K/W}^{1)}$
Operating and storage temperature	T_j , T_{stg}	-40	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

¹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

²⁾ See figure 3 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	1.0	-	K/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	1.6	K/W	
Device on PCB, 6 cm ² cooling area ³⁾	R_{thJA}	-	-	58	K/W	

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2	3	4	V	$V_{DS}=V_{GS}$, $I_D=102\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	10 100	μA	$V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.2	2.8	m	$V_{GS}=10\text{ V}$, $I_D=30\text{ A}$
Gate resistance	R_G	-	0.5	-	Ω	-
Transconductance	g_{fs}	42	83	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=30\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance ⁴⁾	C_{iss}	-	8800	12000	pF	$V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$, $f=1\text{ MHz}$
Output capacitance ⁴⁾	C_{oss}	-	2100	2800	pF	
Reverse transfer capacitance ⁴⁾	C_{rss}	-	64	-	pF	
Turn-on delay time	$t_{d(on)}$	-	21	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=30\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	9	-	ns	
Turn-off delay time	$t_{d(off)}$	-	38	-	ns	
Fall time	t_f	-	6	-	ns	

⁴⁾ See figure 13 for more detailed information

Table 6 Gate charge characteristics ⁵⁾

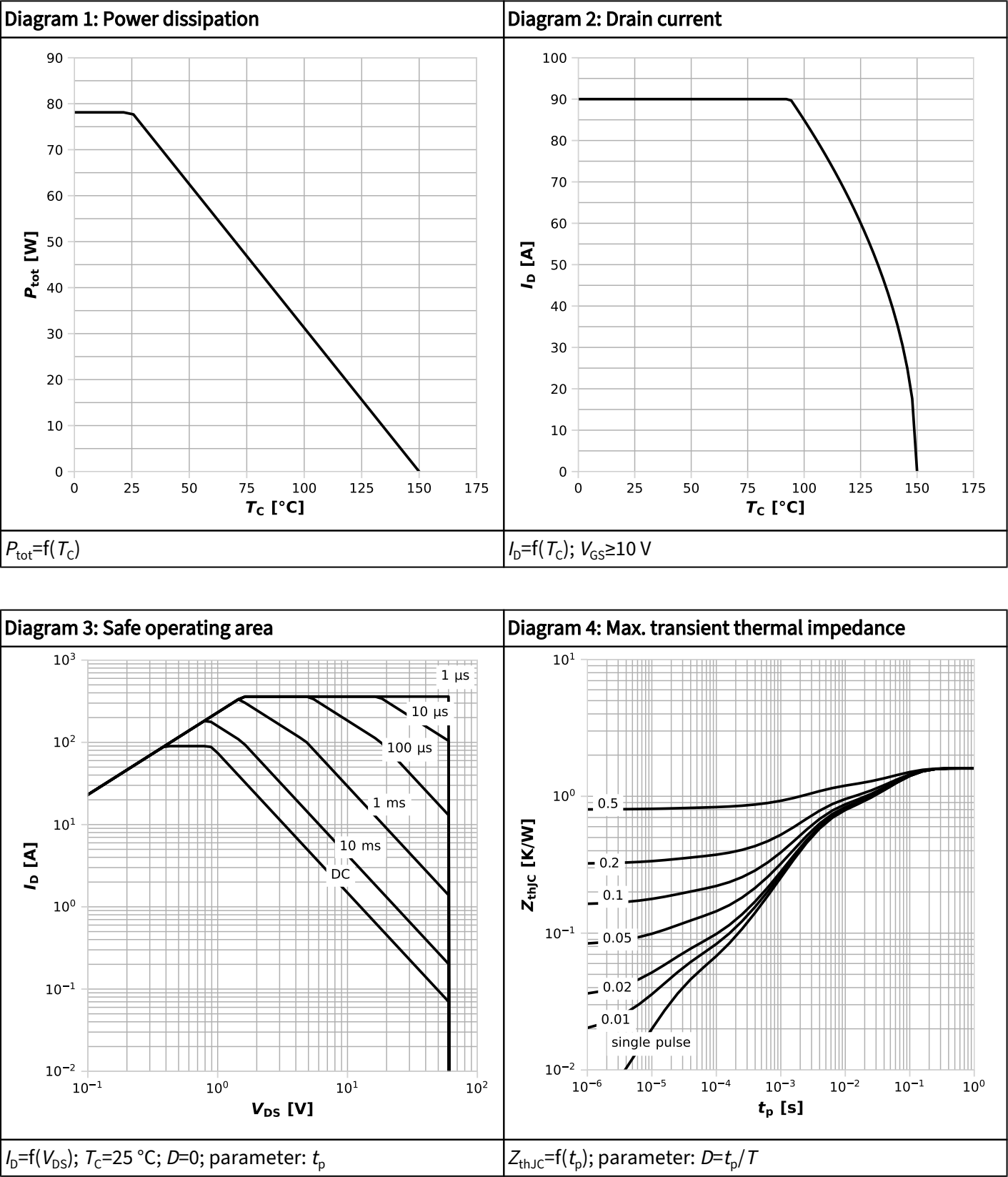
Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	41	-	nC	$V_{DD}=30\text{ V}$, $I_D=30\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	8	-	nC	
Switching charge	Q_{sw}	-	23	-	nC	
Gate charge total	Q_g	-	108	143	nC	
Gate plateau voltage	$V_{plateau}$	-	4.6	-	V	$V_{DD}=30\text{ V}$, $V_{GS}=0\text{ V}$
Output charge	Q_{oss}	-	87	116	-	

⁵⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	30	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	120	A	
Diode forward voltage	V_{SD}	-	0.8	1.2	V	$V_{GS}=0\text{ V}$, $I_F=30\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time	t_{rr}	-	60	-	ns	$V_R=30\text{ V}$, $I_F=I_S$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	87	-	nC	

4 Electrical characteristics diagrams



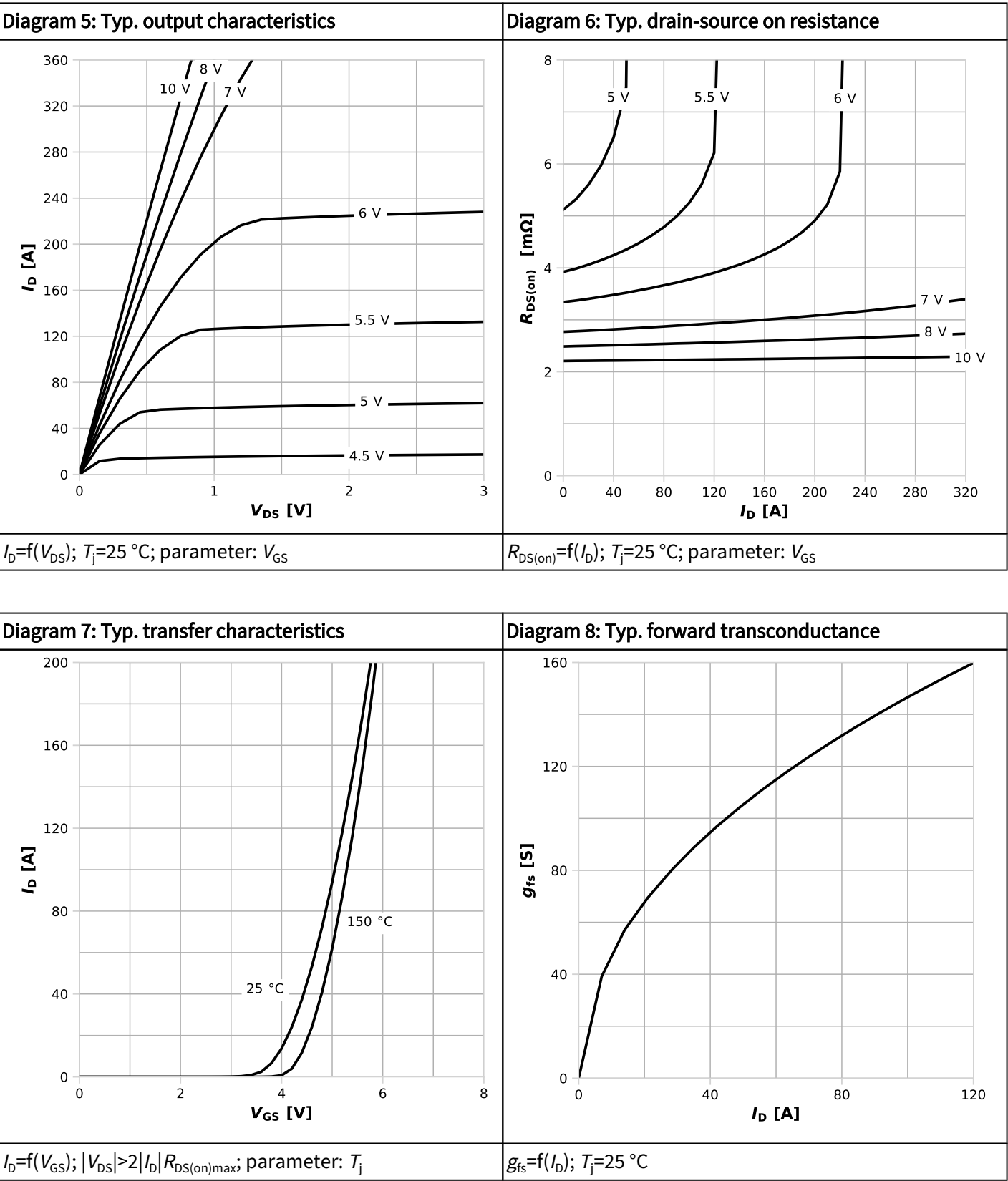
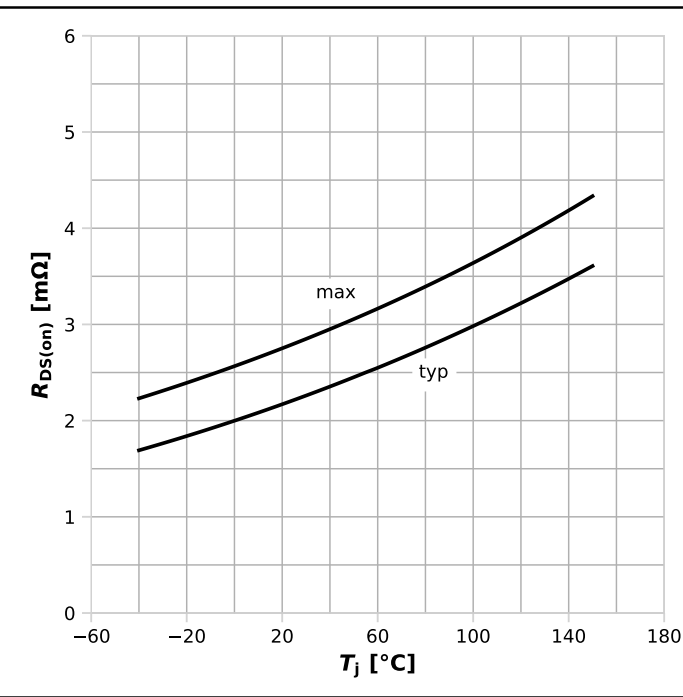
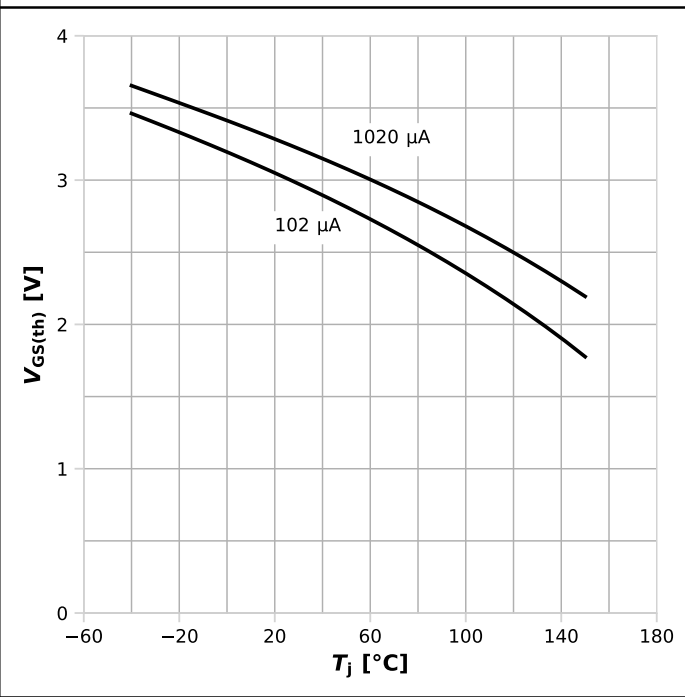


Diagram 9: Drain-source on-state resistance



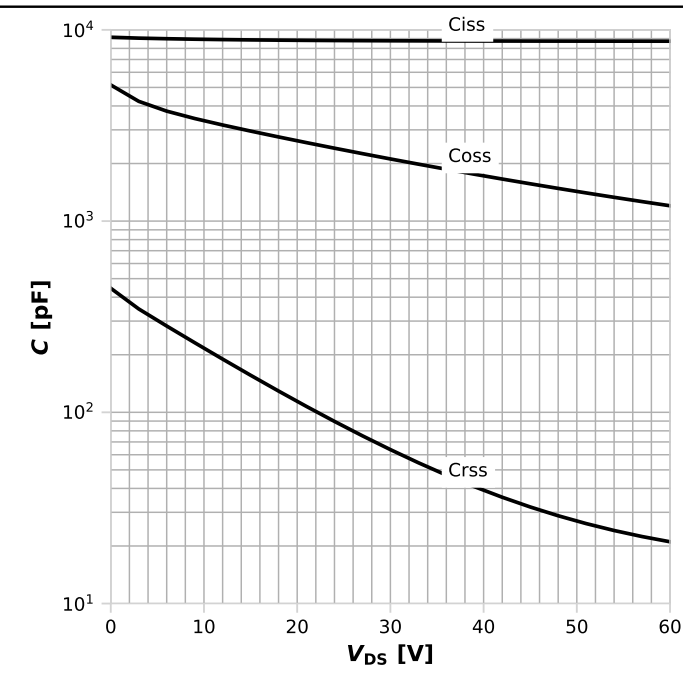
$R_{DS(on)} = f(T_j); I_D = 30 \text{ A}; V_{GS} = 10 \text{ V}$

Diagram 10: Typ. gate threshold voltage



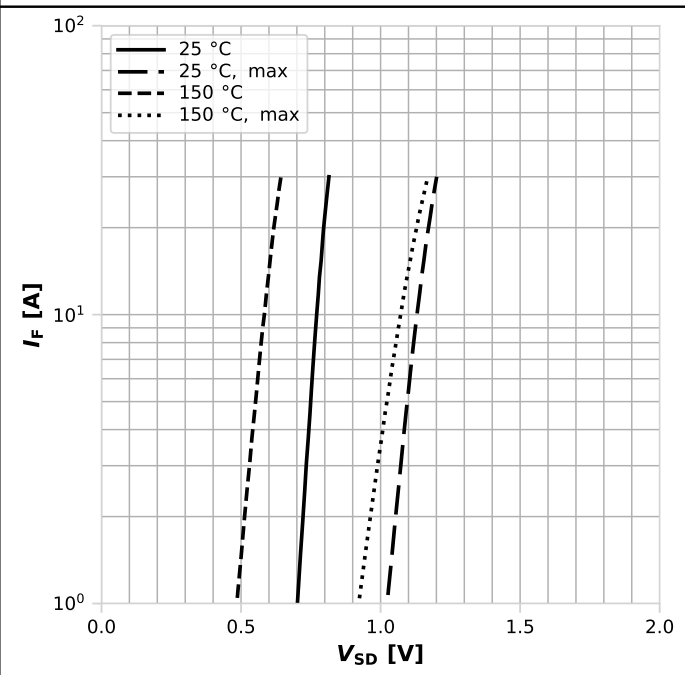
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

Diagram 11: Typ. capacitances



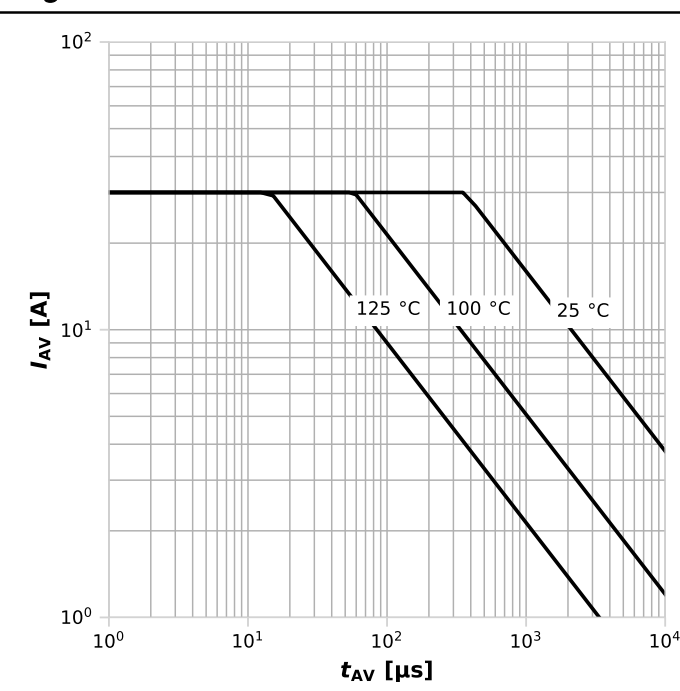
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Diagram 12: Forward characteristics of reverse diode



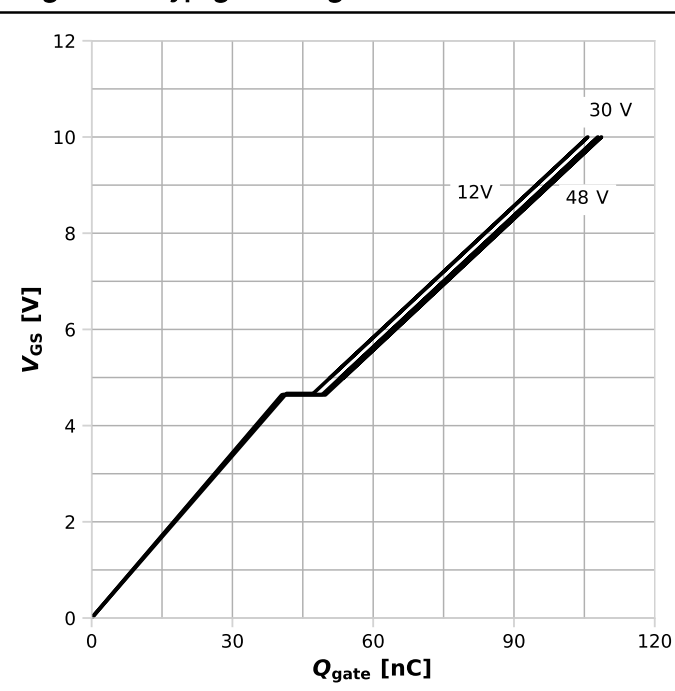
$I_F = f(V_{SD}); \text{parameter: } T_j$

Diagram 13: Avalanche characteristics



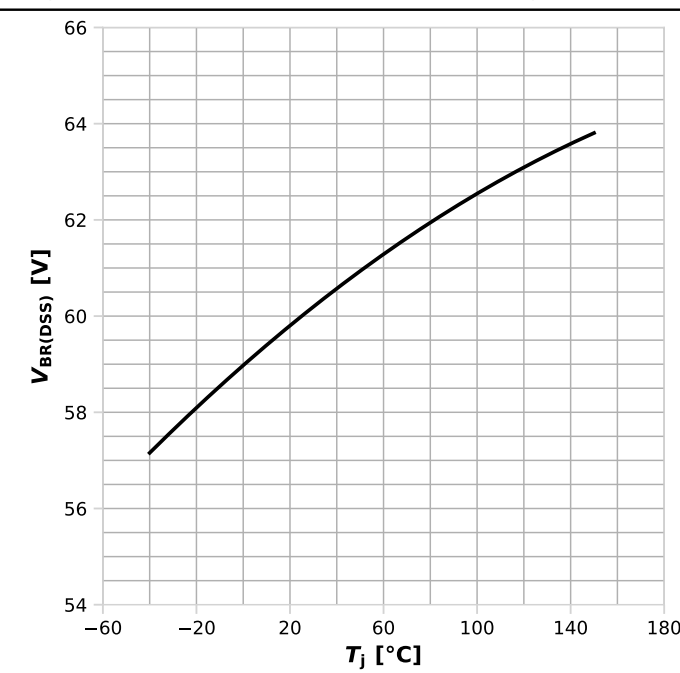
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



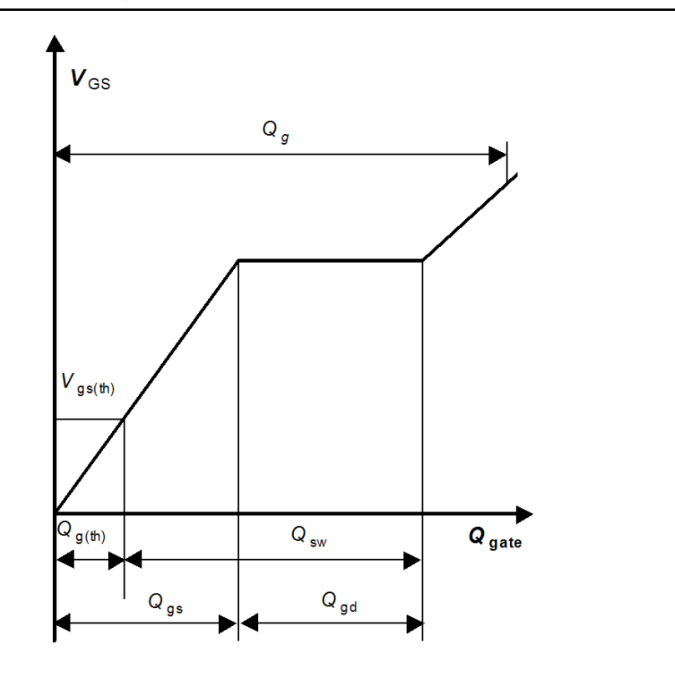
$V_{GS}=f(Q_{gate})$; $I_D=30\text{ A}$ pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j)$; $I_D=1\text{ mA}$

Gate charge waveforms



5 Package outlines

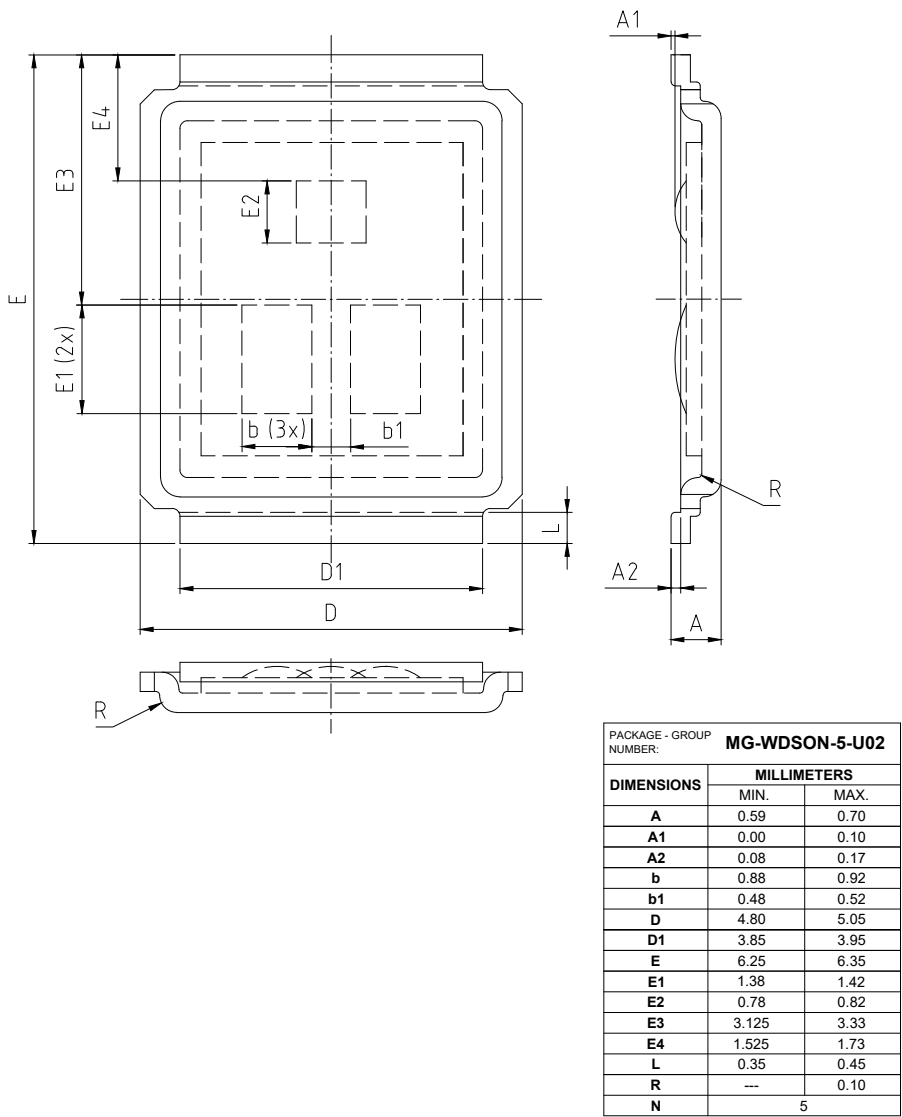
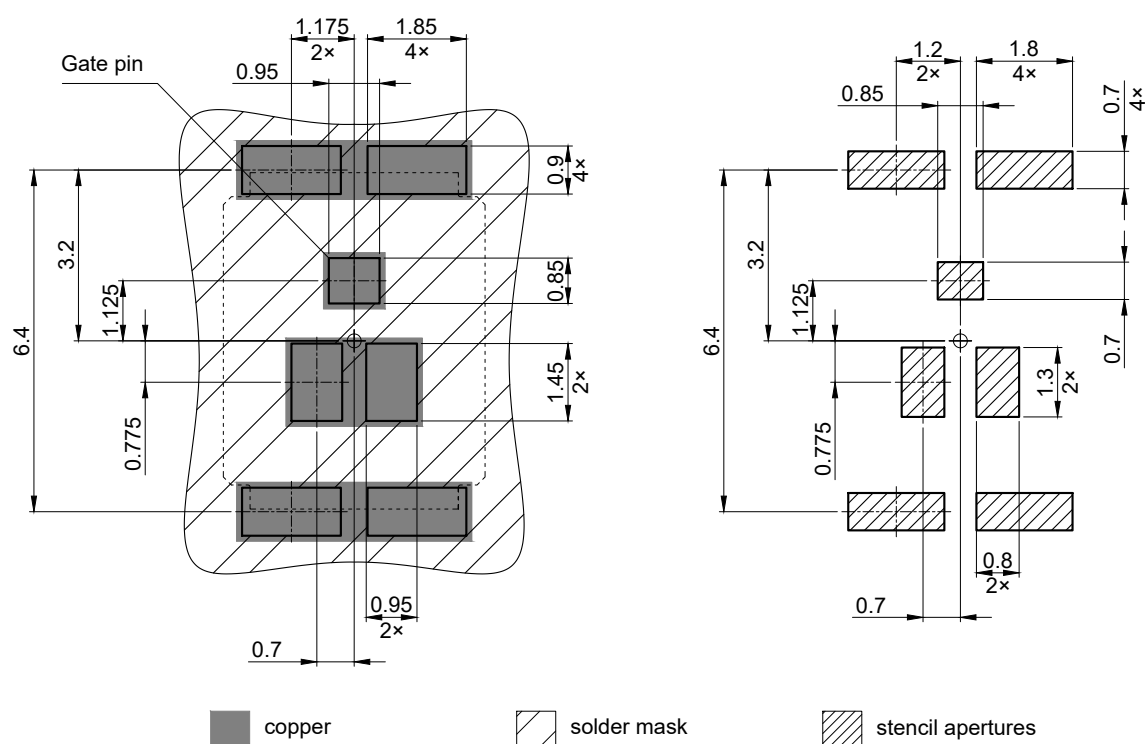
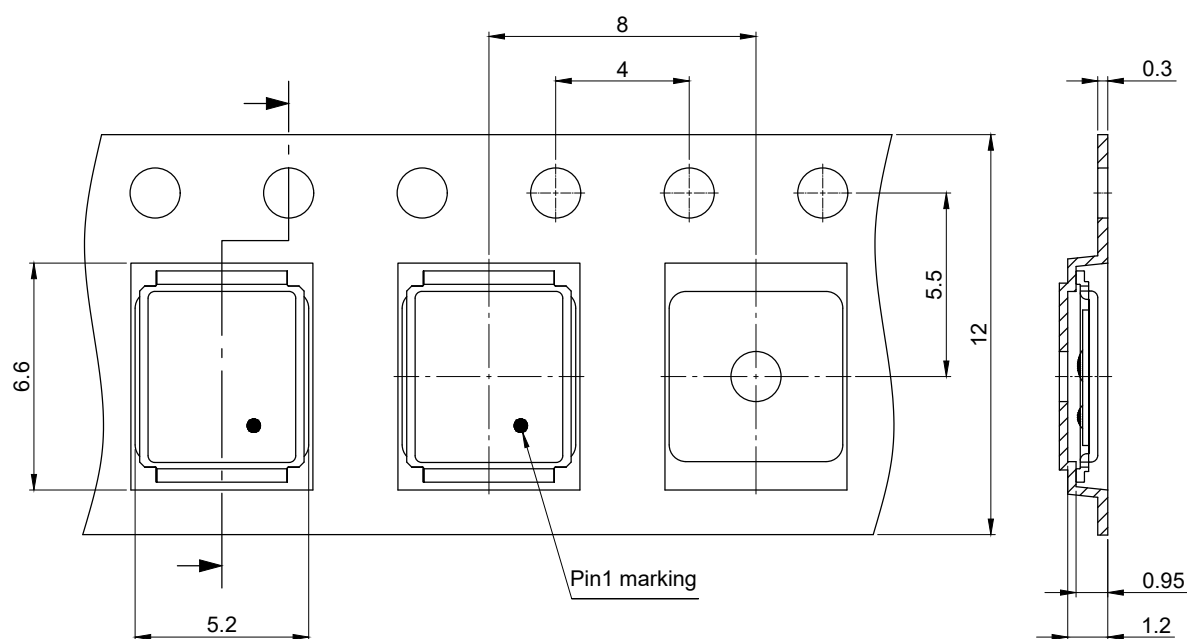


Figure 1 Outline MG-WDSO5-5, dimensions in mm



All dimensions are in units mm
 All pads are solder mask defined

Figure 2 Footprint drawing MG-WDSN-5, dimensions in mm



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 3 Packaging variant MG-WDSO5-5, dimensions in mm

Revision history

BSB028N06NN3 G

Revision 2024-11-09, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2024-11-09	New (Rev. 1.0) number is assigned due to datasheet tool change / improvement Updated POD from "MG-WDSO-2" to "MG-WDSO-5" page 11

Trademarks

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