EiceDRIVER™ 1ED32xxMC12H Two-level slew-rate control (2L-SRC)

Single-channel 5.7kV (rms) isolated gate driver IC with 2L-SRC

Feature list

- Single channel isolated gate driver
- Two-level slew rate control by controlling two independent gate resistors for both turn-on and turn-off
- Enable on the fly & cycle-by-cycle gate resistor change, optimize both EMI and efficiency during different load conditions
- 110ns propagation delay with 15 ns part to part variation
- For use with 600 V/650 V/1200 V/1700 V/2300 V IGBTs, Si and SiC MOSFETs
- Up to 18.0 A typical peak output current
- 40 V absolute maximum output supply voltage
- High common-mode transient immunity CMTI > 200 kV/µs
- Active output clamping
- Active Miller Clamp options available
- Galvanically isolated coreless transformer gate driver
- 3.3 V and 5 V input supply voltage
- Suitable for operation at high ambient temperature and in fast switching applications
- Certification: VDE 0884-11 with V_{IORM}= 1767 V (peak) and UL 1577 with V_{ISO} = 5.7 kV (rms) for 1 min

Potential applications

- AC and brushless DC motor drives
- High voltage DC/DC converter and DC/AC inverter
- UPS systems
- Solar inverters, e.g. for 1500 V (DC) systems

PG-DSO-8-66

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Device information

Product type	Typical output current and configuration	Slew-rate control	Certification	Marking	Package
1ED3240MC12H	10 A, standard	turn-on and turn-off	VDE + UL	1ED3240M	PG-DSO-8-66
1ED3241MC12H	18 A, standard	turn-on and turn-off	VDE + UL	1ED3241M	PG-DSO-8-66
1ED3250MC12H	10 A, Miller clamp	turn-on	VDE + UL	1ED3250M	PG-DSO-8-66
1ED3251MC12H	18 A, Miller clamp	turn-on	VDE + UL	1ED3251M	PG-DSO-8-66

Description

The 1ED32xx family is a group of galvanically isolated single-channel driver ICs in a DSO-8 300 mil package. The driver ICs provide typical peak output currents up to 18 A. The family implements two-level slew rate control (2L-SRC). This feature allows for controlling two independent gate resistors, which enables the optimization of both EMI and switching losses.

The family comprises standard output configuration and active Miller clamp output configurations with the same current rating to protect against parasitic turn-on. The input logic terminals operate safely with supply voltages of 3.3 V and 5 V. All input structures have threshold levels for support of 3.3 V microcontrollers. The driver IC family offers suitable output undervoltage lockout (UVLO) levels to operate various kinds of power transistors. The wide range of the output side supply voltage up to 40 V can be configured arbitrarily for positive and negative voltages as long as the absolute maximum of 40 V is not exceeded. All driver ICs have output sections with active shutdown.

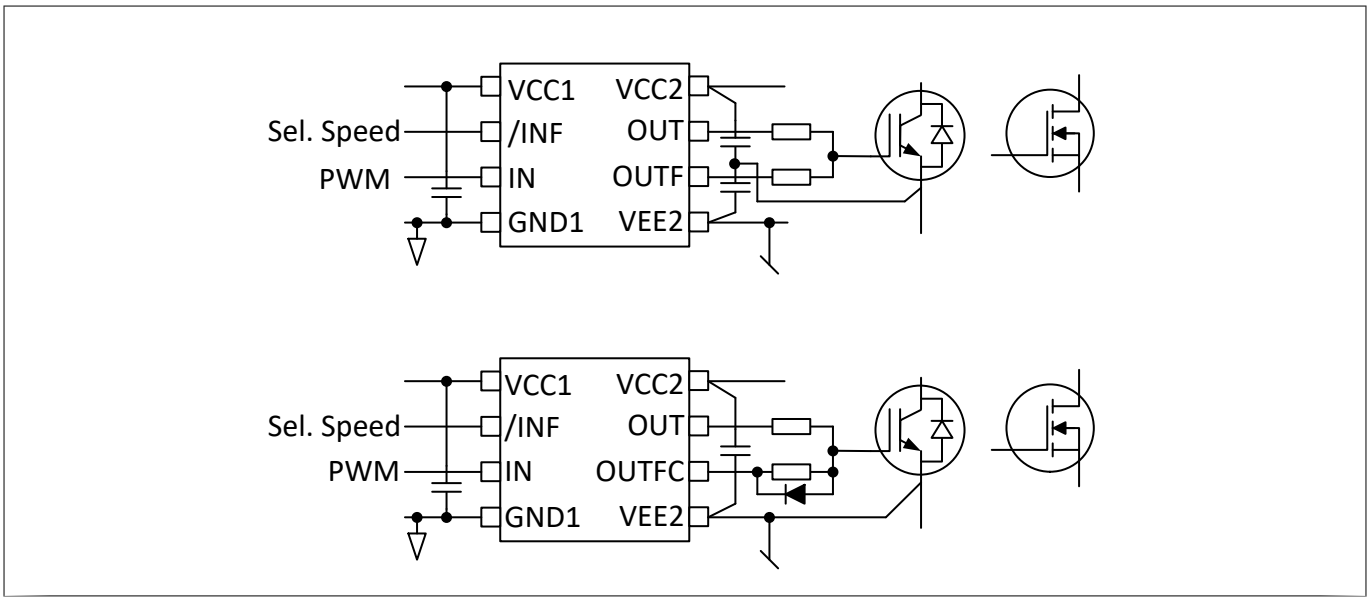

Figure 1 Typical application for standard pinout (top) and CLAMP pinout (bottom)

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1 Block diagram reference

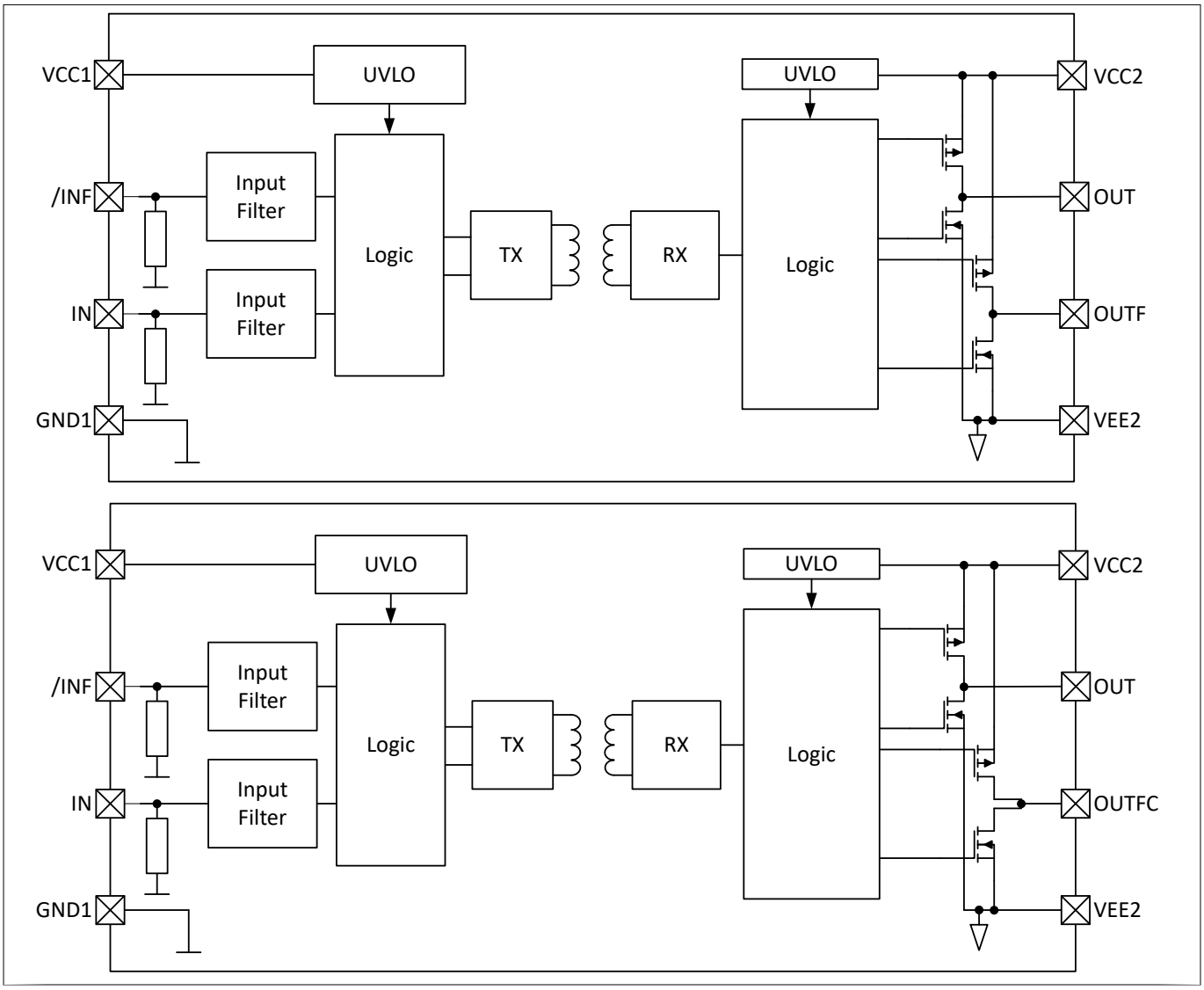

Figure 2 Block diagram for standard variants (top) and for CLAMP variants (bottom)

2 Related products to 1ED32xxMC12H

Note: Please consider the gate driver IC power dissipation and insulation requirements for the selected power switch and operating condition.

Product group	Product name	Description
Evaluation boards	EVAL-1ED3241MC12H	Supporting 1ED3241MC12H and IKQ75N120CT2 for double pulse tests
	EVAL-1ED3251MC12H	Supporting 1ED3251MC12H and IKQ75N120CT2 for double pulse tests
TRENCHSTOP™ IGBT Discrete	IKWH40N65WR6	650 V, 40 A IGBT with anti-parallel diode in TO-247-3-HCC
	IHW30N160R5	1600 V, 30 A IGBT Discrete with anti-parallel diode in TO-247

Product group	Product name	Description
	IKW15N120CS7	1200 V IGBT7 S7, 15 A IGBT with anti-parallel diode in TO247
	IKQ75N120CS7	1200 V IGBT7 S7, 75 A IGBT with anti-parallel diode in TO247-3
CoolSiC™ SiC MOSFET Discrete	IMBF170R1K0M1	1700 V, 1000 mΩ SiC MOSFET in TO-263-7 with extended creepage
	IMZA120R040M1H	1200 V, 40 mΩ SiC MOSFET in TO247-4 package
	IMZA120R014M1H	1200 V, 14 mΩ SiC MOSFET in TO247-4 package
	IMBG120R030M1H	1200 V, 30 mΩ SiC MOSFET in TO-263-7 package
	IMYH200R012M1H	2000 V, 12 mΩ SiC MOSFET in TO-247-PLUS with high creepage and clearance
CoolSiC™ SiC MOSFET Module	FS33MR12W1M1H_B11	EasyPACK™ 1B 1200 V, 33 mΩ sixpack module
	FF17MR12W1M1H_B11	EasyDUAL™ 1B 1200 V, 17 mΩ half-bridge module
	FF4MR12W2M1H_B11	EasyDUAL™ 2B 1200 V, 4 mΩ half-bridge module
	F4-17MR12W1M1H_B11	EasyPACK™ 1B 1200 V, 17 mΩ fourpack module
TRENCHSTOP™ IGBT Modules	F4-100R17N3E4	EconoPACK™ 3 1700 V, 100 A fourpack IGBT module
	F4-200R17N3E4	EconoPACK™ 3 1700 V, 200 A fourpack IGBT module
	FP10R12W1T7_B11	EasyPIM™ 1B 1200 V, 10 A three phase input rectifier PIM IGBT module
	FS100R12W2T7_B11	EasyPACK™ 2B 1200 V, 100 A sixpack IGBT module
	FP150R12KT4_B11	EconoPIM™ 3 1200V three-phase PIM IGBT module
	FS200R12KT4R_B11	EconoPACK™ 3 1200 V, 200 A sixpack IGBT module

3 Pin configuration

Pin configuration

Table 1 Pin configuration

Pin No.	Name	Function
1	*VCC1*	Positive logic supply
2	*/INF*	Driver input (active low) for operation *OUTF* or *OUTFC*
3	*IN*	PWM driver input (active high)
4	*GND1*	Logic ground
5	*VEE2*	Power ground
6	*OUTF / OUTFC*	Additional driver output
7	*OUT*	Regular driver output
8	*VCC2*	Positive power supply output side

Pin configuration

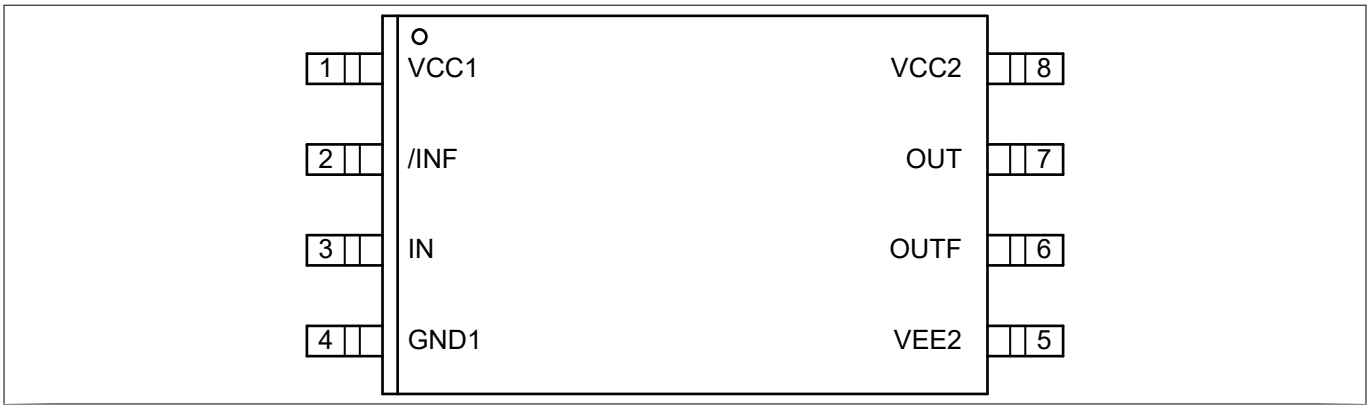

Figure 3 Pinout standard configuration (top view)

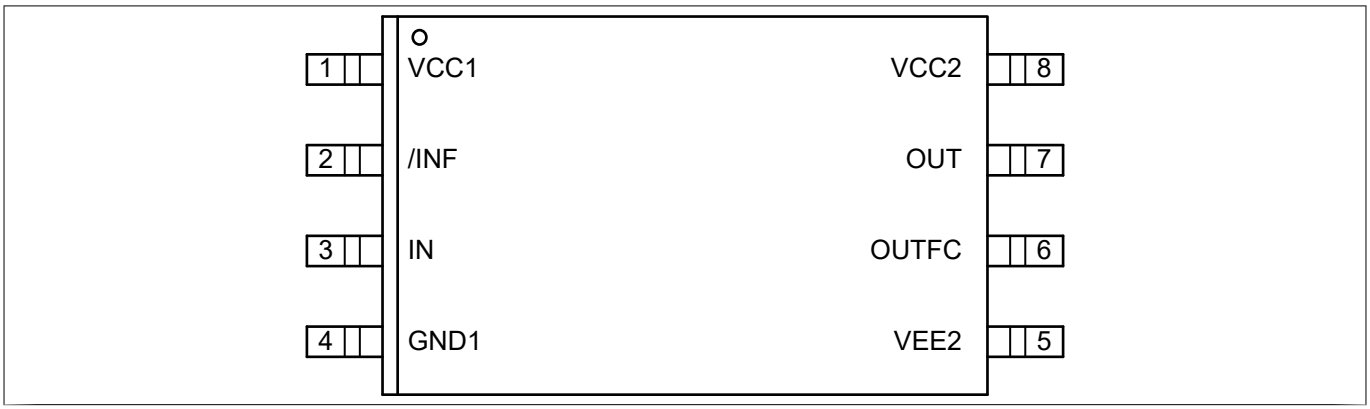

Figure 4 Pinout clamp configuration (top view)

Pin description

- *VCC1*: Logic input supply voltage with wide operating range from 3.3 V up to 15 V. This terminal is referenced to *GND1*
- *GND1*: Ground connection of input circuit. This is the reference point for the input side.
- */INF*: Inverted control signal for controlling the operation of output *OUTF* or *OUTFC* respectively. An internal filter provides robustness against noise at terminal */INF*. An internal weak pull-down resistor favors a low level. This terminal is referenced to *GND1*
- *IN*: Direct control signal for driver output. An internal filter provides robustness against noise at terminal *IN*. An internal weak pull-down resistor favors off-state. This terminal is referenced to *GND1*
- *VCC2*: Positive power supply pin of output driving circuit. A proper blocking capacitor has to be placed close to this supply pin. This terminal is referenced to *VEE2*.
- *VEE2*: Reference ground of the output driving circuit. In case of a bipolar supply (positive and negative voltage referred to IGBT emitter) this pin is connected to the negative supply voltage.
- *OUT*: This driver output terminal follows the signal at terminal *IN* to turn on or off the external power transistor. During on-state the driving output is switched to *VCC2*. This output will be actively pulled down to *VEE2* in case of an UVLO event on either the input side or the output side. The active shutdown keeps the output voltage at a low level in case that the output side supply voltage collapses.
- *OUTF*: This output follows terminal *OUT* according to the signal at terminal */INF*.
- *OUTFC*: This output follows terminal *OUT* according to the signal at terminal */INF* for turn-on only.

4 Functional description

The 1ED32xxMC12H are general purpose gate drivers incorporating two-level slew-rate control functionality (2L-SRC). Based on one additional input control signal */INF*, these drivers enable on-the-fly gate resistor changes.

The integrated galvanic isolation between control input logic and driving output stage grants additional safety. Its input voltage supply range supports the direct connection of various signal sources like DSPs and microcontrollers.

4.1 IC supply

The driver can operate over a wide supply-voltage range at both input side and output side. Both sides have an undervoltage lockout (UVLO) function which suppresses incoming control signals and prevents insufficient supply or gate voltages. The outputs are pulled down in cases of under-voltage lockout on either side.

The input-side power supply at terminal *VCC1* can range from typically 3.3 V up to 15 V. This allows a high safety margin with respect to voltage spikes on the supply voltage when supplying with 3.3 V or 5 V. A minimum of V_{UVLOH1} is required to start-up the input side of the driver IC.

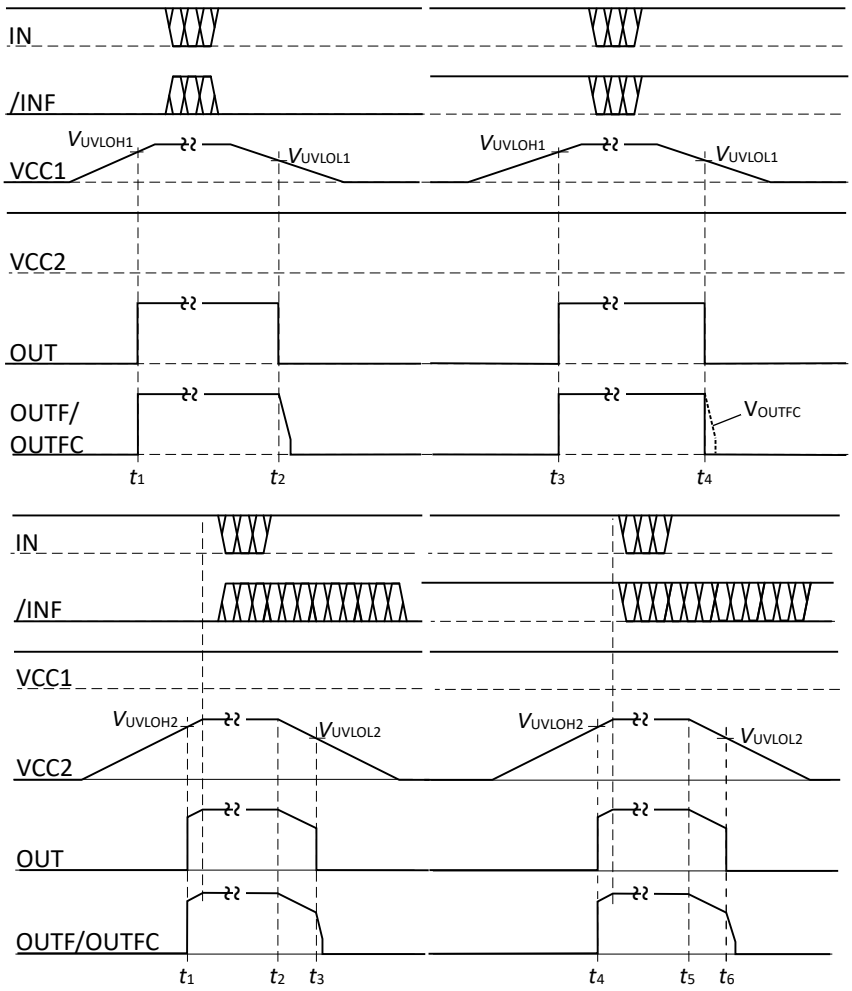

Figure 5 UVLO behavior regarding V_{VCC1} (top) and V_{VCC2} (bottom) after start up

The output side supports negative gate voltage operation, which helps to avoid a parasitic turn-on during off-state. The negative rail is connected to terminal *VEE2* in this case. A minimum voltage of V_{UVLOH2} at terminal *VCC2* is required for a safe start-up of the IC on the output side. The device is equipped with an undervoltage

lockout for input and output independently to ensure correct switching of power transistors . Operation starts only, if both V_{VCC1} and V_{VCC2} have increased above the respective levels V_{UVLOH1} and V_{UVLOH2}.

The input signals at terminals *IN* and */INF* are ignored until V_{VCC1} reaches the power-up voltage V_{UVLOH1}. Terminal *OUT* is activated according to the instantaneous state of terminal *IN*. Terminal *OUTF* or *OUTFC* are activated after a UVLO condition for turn-on according to the default state at terminal */INF*, which is LOW after start up. A new edge at terminal */INF* is required to establish the initial user setting after a UVLO event. A new edge at terminal *IN* is required to replace the */INF* default setting on the output side. If the power supply voltage V_{VCC1} of the input chip drops below V_{UVLOL1} a turn-off signal is sent to the output chip before power-down. Both outputs *OUT* and *OUTF* shut down according to the last transmitted status at terminals *IN* and */INF*.

The input signals at terminals *IN* and */INF* are ignored until V_{VCC2} reaches the power-up voltage V_{UVLOH2} . Terminal *OUT* is activated according to the instantaneous state of terminal *IN*. Terminal *OUTF* or *OUTFC* are activated after a UVLO condition of V_{VCC2} for turn-on according to the default state at terminal */INF*, which is LOW after start up. A new edge at terminal */INF* is required to establish the initial user setting after a UVLO event. A new edge at terminal *IN* is required to replace the */INF* default setting on the output side. If the power supply voltage V_{VCC2} of the output side drops below V_{UVLOL2}, output *OUT* pulls down independent of the last transmitted status at terminals *IN* and */INF*. Output *OUTF* or *OUTFC* pull down in addition when the their voltage is below V_{CLAMPL}.

UVLO events on the output side other than a full IC start-up result in a recovery of the output terminals *OUTF* and *OUTFC* according to the input-to-output control scheme.

Note: The supply voltage V_{VCC2} and related protection functions is always referred to as VEE2. There is no differentiation between unipolar or bipolar supply.

A capacitor that is placed in close proximity to the supply terminals *VCC1* and *GND1* on the input side, and *VCC2* and *VEE2* on the output side, avoids eventual triggering of under-voltage lockout events.

The IC is safe with any start-up sequence regarding its supply voltages V_{VCC1} and V_{VCC2}. However, it is good practice to have the input side supply voltage to start up first, followed by the output side supply.

4.2 Input terminals *IN* and */INF*

The input terminals *IN* and */INF* determine the behavior of the two output terminals *OUT* and *OUTF(C)*. While a PWM signal is connected to the IN terminal, thus determining the switching behavior of *OUT* and *OUTF(C)*, the */INF* terminal controls if only *OUT* or both *OUT* and *OUTF(C)* follow the input terminal *IN*. Since both output terminals *OUT* and *OUTF(C)* are connected to gate resistors, */INF* determines whether a single or both gate resistors are connected to an IGBT's gate.

Both input terminals contain a pull-down resistor to bias the IC into a safe mode in case the connection to the system control is interrupted. The non-inverting Schmitt trigger receives the input control signal and has CMOS-compatible trigger thresholds with minimum $V_{IN,L}$ for LOW level and maximum $V_{IN,H}$ for HIGH level. The input signal at terminal *IN* follows a positive logic, while the signal at terminal */INF* follows an active-low logic.

There is a short-pulse suppression filter after the Schmitt trigger with a filter time T_{INFLT}. All pulses that are below $T_{INFLT,min}$ will be suppressed, and pulses that are longer than $T_{INFLT,max}$ will pass the filter and be transmitted to the output side. External RC-filters with time constants of more than 10 ns, for example 1 nF and 10 Ω, have to be used to further support the integrated short pulse suppression function to filter input noise.

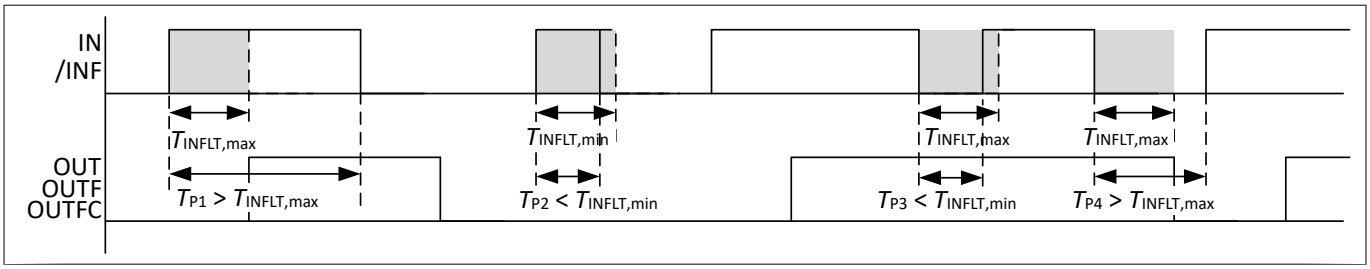

Figure 6 Timing of input signals with respect of the input filter

All changes at terminal */INF* are acknowledged, if they occur earlier than or simultaneously with a change at terminal *IN*. After a signal edge is applied at terminal *IN*, the signal at terminal */INF* has to be kept for at least $T_{/INF,hold}$ for its status to be transmitted to the output side.

4.3 Output terminal *OUT*

The output terminal *OUT* changes its status according to the status of the input signal at terminal *IN*. A high signal at terminal *IN* determines a high signal at terminal *OUT*. A low signal determines a low signal.

The driver IC's output section at terminal *OUT* provides a rail-to-rail output. This feature allows the tight control of gate voltage during on-state and short circuit to be maintained as long as the driver's supply is stable. The switching behavior of the power transistor is mainly controlled by the gate resistor, due to the low internal voltage drop of the IC. In turn, the low voltage drop reduces the power to be dissipated by the driver.

The active shutdown feature of terminal *OUT* ensures a safe off-state of the power transistor in case the output side is not connected to the power supply or an undervoltage lockout is in effect. The transistor's gate is clamped at terminal *OUT* to *VEE2*.

4.4 Output terminal *OUTF*

Terminal *OUTF* is the second output of those gate driver ICs, which have the standard output configuration. *OUTF* changes its status according to the status of the input signals */INF* and *IN*. It turns the power transistor on and off in combination with the terminal *OUT*, so that depending on the status at terminal */INF*, a higher gate current is available, and the switching speed can be modified on the fly. Terminal *OUTF* is also set to clamping mode, if it is not activated for active gate operation. The clamping mode is activated when the gate voltage of the power transistor is below V_{CLAMPL} during off-state or above V_{VCC2}-V_{CLAMPH} during on-state. The clamping mode during on-state helps to achieve better short circuit clamping. The on-state clamping is activated after turn-on, as soon as the filter time of $t_{dCLAMPH}$ is elapsed. A clamping filter time $t_{dCLAMPL}$ for off-state improves the robustness of the IC's Miller clamp function.

The driver IC's output section at terminal *OUTF* provides a rail-to-rail output. This feature allows the tight control of gate voltage during on-state and short circuit to be maintained as long as the driver's supply is stable. The switching behavior of the power transistor is mainly controlled by the gate resistor, due to the low internal voltage drop of the IC. In turn, the low voltage drop reduces the power to be dissipated by the driver.

Terminal *OUTF* features the active shutdown function. This ensures a safe off-state of the power transistor in case the output side is not connected to the power supply, or the power supply of the output side collapses faster than the UVLO can react. The transistor's gate is clamped at terminal *OUTF* to *VEE2*.

The driving capability of terminal *OUTF* is the same as for terminal *OUT*. *OUTF* and *OUT* can be operated in low resistive connection (i.e. direct paralleling) only if the voltage $V_{/INF}$ at terminal */INF* is at the corresponding level at any time.

4.5 Output terminal *OUTFC*

Terminal *OUTFC* is the second output of those gate driver ICs having the Miller clamp function, i.e. the two-level slew-rate control in for turn-on only. *OUTFC* changes its status according to the status of the input signal */INF*

and *IN*. It turns on the power transistor in combination with terminal *OUT*, so that depending on the status at terminal */INF*, a higher gate current is available and the switching speed can be modified for each PWM edge. Terminal *OUTFC* is not activated during the turn-off transient.

Terminal *OUTFC* is set to clamping mode also if it is not activated for active gate turn-on. The clamping mode is activated when the gate voltage of the power transistor is below V_{CLAMPL} during off-state or above V_{VCC2}-V_{CLAMPH} during on-state. The clamping mode during on-state helps to achieve better short circuit clamping. The on-state clamping is activated after turn-on, as soon as the filter time of $t_{dCLAMPH}$ is elapsed. A clamping filter time $t_{dCLAMPL}$ for off-state improves the robustness of the IC's Miller clamp function.

The clamping capability of the output *OUTFC* during off-state of the power transistor is identical to turn-off current capability terminal *OUT*.

The driver IC's output section at terminal *OUTFC* provides a rail-to-rail output. This feature allows the tight control of gate voltage during on-state and short circuit to be maintained as long as the driver's supply is stable. The switching behavior of the power transistor is mainly controlled by the gate resistor, due to the low internal voltage drop of the IC. In turn, the low voltage drop reduces the power to be dissipated by the driver.

Terminal *OUTFC* features the active shutdown function. This ensures a safe off-state of the power transistor in case the output side is not connected to the power supply, or the power supply of the output side collapses faster than the UVLO can react. The transistor's gate is clamped at terminal *OUTFC* to *VEE2*.

The driving capability of terminal *OUTFC* is the same as for terminal *OUT*. *OUTFC* and *OUT* can be operated in low resistive connection (i.e. direct paralleling) only if the voltage $V_{/INF}$ at terminal */INF* is at the corresponding level at any time.

4.6 Input-to-output control scheme

The two-level slew rate control IC family can activate the additional output *OUTF* or *OUTFC* depending on the input signals at the terminals *IN* and */INF*. The relationship between input signals and output signals is defined in the table below.

Table 2 Input-to-output control scheme

State	*IN*	*/INF*	*OUT*	*OUTF* (1ED3240MC12H, 1ED3241MC12H)	*OUTFC* (1ED3250MC12H, 1ED3251MC12H)
1	0	0	0	0*	0*
2	0 → 1	0	0 → 1	0 → 1	0 → 1
3	0	0 → 1	0	0*	0*
4	1	0	1	1*	1*
5	1 → 0	0	1 → 0	1 → HiZ	1 → HiZ
6	1	0 → 1	1	1*	1*
7	0	1	0	0*	0*
8	0	1 → 0	0	0*	0*
9	0 → 1	1	0 → 1	0 → HiZ	0 → HiZ
10	1	1	1	1*	1*
11	1	1 → 0	1	1*	1*
12	1 → 0	1	1 → 0	1 → 0	1 → HiZ
Input UVLO↓	X	X	0	last */INF*	last */INF*
Output UVLO↓	X	X	0	HiZ	HiZ

*) Output is activated when the voltage at terminal *OUTF* or *OUTFC* is higher than V_{VCC2} - V_{CLAMPH} during on-state, or lower than V_{CLAMPL} during off-state.

The control scheme of the gate driver IC family inherently avoids the activation of the two outputs *OUT* or *OUTF* / *OUTFC* in active opposite status. Both outputs *OUTF* and *OUTFC* can have the states 1, 0 and high impedance (HiZ) according to the table above. The status of terminal */INF* can be changed pulse-by-pulse with a short delay with respect to a potential change of status at terminal *IN* according to the timing diagrams below.

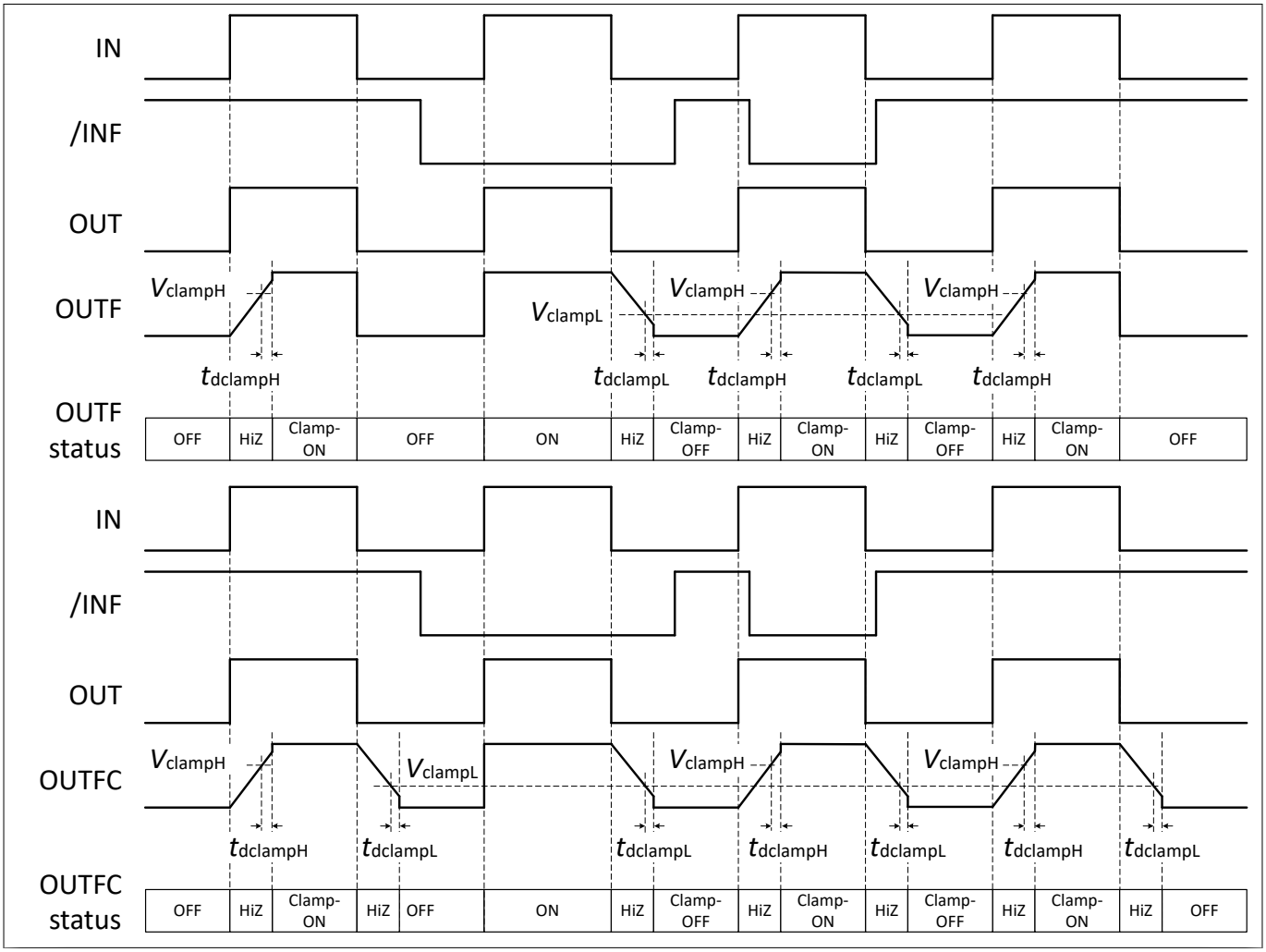

Figure 7 **Timing diagram of input and output signals for standard version (top) and clamp version (bottom)**

5 Electrical characteristics and parameters

5.1 Absolute maximum ratings

Absolute maximum ratings are defined as ratings, that can lead to the destruction of the integrated circuit, if exceeded. Unless otherwise noted all parameters refer to terminal *GND1*.

Table 3 Absolute maximum ratings

Parameter	Symbol	Values		Unit	Note or test condition
		Min.	Max.		
Input to output offset voltage	V_{OFFSET}		2300	V	$V_{VEE2,max}$-$V_{VEE2,min}$ with $V_{VEE2,max} \geq V_{GND1} \geq V_{VEE2,min}$ [1)2)]
Power supply input side	V_{VCC1}	-0.3	15	V	
Power supply input side	$V_{VCC1,dyn}$	-0.3	17	V	$t < 1$ µs [3)]
Logic input voltages (*IN*, */INF*)	V_{IN}	-0.3	15	V	
Dynamic logic input voltages (*IN*, */INF*)	$V_{IN,dyn}$	-0.3	17	V	$t < 1$ µs [3)]
Power supply output side	V_{VCC2}	-0.3	40	V	with respect to *VEE2*
Gate driver output (*OUT*, *OUTF*, *OUTFC*)	V_{OUT}	V_{VEE2} - 0.3	V_{VCC2} +0.3	V	with respect to *VEE2*
Junction temperature	T_J	-40	150	°C	
Storage temperature	T_{stg}	-55	150	°C	
Power dissipation (input side)	$P_{D,IN}$	-	100	mW	T_A = 85 °C, 1s0p [4)]
Power dissipation (output side)	$P_{D,OUT}$	-	625	mW	T_A = 85 °C, 1s0p [5)]
Thermal resistance (input side)	$R_{THJA,IN}$	-	104	K/W	T_A = 85 °C, 1s0p
Thermal resistance (output side)	$R_{THJA,OUT}$	-	104	K/W	T_A = 85 °C, 1s0p
ESD capability	$V_{ESD,HBM}$	-	4	kV	[6)]
	ESD,CDM	-	TC 1000		[7)]

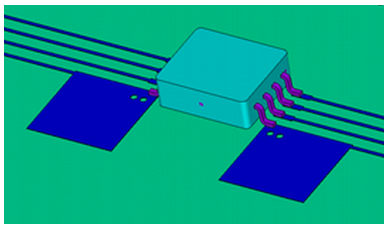

Figure 8 Reference layout for thermal data (1s0p, 2 x 50 mm² cooling area, Copper thickness 35 µm)

This PCB layout represents the reference layout used for the thermal characterization of the 300 mil package.

1 For functional isolation only
2 See also: Insulation characteristics
3 Parameter is not subject of production test - verified by design/ characterization
4 IC output-side power dissipation is derated linearly with 9.62 mW/°C above 139,6 °C
5 IC output-side power dissipation is derated linearly with 9.62 mW/°C above 85 °C
6 According to ANSI/ESDA/JEDEC-JS-001-2017
7 According to ANSI/ESDA/JEDEC-JS-002-2014, TC = test condition in Volt

5.2 Operating parameters

The IC operates as described in the functional description within the operating parameters. Unless otherwise noted all parameters refer to GND1.

Table 4 Operating parameters

Parameter	Symbol	Values		Unit	Note or test condition
		Min.	Max.		
Power supply output side	V_{VCC2}	10	35	V	
Power supply input side	V_{VCC1}	3	15	V	
Logic input voltages (*IN*, */INF*)	V_{IN}	-0.3	5.5	V	
Ambient temperature	T_A	-40	125	°C	
Thermal coefficient, junction-top	$\Psi_{TH,JT}$	-	6.8	K/W	T_A = tbd °C
Common mode transient immunity (CMTI)	|CMTI|	-	200	kV/µs	$V_{OFFSET,test}$ = 1500 V

5.3 Eletrical characteristics

The electrical characteristics include the spread of values in supply voltages, load and junction temperatures given below. Typical values represent the median values at V_{VCC1} = 5 V, V_{VCC2} = 15 V, and T_A = 25°C. Unless otherwise noted all voltages are given with respect to their respective reference *GND1* or *VEE2*.

5.3.1 Power supply

Table 5 Power supply

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
UVLO threshold input side (on)	V_{UVLOH1}	-	2.85	3.1	V	
UVLO threshold input side (off)	V_{UVLOL1}	2.5	2.65	-	V	
UVLO hysteresis input side	V_{HYS1}	0.1	0.2	-	V	
UVLO threshold output side (on)	V_{UVLOH2}	-	11.8	12.5	V	
UVLO threshold output side (off)	V_{UVLOL2}	10.4	10.8	-	V	
UVLO hysteresis output side	V_{HYS2}	0.8	-	-	V	
Quiescent current input side	I_{Q1}	-	1.2	1.4	mA	
Quiescent current output side	I_{Q2}	-	1.9	2.3	mA	
Start up time[8)]	t_{START}	-	7.4	20	µs	

5.3.2 Logic input

Table 6 Logic input

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
IN, */INF* low-input threshold voltage	$V_{IN,L}$	1	1.2	-	V	

(table continues...)

8 Parameter is not subject of production test - verified by design/ characterization

Table 6 (continued) Logic input

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
IN, */INF* high-input threshold voltage	$V_{IN,H}$	-	2.1	2.3	V	
IN, */INF* low/high hysteresis	$V_{IN,HYS}$	0.7	-		V	
IN, */INF* input current	I_{IN}	-	-	100	µA	$V_{IN} = V_{VCC1}$
IN, */INF* pull-down resistor	$R_{IN,PD}$	-	75	-	kΩ	
/INF hold time[9)]	$t_{/INF,hold}$	50	-	-	ns	

5.3.3 Gate driver

Table 7 Gate driver

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
High-level output peak current (*OUT*, *OUTF*, *OUTFC*, 1ED32x0MC12H)[10)]	I_{OH}	-	5	-	A	Output on
Low-level output peak current (*OUT*, *OUTF*, 1ED3240MC12H)[10)]	I_{OL}	-	5	-	A	Output off
High-level output resistance (*OUT*, *OUTF*, *OUTFC*, 1ED32x0MC12H)	$R_{OH,1}$	-	0.92	1.47	Ω	Output on, I_{OH} = 0.1 A
Low-level output resistance (*OUT*, *OUTF*, *OUTFC*, 1ED32x0MC12H)	$R_{OL,1}$	-	0.73	1.1	Ω	Output off, I_{OL} = 0.1 A
High-level output peak current (*OUT*, *OUTF*, *OUTFC*, 1ED32x1MC12H)[10)]	I_{OH}	-	9	-	A	Output on
Low-level output peak current (*OUT*, *OUTF*, 1ED3241MC12H)[10)]	I_{OL}	-	9	-	A	Output off
High-level output resistance (*OUT*, *OUTF*, *OUTFC*, 1ED32x1MC12H)	$R_{OH,2}$	-	0.51	0.81	Ω	Output on, I_{OH} = 0.1 A
Low-level output resistance (*OUT*, *OUTF*, *OUTFC*, 1ED32x1MC12H)	$R_{OL,2}$	-	0.42	0.63	Ω	Output off, I_{OL} = 0.1 A
High-level output voltage (*OUT*, *OUTF*, *OUTFC*)	ΔV_{OH}	-	-	0.1	V	Output on, V_{VCC2}-V_{OH}; I_{OH} = 20 mA
Low-level output voltage (*OUT*, *OUTF*, *OUTFC*)	ΔV_{OL}	-	-	0.1	V	Output off, V_{VCC2}-V_{OH}; I_{OH} = 20 mA
Low-level clamp peak current (*OUTF*, *OUTFC*) [10)]	I_{CLAMPL}	-	2.1	-	A	V_{OL} = 2 V

(table continues...)

9 Parameter is not subject of production test - verified by design/ characterization
10 Parameter is not subject of production test - verified by design/ characterization

Table 7 (continued) Gate driver

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Short-circuit clamp voltage between *OUT* / *OUTF* / *OUTFC* and *VCC2*[10]	V_{CLP}	-	-	1.3	V	Output on, I_{OH} = 500 mA, t < 10 µs
Active Miller clamp threshold voltage OFF (*OUTF*, *OUTFC*)	V_{CLAMPL}	-	2	2.5	V	V_{OL}-V_{VEE2}, $V_{/INF}$ = 0
Clamping ON threshold voltage (*OUTF*, *OUTFC*)	V_{CLAMPH}	0.5	1	-	V	V_{VCC2}-V_{OH}, $V_{/INF}$ = 1
Active Miller clamp delay time (*OUTF*, *OUTFC*)[10]	$t_{dCLAMPL}$	-	-	80	ns	$V_{OL} \le V_{VEE2}+V_{CLAMPL}$, $V_{/INF}$ = 1
Clamping ON delay time (IGBT variants, *OUTF*, *OUTFC*)[10]	$t_{dCLAMPH}$	-	890	-	ns	$V_{OH} \ge V_{VCC2}$-V_{CLAMPH}, $V_{/INF}$ = 1

5.3.4 Dynamic characteristics

The load capacitance is 100 pF if not otherwise noted.

Table 8 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Input-to-output propagation delay ON	t_{PDON}	-	-	110	ns	*IN* turn-on threshold to 10% output on
Input-to-output propagation delay OFF	t_{PDOFF}	-	-	110	ns	*IN* turn-off threshold to 90% output off
Input-to-output propagation delay distortion (t_{PDOFF} - t_{PDON})	t_{PDISTO}	-10	0	5	ns	
Input-pulse suppression time	t_{INFLT}	30	-	40	ns	
Input-to-output propagation delay mismatch OUT vs. OUTF/ OUTFC[11]	$t_{PDOUT-OUTF}$	-	<1	-	ns	
Input-to-output, part to part propagation delay variation	$t_{PD,P2P}$	-	-	15	ns	
Input-to-output propagation delay variation due to temperature	$t_{PD,T}$	-5	-	12	ns	
Rise time	t_{RISE}	-	1.6	15	ns	C_{LOAD} = 100 pF
Fall time	t_{FALL}	-	1.5	15	ns	C_{LOAD} = 100 pF
Rise time	t_{RISE}	-	9	30	ns	C_{LOAD} = 1 nF
Fall time	t_{FALL}	-	8.5	30	ns	C_{LOAD} = 1 nF

10 Parameter is not subject of production test - verified by design/ characterization
11 Parameter is not subject of production test - verified by design/ characterization

5.3.5 Active shutdown

Table 9 Active shutdown

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Active shutdown voltage	$V_{ACTSD,L}$	-	1.5	2.0	V	I_O = 10 mA; V_{VCC2} open

6 Isolation ratings and characteristics

6.1 Safety limiting values

This coupler is suitable for rated insulation only within the given safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Table 10 Safety limiting values

Description	Symbol	Characteristic	Unit
Maximum ambient safety temperature	T_S	150	°C
Maximum input-side power dissipation at T_A = 25°C[12]	P_{SI}	100	mW
Maximum output-side power dissipationat T_A = 25°C[13]	P_{SO}	1100	mW

6.2 Certified according to VDE 0884-11 for reinforced insulation

This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Table 11 Reinforced insulation ratings according to VDE 0884-11

Description	Symbol	Characteristic	Unit
Installation classification per EN 60664-1, Table 1			–
for rated mains voltage ≤ 150 V (rms)		I-IV	
for rated mains voltage ≤ 300 V (rms)		I-IV	
for rated mains voltage ≤ 600 V (rms)		I-III	
for rated mains voltage ≤1000 V (rms)		I-II	
Climatic classification		40/125/21	–
Pollution degree (EN 60664-1)		2	–
Minimum external clearance	*CLR*	>8	mm
Minimum external creepage	*CPG*	>8	mm
Minimum comparative tracking index	*CTI*	400	–
Maximum repetitive insulation voltage	V_{IORM}	1767	V (peak)
Highest allowable overvoltage	V_{IOTM}	8000	V (peak)

(table continues...)

12 IC input-side power dissipation is derated linearly at 9.62 mW/°C above 139.6 °C
13 IC output-side power dissipation is derated linearly at 7.35 mW/°C above 25 °C

Table 11 (continued) Reinforced insulation ratings according to VDE 0884-11

Description	Symbol	Characteristic	Unit
Maximum surge insulation voltage Surge insulation test voltage $V_{TEST} = V_{IOSM} \times 1.6$	V_{IOSM}	6875	V (peak)
Apparent charge, method a $V_{pd(ini),a} = V_{IOTM}$, $V_{pd(m)} = 1.6 \times V_{IORM}$, $t_{ini} = 1$ min	q_c	<5	pC
Apparent charge, method b $V_{pd(ini),b} = 1.2 \times V_{IOTM}$, $V_{pd(m)} = 1.875 \times V_{IORM}$, $t_{ini,b} = 1$ s	q_c	<5	pC
Insulation resistance at $T_{A, max}$	R_{IO}	$> 10^{11}$	Ω
Insulation resistance at T_S	R_{IO}	$> 10^9$	Ω
Insulation capacitance	C_{IO}	1.66	pF

6.3 Recognized under UL 1577 (File E311313)

Table 12 Recognized under UL 1577

Description	Symbol	Characteristic	Unit
Insulation withstand voltage/1 min	V_{ISO}	5700	V (rms)
Insulation test voltage/1 s	$V_{ISO, TEST}$	6840	V (rms)

7 Timing diagrams

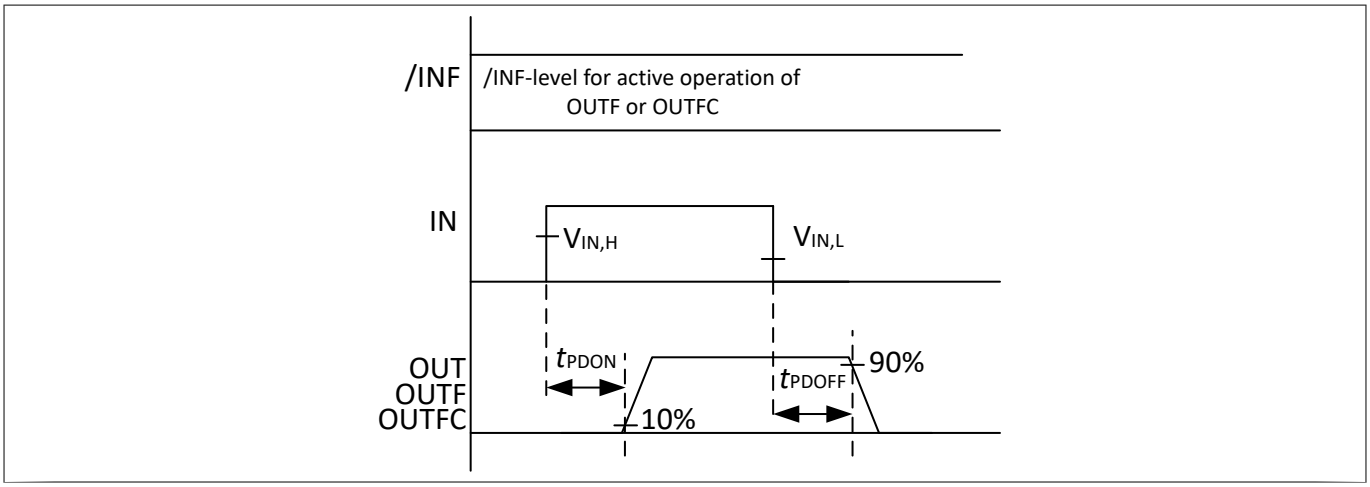

Figure 9 Propagation delay

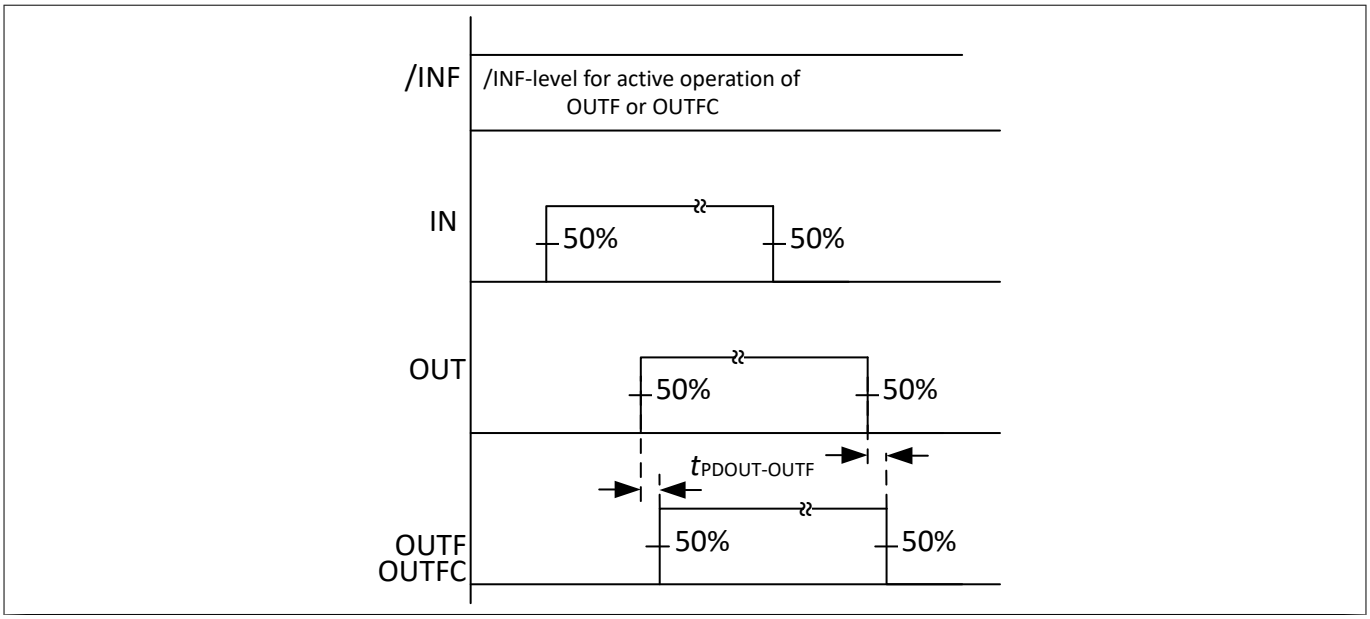

Figure 10 OUT - OUTF/OUTFC propagation delay mismatch

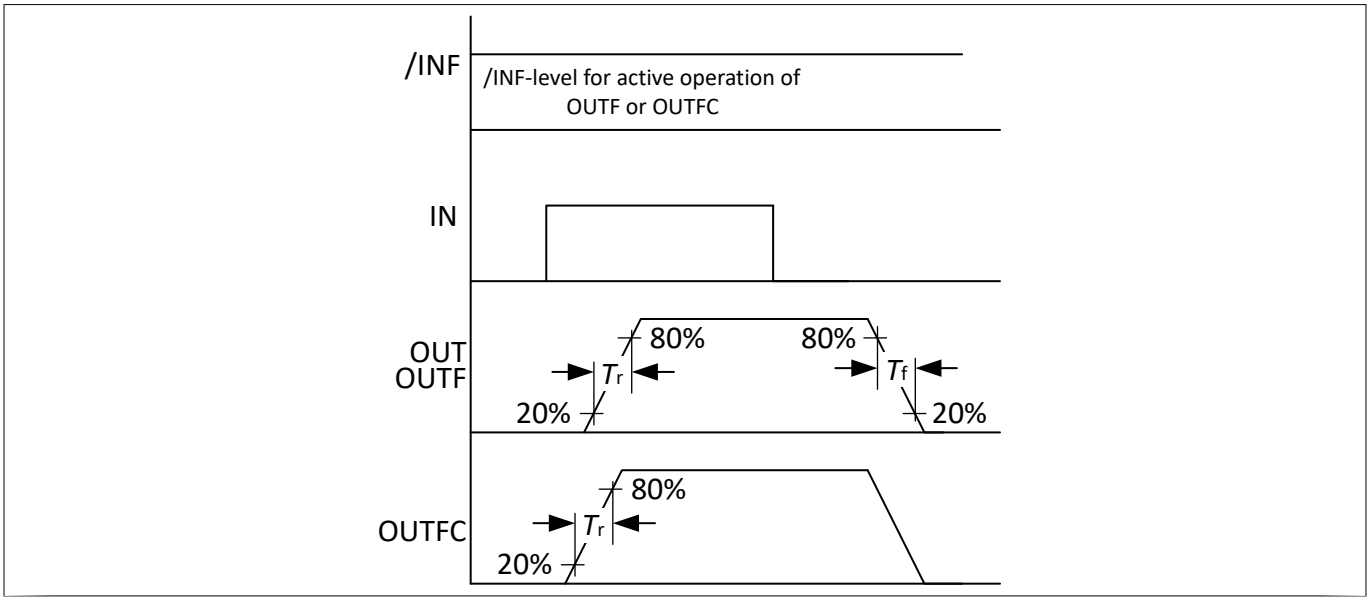

Figure 11 Rise and fall time

Timing diagrams

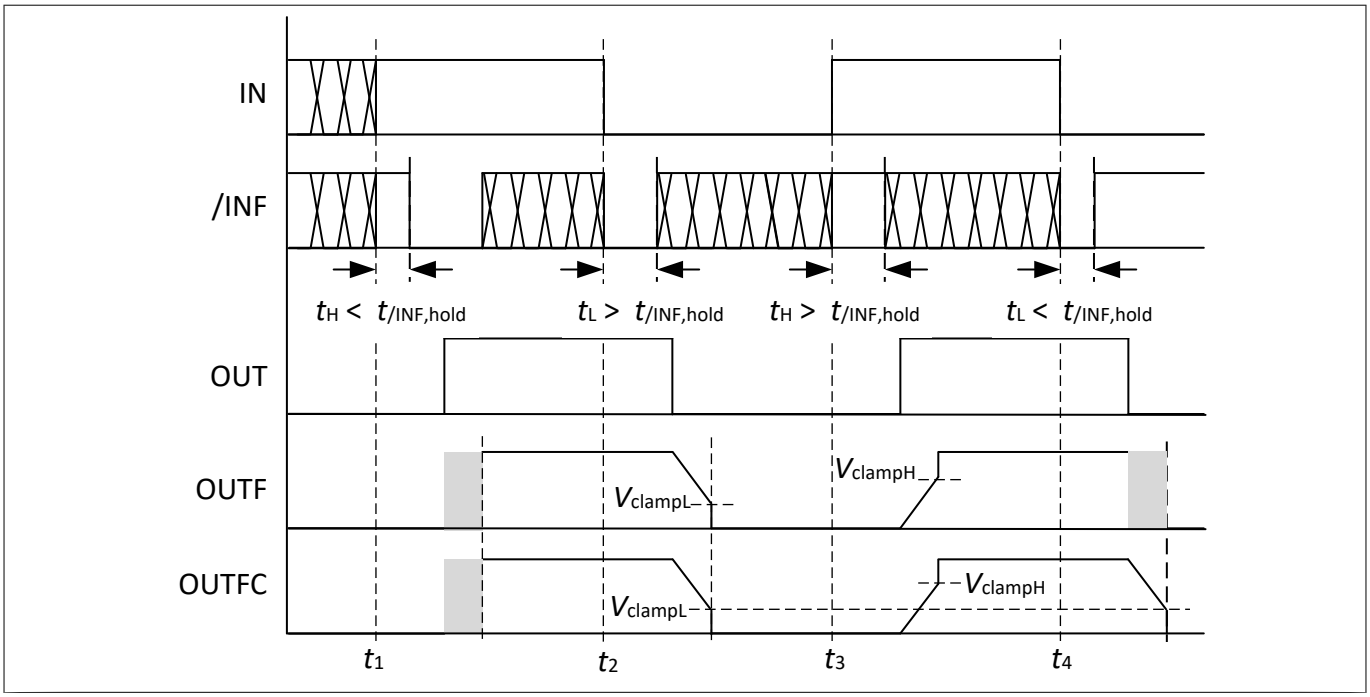

Figure 12 /INF hold time

8 Package dimensions

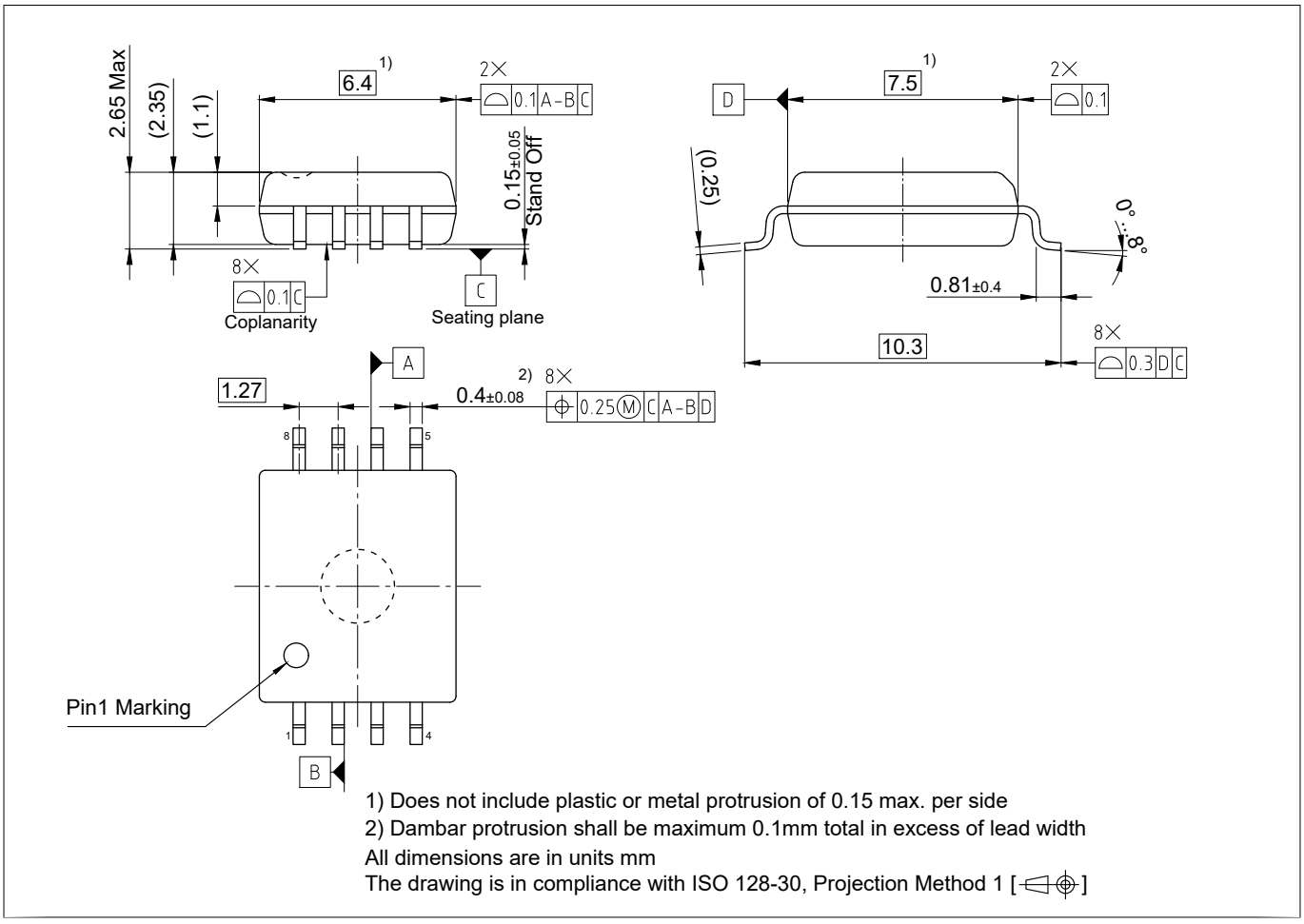

Figure 13 PG-DSO-8-66 (Plastic (green) dual small outline package)

Revision history

Document version	Date of release	Description of changes
2.0	9.4.2021	initial release
	1.9.2021	New version number schema: Target/Preliminary datasheet: 0.XY; Final datasheet: 1.XY
1.10	15.2.2023	Updated feature list and potential applications, corrected caption of fig. 1, updated related products, updated certification status, added marking information, corrected second paragraph of subchapter "Output terminal OUTFC", updated links to Evaluation Boards, corrected fig. 7

Glossary

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