

# Single D Flip Flop

## NL17SZ74

The NL17SZ74 is a high performance, full function Edge triggered D Flip Flop, with all the features of a standard logic device such as the 74LCX74.

### Features

- Designed for 1.65 V to 5.5 V V<sub>CC</sub> Operation
- 2.6 ns t<sub>PD</sub> at V<sub>CC</sub> = 5 V (typ)
- Inputs/Outputs Overvoltage Tolerant up to 5.5 V
- I<sub>OFF</sub> Supports Partial Power Down Protection
- Source/Sink 24 mA at 3.0 V
- Available in US8, UDFN8 and UQFN8 Packages
- Chip Complexity < 100 FETs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

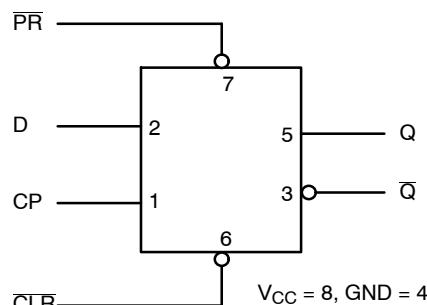


Figure 1. Logic Symbol



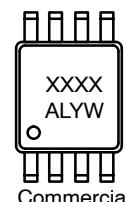
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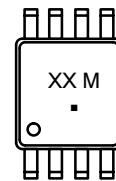
### MARKING DIAGRAMS



US8  
US SUFFIX  
CASE 493



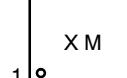
Commercial



NLV Prefix



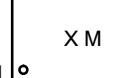
UDFN8, 1.45x1.0  
MU3 SUFFIX  
CASE 517BZ



XM



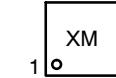
UDFN8, 1.95x1.0  
MU1 SUFFIX  
CASE 517CA



XM



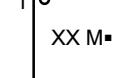
UQFN8, 1.4x1.2  
MQ2 SUFFIX  
CASE 523AS



XM



UQFN8, 1.6x1.6  
MQ1 SUFFIX  
CASE 523AN



XX M-

X, XX, XXXX	= Specific Device Code
A	= Assembly Location
L	= Lot Code
Y	= Year Code
W	= Week Code
M	= Date Code
▪	= Pb-Free Package

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 8 of this data sheet.

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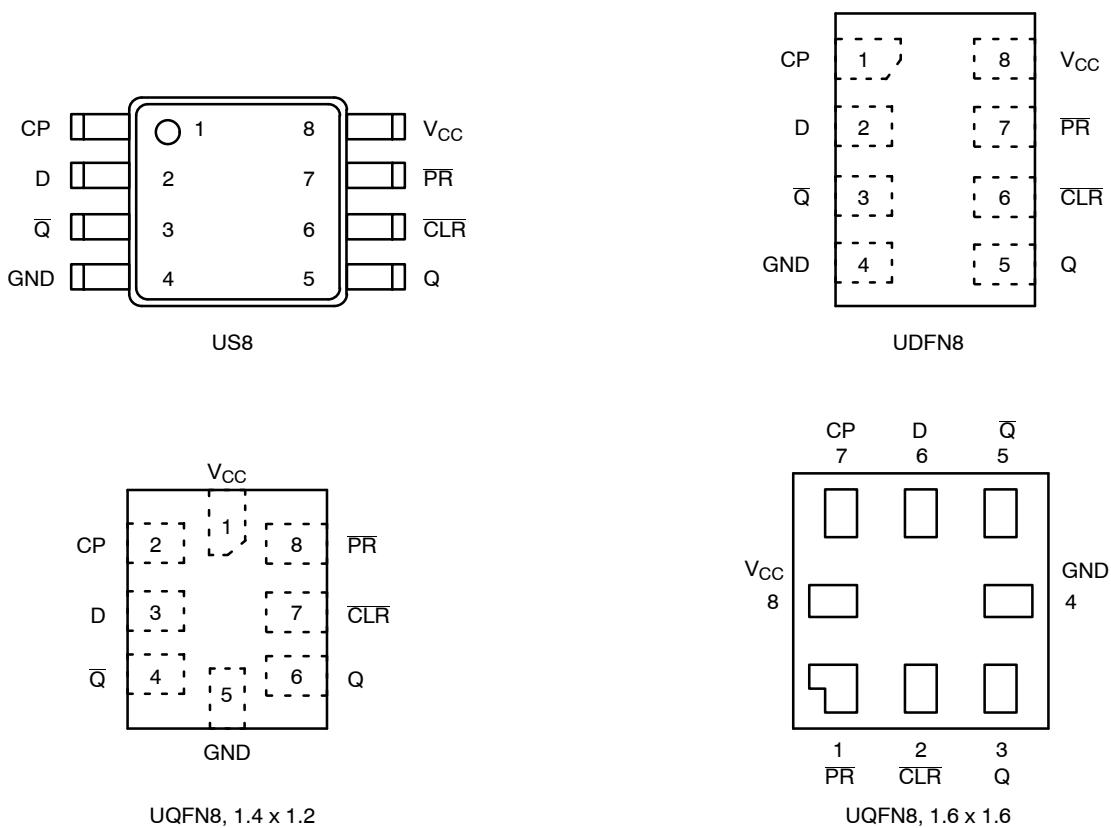


Figure 2. Pinout (Top View)

## PIN ASSIGNMENT

Pin	US8	UDFN8	UQFN8, 1.4x1.2	UQFN8, 1.6x1.6
1	CP	CP	V <sub>CC</sub>	PR
2	D	D	CP	CLR
3	Q	Q	D	Q
4	GND	GND	Q	GND
5	Q	Q	GND	Q
6	CLR	CLR	Q	D
7	PR	PR	CLR	CP
8	V <sub>CC</sub>	V <sub>CC</sub>	PR	V <sub>CC</sub>

## FUNCTION TABLE

Inputs				Outputs		Operating Mode
PR	CLR	CP	D	Q	Q̄	
L	H	X	X	H	L	Asynchronous Set
H	L	X	X	L	H	Asynchronous Clear
L	L	X	X	H	H	Underdetermined
H	H	↑	h	H	L	Load and Read Register
H	H	↑	I	L	H	
H	H	†	X	NC	NC	Hold

H = High Voltage Level

h = High Voltage Level One Setup Time Prior to Low-to-High Clock Transition

L = Low Voltage Level

I = Low Voltage Level One Setup Time Prior to Low-to-High Clock Transition

NC = No Change

X = High or Low Voltage Level and Transitions are Acceptable

↑ = Low-to-High Transition

† = Low-to-High Transition

For I<sub>CC</sub> reasons, DO NOT FLOAT Inputs

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## MAXIMUM RATINGS

Symbol	Characteristics	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	NLV −0.5 to +7.0 −0.5 to +6.5	V
V <sub>IN</sub>	DC Input Voltage	NLV −0.5 to +7.0 −0.5 to +6.5	V
V <sub>OUT</sub>	DC Output Voltage (NLV) Active–Mode (High or Low State) Tri–State Mode (Note 6) Power–Down Mode (V <sub>CC</sub> = 0 V)	−0.5 to V <sub>CC</sub> + 0.5 −0.5 to +7.0 −0.5 to +7.0	V
	DC Output Voltage Active–Mode (High or Low State) Tri–State Mode (Note 6) Power–Down Mode (V <sub>CC</sub> = 0 V)	−0.5 to V <sub>CC</sub> + 0.5 −0.5 to +6.5 −0.5 to +6.5	V
I <sub>IK</sub>	DC Input Diode Current V <sub>IN</sub> < GND	−50	mA
I <sub>OK</sub>	DC Output Diode Current V <sub>OUT</sub> < GND	−50	mA
I <sub>OUT</sub>	DC Output Source/Sink Current	±50	mA
I <sub>CC</sub> or I <sub>GND</sub>	DC Supply Current per Supply Pin or Ground Pin	±100	mA
T <sub>STG</sub>	Storage Temperature Range	−65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 secs	260	°C
T <sub>J</sub>	Junction Temperature Under Bias	+150	°C
θ <sub>JA</sub>	Thermal Resistance (Note 7) US8 UQFN8 UDFN8	250 210 231	°C/W
P <sub>D</sub>	Power Dissipation in Still Air US8 UQFN8 UDFN8	500 595 541	mW
MSL	Moisture Sensitivity	Level 1	—
F <sub>R</sub>	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in
V <sub>ESD</sub>	ESD Withstand Voltage (Note 8) Human Body Model Charged Device Model	2000 1000	V
I <sub>Latchup</sub>	Latchup Performance (Note 9)	±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Applicable to devices with outputs that may be tri–stated.
- Measured with minimum pad spacing on an FR4 board, using 10mm–by–1inch, 2 ounce copper trace no air flow per JESD51–7.
- HBM tested to ANSI/ESDA/JEDEC JS–001–2017. CDM tested to EIA/JESD22–C101–F. JEDEC recommends that ESD qualification to EIA/JESD22–A115–A (Machine Model) be discontinued per JEDEC/JEP172A.
- Tested to EIA/JESD78 Class II.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V <sub>CC</sub>	Positive DC Supply Voltage	1.65	5.5	V
V <sub>IN</sub>	DC Input Voltage	0	5.5	V
V <sub>OUT</sub>	DC Output Voltage Active–Mode (High or Low State) Tri–State Mode (Note 6) Power–Down Mode (V <sub>CC</sub> = 0 V)	0 0 0	V <sub>CC</sub> 5.5 5.5	
T <sub>A</sub>	Operating Temperature Range	−55	+125	°C
	Input Rise and Fall Time V <sub>CC</sub> = 1.65 V to 1.95 V V <sub>CC</sub> = 2.3 V to 2.7 V V <sub>CC</sub> = 3.0 V to 3.6 V V <sub>CC</sub> = 4.5 V to 5.5 V	0 0 0 0	20 20 10 5	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			-55°C ≤ T <sub>A</sub> ≤ 125°C		Units
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	High-Level Input Voltage		1.65 to 1.95	0.65 V <sub>CC</sub>	–	–	0.65 V <sub>CC</sub>	–	V
			2.3 to 5.5	0.70 V <sub>CC</sub>	–	–	0.70 V <sub>CC</sub>	–	
V <sub>IL</sub>	Low-Level Input Voltage		1.65 to 1.95	–	–	0.35 V <sub>CC</sub>	–	0.35 V <sub>CC</sub>	V
			2.3 to 5.5	–	–	0.30 V <sub>CC</sub>	–	0.30 V <sub>CC</sub>	
V <sub>OH</sub>	High-Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -100 µA I <sub>OH</sub> = -4 mA I <sub>OH</sub> = -8 mA I <sub>OH</sub> = -12 mA I <sub>OH</sub> = -16 mA I <sub>OH</sub> = -24 mA I <sub>OH</sub> = -32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 3.0 4.5	V <sub>CC</sub> – 0.1 1.29 1.4 2.1 2.2 2.4 2.7 3.8	V <sub>CC</sub> – – – – – – –	– – – – – – – –	V <sub>CC</sub> – 0.1 1.29 1.9 2.2 2.4 2.7 3.8	– – – – – – – –	V
V <sub>OL</sub>	Low-Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 100 µA I <sub>OL</sub> = 4 mA I <sub>OL</sub> = 8 mA I <sub>OL</sub> = 12 mA I <sub>OL</sub> = 16 mA I <sub>OL</sub> = 24 mA I <sub>OL</sub> = 32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 3.0 4.5	– – – – – – – –	– 0.08 0.2 0.22 0.28 0.38 0.42	0.1 0.24 0.3 0.4 0.4 0.55 0.55	– – – – – – –	0.1 0.24 0.3 0.4 0.4 0.55 0.55	V
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = 5.5 V or GND	1.65 to 5.5	–	–	±0.1	–	±1.0	µA
I <sub>OFF</sub>	Power Off Leakage Current	V <sub>IN</sub> = 5.5 V or V <sub>OUT</sub> = 5.5 V	0	–	–	1.0	–	10	µA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	–	–	1.0	–	10	µA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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## AC ELECTRICAL CHARACTERISTICS

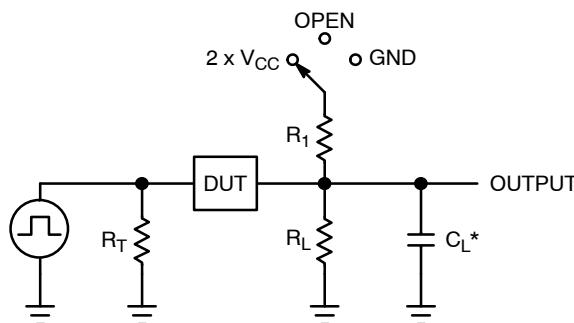
Symbol	Parameter	V <sub>CC</sub> (V)	Test Conditions	T <sub>A</sub> = 25°C			T <sub>A</sub> = -55 to 125°C		Units
				Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency (50% Duty Cycle) (Waveform 1)	1.65 to 1.95	C <sub>L</sub> = 15 pF R <sub>L</sub> = 1 MΩ S <sub>1</sub> = Open	75	-	-	75	-	MHz
		2.3 to 2.7		150	-	-	150	-	
		3.0 to 3.6		200	-	-	200	-	
		4.5 to 5.5		250	-	-	250	-	
		3.0 to 3.6	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, S <sub>1</sub> = Open	175	-	-	175	-	
		4.5 to 5.5		200	-	-	200	-	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, CP to Q or $\bar{Q}$ (Waveform 1)	1.65 to 1.95	C <sub>L</sub> = 15 pF R <sub>L</sub> = 1 MΩ S <sub>1</sub> = Open	-	6.5	12.5	-	13	ns
		2.3 to 2.7		-	3.8	7.5	-	8.0	
		3.0 to 3.6		-	2.8	6.5	-	7.0	
		4.5 to 5.5		-	2.2	4.5	-	5.0	
		3.0 to 3.6	C <sub>L</sub> = 50 pF, R <sub>D</sub> = 500 Ω, S <sub>1</sub> = Open	-	3.4	7.0	-	7.5	
		4.5 to 5.5		-	2.6	5.0	-	5.5	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, $\bar{P}R$ or CLR to Q or $\bar{Q}$ (Waveform 2)	1.65 to 1.95	C <sub>L</sub> = 15 pF R <sub>L</sub> = 1 MΩ S <sub>1</sub> = Open	-	6.5	14	-	14.5	ns
		2.3 to 2.7		-	3.8	9.0	-	9.5	
		3.0 to 3.6		-	2.8	6.5	-	7.0	
		4.5 to 5.5		-	2.2	5.0	-	5.5	
		3.0 to 3.6	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, S <sub>1</sub> = Open	-	3.4	7.0	-	7.5	
		4.5 to 5.5		-	2.6	5.0	-	5.5	
t <sub>S</sub>	Setup Time, D to CP (Waveform 1)	1.65 to 1.95	C <sub>L</sub> = 15 pF R <sub>L</sub> = 1 MΩ S <sub>1</sub> = Open	6.5	-	-	6.5	-	ns
		2.3 to 2.7		3.5	-	-	3.5	-	
		3.0 to 3.6		2.0	-	-	2.0	-	
		4.5 to 5.5		1.5	-	-	1.5	-	
		3.0 to 3.6	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, S <sub>1</sub> = Open	2.0	-	-	2.0	-	
		4.5 to 5.5		1.5	-	-	1.5	-	
t <sub>H</sub>	Hold Time, D to CP (Waveform 1)	1.65 to 1.95	C <sub>L</sub> = 15 pF R <sub>L</sub> = 1 MΩ S <sub>1</sub> = Open	0.5	-	-	0.5	-	ns
		2.3 to 2.7		0.5	-	-	0.5	-	
		3.0 to 3.6		0.5	-	-	0.5	-	
		4.5 to 5.5		0.5	-	-	0.5	-	
		3.0 to 3.6	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, S <sub>1</sub> = Open	0.5	-	-	0.5	-	
		4.5 to 5.5		0.5	-	-	0.5	-	
t <sub>W</sub>	Pulse Width, CP, CLR, $\bar{P}R$ (Waveform 3)	1.65 to 1.95	C <sub>L</sub> = 15 pF R <sub>L</sub> = 1 MΩ S <sub>1</sub> = Open	6.0	-	-	6.0	-	ns
		2.3 to 2.7		4.0	-	-	4.0	-	
		3.0 to 3.6		3.0	-	-	3.0	-	
		4.5 to 5.5		2.0	-	-	2.0	-	
		3.0 to 3.6	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, S <sub>1</sub> = Open	3.0	-	-	3.0	-	
		4.5 to 5.5		2.0	-	-	2.0	-	
t <sub>REC</sub>	Recover Time $\bar{P}R$ ; CLR to CP (Waveform 3)	1.65 to 1.95	C <sub>L</sub> = 15 pF R <sub>D</sub> = 1 MΩ S <sub>1</sub> = Open	8.0	-	-	8.0	-	ns
		2.3 to 2.7		4.5	-	-	4.5	-	
		3.0 to 3.6		3.0	-	-	3.0	-	
		4.5 to 5.5		3.0	-	-	3.0	-	
		3.0 to 3.6	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, S <sub>1</sub> = Open	3.0	-	-	3.0	-	
		4.5 to 5.5		3.0	-	-	3.0	-	

5. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/2 (per flip-flop). C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
$C_{IN}$	Input Capacitance	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 0 \text{ V}$ or $V_{CC}$	2.5	pF
$C_{OUT}$	Output Capacitance	$V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 0 \text{ V}$ or $V_{CC}$	2.5	pF
$C_{PD}$	Power Dissipation Capacitance (Note 6)	10 MHz, $V_{CC} = 3.3 \text{ V}$ , $V_{IN} = 0 \text{ V}$ or $V_{CC}$ 10 MHz, $V_{CC} = 5.5 \text{ V}$ , $V_{IN} = 0 \text{ V}$ or $V_{CC}$	9 11	pF

6.  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$ .  $C_{PD}$  is used to determine the no-load dynamic power consumption;  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$ .



$C_L$  includes probe and jig capacitance

$R_T$  is  $Z_{OUT}$  of pulse generator (typically 50  $\Omega$ )  
 $f = 1 \text{ MHz}$

Figure 3. Test Circuit

Test	Switch Position	$C_L, \text{ pF}$	$R_L, \Omega$	$R_1, \Omega$
$t_{PLH} / t_{PHL}$	Open	See AC Characteristics Table		
$t_{PLZ} / t_{PZL}$	$2 \times V_{CC}$	50	500	500
$t_{PHZ} / t_{PZH}$	GND	50	500	500

X = Don't Care

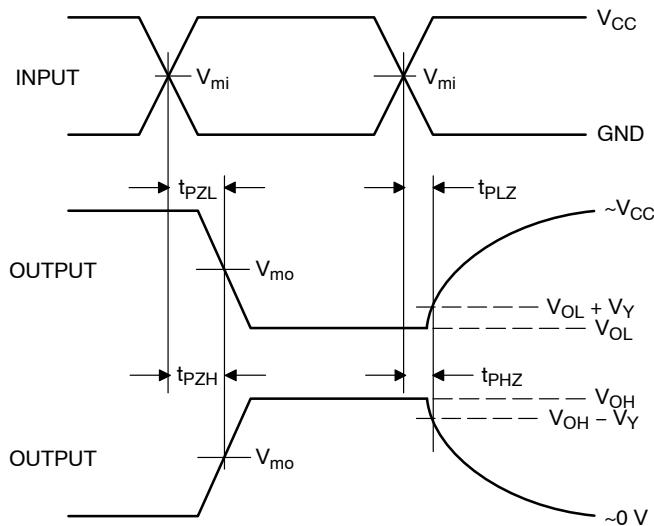
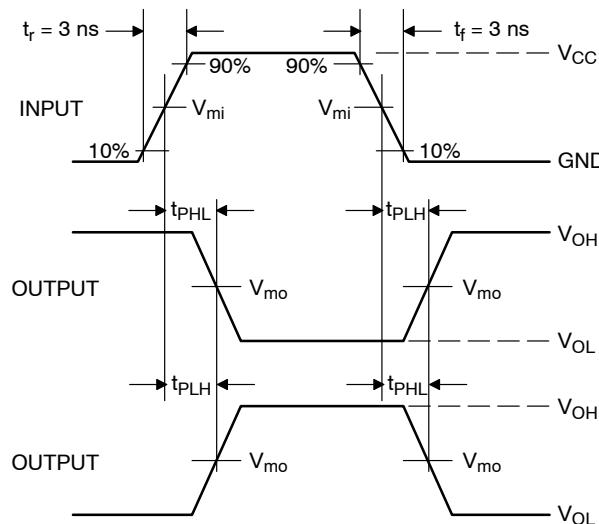


Figure 4. Switching Waveforms

# NL17SZ74

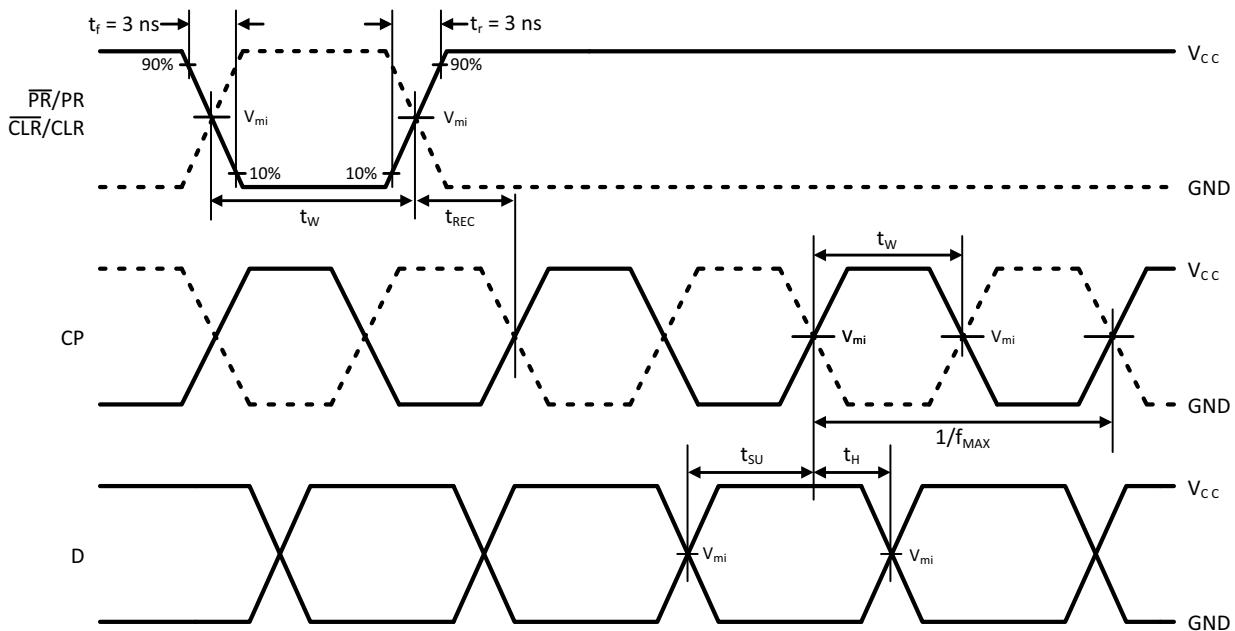


Figure 5. Setup, Hold and Recovery Time Waveforms

V <sub>CC</sub> , V	V <sub>mi</sub> , V	V <sub>mo</sub> , V		V <sub>Y</sub> , V
		t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub> , t <sub>PZH</sub> , t <sub>PHZ</sub>	
1.65 to 1.95	V <sub>CC</sub> /2	V <sub>CC</sub> /2	V <sub>CC</sub> /2	0.15
2.3 to 2.7	V <sub>CC</sub> /2	V <sub>CC</sub> /2	V <sub>CC</sub> /2	0.15
3.0 to 3.6	V <sub>CC</sub> /2	V <sub>CC</sub> /2	V <sub>CC</sub> /2	0.3
4.5 to 5.5	V <sub>CC</sub> /2	V <sub>CC</sub> /2	V <sub>CC</sub> /2	0.3

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## DEVICE ORDERING INFORMATION

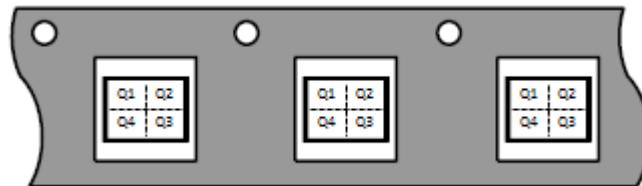
Device	Packages	Marking	Pin 1 Orientation (See below)	Shipping <sup>†</sup>
NL17SZ74USG	US8	MH	Q4	3000 / Tape & Reel
NLV17SZ74USG*	US8	MH	Q4	3000 / Tape & Reel
NL17SZ74MQ1TCG	UQFN8, 1.6 x 1.6, 0.5P	AA	Q1	3000 / Tape & Reel
NLV17SZ74MQ1TCG* (In Development)	UQFN8, 1.6 x 1.6, 0.5P	AA	Q1	3000 / Tape & Reel
NL17SZ74MU1TCG (In Development)	UDFN8, 1.95 x 1.0, 0.5P	TBD	Q4	3000 / Tape & Reel
NL17SZ74MU3TCG (In Development)	UDFN8, 1.45 x 1.0, 0.35P	TBD	Q4	3000 / Tape & Reel
NL17SZ74MQ2TCG (In Development)	UQFN8, 1.4 x 1.2, 0.4P	TBD	TBD	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

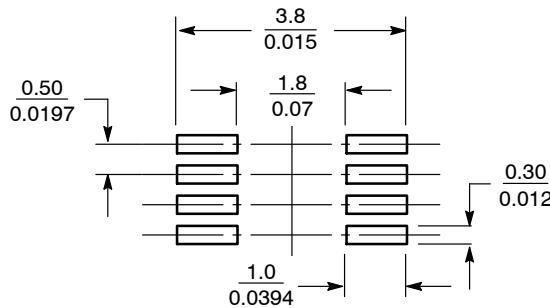
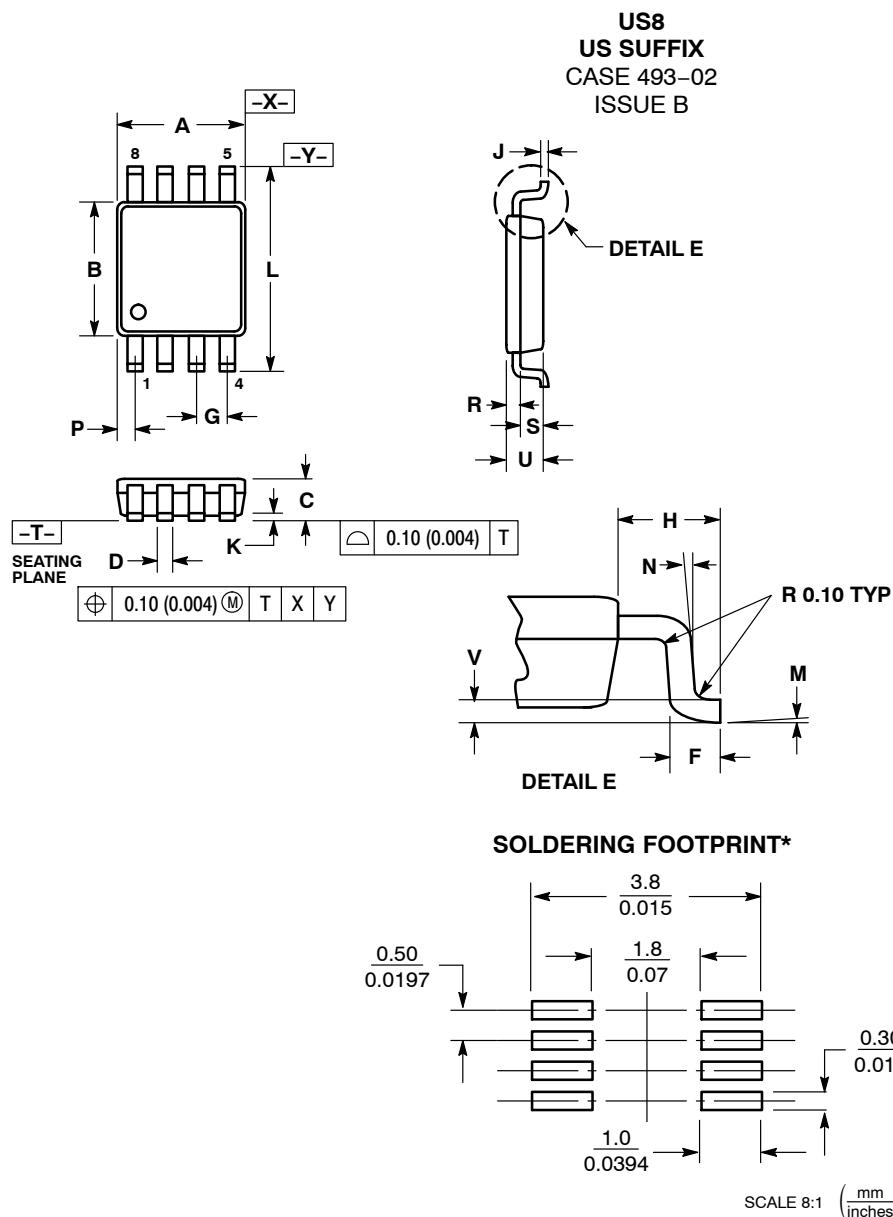
\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

## Pin 1 Orientation in Tape and Reel

### Direction of Feed



## PACKAGE DIMENSIONS



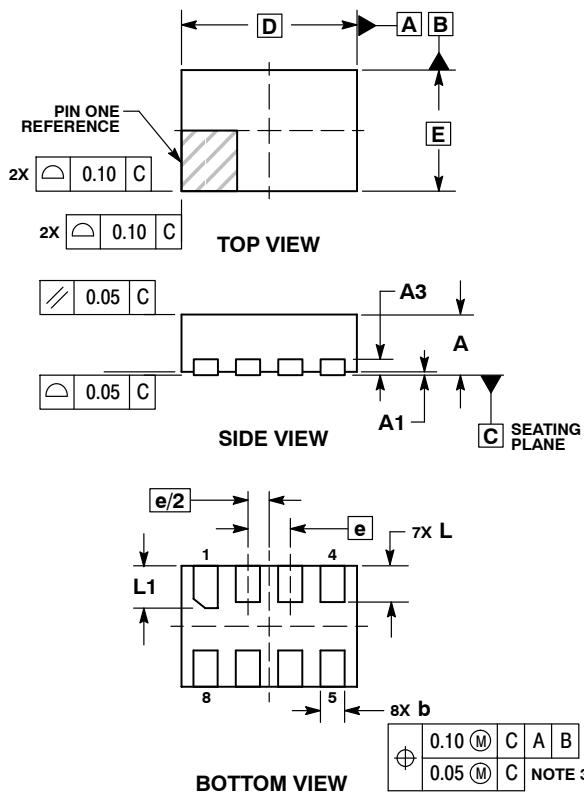
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

UDFN8, 1.45x1, 0.35P

CASE 517BZ

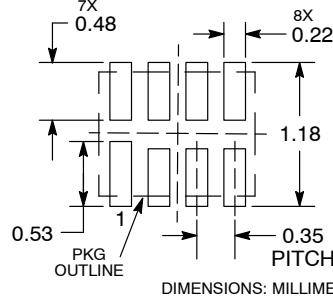
ISSUE O



## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

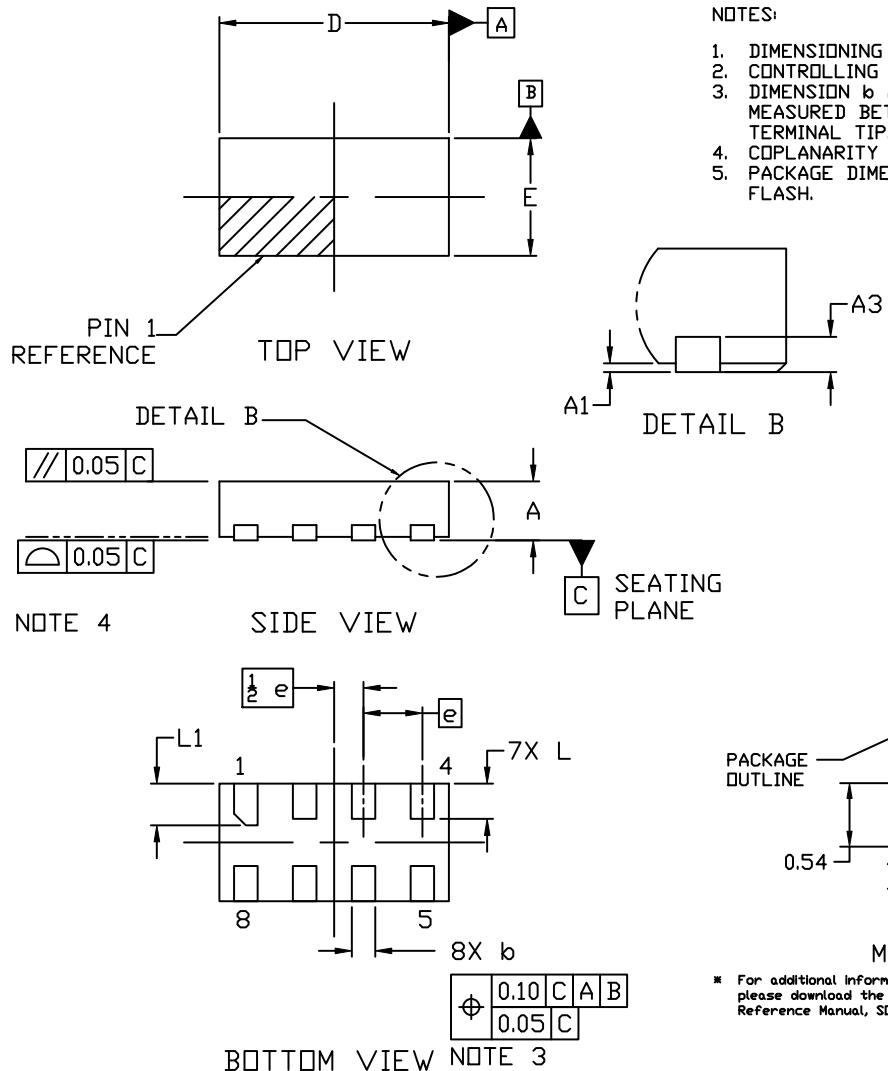
DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	1.45 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

RECOMMENDED  
SOLDERING FOOTPRINT\*

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

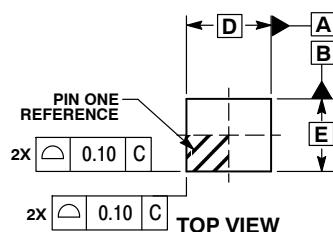
## PACKAGE DIMENSIONS

UDFN8, 1.95x1.0, 0.5P

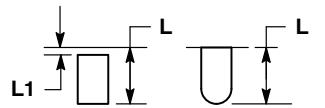
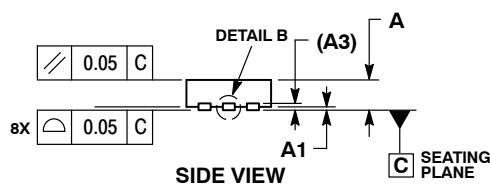
CASE 517CA  
ISSUE A

## PACKAGE DIMENSIONS

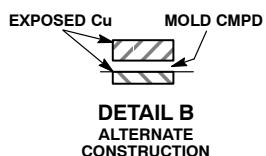
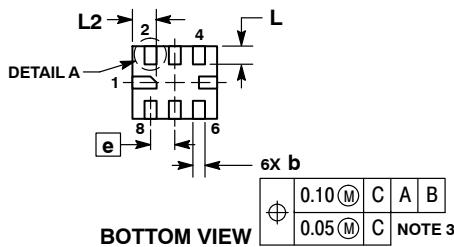
**UQFN8, 1.4x1.2, 0.4P**  
**CASE 523AS**  
**ISSUE A**



TOP VIEW

DETAIL A  
ALTERNATE CONSTRUCTIONS

SIDE VIEW

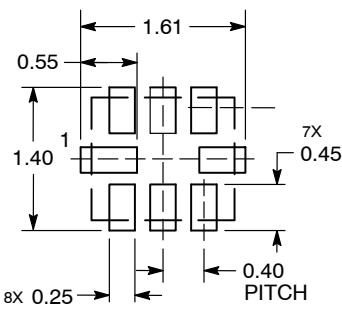
DETAIL B  
ALTERNATE CONSTRUCTION

BOTTOM VIEW

NOTES:  
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.  
2. CONTROLLING DIMENSION: MILLIMETERS.  
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 mm FROM THE TERMINAL TIP.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	1.40 BSC	
E	1.20 BSC	
e	0.40 BSC	
L	0.20	0.40
L1	---	0.15
L2	0.30	0.50

## SOLDERING FOOTPRINT\*

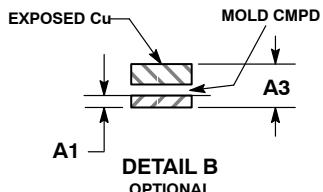
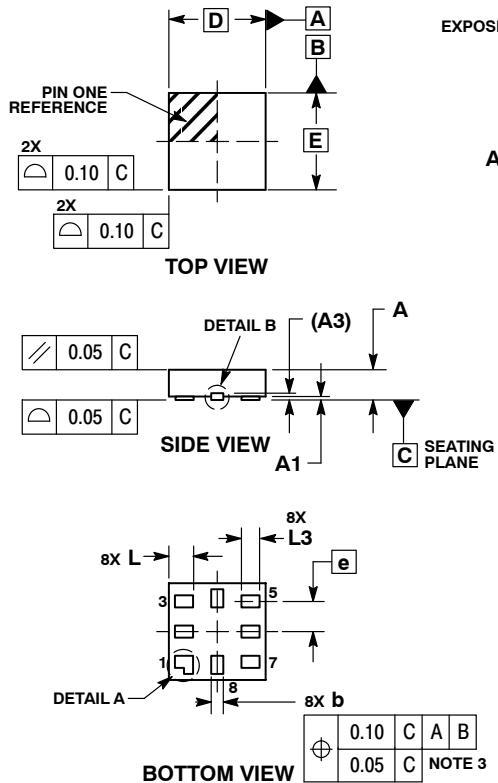


DIMENSIONS: MILLIMETERS

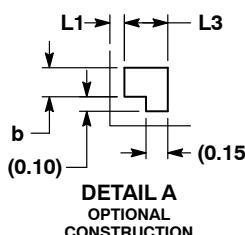
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

**UQFN8, 1.6x1.6, 0.5P**  
**CASE 523AN**  
**ISSUE O**



**DETAIL B**  
**OPTIONAL CONSTRUCTION**



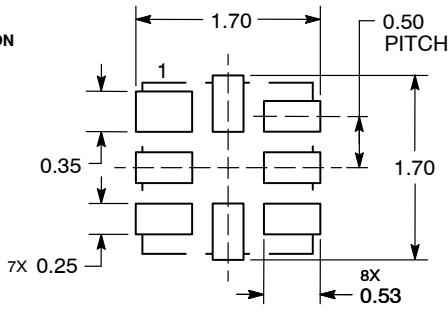
**DETAIL A**  
**OPTIONAL CONSTRUCTION**

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.60
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	1.60 BSC	
E	1.60 BSC	
e	0.50 BSC	
L	0.35	0.45
L1	---	0.15
L3	0.25	0.35

**SOLDERING FOOTPRINT\***



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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