



PRMD10

50 V, 100 mA NPN/PNP Resistor-Equipped double Transistors (RET)

25 August 2025

Product data sheet

1. General description

NPN/PNP Resistor-Equipped double Transistors (RET) in an ultra small DFN1412-6 (SOT1268) leadless Surface-Mounted Device (SMD) plastic package.

NPN/PNP complement: PRMH10.

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- Low package height of 0.5 mm
- AEC-Q101 qualified

3. Applications

- Digital applications
- Cost-saving alternative to BC847/BC857 series in digital applications
- Control of IC inputs
- Switching loads

4. Quick reference data

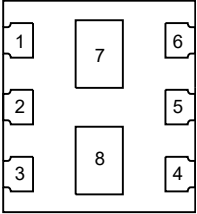
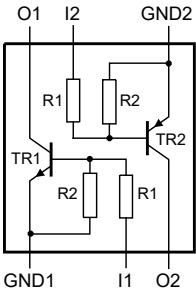
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor, for the PNP transistor with negative polarity						
V_{CEO}	collector-emitter voltage	open base	-	-	50	V
I_O	output current		-	-	100	mA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}; I_C = 10\text{ mA}; T_{amb} = 25\text{ }^{\circ}\text{C}$	100	-	-	
R1	bias resistor 1 (input)	$T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	1.54	2.2	2.86 k Ω
R2/R1	bias resistor ratio		[1]	17	21	26

[1] See section "Test information" for resistor calculation and test conditions.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 Transparent top view DFN1412-6 (SOT1268)	 aaa-007379
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		
7	O1	output (collector) TR1		
8	O2	output (collector) TR2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PRMD10	DFN1412-6	plastic, thin small outline package; no leads; 6 terminals; 1.4 mm x 1.2 mm x 0.47 mm body	SOT1268

7. Marking

Table 4. Marking codes

Type number	Marking code
PRMD10	B5

8. Limiting values

Table 5. Limiting values

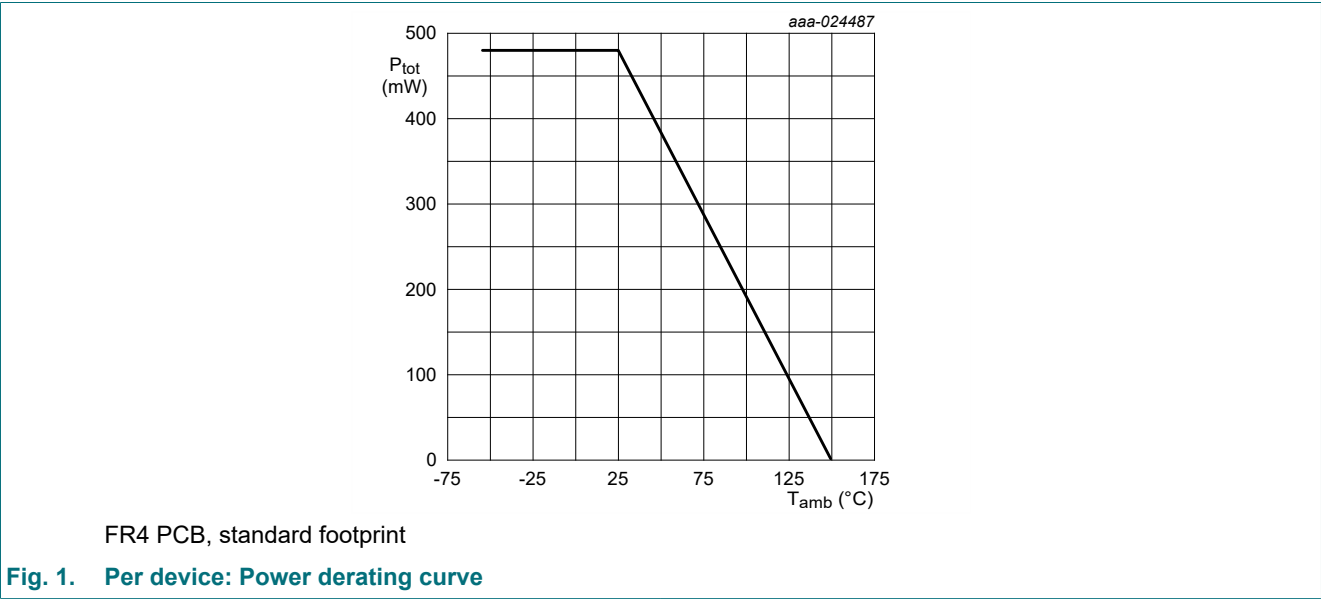
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor, for the PNP transistor with negative polarity						
V _{CBO}	collector-base voltage	open emitter		-	50	V
V _{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector		-	5	V
V _I	input voltage	positive		-	12	V
		negative		-	-5	V
I _O	output current			-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	325	mW
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	480	mW
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C

50 V, 100 mA NPN/PNP Resistor-Equipped double Transistors (RET)

Symbol	Parameter	Conditions		Min	Max	Unit
T _{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

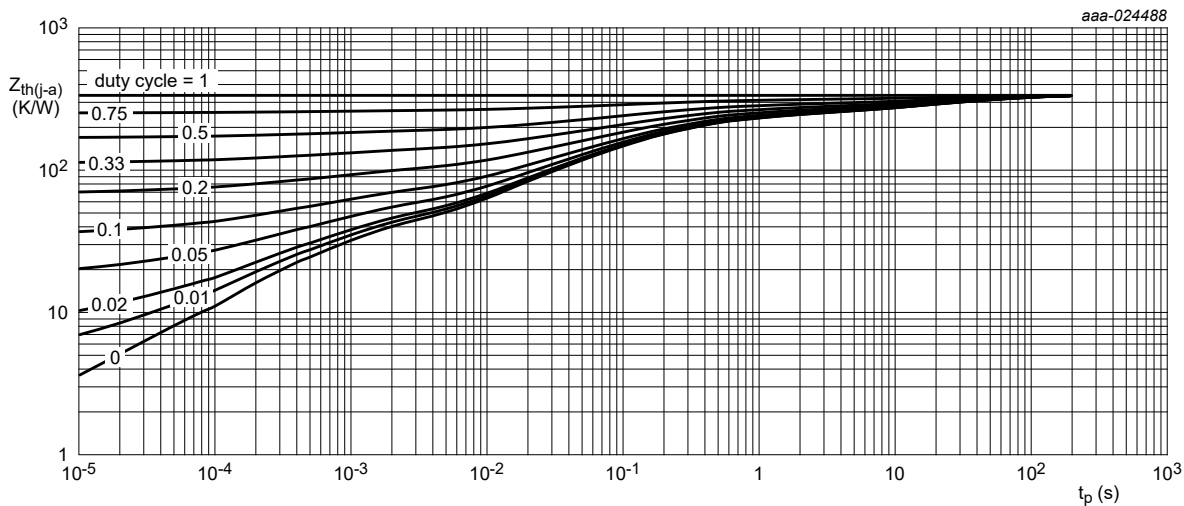


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	385	K/W
Per device							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	261	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



FR4 PCB, standard footprint

Fig. 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor, for the PNP transistor with negative polarity							
I_{CBO}	collector-base cut-off current	$V_{CB} = 50\text{ V}$; $I_E = 0\text{ A}$; $T_{amb} = 25\text{ °C}$		-	-	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30\text{ V}$; $I_B = 0\text{ A}$; $T_{amb} = 25\text{ °C}$		-	-	100	nA
		$V_{CE} = 30\text{ V}$; $I_B = 0\text{ A}$; $T_{amb} = 150\text{ °C}$		-	-	5	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}$; $I_C = 0\text{ A}$; $T_{amb} = 25\text{ °C}$		-	-	180	μA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}$; $I_C = 10\text{ mA}$; $T_{amb} = 25\text{ °C}$		100	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 5\text{ mA}$; $I_B = 0.25\text{ mA}$; $T_{amb} = 25\text{ °C}$		-	-	100	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}$; $I_C = 100\text{ μA}$; $T_{amb} = 25\text{ °C}$		-	0.6	0.5	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}$; $I_C = 5\text{ mA}$; $T_{amb} = 25\text{ °C}$		1.1	0.75	-	V
R1	bias resistor 1 (input)	$T_{amb} = 25\text{ °C}$	[1]	1.54	2.2	2.86	kΩ
R2/R1	bias resistor ratio		[1]	17	21	26	
C_c	collector capacitance	$V_{CB} = 10\text{ V}$; $I_E = 0\text{ A}$; $i_e = 0\text{ A}$; $f = 1\text{ MHz}$; $T_{amb} = 25\text{ °C}$		-	-	2.5	pF
		$V_{CB} = -10\text{ V}$; $I_E = 0\text{ A}$; $i_e = 0\text{ A}$; $f = 1\text{ MHz}$; $T_{amb} = 25\text{ °C}$		-	-	3	pF
f_T	transition frequency	$V_{CE} = 5\text{ V}$; $I_C = 10\text{ mA}$; $f = 100\text{ MHz}$; $T_{amb} = 25\text{ °C}$	[2]	-	230	-	MHz
		$V_{CE} = -5\text{ V}$; $I_C = -10\text{ mA}$; $f = 100\text{ MHz}$; $T_{amb} = 25\text{ °C}$	[2]	-	180	-	MHz

[1] See section "Test information" for resistor calculation and test conditions.
[2] Characteristics of built-in transistor.

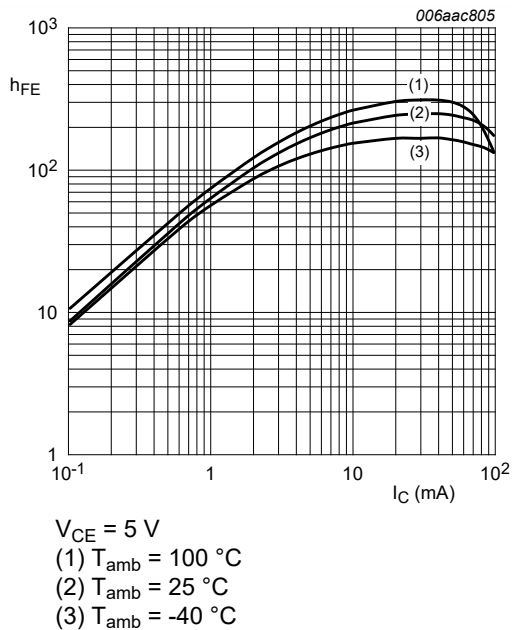


Fig. 3. NPN transistor: DC current gain as a function of collector current; typical values

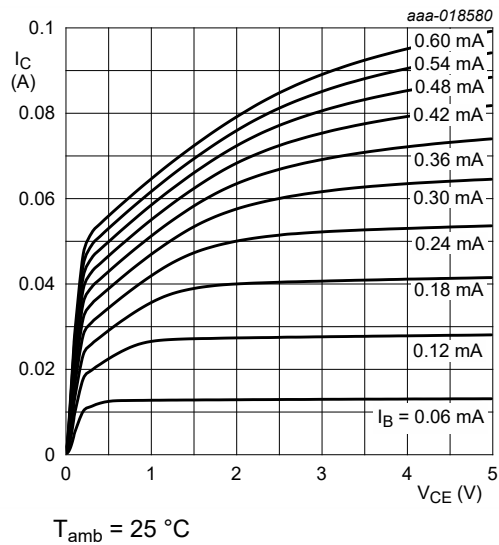


Fig. 4. NPN transistor: Collector current as a function of collector-emitter voltage; typical values

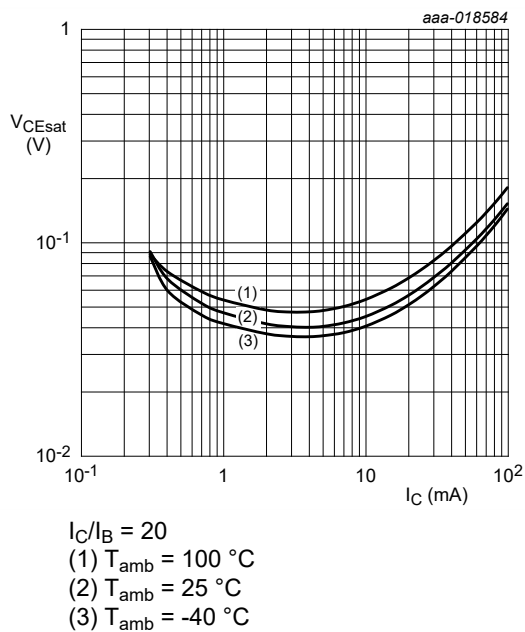


Fig. 5. NPN transistor: Collector-emitter saturation voltage as a function of collector current; typical values

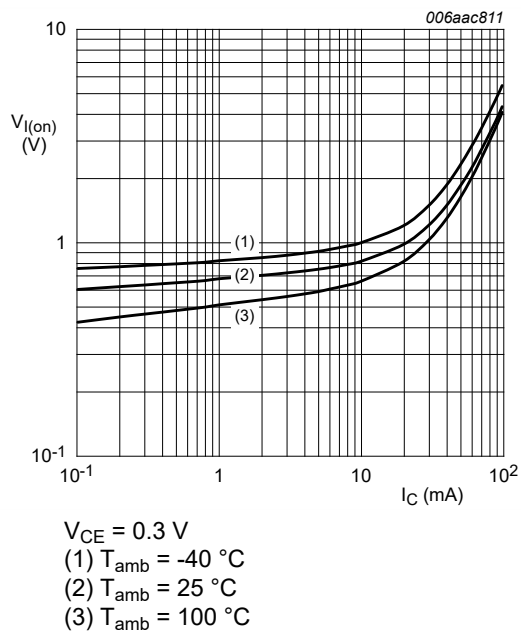


Fig. 6. NPN transistor: On-state input voltage as a function of collector current; typical values

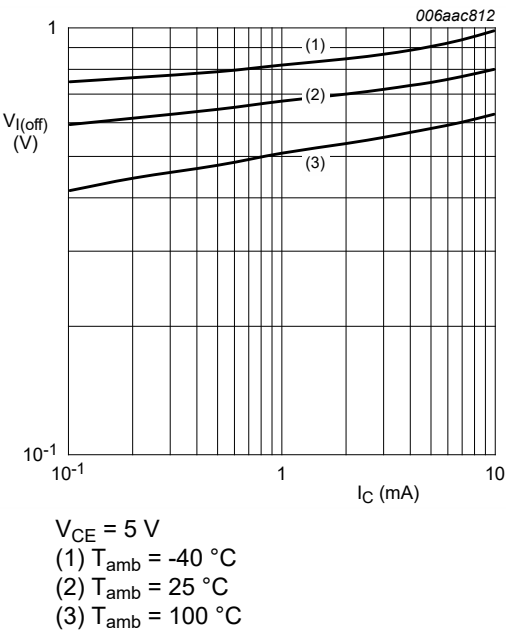


Fig. 7. NPN transistor: Off-state input voltage as a function of collector current; typical values

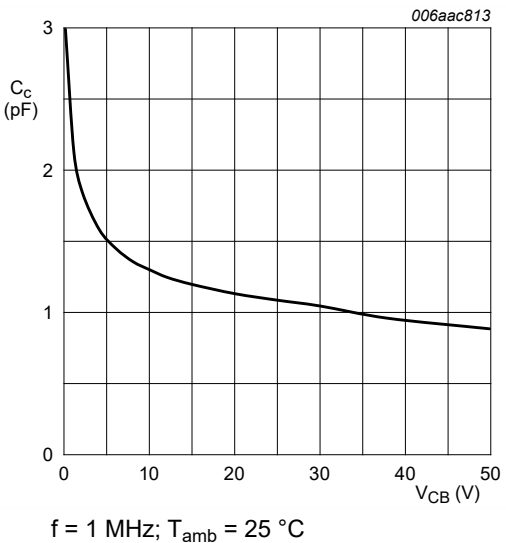


Fig. 8. NPN transistor: Collector capacitance as a function of collector-base voltage; typical values

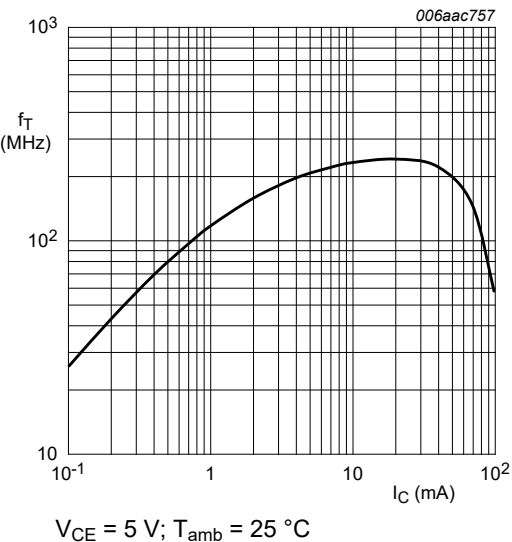


Fig. 9. NPN transistor: Transition frequency as a function of collector current; typical values of built-in transistor

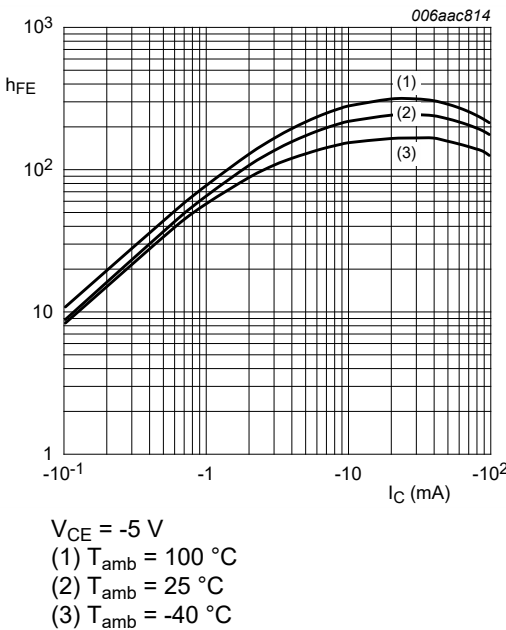


Fig. 10. PNP transistor: DC current gain as a function of collector current; typical values

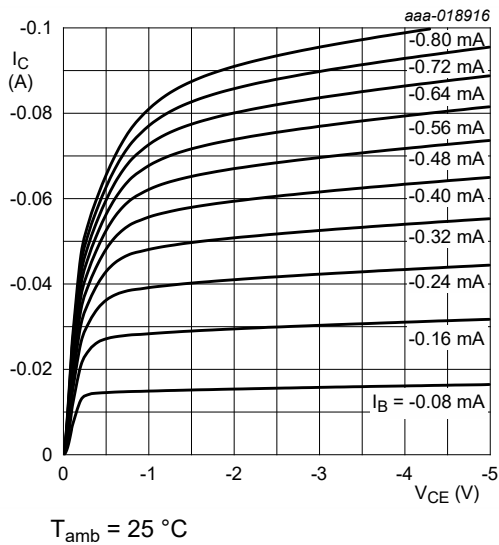


Fig. 11. PNP transistor: Collector current as a function of collector-emitter voltage; typical values

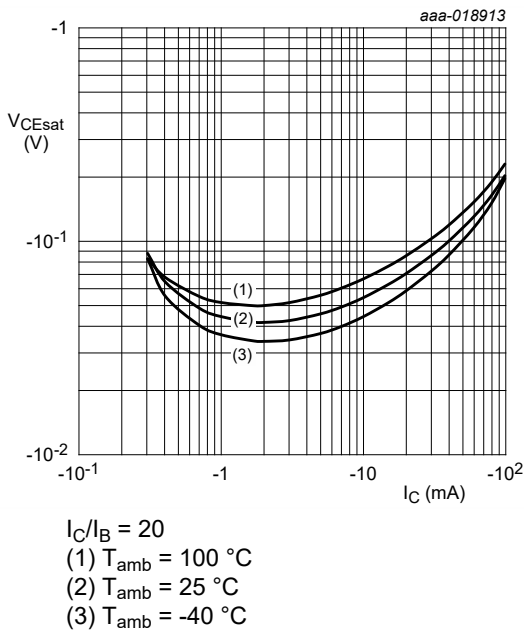


Fig. 12. PNP transistor: Collector-emitter saturation voltage as a function of collector current; typical values

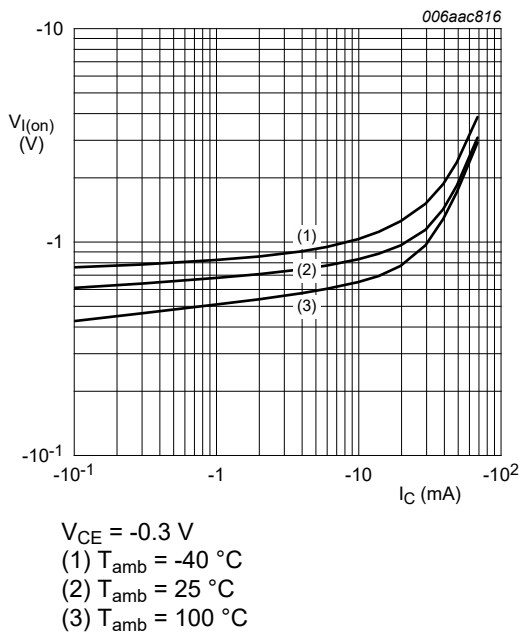


Fig. 13. PNP transistor: On-state input voltage as a function of collector current; typical values

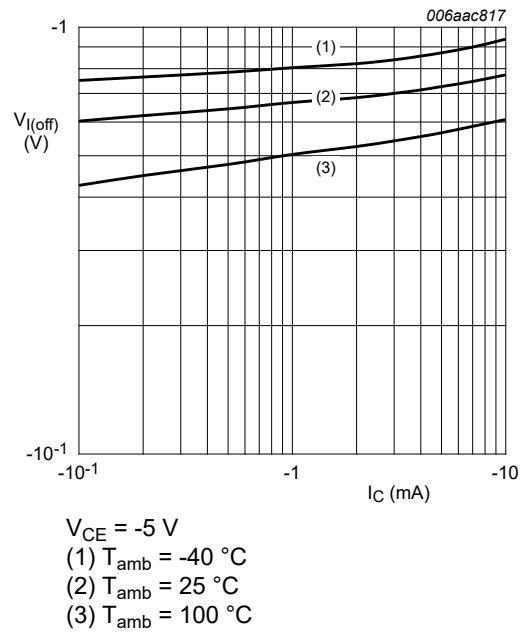
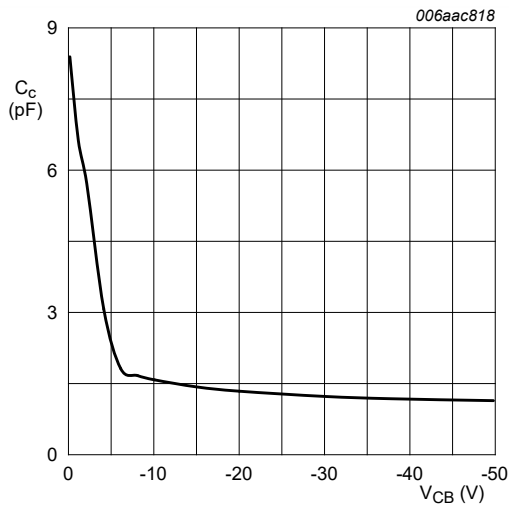
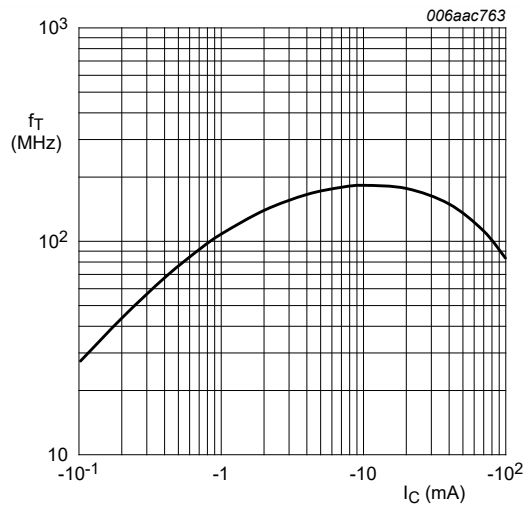


Fig. 14. PNP transistor: Off-state input voltage as a function of collector current; typical values



$f = 1 \text{ MHz}$; $T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$

Fig. 15. PNP transistor: Collector capacitance as a function of collector-base voltage; typical values



$V_{CE} = -5 \text{ V}$; $T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$

Fig. 16. PNP transistor: Transition frequency as a function of collector current; typical values of built-in transistor

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

Resistor calculation

- Calculation of bias resistor 1 (R_1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R_2/R_1)

$$\frac{R_2}{R_1} = \frac{V(I_4) - V(I_3)}{R_1 \cdot (I_4 - I_3)} - 1$$

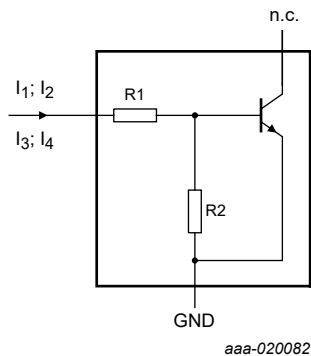
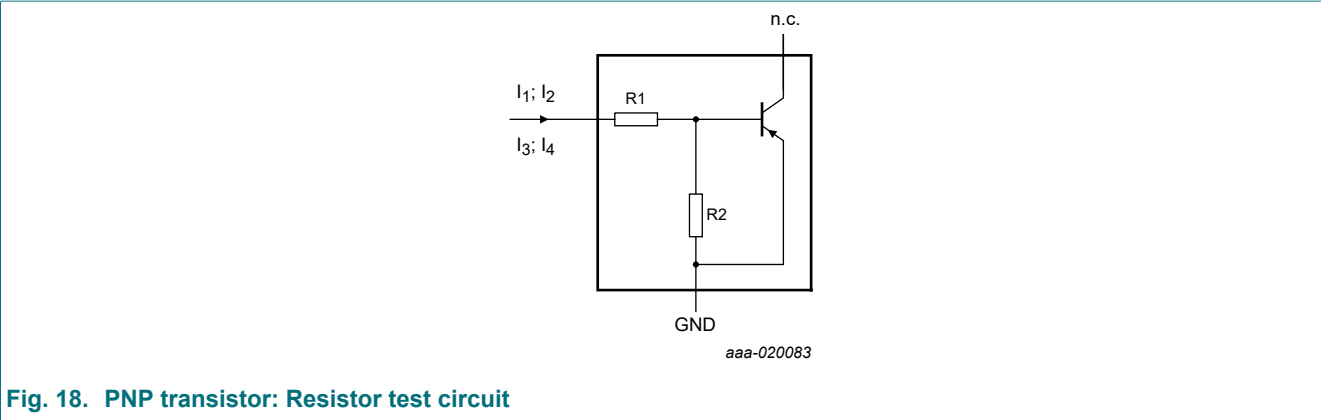


Fig. 17. NPN transistor: Resistor test circuit

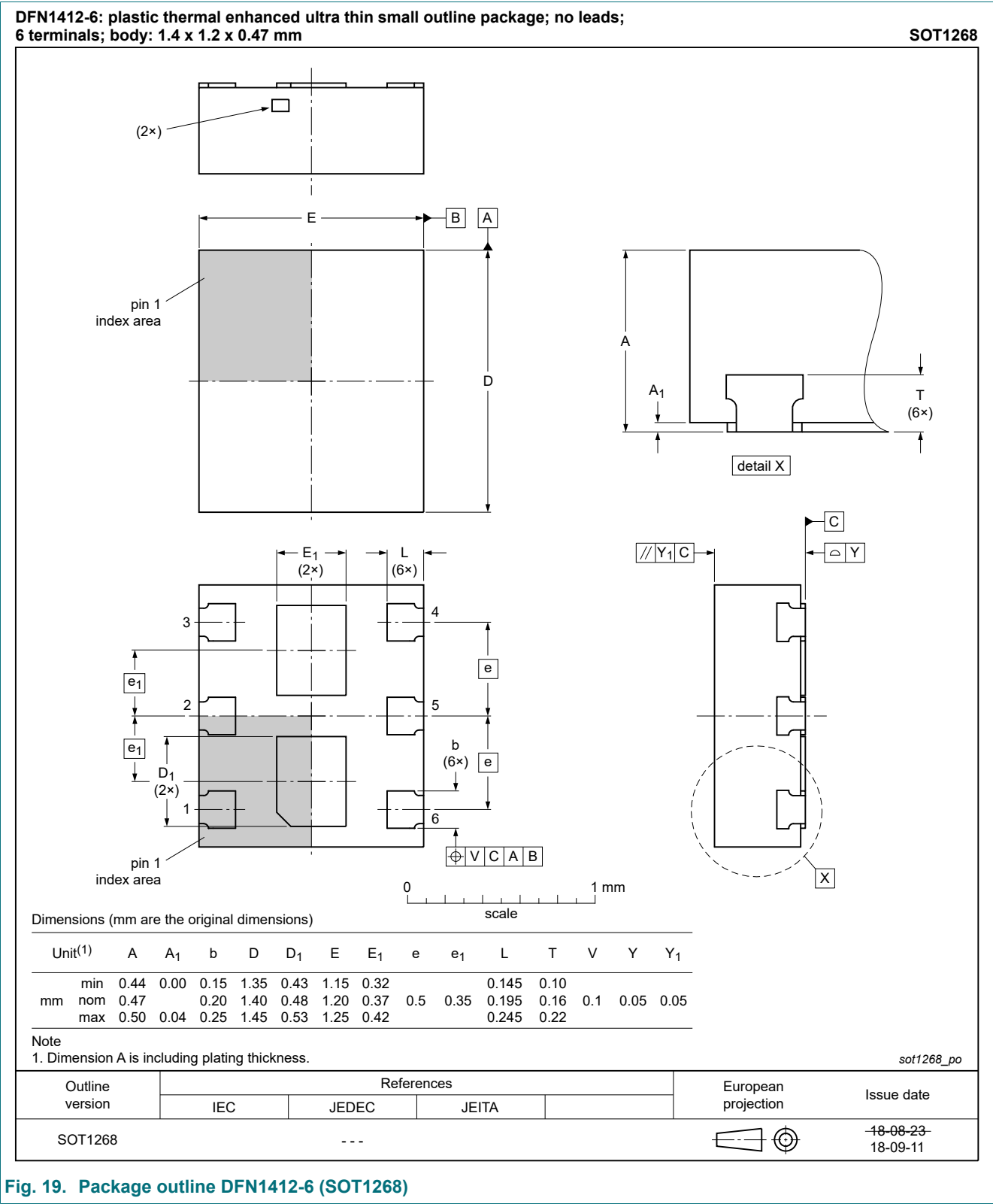


Resistor test conditions

Table 8. Resistor test conditions

Product	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I ₁	I ₂	I ₃	I ₄
TR1 (NPN)	2.2	47	90 μA	140 μA	-55 μA	-105 μA
TR2 (PNP)	2.2	47	-90 μA	-140 μA	55 μA	105 μA

12. Package outline



13. Soldering

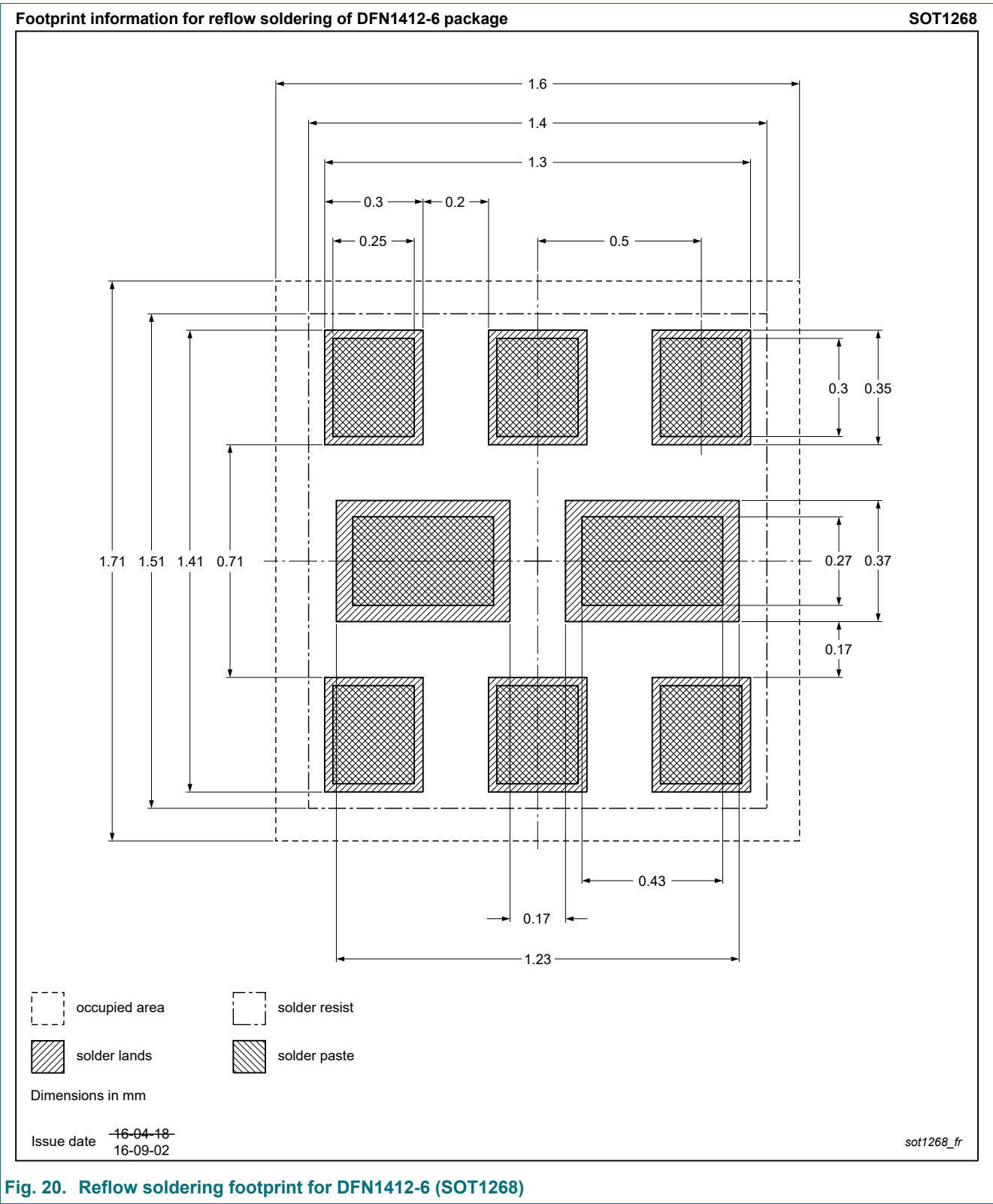


Fig. 20. Reflow soldering footprint for DFN1412-6 (SOT1268)

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PRMD10 v.3	2025mmdd	Product data sheet	-	PRMD10 v.2
Modifications:	• Characteristics: Graph 006aac816 of Fig 13 changed			
PRMD10 v.2	20180914	Product data sheet	-	PRMD10 v.1
PRMD10 v.1	20170627	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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