REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Made changes to Table IA, parameters: I_{DDDOP3} , I_{DDDOP1}, $I_{DDDOPW1}$, $I_{DDOPW40}$, $I_{DDDOPW40}$, I_{DDOPR1}, $I_{DDDOPR1}$, $I_{DDOPR40}$, $I_{DDDOPR40}$, C_{INA}, C_{INC}. ksr	08-12-12	Robert M. Heber
B	Made changes to Table IA, parameters: Standby current CS disabled (I_{DDSB2}), from 25mA to 30 mA, and Standby current enabled (I_{DDSB}) from 25 mA to 30 mA. ksr	09-07-17	Charles Saffle

REV																				
SHEET																				
REV	B	B	B	B	B	B	B	B	B	B	B	B								
SHEET	15	16	17	18	19	20	21	22	23	24	25	26								

REV STATUS OF SHEETS															
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

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DRAWING APPROVAL DATE
08-07-08

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY All DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, MEMORY, DIGITAL, CMOS/SOI, 2M x 8-BIT, RADIATION-HARDENED, LOW VOLTAGE SRAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	**5962-08202**

SHEET 1 OF 26

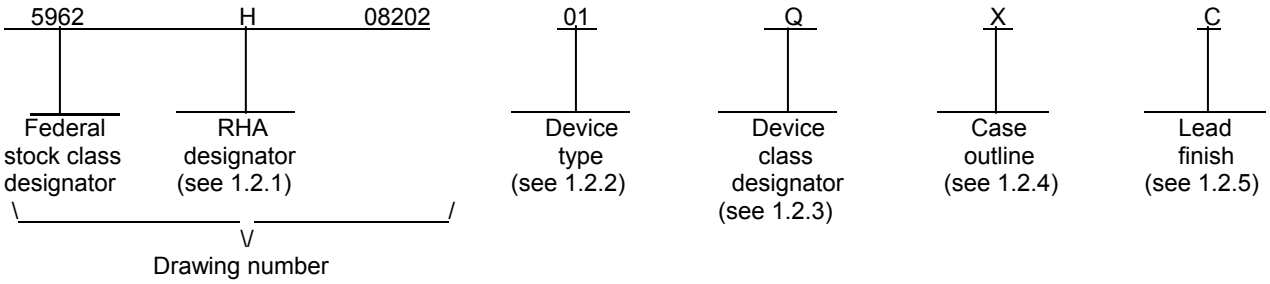
DSCC FORM 2233
APR 97

5962-E394-09

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	HXSR01608-A(Q or V)H	2M X 8-bit rad-hard CMOS/SOI SRAM 1MRAD	20 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q, V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	40	Flat pack

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38535 for classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range I/O (V_{DDD})	-0.5 V dc to +4.4 V dc
Supply voltage range Core (V_{DD})	-0.5 V dc to +2.4 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{DDD} + 0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{DDD} + 0.5 V dc
DC or average output current (I_{OUT})	15 mA
Storage temperature	-65°C to +150°C
Lead temperature (soldering 5 seconds)	+270°C
Thermal resistance, junction to case (Θ_{JC})	2.5 °C/W
Output voltage applied to high Z-state	-0.5 V dc to V_{DDD} + 0.5V dc
Maximum power dissipation	2.5 W
Case operating temperature range (T_C)	-55°C to +125°C
Maximum junction temperature (T_J)	150°C

1.4 Recommended operating conditions. 3/

Supply voltage range I/O (V_{DDD})	3.0 V dc to 3.6 V dc
Optional Supply voltage range I/O (V_{DDD})	2.3 V dc to 2.7 V dc
Supply voltage range Core (V_{DD})	1.65 V dc to 1.95 V dc
Supply voltage reference (V_{SS})	0.0 V dc
High level input voltage range (V_{IH})	0.7 x V_{DDD} to V_{DDD} + 0.3 V dc
Low level input voltage range (V_{IL})	-0.3 V dc to 0.3 x V_{DDD}
Voltage on any pin (V_{IN})	-0.3 V dc to V_{DDD} + 0.3
Power Down Time	5 ms minimum
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, method 5012)	100 percent

1.6 Radiation features.

Maximum total dose available (dose rate = <50 rad/s)	≥ 1E6 Rads(Si)
Maximum total dose available (dose rate = 300 rad/s – X-ray source)	≥ 1E6 Rads(Si)
Heavy Ion Single event upset rate (Adam's 10% worst case environment)	≤ 1E-12 upsets/bit-day 4/
Proton Single event upset rate (Adam's 10% worst case environment)	≤ 2E-12 upsets/bit-day 4/
Neutron irradiation	≥1E14 neutrons/cm^2 5/
Dose rate data upset	≥1E10 Rad(Si)/sec for < 50 nsec
Dose rate survivability	1E12 Rad(Si)/sec for < 50 nsec
Latchup	Immune by SOI technology

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ All voltages are referenced to V_{SS}.

3/ Maximum applied voltage shall not exceed 4.4 V.

4/ Weibull parameters available from vendor for calculation of upset rates in other orbits using CREME96.

5/ Guaranteed but not tested for 1MeV equivalent neutrons.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; http://www.astm.org.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard EIA/JESD78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201; http://www.jedec.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see Appendix B to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and Figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on Figure 2.

3.2.3 Truth table. The truth table shall be as specified on Figure 3.

3.2.4 Output load circuit. The output load circuit for functional tests shall be as specified on Figure 4.

3.2.5 Tester timing characteristics and timing waveforms. The tester AC timing characteristics and timing waveforms shall be as specified on Figure 5 and applies to capacitance, read cycle, and write cycle measurements unless otherwise specified.

3.2.6 Radiation exposure circuit. The radiation test circuit shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request.

3.2.7 Functional tests. Various functional tests used to test this device are contained in the appendix (herein). If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V, alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in Table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA and IIB herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7, 8A, and 8B tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device.

TABLE IA. Electrical performance characteristics. 1/ 2/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{DDD} \le 3.6\ V$ $1.65\ V \le V_{DD} \le 1.95\ V$ unless otherwise specified	Group A Sub-groups	Device type	Limits		Unit
					Min	Max	
Standby Current – NCS disabled	I_{DDSB2} I_{DDDSB2}	F=0MHz, NCS, NOE, NWE = V_{DDD}	1, 2, 3	01		30.0 0.3	mA
Standby Current –enabled	I_{DDSB} I_{DDDSB}	F=0MHz, NCS, NOE, NWE=V_{SS}	1, 2, 3	01		30.0 0.3	mA
Operating Supply Current Disabled, address bus at max frequency 3/	I_{DDOP3} I_{DDDOP3}	F=40MHz, NCS, NOE, NWE = V_{DDD}	1, 2, 3	01		2 5	mA
Operating Supply Current Deselected, write mode 3/	I_{DDOP1} I_{DDDOP1}	NCS, NOE = V_{DDD}, 1MHz NWE vector controlled	1, 2, 3	01		0.1 0.15	mA
Operating Supply Current Selected, write mode low frequency 3/	I_{DDOPW1} $I_{DDDOPW1}$	F=1MHz, NCS=V_{SS}, NOE=V_{DDD}, NWE vector controlled	1, 2, 3	01		2 0.2	mA
Operating Supply Current Selected, write mode high frequency 3/	$I_{DDOPW40}$ $I_{DDDOPW40}$	F=40MHz, NCS=V_{SS}, NOE=V_{DDD}, NWE vector controlled	1, 2, 3	01		80 8.0	mA
Operating Supply Current Selected, read mode low frequency 3/	I_{DDOPR1} $I_{DDDOPR1}$	F=1MHz, NCS=V_{SS}, NOE, NWE =V_{DD}	1, 2, 3	01		1.0 0.2	mA
Operating Supply Current Selected, read mode high frequency 3/	$I_{DDOPR40}$ $I_{DDDOPR40}$	F=40MHz, NCS=V_{SS}, NOE, NWE =V_{DD}	1, 2, 3	01		40 8.0	mA
Data Retention Current	I_{DR1} I_{DR2}	V_{DD} = 1.0 V V_{DDD} = 2.0 V	1, 2, 3	01		20 0.2	mA
Low level output voltage	V_{OL}	V_{DDD} = 3.0 V, V_{DD} = 1.65 V, I_{OL}=10mA, V_{IL} =V_{SS}, V_{IH} = V_{DDD}	1, 2, 3	01		0.4	V
High level output voltage	V_{OH}	V_{DDD} = 3.0 V, V_{DD} =1.65 V, I_{OH}=-5mA, V_{IL} = V_{SS}, V_{IH} = V_{DDD}	1, 2, 3	01	2.7		V
Input leakage current	I_{ILK}	V_{IN} = 3.6 V, V_{DDD} = 3.6 V, V_{DD} = 1.95 V, all other pins at 3.6 V	1, 2, 3	01		5	µA
Output leakage current	I_{OLK}	V_{OUT} = 3.6V, V_{DDD} = 3.6 V, V_{DD} = 1.95 all other pins at 3.6 V	1, 2, 3	01		10	µA
Input capacitance 4/ (address and control)	C_{INA} C_{INC}	V_{IN} = V_{DDD} or V_{SS}, f = 1 MHz	4	01		7 15	pF
Output capacitance 4/	C_{OUT}	See 4.4.1e	4	01		7	pF
Functional tests		See 3.2.7 and 4.4.1.c	7, 8	01			
Data retention voltage	V_{DR}	V_{DDD} = 2.0 V, V_{DD} = 1.0 V	7, 8	01	5/		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued. 1/ 2/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{DDD} \le 3.6\ V$ or $2.3\ V \le V_{DDD} \le 2.7\ V$ $1.65\ V \le V_{DD} \le 1.95\ V$ $V_{IH}=V_{DDD}$, $V_{IL}=V_{SS}$ unless otherwise specified See figure 5	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read cycle time	t_{AVAVR}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	20 22		ns
Address access time	t_{AVQV}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01		20 22	ns
Address change output invalid time	t_{AXQX}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	4 4		ns
Chip select access time	t_{SLQV}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01		20 22	ns
Chip select to output enable time	t_{SLQX}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	0 0		ns
Chip select to output disable time	t_{SHQZ}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01		4 4	ns
Output enable access time	t_{GLQV}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01		6 6	ns
Output enable to output active time	t_{GLQX}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	0 0		ns
Output enable to output disable time	t_{GHQZ}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01		4 4	ns
Write cycle time	t_{AVAVW}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	12 12		ns
Mininum write enable pulse width	t_{WLWH}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	7 7		ns
Chip select to end of write time	t_{SLWH}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	10 10		ns
Data valid to end of write time	t_{DVWH}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	6 6		ns
Address valid to end of write time	t_{AVWH}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	12 12		ns
Data hold time after end of write time	t_{WHDX}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	0 0		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued. 1/ 2/

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{DDD} \le 3.6\ V$ or $2.3\ V \le V_{DDD} \le 2.7\ V$ $1.65\ V \le V_{DD} \le 1.95\ V$ $V_{IH}=V_{DDD}$, $V_{IL}=V_{SS}$ unless otherwise specified See figure 5	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Address valid setup to start of write time	t_{AVWL}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	0 0		ns
Address valid hold after end of write time	t_{WHAX}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	0 0		ns
Write enable to output disable time	t_{WLQZ}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01		4 4	ns
Write disable to output enable time	t_{WHQX}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	0 0		ns
Write disable write enable pulse width 6/	t_{WHWL}	$3.0\ V \le V_{DDD} \le 3.6\ V$ $2.3\ V \le V_{DDD} \le 2.7\ V$	9, 10, 11	01	5 5		ns

1/ Pre-irradiation values for RHA marked devices shall also be the post-irradiation values unless otherwise specified.
2/ When performing post-irradiation electrical measurements for any RHA level $T_A = +25°C$. Limits shown are guaranteed at $T_A = +25°C \pm 5°C$.
3/ These dynamic operating mode current measurements (I_{DDOPx} and I_{DDDOPx}) exclude standby mode currents (I_{DDS} and I_{DDDS}).
4/ Tested initially and after any design or process changes which may affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
5/ As verified by functional tests.
6/ Guaranteed but not tested.

TABLE IB. SEP Test Limits 1/ 2/

Device Type	T_A = Temperature ±10°C 3/	ION Type	Memory pattern	V_{DDD} = 3.0 V		Bias for latch-up test V_{DDD} =3.6 V No latch-up LET = 3/
				SER Adam 90% environment	Effective LET no upsets	
All	+125°C	Heavy ion	4/	< 1E-12 upsets/bit-day 5/	>24 [MEV/mg/cm^2]	≥120 [MEV/mg/cm^2]
All	+25°C	Proton	4/	≤ 2E-12 upsets/bit-day 5/	>40 [MEV]	≥200 [MEV]

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Worst case temperature $T_A = +125°C$.
4/ Testing shall be performed using checkerboard and checkerboard bar test patterns.
5/ CRÈME 96 with Weibull parameters.

4.4.1 Group A inspection - Continued.

d. O/V (Latch up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V, the procedures and circuit shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535.

a. End-point electrical parameters shall be as specified in table IIA herein.

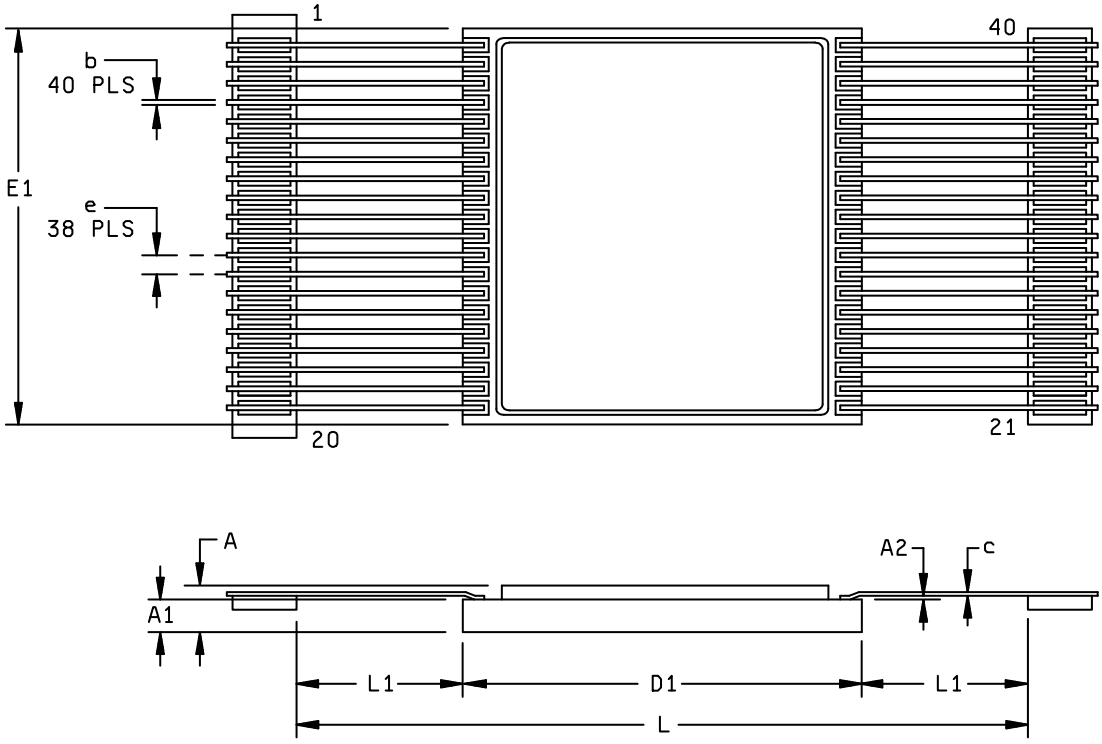
b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition B, and as specified herein. The total dose requirements shall be as defined within paragraph 1.6 herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed in accordance with MIL-STD-883 method 1019 condition B, and as specified herein. The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Test shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

Case outline X



Symbol	Millimeters			Inches		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.62	2.87	3.13	.102	.112	.122
A1	2.17	2.41	2.65	.086	.095	.104
b	0.41	0.46	0.51	.016	.018	.020
c	0.10	0.15	0.20	.004	.006	.008
D1	21.47	21.67	21.87	.845	.853	.891
e	1.14	1.27	1.40	.045	.050	.055
E1	25.45	25.65	25.82	1.002	1.010	1.018
L	---	40.89	---	---	1.610	---
L1	9.25	9.61	---	.364	.379	---
L2	3.10	3.30	3.50	.122	.130	.138

1. The U.S. Government preferred system of measurement is the metric SI system. However, since this item originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. All exposed metalized areas are gold plated over electroplated nickel.
3. Package lid is electrically connected to V_{SS} for package X.

FIGURE 1. Case outline.

Device types	All
Case outlines	X
Terminal number	Terminal symbol
1	VSS
2	A0
3	A1
4	A2
5	A3
6	A4
7	NCS
8	D0
9	D1
10	VDDD
11	VSS
12	D2
13	D3
14	NWE
15	A5
16	A6
17	A7
18	A8
19	A9
20	VDD
21	VSS
22	A10
23	A11
24	A12
25	A13
26	A14
27	A15
28	D4
29	D5
30	VDDD
31	VSS
32	D6
33	D7
34	NOE
35	A16
36	A17
37	A18
38	A19
39	A20
40	VDD

FIGURE 2. Terminal connections.

NCS	NWE	NOE	MODE	DQ
L	H	L	READ	Data Out
L	L	X	WRITE	Data In
H	X	X	Deselected	High Z

Note : L=low, H=high, X=low or high

FIGURE 3. Truth table.

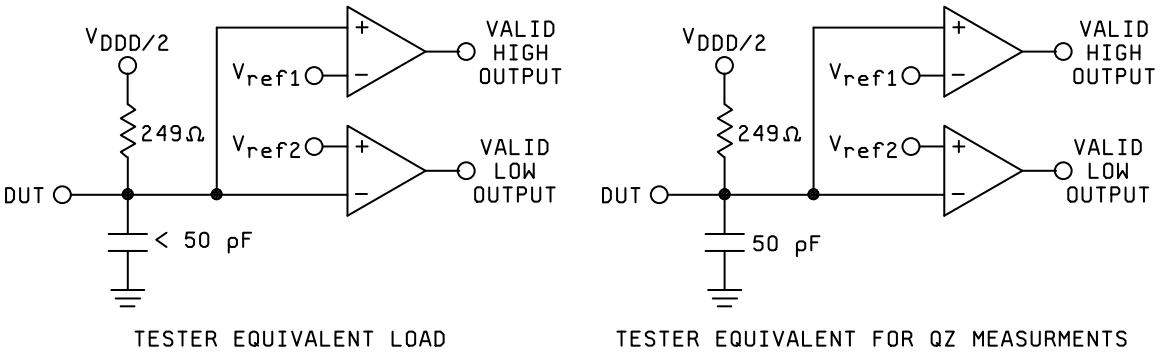
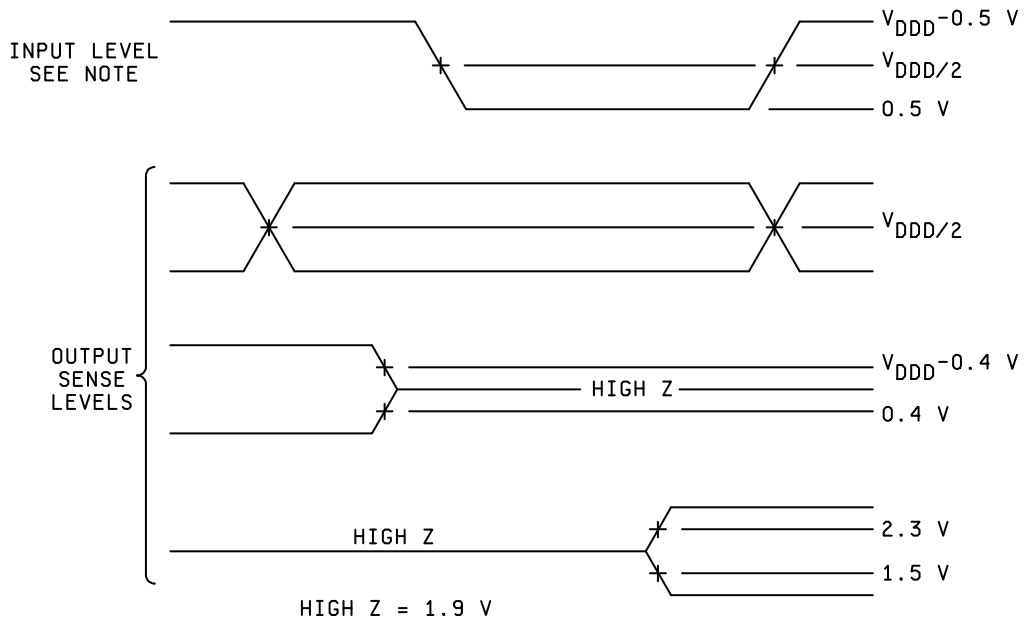


FIGURE 4. Output load circuit

TESTER TIMING CHARACTERISTICS



NOTE: Input rise and fall times < 5 ns.

READ CYCLE TIMING WAVEFORM

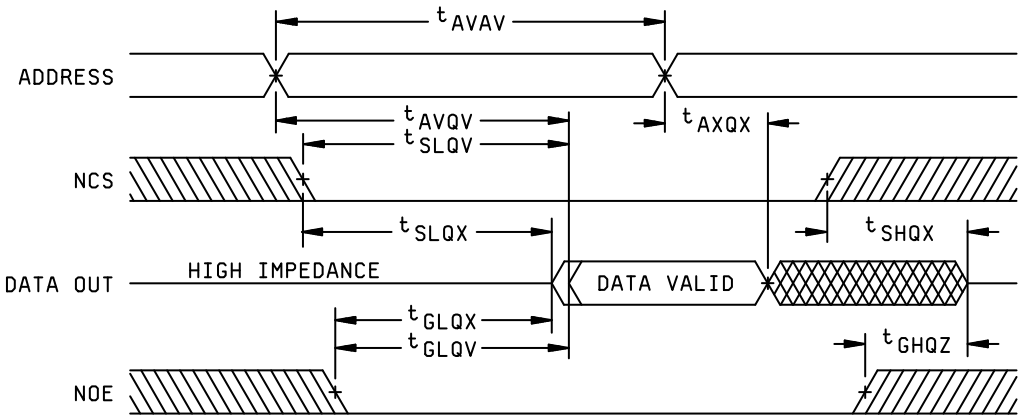


FIGURE 5. Timing waveforms.

WRITE CYCLE TIMING WAVEFORM

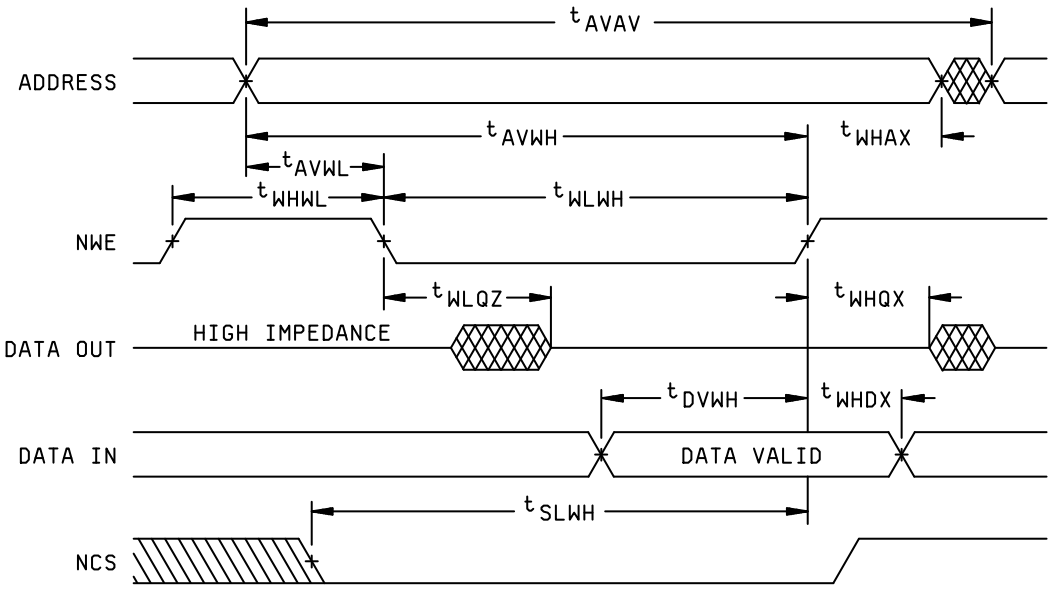


FIGURE 5. Timing waveforms - continued.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
2	Static burn-in (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7, 8A, and 8B functional tests shall verify the truth table.

4/ * indicates PDA applies to subgroup 1 and 7.

5/ ** see 4.4.1e.

6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).

7/ See 4.4.1d.

Table IIB. Delta limits. 1/ 2/

Symbol	Parameter	Delta ±
I_{DDSB}	Core Standby Current	10% of referenced spec or 100µA
I_{DDDSB}	I/O Standby Current	10% of referenced spec or 100µA
I_{DR1}	Core Data Retention Current	10% of referenced spec or 50µA
I_{DR2}	I/O Data Retention Current	10% of referenced spec or 50µA
I_{ILK}	Input Current	10% of referenced spec or .5µA
I_{OLK}	Output Leakage Current	10% of referenced spec or 1.0µA
V_{DD} MIN	Minimum Functional Voltage	200 mV
V_{DDD} MIN	Minimum V_{DDD} for functionality	200 mv

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

2/ Parameter shifts for leakage parameters are calculated at –55°C only. Parameter shifts for V_{DD} MIN and V_{DDD} MIN are calculated at –55°C, 25°C, and 125°C

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be normal to the die surface and 60 degrees to the normal, inclusive (i.e., 0° ≤ angled ≤ 60 degrees). No shadowing of the ion beam due to fixturing or package related effects are allowed.

b. The fluence shall be greater than 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ion/cm^2/s. The cross section shall be verified to be flux independent by measuring the cross section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature +125°C.

f. Bias conditions shall be V_{DD}= 3.0 V dc for the upset measurements and V_{DD}= 3.6 V dc for the latchup measurements.

g. Test four devices with zero failures.

h. For SEP test limits see table IB herein.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614)692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.
b. Test conditions (SEP).
c. Number of upsets (SEP).
d. Number of transients (SEP).
e. Occurrence of latchup (SEP).

APPENDIX A

Appendix A forms a part of SMD 5962- 08202

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.1.1.1 Functional Test Conditions. V_{IH} and V_{IL} levels during functional testing shall comply with the requirements of 3.2.7 herein.

A.1.1.2 Functional Test Sequence. Functional test patterns may be performed in any order.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March Left-Right.
Step 1. Increment address from minimum to maximum writing each address with alternating data pattern (x55).
Step 2. Increment address from minimum to maximum while performing 2a and 2b
Step 2a. Read and verify an address.
Step 2b. Write the address with complement data.
Step 3. Decrement address from maximum to minimum while performing 3a, 3b, 3c, 3d
Step 3a. Read and verify an address.
Step 3b. Write the address with complement data.
Step 3c. Read and verify the address.
Step 3d. Write the address with complement data.
Step 4. Decrement address from maximum to minimum while performing 4a and 4b
Step 4a. Read and verify the address
Step 4b. Write the address with complement data
Step 5. Decrement address from maximum to minimum while performing 5a, 5b, 5c, and 5d
Step 5a. Read and verify the address
Step 5b. Write the address with complement data
Step 5c. Read and verify the address
Step 5d. Write the address with complement data
Step 6. Decrement address from maximum to minimum while performing 6a
Step 6a. Read and verify the address

A.3.3 Algorithm C (pattern 3).

A.3.3.1 Solids.

Step1. Write x00 data pattern to all addresses from minimum to maximum.
Step 2. Read and verify x00 data pattern at all addresses.
Step 3. Write xFF data pattern to all addresses from minimum to maximum.
Step 4. Read and verify xFF data pattern at all addresses.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 Control Signals Functional Verfication.

Each test performed independently.
NOE Functional test: Read with NOE = V_{IH} and confirm high-Z outputs
NCS Functional test: Read with NCS = V_{IH} and verify high-Z outputs

Appendix B

Appendix B forms a part of SMD 5962- 08202

B.1 Scope

B1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QML plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

B.1.2 PIN. The PIN is as shown in the following example:

5962	-	08202	01	Q	9	X
Federal stock class designator	RHA designator (B1.2.1)		Device type (see B1.2.2)	Device class (see B1.2.3)	Die Code (see B1.2.4)	Die details (see B1.2.5)

_____ _____/
V
Drawing number

B.1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

B.1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Circuit function	Access time
01	2M X 8 CMOS/SOI SRAM 1MRAD	20 ns

B.1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

B.1.2.4 Die code. The die code designator shall be a number 9 for all devices supplied as die only with no case outline. Die are delivered as, known good die (KGD), which have been burned in.

B.1.2.5 Die details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

B.1.2.5.1 Die physical dimensions.

Device type	Die size	Die thickness	Die Detail	Figure Number
All	18602 µm X 12762 µm	725 ± 20 µm	A	B-1

B.1.2.5.2 Die bonding pad locations and electrical functions.

Device type	Die Detail	Figure Number
All	A	B-1

B.1.2.5.3 Interface materials

Device type	Top metallization	Backside metallization	Die Detail	Figure Number
All	Al/Cu, 9kÅ - 11.0 kÅ	None (backgrind)	A	B-1

B.1.2.5.4 Assembly related information.

Device type	Glassivation	Die Detail	Figure Number
All	Nitride 9kÅ	A	B-1

B.1.2.5.5 Wafer fabrication source.

Device type	Source	Die Detail	Figure Number
All	Honeywell Aerospace Defense & Space, Plymouth	A	B-1

B.1.3 Absolute maximum ratings. See paragraph 1.3 within the body of this drawing for details.

B.1.4 Recommended operating conditions. See paragraph 1.4 within the body of this drawing for details.

B.2 APPLICABLE DOCUMENTS.

B.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK - 103 - List of Standard Microcircuit Drawings
MIL-HDBK - 780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

B.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

B.3 REQUIREMENTS.

B.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MILPRF-389535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The Modification in the QM plan shall not effect the form, fit or function as described herein.

B.3.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

B.3.2.1 Die physical dimensions. The die physical dimensions shall be specified in B.1.2.5.1 and on figure B-1.

B.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in B.1.2.5.2 and on figure A-1. Bond pads may contain stub bonds that require compound bonding.

B.3.2.2.1 Additional die pads bonding instructions. The die contains a number of bonding pads for functions not pinned out in the single chip package configuration. The purchaser should contact the manufacturer for specific instructions for each application. The following paragraphs describe these additional functions. Failure to bond these functions appropriately may result in incorrect operation of the device.

B.3.2.2.1.1 Mode Select (X8/X32) Two X8/X32 pads are tied to VDDD for 8 bit operation

B.3.2.2.1.2 Slew Rate 0 and Slew Rate 1 (ISR0, and ISR1). SR0 and SR1 control the slew rate of the output buffers. The maximum slew rate is attained with the pads bonded to V_{DDD}. These signals occur on the top and bottom of the die.

B.3.2.2.1.3 Sense Amp Timing Control (SA2-5,SA9-11). These signal pads control the timing of the sense amps and are either tied to Vss or VDDD. These signals occur on the top and bottom of the die

B.3.2.2.1.4 Temperature Diode (Cathode, Anode). Access Is provided to two on-chip diodes for temperature monitoring. If not used, the pads are tied to Vss.

B.3.2.2.1.5 Power up (Pwrup). The pad is tied to Vss

B.3.2.2.1.6 Hardening Element Bypass (schottky). The pad is tied to Vss

B.3.2.2.1.7 Data In Delay (DinDelen). The pad is tied to VDDD.

B.3.2.3 Interface materials. The interface materials for the die shall be as specified in B.1.2.5.3 and on figure A-1.

B.3.2.4 Assembly related information. The assembly related information shall be as specified in B.1.2.5.4 and figure B-1. Bond pads may contain stub bonds that require compound bonding.

B.3.2.5 Truth table(s). Where technically applicable, (for die) the truth table(s) shall be as defined within paragraph 3.2.3 of the body of this document.

B.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

B.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

B.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in B.1.2 herein. The certification mark shall be "QML" or "Q" as required by MIL-PRF-38535.

B.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see B.6.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

B.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

B.4 VERIFICATION

B4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

B.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer lot acceptance for Class V product using the criteria within MIL-STD-883 method 5007.
b) 100% wafer probe (see paragraph B.3.4)
c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 method 2010 or the alternate procedures allowed within MIL-STD-883 method 5004.

B.4.3 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed including groups A, B, C, D and E inspections and as specified herein except where MIL-PRF-38535 permits alternate in-line control testing.

B.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see B.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified within paragraphs 4.4.4, 4.4.4.1, 4.4.4.1.1, 4.4.4.2, 4.4.4.3, and 4.4.4.4.

B.5 DIE CARRIER

B.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

B.6 NOTES

B6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit application (original equipment), design applications and logistics purposes.

B.6.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0547.

B.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined within MIL-PRF-38535 and MIL-HDBK-1331.

B.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see B.3.6 herein) to DSCC-VA and have agreed to this drawing.

PAD NAME	PAD TYPE	X Coordinate	Y Coordinate
X8/X32	DC	-8879.575	6238.605
ISR0	DC	-8654.575	6238.605
ISR1	DC	-8429.575	6238.605
VDDD	DC	-8204.575	6238.605
VDD	DC	-7979.575	6238.605
VSS	DC	-7754.575	6238.605
NC		-7529.575	6238.605
NC		-7304.575	6238.605
SA2	DC	-7079.575	6238.605
SA3	DC	-6854.575	6238.605
SA4	DC	-6629.575	6238.605
SA5	DC	-6404.575	6238.605
SA6	DC	-6179.575	6238.605
VSS	DC	-5954.575	6238.605
VDDD	DC	-5729.575	6238.605
A20	AC	-5504.575	6238.605
A19	AC	-5279.575	6238.605
VDD	DC	-5054.575	6238.605
A18	AC	-4829.575	6238.605
A17	AC	-4604.575	6238.605
A16	AC	-4379.575	6238.605
VSS	DC	-4154.575	6238.605
VDDD	DC	-3929.575	6238.605
D31	AC	-3704.575	6238.605
D30	AC	-3479.575	6238.605
D29	AC	-3254.575	6238.605
VDD	DC	-3029.575	6238.605
D28	AC	-2804.575	6238.605
D27	AC	-2579.575	6238.605
D26	AC	-2354.575	6238.605
VSS	DC	-2129.575	6238.605
VDDD	DC	-1904.575	6238.605
NBE3	AC	-1679.575	6238.605
NCS	AC	-1454.575	6238.605
NC		-1229.575	6238.605
NOE	AC	-1004.575	6238.605
VDD	DC	-779.575	6238.605
D25	AC	-554.575	6238.605
D24	AC	-329.575	6238.605
VDDD	DC	-104.575	6238.605

PAD NAME	PAD TYPE	X Coordinate	Y Coordinate
X8/X32	DC	-8879.575	-6239.36
ISR0	DC	-8654.575	-6239.36
ISR1	DC	-8429.575	-6239.36
VDDD	DC	-8204.575	-6239.36
VDD	DC	-7979.575	-6239.36
VSS	DC	-7754.575	-6239.36
ANODEB	DC	-7529.575	-6239.36
CATHODEB	DC	-7304.575	-6239.36
SA2	DC	-7079.575	-6239.36
SA3	DC	-6854.575	-6239.36
SA4	DC	-6629.575	-6239.36
SA5	DC	-6404.575	-6239.36
SA6	DC	-6179.575	-6239.36
VSS	DC	-5954.575	-6239.36
VDDD	DC	-5729.575	-6239.36
A0	AC	-5504.575	-6239.36
A1	AC	-5279.575	-6239.36
VDD	DC	-5054.575	-6239.36
A2	AC	-4829.575	-6239.36
A3	AC	-4604.575	-6239.36
A4	AC	-4379.575	-6239.36
VSS	DC	-4154.575	-6239.36
VDDD	DC	-3929.575	-6239.36
D0	AC	-3704.575	-6239.36
D1	AC	-3479.575	-6239.36
D2	AC	-3254.575	-6239.36
VDD	DC	-3029.575	-6239.36
D3	AC	-2804.575	-6239.36
D4	AC	-2579.575	-6239.36
D5	AC	-2354.575	-6239.36
VSS	DC	-2129.575	-6239.36
VDDD	DC	-1904.575	-6239.36
NBE0	AC	-1679.575	-6239.36
NC		-1454.575	-6239.36
NCS	AC	-1229.575	-6239.36
NOE	AC	-1004.575	-6239.36
VDD	DC	-779.575	-6239.36
D6	AC	-554.575	-6239.36
D7	AC	-329.575	-6239.36
VDDD	DC	-104.575	-6239.36

Note: Bond pads may contain stub bonds that require compound bonding.

Figure B-1. Bond Pad Locations and Functions for Devices.

PAD NAME	PAD TYPE	X Coordinate	Y Coordinate	PAD NAME	PAD TYPE	X Coordinate	Y Coordinate
VSS	DC	120.425	6238.605	VSS	DC	120.425	-6239.36
D23	AC	345.425	6238.605	D8	AC	345.425	-6239.36
D22	AC	570.425	6238.605	D9	AC	570.425	-6239.36
VDD	DC	795.425	6238.605	VDD	DC	795.425	-6239.36
NWE	AC	1020.425	6238.605	NWE	AC	1020.425	-6239.36
CE	AC	1245.425	6238.605	NC		1245.425	-6239.36
NC		1470.425	6238.605	CE	AC	1470.425	-6239.36
NBE2	AC	1695.425	6238.605	NBE1	AC	1695.425	-6239.36
VSS	DC	1920.425	6238.605	VSS	DC	1920.425	-6239.36
VDDD	DC	2145.425	6238.605	VDDD	DC	2145.425	-6239.36
D21	AC	2370.425	6238.605	D10	AC	2370.425	-6239.36
D20	AC	2595.425	6238.605	D11	AC	2595.425	-6239.36
D19	AC	2820.425	6238.605	D12	AC	2820.425	-6239.36
VDD	DC	3045.425	6238.605	VDD	DC	3045.425	-6239.36
D18	AC	3270.425	6238.605	D13	AC	3270.425	-6239.36
D17	AC	3495.425	6238.605	D14	AC	3495.425	-6239.36
D16	AC	3720.425	6238.605	D15	AC	3720.425	-6239.36
VSS	DC	3945.425	6238.605	VSS	DC	3945.425	-6239.36
VDDD	DC	4170.425	6238.605	VDDD	DC	4170.425	-6239.36
A15	AC	4395.425	6238.605	A5	AC	4395.425	-6239.36
A14	AC	4620.425	6238.605	A6	AC	4620.425	-6239.36
A13	AC	4845.425	6238.605	A7	AC	4845.425	-6239.36
VDD	DC	5070.425	6238.605	VDD	DC	5070.425	-6239.36
A12	AC	5295.425	6238.605	A8	AC	5295.425	-6239.36
A11	AC	5520.425	6238.605	A9	AC	5520.425	-6239.36
A10	AC	5745.425	6238.605	NC		5745.425	-6239.36
VDDD	DC	5970.425	6238.605	VDDD	DC	5970.425	-6239.36
VSS	DC	6195.425	6238.605	VSS	DC	6195.425	-6239.36
ATD0	DC	6420.425	6238.605	ATD0	DC	6420.425	-6239.36
ATD1	DC	6645.425	6238.605	ATD1	DC	6645.425	-6239.36
Schottky	DC	6870.425	6238.605	Schottky	DC	6870.425	-6239.36
Pwrup	DC	7095.425	6238.605	Pwrup	DC	7095.425	-6239.36
DinDelEn	DC	7320.425	6238.605	DinDelEn	DC	7320.425	-6239.36
ANODET	DC	7545.425	6238.605	NC		7545.425	-6239.36
CATHODET	DC	7770.425	6238.605	NC		7770.425	-6239.36
VSS	DC	7995.425	6238.605	VSS	DC	7995.425	-6239.36
VDD	DC	8220.425	6238.605	VDD	DC	8220.425	-6239.36
VDDD	DC	8445.425	6238.605	VDDD	DC	8445.425	-6239.36
SA9	DC	8670.425	6238.605	SA9	DC	8670.425	-6239.36
SA10	DC	8895.425	6238.605	SA10	DC	8895.425	-6239.36
SA11	DC	9120.425	6238.605	SA11	DC	9120.425	-6239.36

Note: Bond pads may contain stub bonds that require compound bonding.

Figure B-1. Bond Pad Locations and Functions for Devices – Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 09-07-17

Approved sources of supply for SMD 5962-08202 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H0820201QXC	34168	HXSR01608-AQH
5962H0820201VXC	34168	HXSR01608-AVH

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34168	Honeywell Inc. 12001 State Highway 55 Plymouth, MN 55441

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.