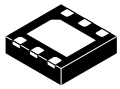
# High-Efficiency Step-Down DC-DC Converter

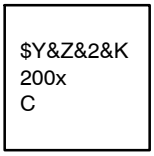
## 1 A

# FAN2001/FAN2002



**WDFN6**
**CASE 511CP**

### MARKING DIAGRAM




$Y = **onsemi** Logo
&Z = Assembly Plant Code
&2 = 2−Digit Data Code
&K = Lot Run Traceability Code
200xC = Specific Device Code
x = 1 or 2

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| FAN2001MPX | WDFN6 (Pb−Free, Halide Free) | 3000 / Tape & Reel |
| FAN2002MPX | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

### Description

Designed for use in battery−powered applications, the FAN2001/FAN2002 is a high−efficiency, low−noise synchronous PWM current mode and Pulse Skip (Power Save) mode dc−dc converter. It can provide up to 1 A of output current over a wide input range from 2.5 V to 5.5 V. The output voltage can be externally adjusted over a wide range of 0.8 V to 5.5 V by means of an external voltage divider.

At moderate and light loads, pulse skipping modulation is used. Dynamic voltage positioning is applied, and the output voltage is shifted 0.8% above nominal value for increased headroom during load transients. At higher loads the system automatically switches over to current mode PWM control, operating at 1.3 MHz. A current mode control loop with fast transient response ensures excellent line and load regulation. To achieve high efficiency and ensure long battery life, the quiescent current is reduced to 25 μA in Power Save mode, and the supply current drops below 1 μA in shut−down mode. The FAN2001/FAN2002 is available in a 3x3 mm 6−lead MLP package.

### Features

- 96% Efficiency, Synchronous Operation
- Adjustable Output Voltage Options from 0.8 V to $V_{IN}$
- 2.5 V to 5.5 V Input Voltage Range
- Up to 1 A Output Current
- Fixed Frequency 1.3 MHz PWM Operation
- High Efficiency Power Save Mode
- 100% Duty Cycle Low Dropout Operation
- Soft Start
- Output Over−Voltage Protection
- Dynamic Output Voltage Positioning
- 25 μA Quiescent Current
- Thermal Shutdown and Short Circuit Protection
- Pb−Free and Halide Free

### Applications

- Pocket PCs, PDAs
- Cell Phones
- Battery−Powered Portable Devices
- Digital Cameras
- Hard Disk Drives
- Set−Top−Boxes
- Point−of−Load Power
- Notebook Computers
- Communications Equipment

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## TYPICAL APPLICATION

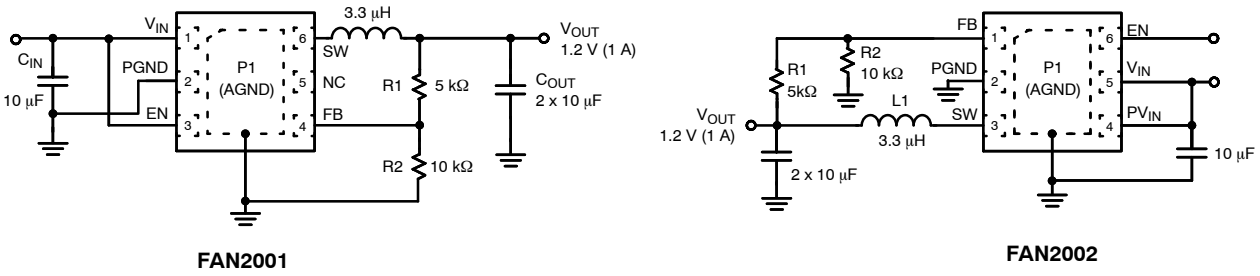



**Figure 1. Typical Application**

## PIN ASSIGNMENT AND DESCRIPTION

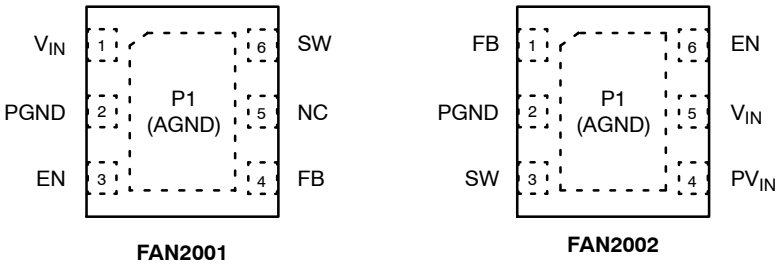



**Figure 2. Pin Assignment (Top View)**

### PIN DESCRIPTION

| Pin No. | Pin Name | Description |
|---|---|---|
| **FAN2001** | | |
| P1 | AGND | **Analog Ground.** P1 must be soldered to the PCB ground. |
| 1 | $V_{IN}$ | **Supply Voltage Input.** |
| 2 | PGND | **Power Ground.** This pin is connected to the internal MOSFET switches. This pin must be externally connected to AGND. |
| 3 | EN | **Enable Input.** Logic high enables the chip and logic low disables the chip, reducing the supply current to less than 1 µA. Do not float this pin. |
| 4 | FB | **Feedback Input.** Adjustable voltage option, connect this pin to the resistor divider. |
| 5 | NC | **No Connection Pin.** |
| 6 | SW | **Switching Node.** This pin is connected to the internal MOSFET switches. |
| **FAN2002** | | |
| P1 | AGND | **Analog Ground.** P1 must be soldered to the PCB ground. |
| 1 | FB | **Feedback Input.** Adjustable voltage option, connect this pin to the resistor divider. |
| 2 | PGND | **Power Ground.** This pin is connected to the internal MOSFET switches. This pin must be externally connected to AGND. |
| 3 | SW | **Switching Node.** This pin is connected to the internal MOSFET switches. |
| 4 | $PV_{IN}$ | **Supply Voltage Input.** This pin is connected to the internal MOSFET switches. |
| 5 | $V_{IN}$ | **Supply Voltage Input.** |
| 6 | EN | **Enable Input.** Logic high enables the chip and logic low disables the chip, reducing the supply current to less than 1 µA. Do not float this pin. |



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**ABSOLUTE MAXIMUM RATINGS** (Unless otherwise specified, all other voltages are referenced to AGND.)

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| $V_{IN}$, $PV_{IN}$ | | −0.3 | 7 | V |
| Voltage On Any Other Pin | | −0.3 | $V_{IN}$ | V |
| Lead Soldering Temperature (10 seconds) | | | 260 | °C |
| Junction Temperature | | | 150 | °C |
| Storage Temperature | | −65 | 150 | °C |
| Thermal Resistance−Junction to Tab ($\theta_{JC}$), 3x3 mm 6−lead MLP (Note 1) | | | 8 | °C/W |
| Electrostatic Discharge Protection (ESD) Level (Note 2) | HBM | 4 | | kV |
| | CDM | 1 | | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Junction to ambient thermal resistance, $\theta_{JA}$, is a strong function of PCB material, board thickness, thickness and number of copper planes, number of via used, diameter of via used, available copper surface, and attached heat sink characteristics.
2. Using Mil Std. 883E, method 3015.7(Human Body Model) and EIA/JESD22C101−A (Charge Device Model).

**RECOMMENDED OPERATING CONDITIONS** (Unless otherwise specified, all other voltages are referenced to AGND.)

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Supply Voltage Range | 2.5 | | 5.5 | V |
| Output Voltage Range, Adjustable Version | 0.8 | | $V_{IN}$ | V |
| Output Current | | | 1 | A |
| Inductor (Note 3) | | 3.3 | | μH |
| Input Capacitor (Note 3) | | 10 | | μF |
| Output Capacitor (Note 3) | | 2 x 10 | | μF |
| Operating Ambient Temperature Range | −40 | | +85 | °C |
| Operating Junction Temperature Range | −40 | | +125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Refer to the Applications section for further details.



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## ELECTRICAL CHARACTERISTICS

($V_{IN}$ = $V_{OUT}$ + 0.6 V (min. 2.5 V) to 5.5 V, $I_{OUT}$ = 350 mA, $V_{OUT}$ = 1.2 V, EN = $V_{IN}$, $T_A$ = −40°C to +85°C, Unless otherwise noted. Typical values are at $T_A$ = 25°C.)

| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Input Voltage | 0 mA ≤ $I_{OUT}$ ≤ 600 mA | | 2.5 | | 5.5 | V |
| | | 0 mA ≤ $I_{OUT}$ ≤ 1000 mA | | 2.7 | | 5.5 | V |
| $I_Q$ | Quiescent Current | $I_{OUT}$ = 0 mA, Device is not switching | | | 20 | 35 | μA |
| | | $I_{OUT}$ = 0 mA, Device is switching (Note 4) | R2 = 10 kΩ | | 50 | | μA |
| | | | R2 = 100 kΩ | | 25 | | μA |
| | Shutdown Supply Current | EN = GND | | | 0.1 | 1 | μA |
| | Undervoltage Lockout Threshold | $V_{IN}$ Rising | | 1.9 | 2.1 | 2.3 | V |
| | | Hysteresis | | | 150 | | mV |
| $V_{ENH}$ | Enable High Input Voltage | | | 1.3 | | | V |
| $V_{ENL}$ | Enable Low Input Voltage | | | | | 0.4 | V |
| $I_{EN}$ | EN Input Bias Current | EN = $V_{IN}$ or GND | | | 0.01 | 0.1 | μA |
| $R_{DS(on)}$ | PMOS On Resistance | $V_{IN}$ = $V_{GS}$ = 5.5 V | | | 250 | 350 | mΩ |
| | | $V_{IN}$ = $V_{GS}$ = 2.5 V | | | 300 | 400 | |
| | NMOS On Resistance | $V_{IN}$ = $V_{GS}$ = 5.5 V | | | 200 | 300 | mΩ |
| | | $V_{IN}$ = $V_{GS}$ = 2.5 V | | | 250 | 350 | |
| $I_{LIM}$ | P−channel Current Limit | 2.5 V < $V_{IN}$ < 5.5 V | | 1300 | 1500 | 2000 | mA |
| | Oscillator Frequency | | | 1000 | 1300 | 1500 | kHz |
| $I_{lkg_(N)}$ | N−channel Leakage Current | $V_{DS}$ = 5.5 V | | | 0.1 | 1 | μA |
| $I_{lkg_(P)}$ | P−channel Leakage Current | $V_{DS}$ = 5.5 V | | | 0.1 | 1 | μA |
| | Line Regulation | $I_{OUT}$ ≤ 10 mA | | | 0.16 | | %/V |
| | Load Regulation | 350 mA ≤ $I_{OUT}$ ≤ 1000 mA | | | 0.15 | | % |
| $V_{ref}$ | Reference Voltage | | | | 0.8 | | V |
| | Output DC Voltage Accuracy (Note 5) | 0 mA ≤ $I_{OUT}$ ≤ 1000 mA | | −3 | | +3 | % |
| | Over−Temperature Protection | PWM Mode Only 350 mA ≤ $I_{OUT}$ ≤ 1000 mA | Rising Temperature | | 150 | | °C |
| | | | Hysteresis | | 20 | | °C |
| | Start−Up Time | $I_{OUT}$ = 1000 mA, $C_{OUT}$ = 20 μF | | | 800 | | μs |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Refer to the applications section for further details.
5. For output voltages ≤ 1.2 V a 40 μF output capacitor value is required to achieve a maximum output accuracy of 3% while operating in power save mode (PFM mode).



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## TYPICAL PERFORMANCE CHARACTERISTICS

($T_A$ = 25°C, $C_{IN}$ = 10 μF, $C_{OUT}$ = 20 μF, L = 3.3 μH, R2 = 10 kΩ, unless otherwise noted.)

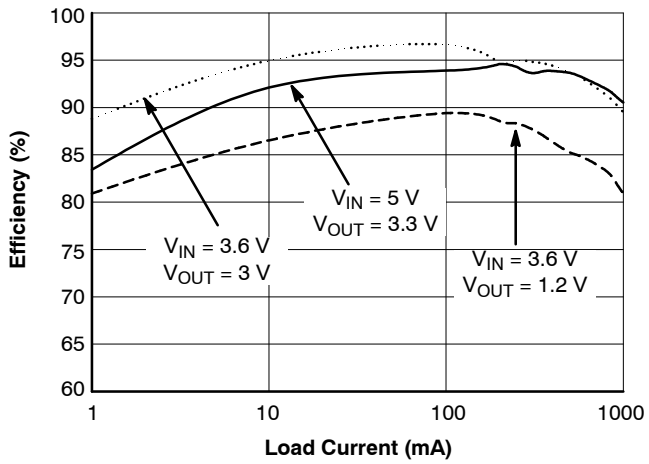



**Figure 3. Efficiency vs. Load Current**

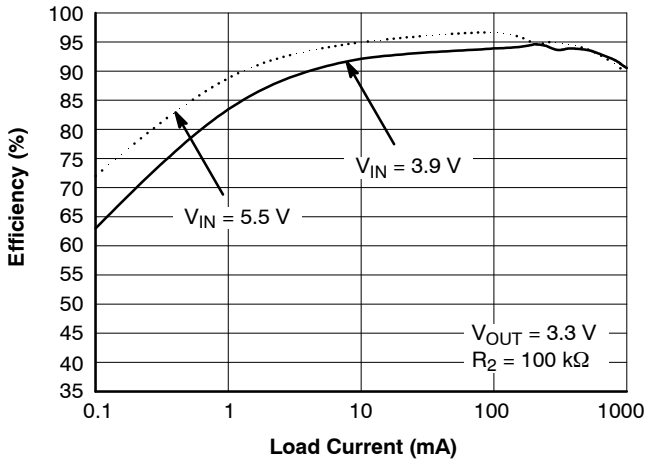



**Figure 4. Efficiency vs. Load Current**

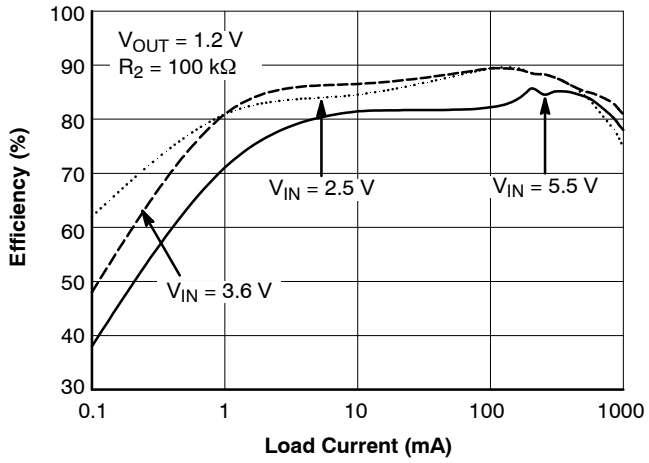



**Figure 5. Efficiency vs. Load Current**

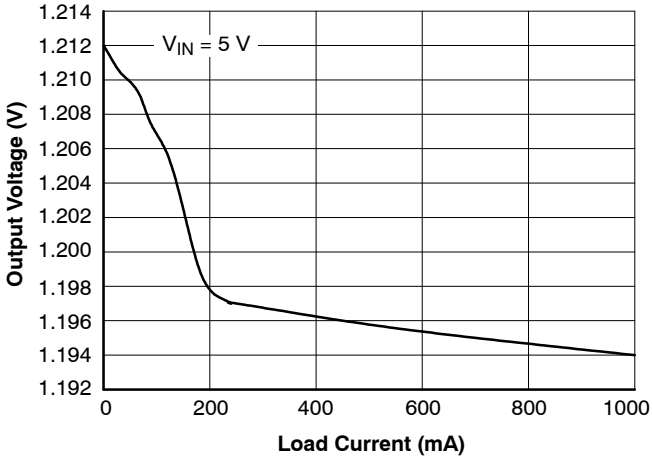



**Figure 6. Output Voltage vs. Load Current**

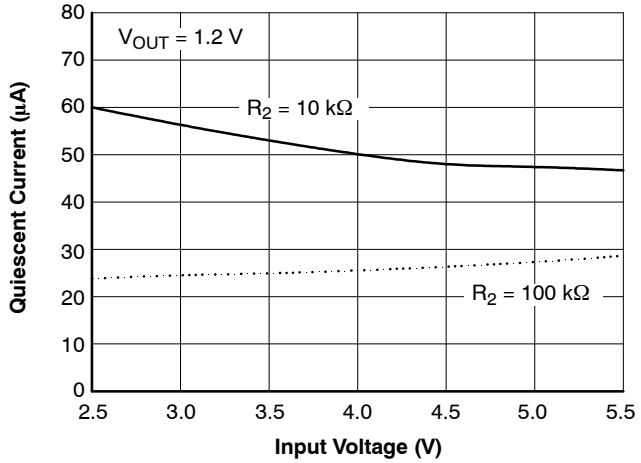



**Figure 7. Quiescent Current vs. Input Voltage**

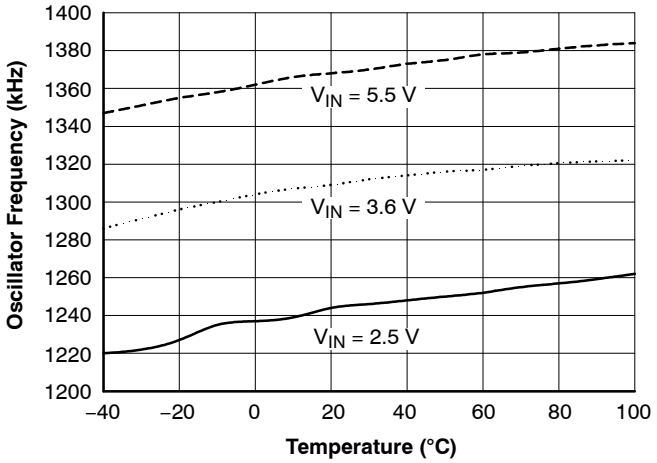



**Figure 8. Frequency vs. Temperature**



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## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

($T_A$ = 25°C, $C_{IN}$ = 10 μF, $C_{OUT}$ = 20 μF, L = 3.3 μH, R2 = 10 kΩ, unless otherwise noted.)

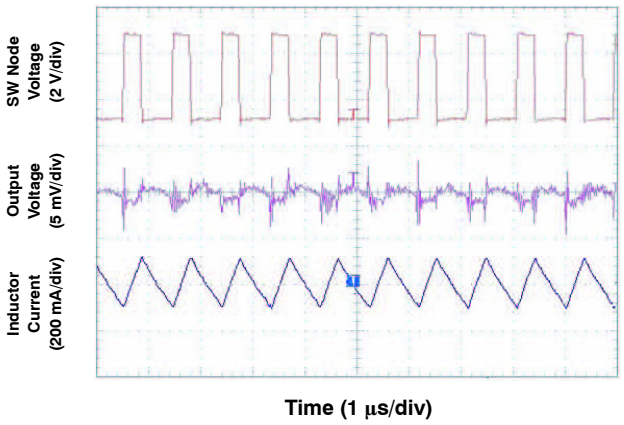



Figure 9. PWM Mode

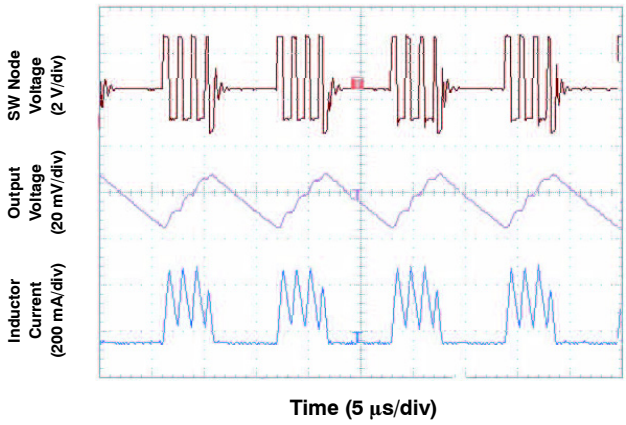



Figure 10. Power Save Mode

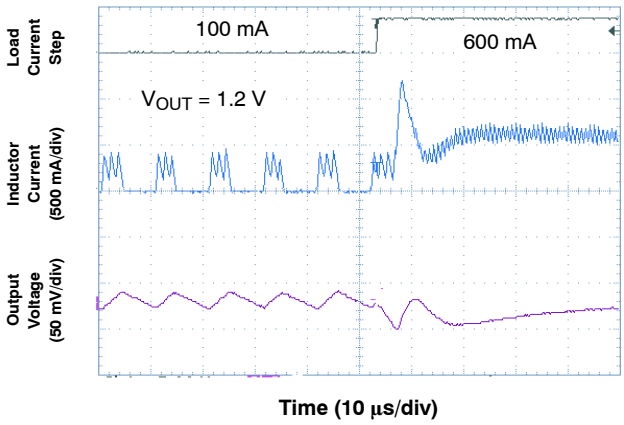



Figure 11. Load Transient Response

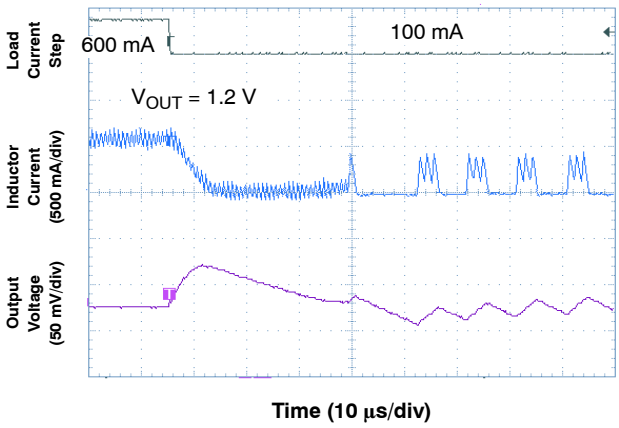



Figure 12. Load Transient Response

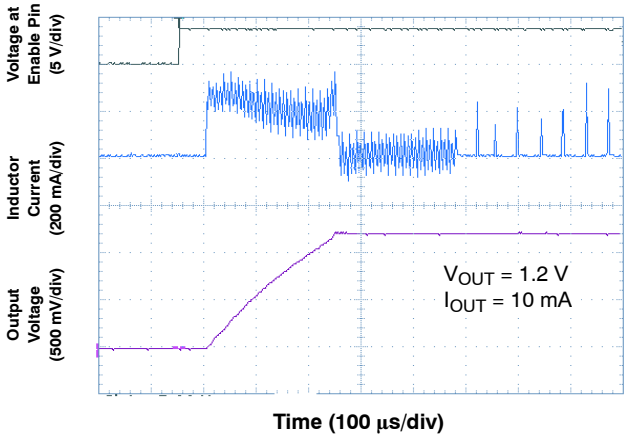



Figure 13. Start−Up Response

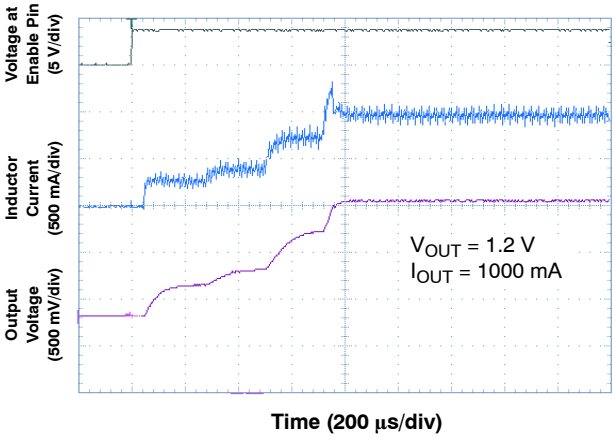



Figure 14. Start−Up Response



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## BLOCK DIAGRAM

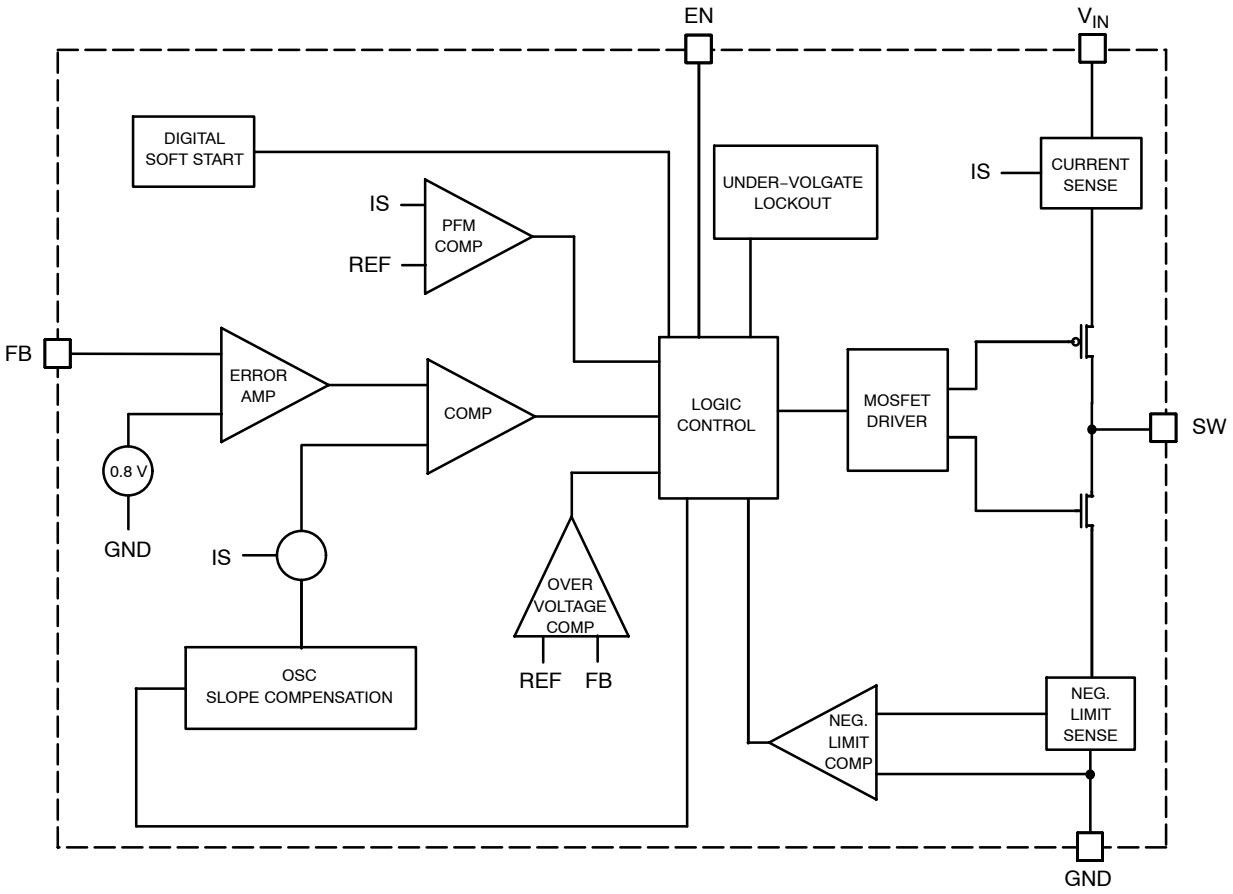



**Figure 15. Block Diagram**

## DETAILED OPERATION DESCRIPTION

The FAN2001/FAN2002 is a step−down converter operating in a current−mode PFM/PWM architecture with a typical switching frequency of 1.3 MHz. At moderate to heavy loads, the converter operates in pulse−width−modulation (PWM) mode. At light loads the converter enters a power−save mode (PFM pulse skipping) to keep the efficiency high.

### PWM Mode

In PWM mode, the device operates at a fixed frequency of 1.3 MHz. At the beginning of each clock cycle, the P−channel transistor is turned on. The inductor current ramps up and is monitored via an internal circuit. The P−channel switch is turned off when the sensed current causes the PWM comparator to trip when the output voltage is in regulation or when the inductor current reaches the current limit (set internally to typically 1500 mA). After a minimum dead time the N−channel transistor is turned on and the inductor current ramps down. As the clock cycle is completed, the N−channel switch is turned off and the next clock cycle starts.

### PFM (Power Save) Mode

As the load current decreases and the inductor current reaches negative value, the converter enters pulse−frequency−modulation (PFM) mode. The transition point for the PFM mode is given by the equation:

$$I_{OUT} = V_{OUT} \times \frac{1 - \left(\frac{V_{OUT}}{V_{IN}}\right)}{2 \times L \times f} \qquad \text{(eq. 1)}$$

The typical output current when the device enters PFM mode is 150 mA for input voltage of 3.6 V and output voltage of 1.2 V. In minimum. Consequently, the high efficiency is maintained at light loads. As soon as the output voltage falls below a threshold, set at 0.8% above the nominal value, the P−channel transistor is turned on and the inductor current ramps up. The P−channel switch turns off and the N−channel turns on as the peak inductor current is reached (typical 450 mA).

The N−channel transistor is turned off before the inductor current becomes negative. At this time the P−channel is switched on again starting the next pulse. The converter



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continues these pulses until the high threshold (typical 1.6% above nominal value) is reached. A higher output voltage in PFM mode gives additional headroom for the voltage drop during a load transient from light to full load. The voltage overshoot during this load transient is also minimized due to active regulation during turn on of the N−channel rectifier switch. The device stays in sleep mode until the output voltage falls below the low threshold. The FAN2001/FAN2002 enters the PWM mode as soon as the output voltage can no longer be regulated in PFM with constant peak current.

### 100% Duty Cycle Operation

As the input voltage approaches the output voltage and the duty cycle exceeds the typical 95%, the converter turns the P−channel transistor continuously on. In this mode the output voltage is equal to the input voltage minus the voltage drop across the P−channel transistor:

$$V_{OUT} = V_{IN} - I_{LOAD} \times (R_{DS(on)} + R_L) \qquad \text{(eq. 2)}$$

where:

$R_{DS(on)}$ = P−channel Switch ON Resistance
$I_{LOAD}$ = Output Current
$R_L$ = Inductor DC Resistance

### UVLO and Soft Start

The reference and the circuit remain reset until the $V_{IN}$ crosses its UVLO threshold.

The FAN2001/FAN2002 has an internal soft−start circuit that limits the in−rush current during start−up. This prevents possible voltage drops of the input voltage and eliminates the output voltage overshoot. The soft−start is implemented as a digital circuit increasing the switch current in four steps to the P−channel current limit (1500 mA). Typical start−up time for a 20 μF output capacitor and a load current of 1000 mA is 800 μs.

### Short Circuit Protection

The switch peak current is limited cycle−by−cycle to a typical value of 1500 mA. In the event of an output voltage short circuit, the device operates with a frequency of 400 kHz and minimum duty cycle, therefore the average input current is typically 200 mA.

### Thermal Shutdown

When the die temperature exceeds 150°C, a reset occurs and will remain in effect until the die cools to 130°C, at that time the circuit will be allowed to restart.

## APPLICATIONS INFORMATION

### Setting the Output Voltage

The internal reference is 0.8 V (Typical). The output voltage is divided by a resistor divider, R1 and R2 to the FB pin. The output voltage is given by:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \qquad \text{(eq. 3)}$$

where:

$R_1 + R_2 < 800\ k\Omega$

According to this equation, and assuming desired output voltage of 1.5096 V, and given R2 = 10 kΩ, the calculated value of R1 is 8.87 kΩ. If quiescent current is a key design parameter a higher value feedback resistor can be used (e.g. R2 = 100 kΩ) and a small bypass capacitor of 10 pF is required in parallel with the upper resistor as shown in Figure 16.

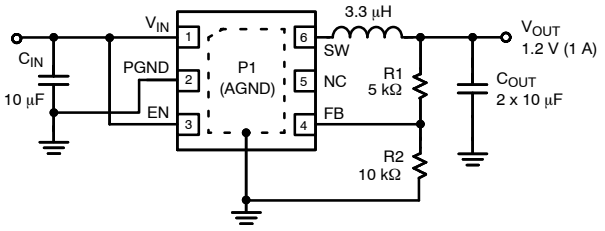



**Figure 16. Setting the Output Voltage**

### Inductor Selection

The inductor parameters directly related to the device's performances are saturation current and dc resistance. The FAN2001/FAN2002 operates with a typical inductor value of 3.3 μH. The lower the dc resistance, the higher the efficiency. For saturation current, the inductor should be rated higher than the maximum load current plus half of the inductor ripple current.

This is calculated as follows:

$$\Delta I_L = V_{OUT} \times \frac{1 - \left(\frac{V_{OUT}}{V_{IN}}\right)}{L \times f} \qquad \text{(eq. 4)}$$

where:

$\Delta I_L$ = Inductor Ripple Current
f = Switching Frequency
L = Inductor Value

Some recommended inductors are suggested in the table below:

**Table 1. RECOMMENDED INDUCTORS**

| Inductor Value | Vendor | Part Number |
|---|---|---|
| 3.3 μH | Panasonic | ELL6PM3R3N |
| 3.3 μH | Murata | LQS66C3R3M04 |



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### Capacitors Selection

For best performances, a low ESR input capacitor is required. A ceramic capacitor of at least 10 μF, placed as close to the $V_{IN}$ and AGND pins of the device is recommended. The output capacitor determines the output ripple and the transient response.

**Table 2. RECOMMENDED CAPACITORS**

| Capacitor Value | Vendor | Part Number |
|---|---|---|
| 10 μF | Taiyo Yuden | JMK212BJ106MG |
| | | JMK316BJ106KL |
| | TDK | C2012X5ROJ106K |
| | | C3216X5ROJ106M |
| | Murata | GRM32ER61C106K |

### PCB Layout Recommendations

The recommended PCB layout is shown in Figures 17 and 18. The inherently high peak currents and switching frequency of power supplies require a careful PCB layout design.

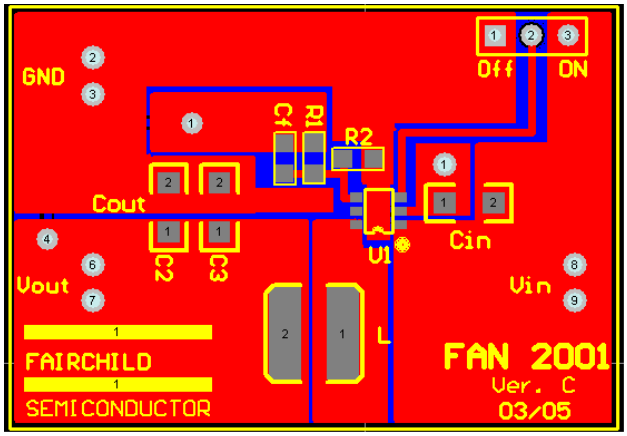



**Figure 17. Recommended PCB Layout (FAN2001)**

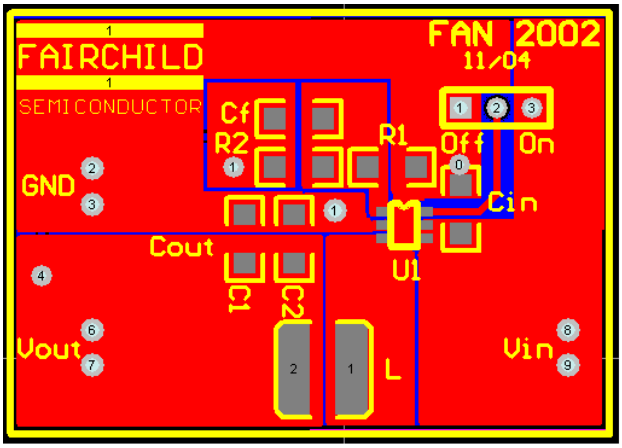



**Figure 18. Recommended PCB Layout (FAN2002)**

Therefore, use wide traces for high current paths and place the input capacitor, the inductor, and the output capacitor as close as possible to the integrated circuit terminals. In order to minimize voltage stress to the device resulting from ever present switching spikes, use an input bypass capacitor with low ESR. Note that the peak amplitude of the switching spikes depends upon the load current; the higher the load current, the higher the switching spikes. The resistor divider that sets the output voltage should be routed away from the inductor to avoid RF coupling. The ground plane at the bottom side of the PCB acts as an electromagnetic shield to reduce EMI.

For more board layout recommendations download the application note “PCB Grounding System and FAN2001/FAN2011 High Performance DC−DC Converters” (AN−42036/D).

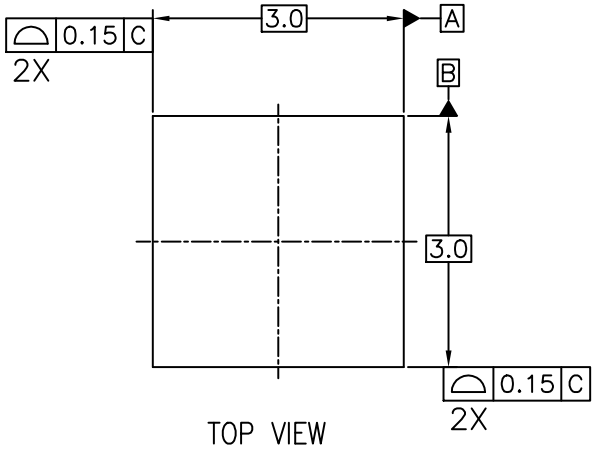
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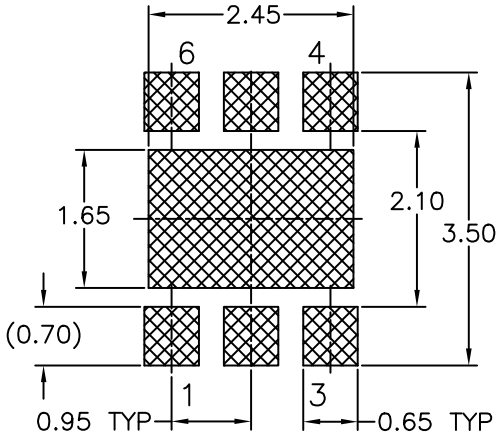
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**WDFN6 3x3, 0.95P**
CASE 511CP
ISSUE O

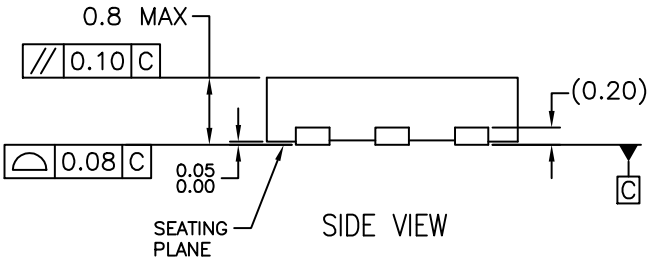
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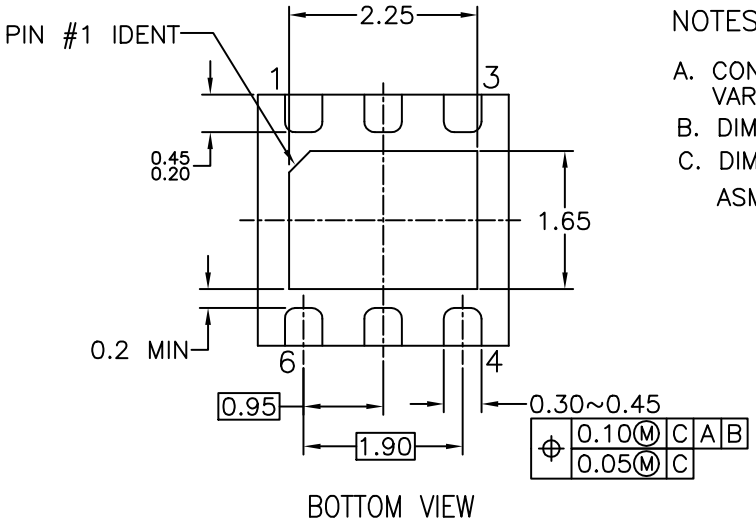

TOP VIEW




RECOMMENDED LAND PATTERN




SIDE VIEW




BOTTOM VIEW

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO−229, VARIATION WEEA, DATED 11/2001
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

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