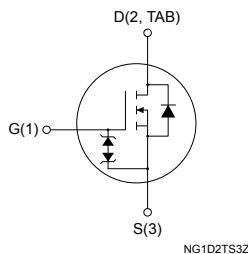
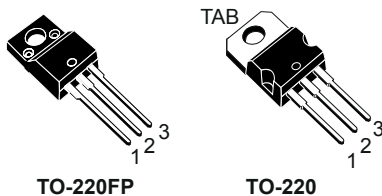


N-channel 1000 V, 1.45 Ω typ., 6.5 A SuperMESH Power MOSFET in a TO-220FP and TO-220 packages



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STF8NK100Z	1000 V	1.85 Ω	6.5 A
STP8NK100Z			

- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Applications

- Switching applications

Description

These high-voltage devices are Zener-protected N-channel Power MOSFETs developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, these devices are designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status links

[STF8NK100Z](#)

[STP8NK100Z](#)

Product summary

Order code	STF8NK100Z
Marking	F8NK100Z
Package	TO-220FP
Packing	Tube
Order code	STP8NK100Z
Marking	P8NK100Z
Package	TO-220
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
V_{DS}	Drain-source voltage	1000		V
V_{GS}	Gate-source voltage	± 30		V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	6.5	6.5 ⁽¹⁾	A
	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	4.3	4.3 ⁽¹⁾	
$I_{DM}^{(2)}$	Drain current (pulsed)	26	26 ⁽¹⁾	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	160	40	W
ESD	Gate-source human body model ($C = 100\text{ pF}$, $R = 1.5\text{ k}\Omega$)	4		kV
$dv/dt^{(3)}$	Peak diode recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ }^{\circ}\text{C}$)	-	2.5	kV
T_{stg}	Storage temperature range	-55 to 150		$^{\circ}\text{C}$
T_J	Operating junction temperature range			$^{\circ}\text{C}$

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 6.5\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DS}(\text{peak}) < V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
R_{thJC}	Thermal resistance, junction-to-case	0.78	3.1	$^{\circ}\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient	62.5		$^{\circ}\text{C}/\text{W}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	6.5	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	320	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	1000	-	-	V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 1000\text{ V}$	-	-	1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 1000\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$	-	-	50	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$	-	-	± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 3.15\text{ A}$	-	1.45	1.85	Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	2180	-	pF
C_{oss}	Output capacitance		-	174	-	pF
C_{rss}	Reverse transfer capacitance		-	36	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }800\text{ V}$, $V_{GS} = 0\text{ V}$	-	83	-	pF
Q_g	Total gate charge	$V_{DD} = 800\text{ V}$, $I_D = 6.3\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see the Figure 16. Test circuit for gate charge behavior)	-	73	102 ⁽²⁾	nC
Q_{gs}	Gate-source charge		-	12	-	nC
Q_{gd}	Gate-drain charge		-	40	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

2. Specified by design, not tested in production.

Table 6. Switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 500\text{ V}$, $I_D = 3.15\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	28	-	ns
t_r	Rise time		-	19	-	ns
$t_{d(off)}$	Turn-off delay time	(see the Figure 15. Test circuit for resistive load switching times and Figure 20. Switching time waveform)	-	59	-	ns
t_f	Fall time		-	30	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	6.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-	26	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 6.3 \text{ A}$, $V_{GS} = 0 \text{ V}$	-	-	1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 6.3 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 50 \text{ V}$	-	620	-	ns
Q_{rr}	Reverse recovery charge		-	5.3	-	μC
I_{RRM}	Reverse recovery current	(see the Figure 17. Test circuit for inductive load switching and diode recovery times)	-	17	-	A
t_{rr}	Reverse recovery time	$I_{SD} = 6.3 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 50 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$	-	840	-	ns
Q_{rr}	Reverse recovery charge		-	7.5	-	μC
I_{RRM}	Reverse recovery current	(see the Figure 17. Test circuit for inductive load switching and diode recovery times)	-	18	-	A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics curves

Figure 1. Safe operating area for TO-220

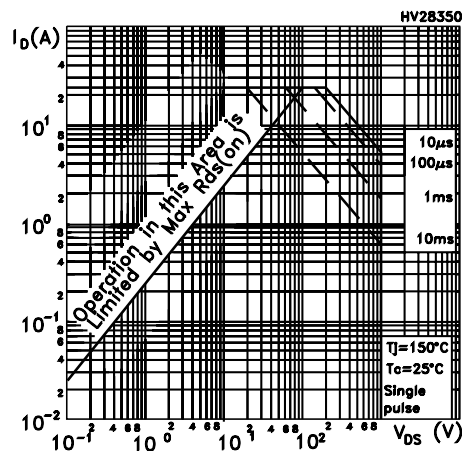


Figure 2. Normalized transient thermal impedance for TO-220

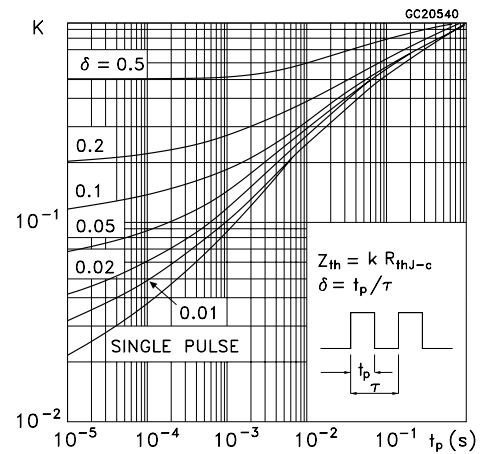


Figure 3. Safe operating area for TO-220FP

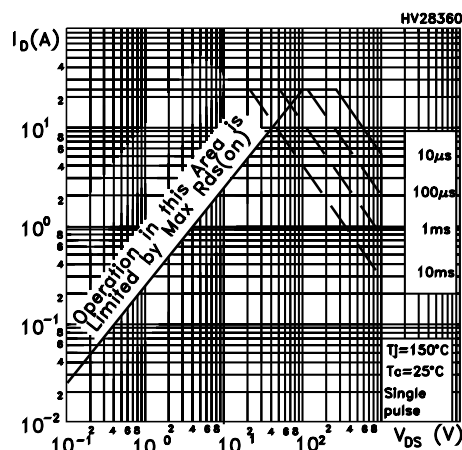


Figure 4. Normalized transient thermal impedance for TO-220FP

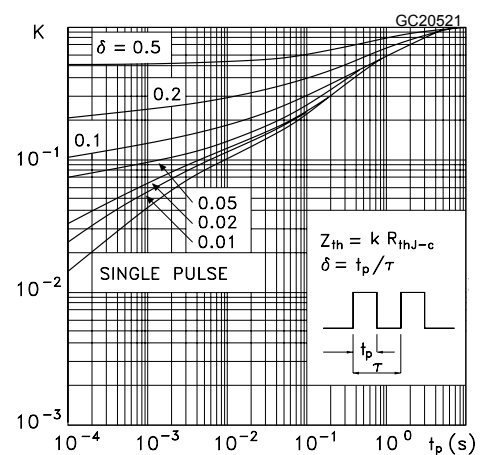


Figure 5. Typical output characteristics

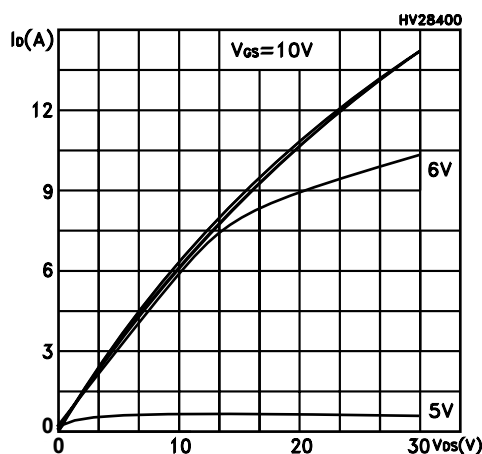


Figure 6. Typical transfer characteristics

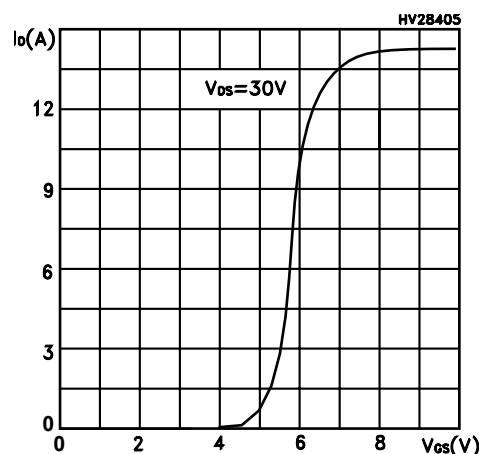


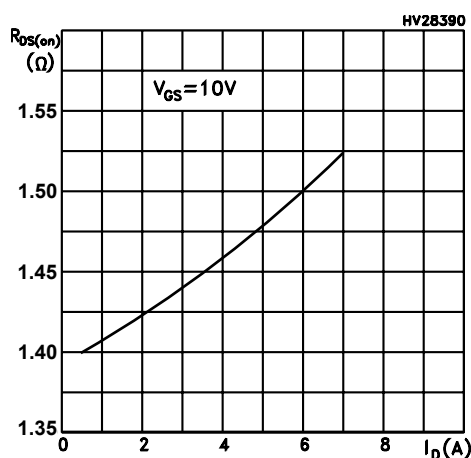
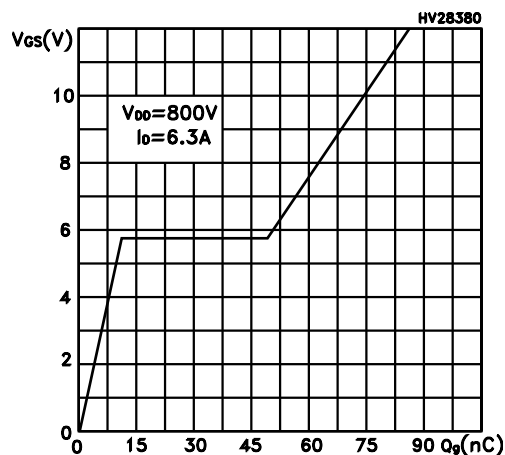
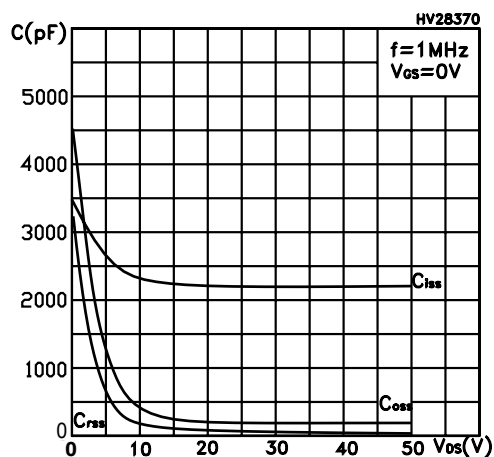
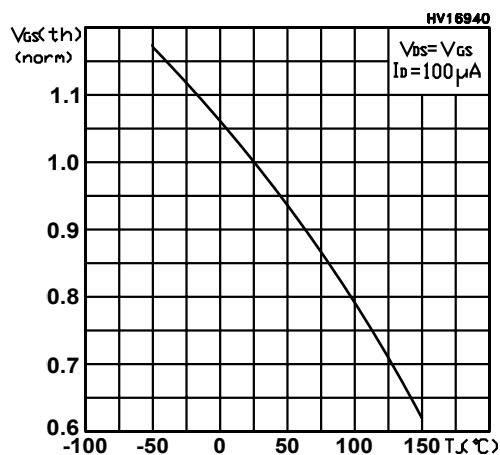
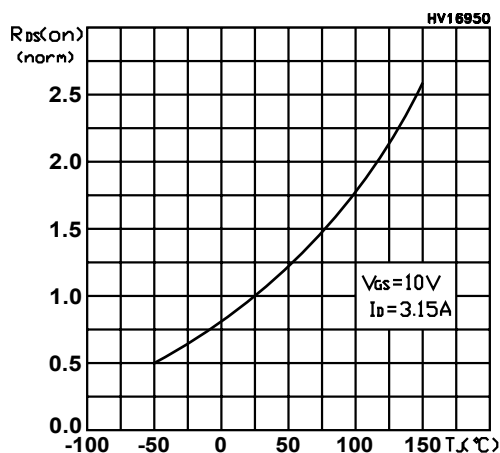
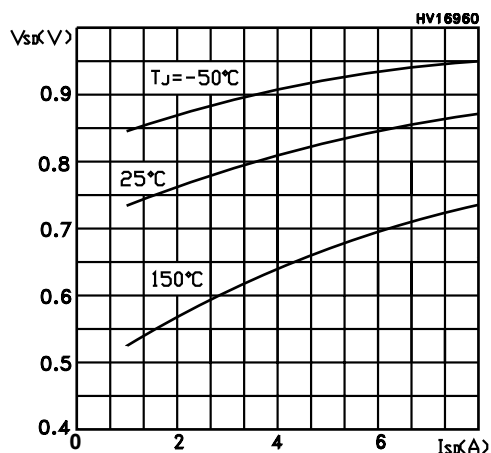
Figure 7. Typical static drain-source on-resistance

Figure 8. Typical gate charge characteristics

Figure 9. Typical capacitance variations

Figure 10. Normalized gate threshold vs temperature

Figure 11. Normalized on-resistance vs temperature

Figure 12. Typical reverse diode forward characteristics


Figure 13. Normalized breakdown voltage vs temperature

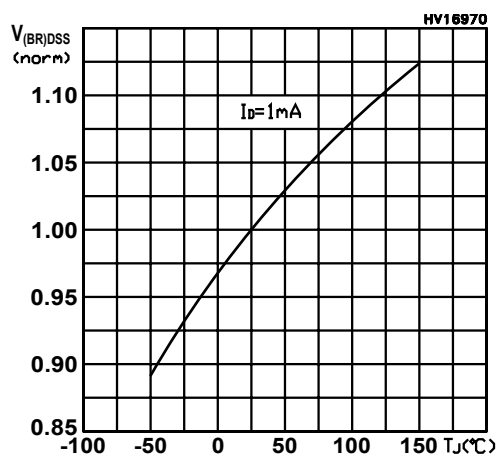
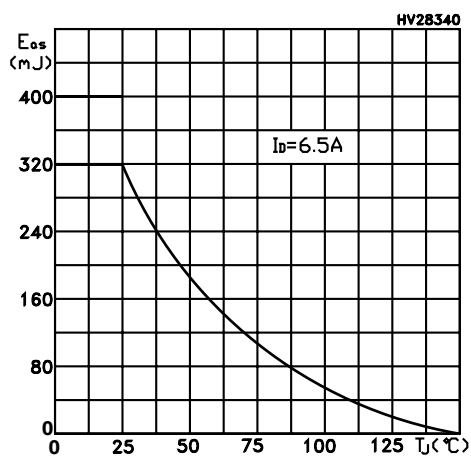
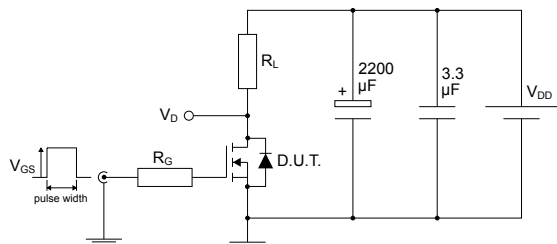


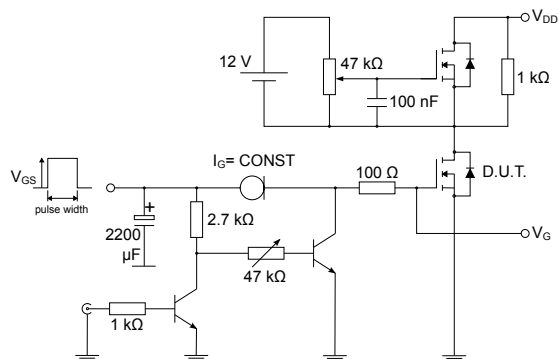
Figure 14. Maximum avalanche energy vs temperature



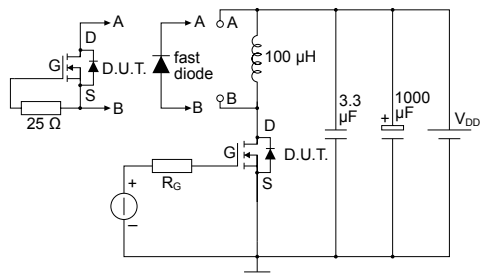
3 Test circuits

Figure 15. Test circuit for resistive load switching times


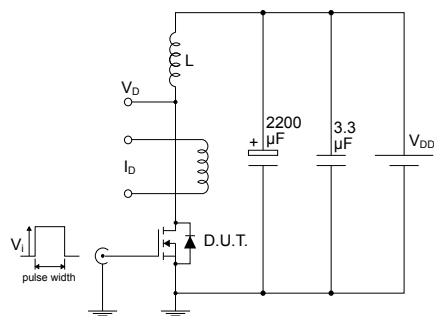
AM01468v1

Figure 16. Test circuit for gate charge behavior


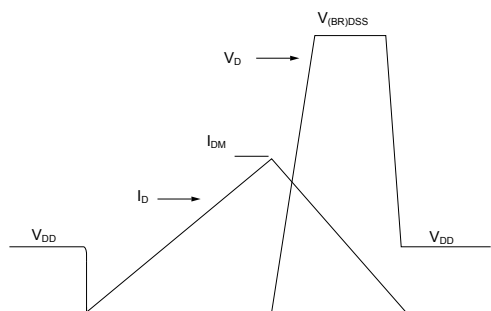
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Figure 17. Test circuit for inductive load switching and diode recovery times


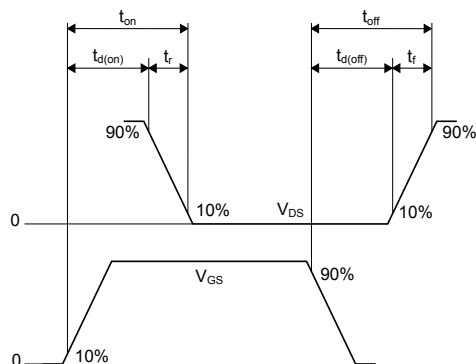
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Figure 18. Unclamped inductive load test circuit


AM01471v1

Figure 19. Unclamped inductive waveform


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Figure 20. Switching time waveform


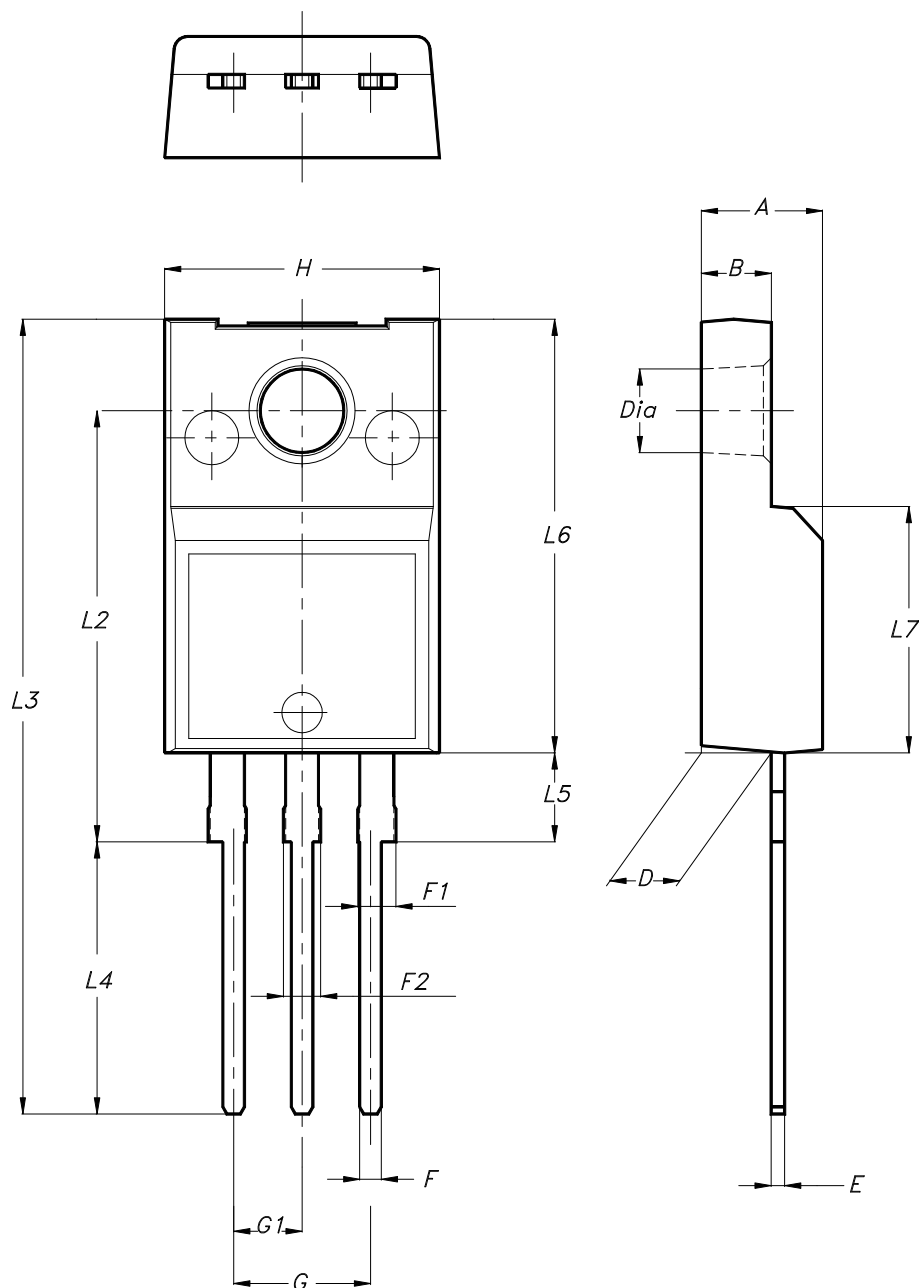
AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP type B package information

Figure 21. TO-220FP type B package outline



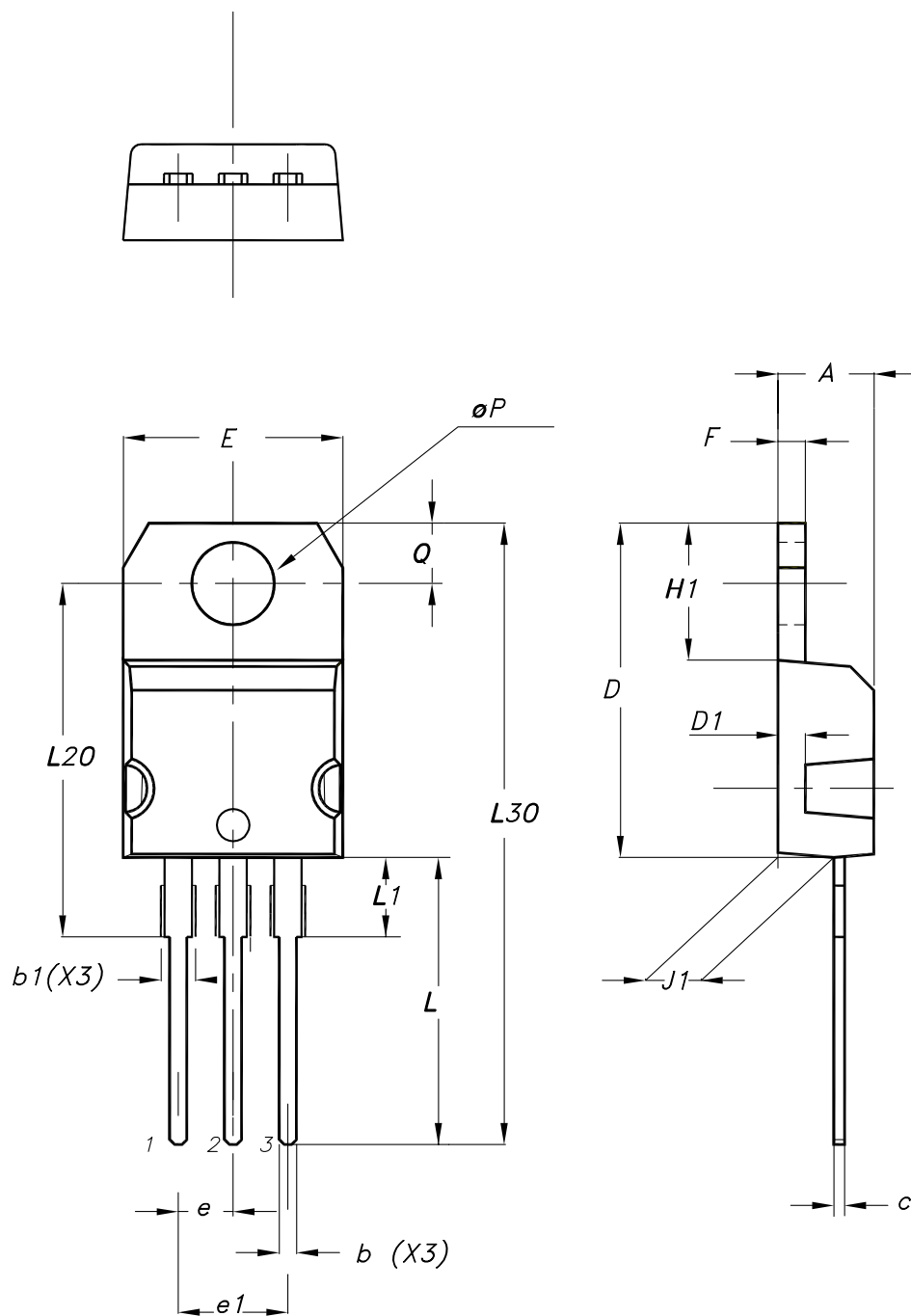
7012510_B_rev.14

Table 8. TO-220FP type B package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

4.2 TO-220 type A package information

Figure 22. TO-220 type A package outline



0015988_typeA_Rev_24

Table 9. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

Revision history

Table 10. Document revision history

Date	Version	Changes
04-Nov-2005	1	First release.
24-Mar-2026	2	Updated Section 4: Package information . Minor text changes.



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