LOW-NOISE DUAL OPERATIONAL AMPLIFIER

■ GENERAL DESCRIPTION

The NJM5532 is a high performance dual low noise operational amplifier. Compared to the standard dual operational amplifiers, such as the NJM4558, it shows better noise performance, improved output drive capability, and considerably higher small-signal and power bandwidths. it is compensated internally for voltage follower circuit. This makes the device especially suitable for application in high quality and professional audio equipment, instrumentation, control circuits, and telephone channel amplifiers.

If very low noise characteristic is of prime importance, it is recommended D-Rank type product (NJM5532MD). These have specified maximum limits for equivalent input noise voltage.

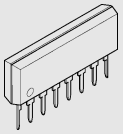
■ PACKAGE OUTLINE

Discontinued



NJM5532D
(DIP8)

Discontinued



NJM5532L
(SIP8)



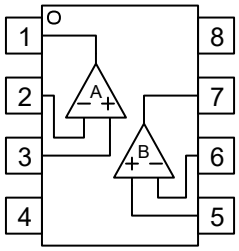
NJM5532M
(DMP8)

■ FEATURES

- Operating Voltage ±3V~±22V
- Small Signal Bandwidth 10MHz typ.
- Output Drive Capability 600Ω,10Vrms typ.
- Input Noise Voltage 5nV/√Hz typ.
- Power Bandwidth 140kHz typ.
- Slew Rate 8V/μs typ.
- Bipolar Technology
- Package Outline DIP8 (Discontinued), SIP8 (Discontinued), DMP8

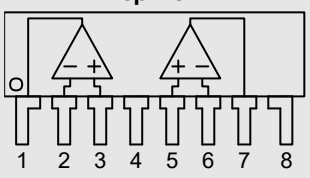
■ PIN CONFIGURATION

Top View



DIP8 (Discontinued),
DMP8 Package

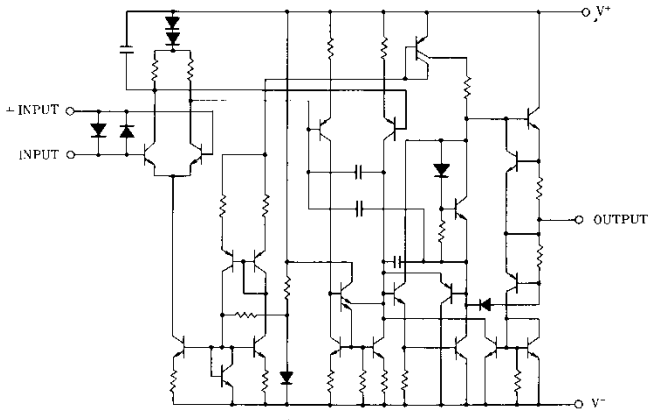
Top View



SIP8 Package
(Discontinued)

PIN FUNCTION
1.A OUTPUT
2.A -INPUT
3.A +INPUT
4.V⁻
5.B +INPUT
6.B -INPUT
7.B OUTPUT
8.V⁺

■ EQUIVALENT CIRCUIT (1/2 Shown)



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■ ABSOLUTE MAXIMUM RATINGS (Ta=25˚C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V^+/V^-	±22	V
Common Mode Input Voltage Range	V_{ICM}	V^+/V^-	V
Differential Input Voltage Range	V_{ID}	±0.5	V
Power Dissipation	P_D	DIP8 : 500 DMP8 : 600(Note1) SIP8 : 800	mW
Operating Temperature Range	Topr	-20~+75	°C
Storage Temperature Range	Tstg	-40~+125	°C

(Note1) On the cermic PCB (10x20x0.635mm)

■ RECOMMENDED OPERATING VOLTAGE (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V^+/V^-	±3~±22	V

■ ELECTRICAL CHARACTERISTICS (V^+/V^-=±15V,Ta=25˚C, unless otherwise noted.)

● DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	R_S≤10kΩ	-	0.5	4	mV
Input Offset Current	I_{IO}		-	10	150	nA
Input Bias Current	I_B		-	200	800	nA
Supply Current	I_{CC}	R_L=∞	-	9	16	mA
Common Mode Input Voltage Range	V_{ICM}		± 12	± 13	-	V
Common Mode Rejection Ratio	CMR	R_S≤10kΩ	70	100	-	dB
Supply Voltage Rejection Ratio	SVR	R_S≤10kΩ	80	100	-	dB
Voltage Gain1	A_{V1}	R_L≥2kΩ, V_O=±10V	88	100	-	dB
Voltage Gain2	A_{V2}	R_L≥600Ω, V_O=±10V	83.5	94	-	dB
Maximum Output Voltage1	V_{OM1}	R_L≥600Ω	± 12	± 13	-	V
Maximum Output Voltage2	V_{OM2}	R_L≥600Ω, V^+/V^-=±18V	± 15	± 16	-	V
Input Resistance	R_{IN}		30	300	-	kΩ
Short Circuit Output Current	I_{OS}		-	38	-	mA

● AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Resistance	R_O	A_V=30dB,f=10kHz, R_L=600Ω	-	0.3	-	Ω
Overshoot		A_V=1, V_{IN}=100mV_{PP}, R_L=100pF, R_L=600Ω	-	10	-	%
Voltage Gain	A_V	f=10kHz	-	67	-	dB
Slew Rate	SR		-	8	-	V/μs
Gain Bandwidth Product	GB	C_L=100pF, R_L=600Ω	-	10	-	MHz
Power Bandwidth	W_{PG}	V_O=±10V	-	140	-	kHz
	W_{PG}	V_O=±14V, R_L=600Ω, V^+/V^-=±18V	-	100	-	kHz
Equivalent Input Noise Voltage	e_n	f_O=30Hz	-	8	-	nV/√Hz
	e_n	f_O=1kHz	-	5	-	nV/√Hz
Equivalent Input Noise Current	i_n	f_O=30Hz	-	2.7	-	pA/√Hz
	i_n	f_O=1kHz	-	0.7	-	pA/√Hz
Channel Separation	CS	f=1kHz, R_S=5kΩ	-	110	-	dB

■ ELECTRICAL CHARACTERISTICS (D-ranktype(Note2), V^+/V^-=±15V, Ta=25˚C, unless otherwise noted.)

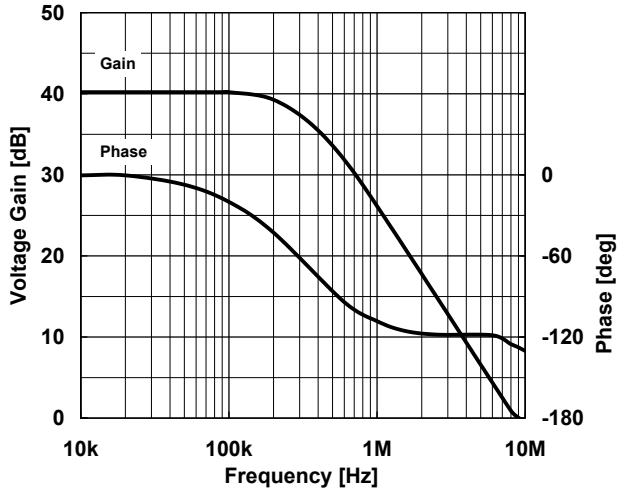
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Equivalent Input Noise Voltage	V_{NI}	RIAA, R_S=2.2kΩ	-	-	1.4	μVrms

(Note2)D-rank type is a Equivalent Input Noise Voltage selected product.

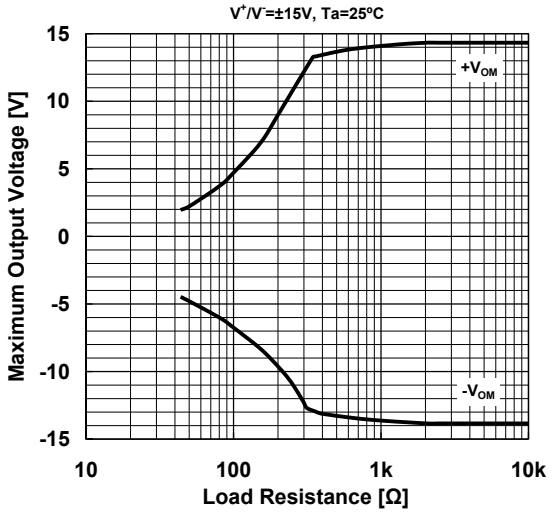
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■ TYPICAL CHARACTERISTICS

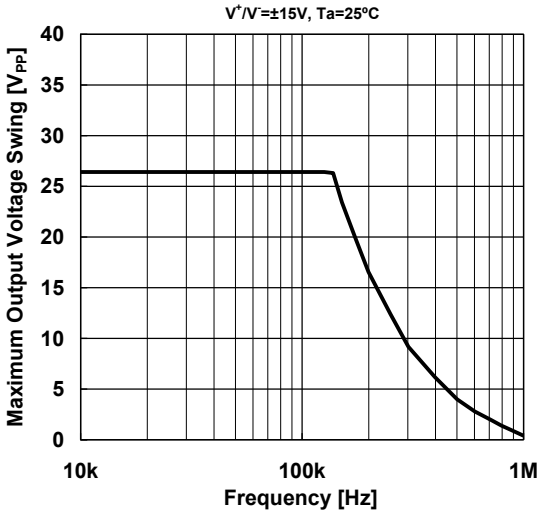
Gain/Phase vs. Frequency
Ta=25°C



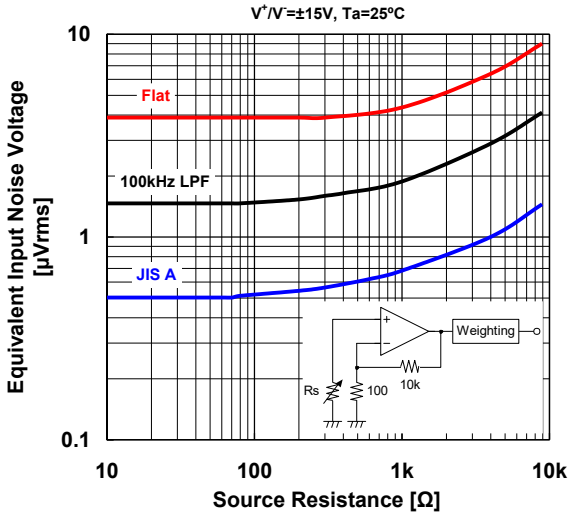
Maximum Output Voltage vs. Load Resistance
V^+/V^-=±15V, Ta=25°C



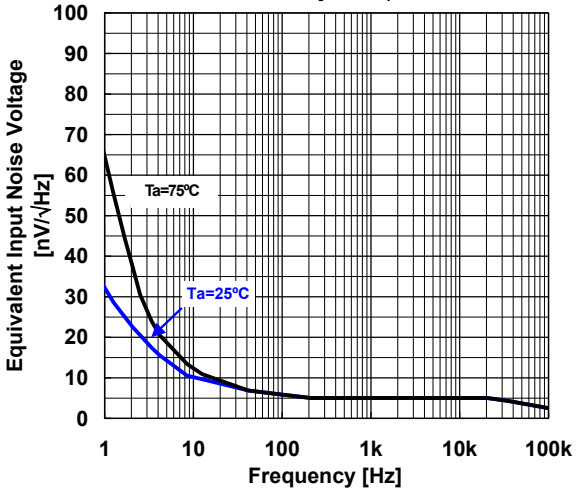
Maximum Output Voltage Swing vs. Frequency
V^+/V^-=±15V, Ta=25°C



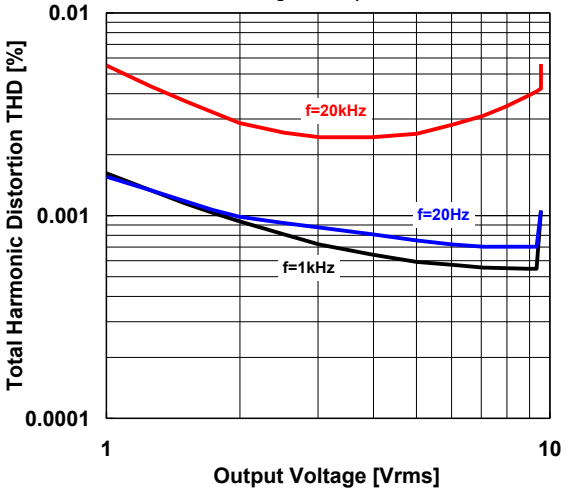
Voltage Noise vs. Source Resistance
V^+/V^-=±15V, Ta=25°C



Voltage Noise vs. Frequency
V^+/V^-=±15V, R_S=50Ω, A_V=60dB



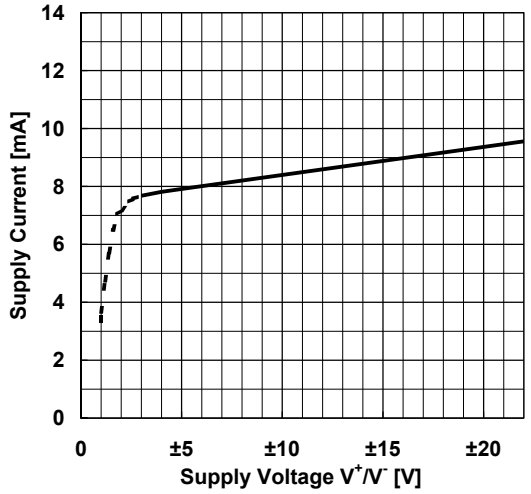
THD vs. Output Voltage
V^+/V^-=±15V, R_L=10kΩ, G_V=20dB, Ta=25°C



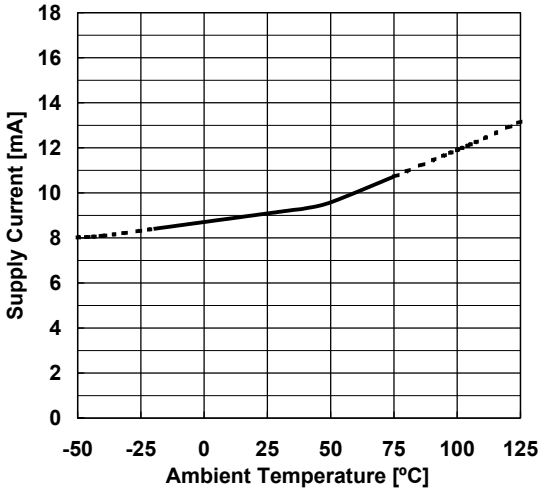
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■ TYPICAL CHARACTERISTICS

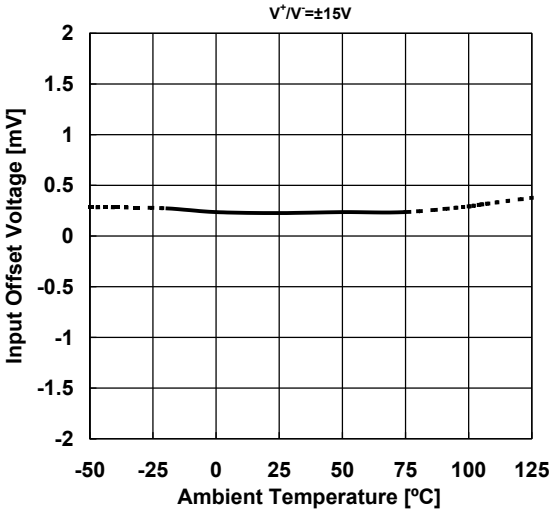
Supply Current vs. Supply Voltage
Ta=25ºC



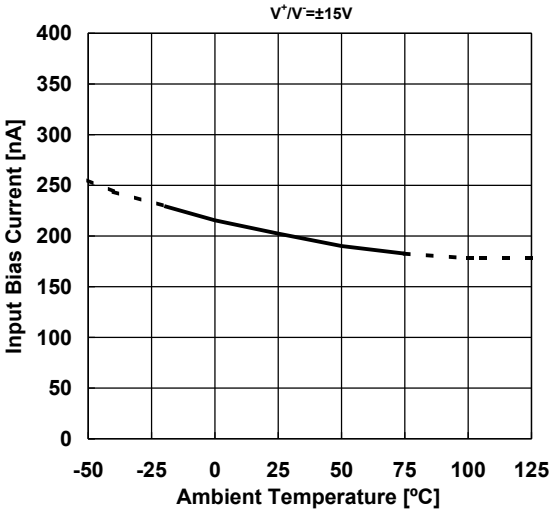
Supply Current vs. Temperature
V+/V-=±15V



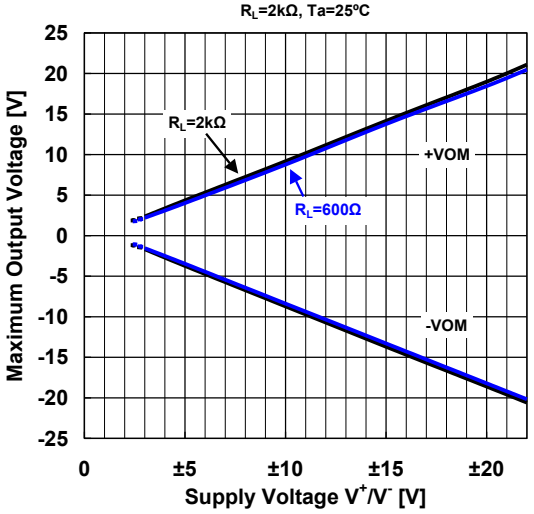
Input Offset Voltage vs. Temperature
V+/V-=±15V



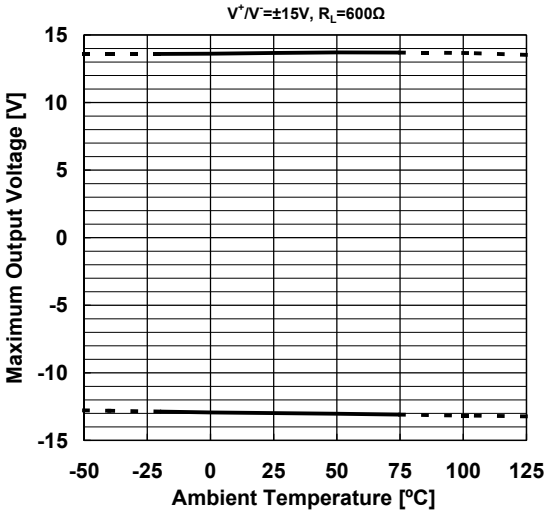
Input Bias Current vs. Temperature
V+/V-=±15V



Maximum Output Voltage vs. Supply Voltage
RL=2kΩ, Ta=25ºC



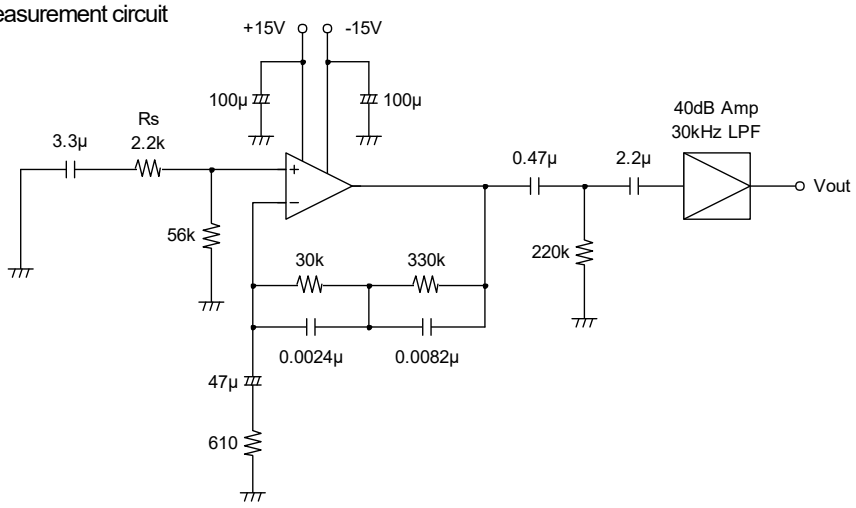
Maximum Output Voltage vs. Temperature
V+/V-=±15V, RL=600Ω



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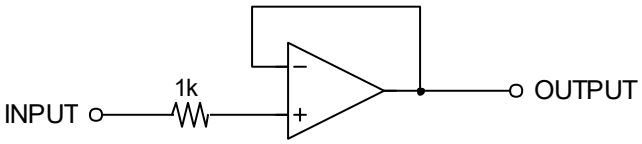
■ TEST CIRCUIT

Noise Voltage (RIAA) measurement circuit



■ NOTICE

When used in voltage follower circuit, put a current limit resistor into non-inverting input terminal in order to avoid inside input diode destruction when the power supply is turned on. (ref.Fig.1)



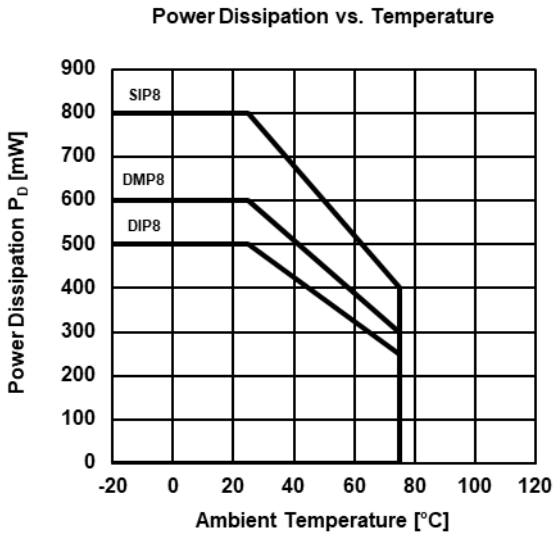
(Fig.1)

■ Caution to Thermal Design

If the NJM5532 junction temperature (Tj) exceeds guaranteed value (125 degree) or the package power dissipation (P_D), there is possibility of the NJM5532 deterioration or breakdown.

The NJM5532 supply current is higher (I_{CCMAX}=16mA at V^+/V^-=±15V,Ta=+25˚C) and has positive temperature coefficient (Refer to Supply Current vs. Temperature characteristic).

Therefore, you should carefully design with due attention to the supply voltage, the internal power dissipation and the ambient temperature.



DMP8 : On the ceramic PCB (10x20x0.635mm)

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■ **Countermeasure to Excess Current by Parasitic Circuit**

When the NJM5532 V^+ is open (Fig.2), the NJM5532 may be burnt flowing the excess current by internal parasitic circuit(Fig.3).The excess current generating condition is following:

/ Between input terminal and V^- voltage difference is higher.

/ Input terminal has no resistance of 1kΩ or more.

/ V^+ terminal is connected with low impedance. (Ietc is higher)

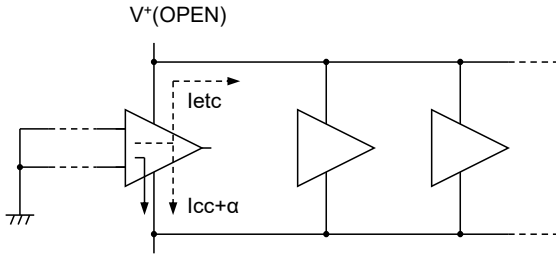


Fig.2

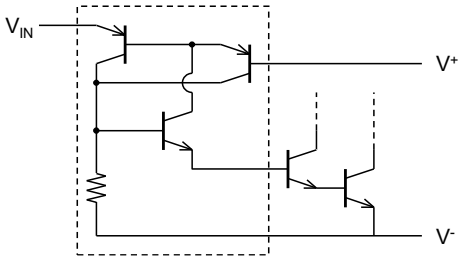


Fig.3

For countermeasure to excess current by parasitic circuit, NJRC recommends the following method.

/ prevent operating of a parasitic circuit by inserting a SBD (Fig.4-1/4-2).

/ limiting a parasitic circuit operation by inserting a resistance (1kΩ or more) (Fig.5).

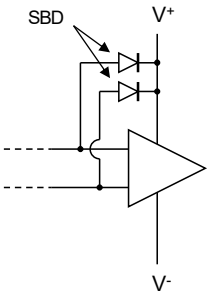


Fig.4-1

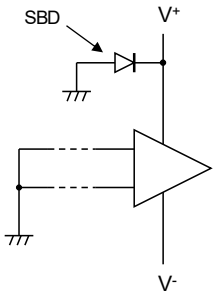


Fig.4-2

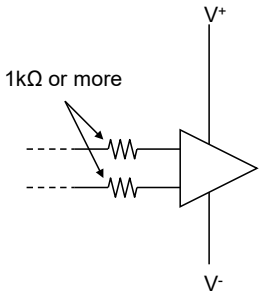


Fig.5

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