AUTOMOTIVE COMPLIANT WIDE INPUT VOLTAGE RANGE 300mA ULDO REGULATOR

Description

The AP7375Q series consists of wide input voltage range (45V), low quiescent current (2.1μA), low-dropout linear regulators (LDOs) able to provide 300mA load current. The AP7375Q LDO family offers an EN pin to enable and disable the LDO output. The EN pin can take an input voltage of 45V.

The device provides a very fast response against line voltage transient and load current transient, and ensures no overshoot voltage occurs during startup and short-circuit recovery. It also features integrated short-circuit and thermal-shutdown protection.

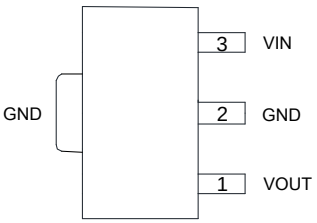
The AP7375Q has 1.8V, 3.0V, 3.3V, and 5.0V fixed output voltage versions, and is available in the SOT89, SO-8EP, SOT25, and U-DFN2020-6 (SWP) (Type UXC) packages.

Features

- Wide Input Voltage Range: 3V to 45V
- Maximum Output Current: 300mA
- Low Dropout Voltage:
  - V_{DROP} = 35mV@I_{OUT} = 10mA (typ)
  - V_{DROP} = 350mV@ I_{OUT} = 100mA (typ)
- Low Quiescent Current: 2.1μA (typ)
- Fixed Output Voltages: 1.8V, 3.0V, 3.3V and 5.0V
- High Output Voltage Accuracy: ±2%
- High PSRR: 85dB@1kHz
- Excellent Line/Load Regulation
- Thermal Shutdown Function
- Short-Current Protection Function
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The AP7375Q is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

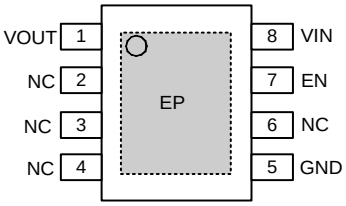
Pin Assignments

(Top View)



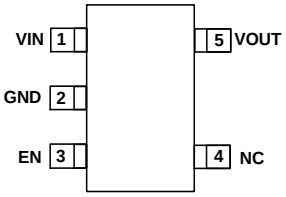
SOT89

(Top View)



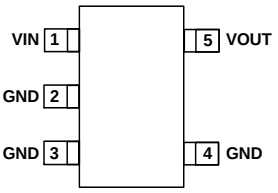
SO-8EP

(Top View)



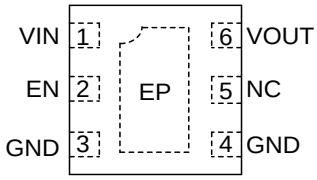
SOT25
(Package Code: W5)

(Top View)



SOT25
(Package Code: WR)

(Top View)



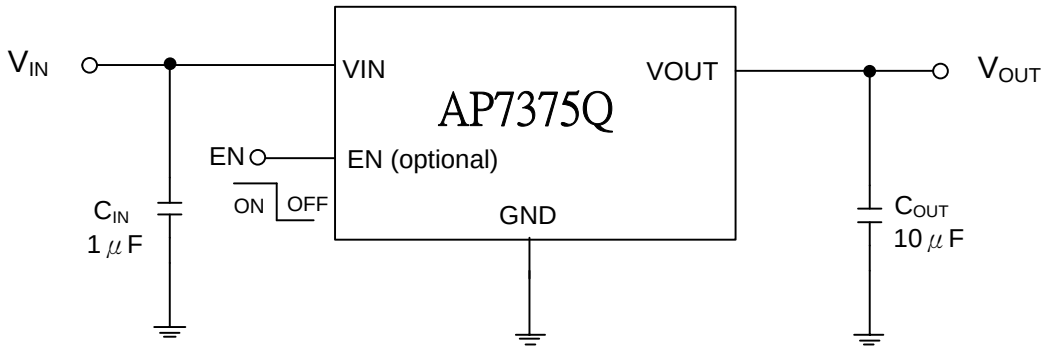
U-DFN2020-6 (SWP) (Type UXC)

Applications

- Powering MCUs and CAN/LIN transceivers
- Automotive head units
- EV and HEV battery management systems
- Body control modules
- Transmission control units (TCUs)

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

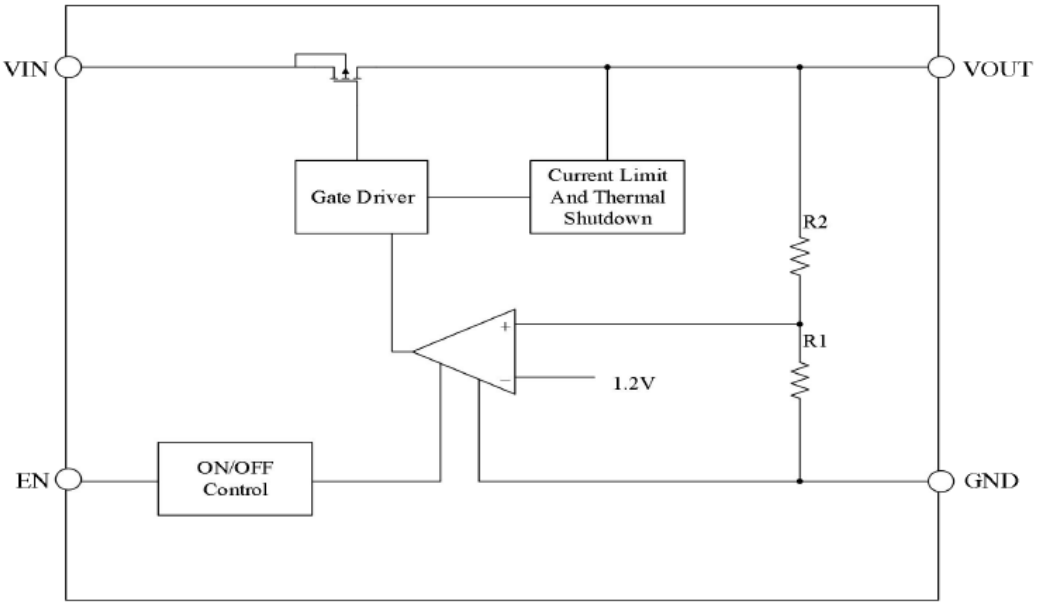
Typical Applications Circuit



Pin Descriptions

Pin Number					Pin Name	Function
SOT89	SO-8EP	SOT25 (Package Code: W5)	SOT25 (Package Code: WR)	U-DFN2020-6 (SWP) (Type UXC)		
3	8	1	1	1	VIN	Input voltage
2	5	2	2, 3, 4	3, 4	GND	Ground
—	7	3	—	2	EN	Enable
1	1	5	5	6	VOUT	Regulated output voltage
—	2, 3, 4, 6	4	—	5	NC	Not connected internally, recommend connect to GND to maximize PCB copper for thermal dissipation.
—	EP	—	—	EP	Expose Pad	In PCB layout, prefer to use large copper area to cover this pad for better thermal dissipation, then connect this area to GND or leave it open. However, do not use it as GND electrode function alone

Functional Block Diagram



Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating		Unit
V_{IN}	Supply Input Voltage	-0.3 to 55		V
V_{OUT}	Regulated Output Voltage	-0.3 to 6		V
V_{EN}	EN to GND	-0.3 to 55		V
I_{OUT}	Output Current	Internally limited		mA
T_{LEAD}	Lead Temperature (Soldering, 10sec)	+260		°C
T_J	Operating Junction Temperature	+150		°C
T_A	Operating Ambient Temperature	-40 to +125		°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	SOT89	94.5	°C/W
		SO-8EP	47.7	
		SOT25	135.5	
		U-DFN2020-6 (SWP) (Type UXC)	99.5	
T_{STG}	Storage Temperature Range	-40 to +150		°C
CDM	ESD (Charge Device Model)	±1.5		kV
HBM	ESD (Human Body Model)	3		kV

Note: 4. a). Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
b). Ratings apply to ambient temperature at +25°C. The JEDEC STD.51 High-K board design used to derive this data was a 3 inch x 3 inch multilayer board with 1oz. internal power and ground planes and 2oz. copper traces on the top and bottom of the board.

Recommended Operating Conditions

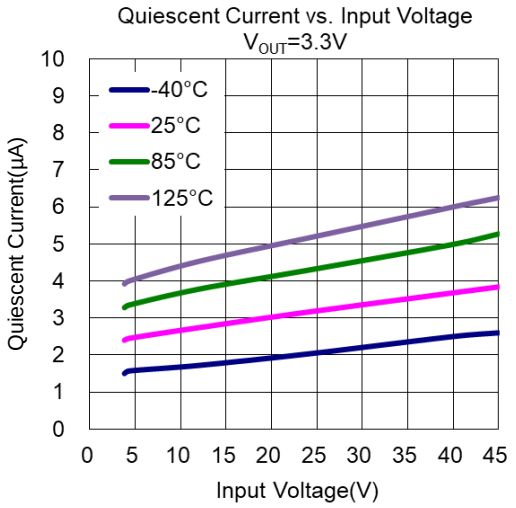
Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Supply Input Voltage	3.0	—	45	V
V_{OUT}	Output Voltage	—	—	5	V
T_J	Operating Junction Temperature	-40	—	+125	°C
C_{IN}	Input Capacitor	—	1	—	µF
C_{OUT}	Output Capacitor	1	10	—	µF

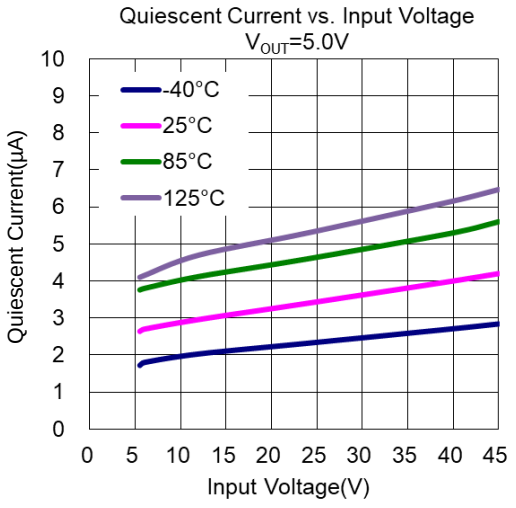
Electrical Characteristics (T_A = -40°C to +125°C, I_{OUT} = 1mA, C_{IN} = 1µF, C_{OUT} = 10µF ceramic capacitor, V_{IN} = V_{OUTNOM} +2.0V)

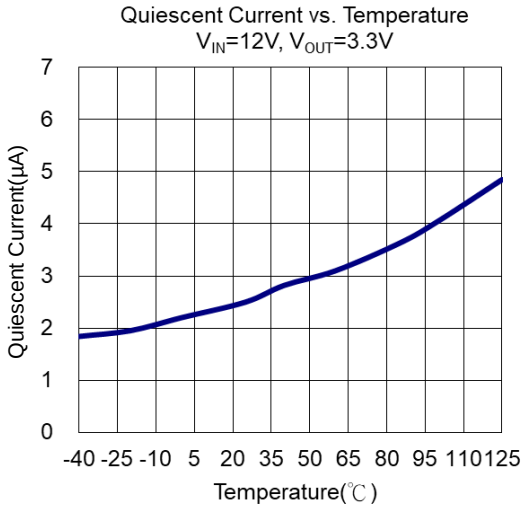
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage	—	3	—	45	V
I_{GND}	Quiescent Current	V_{IN} = 12V, No load	—	2.1	8	µA
V_{OUT}	Output Voltage	V_{IN} = 12V, I_{OUT} = 10mA	V_{OUT} x 98%	—	V_{OUT} x 102%	V
I_{OUT_MAX}	Output Current	—	300	350	—	mA
V_{DROP}	Dropout Voltage (Note 5)	I_{OUT} = 10mA, V_{IN} = V_{OUTNOM} – 0.1V	—	35	80	mV
		I_{OUT} = 100mA, V_{IN} = V_{OUTNOM} – 0.1V	—	350	580	mV
		I_{OUT} = 300mA, V_{IN} = V_{OUTNOM} – 0.1V T_A = +25°C	—	1200	1400	mV
$\Delta V_{OUT}(\Delta I_{OUT})$	Load Regulation (Note 6)	V_{IN} = 12V, 1mA ≤ I_{OUT} ≤ 100mA	—	0.02	0.025	%/mA
$\Delta V_{OUT}(\Delta V_{IN})$	Line Regulation	V_{OUTNOM} + 2V ≤ V_{IN} ≤ 45V I_{OUT} = 1mA	—	0.01	0.02	%/V
I_{LIMIT}	Current Limit	—	—	500	—	mA
T_{OTSD}	Thermal Shutdown Temperature	—	—	+150	—	°C
T_{HYOTSD}	Thermal Shutdown Hysteresis	—	—	+10	—	°C
PSRR	Power Supply Rejection Ratio	V_{IN} = 12V, I_{OUT} = 10mA V_{OUT} = 3.3V@1kHz	—	85	—	dB
V_n	Output Noise Voltage	BW = 10Hz to 100kHz, I_{OUT} = 30mA	—	120	—	µVrms
VENH	EN High Level	Enabled	1	—	—	V
VENL	EN Low Level	Disabled	—	—	0.4	V
θ_{JC}	Thermal Resistance Junction to Case (Note 4)	SOT89	—	43.7	—	°C/W
		SO-8EP	—	17.4	—	
		SOT25	—	36.7	—	
		U-DFN2020-6 (SWP) (Type UXC)	—	15.8	—	

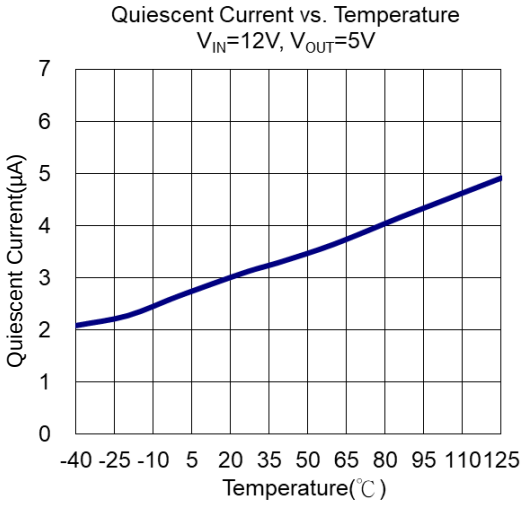
Notes:
4. a). Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
   b). Ratings apply to ambient temperature at +25°C. The JEDEC STD.51 High-K board design used to derive this data was a 3 inch x 3 inch multilayer board with 1oz. internal power and ground planes and 2oz. copper traces on the top and bottom of the board.
5. Dropout voltage is the voltage difference between the input and output at which the output voltage drops 100mV below its nominal value. This parameter only applies to output voltages above 3.0V since minimum V_{IN} = 3.0V.
6. The AP7375Q internal circuitry is not fully operational until V_{IN} is at least the greater of 3V or (V_{OUT} + $V_{DROPOUT(MAX)}$).

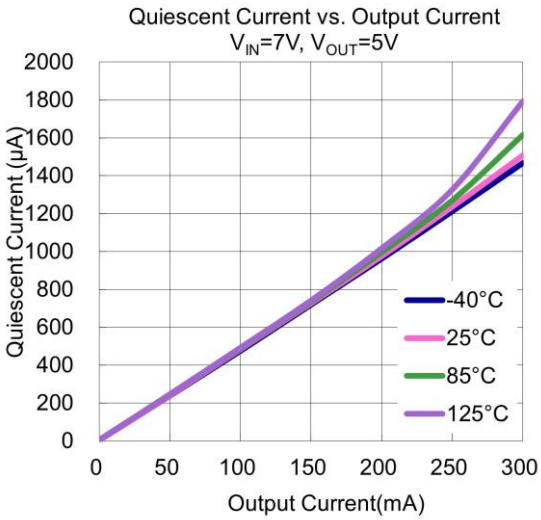
Performance Characteristics



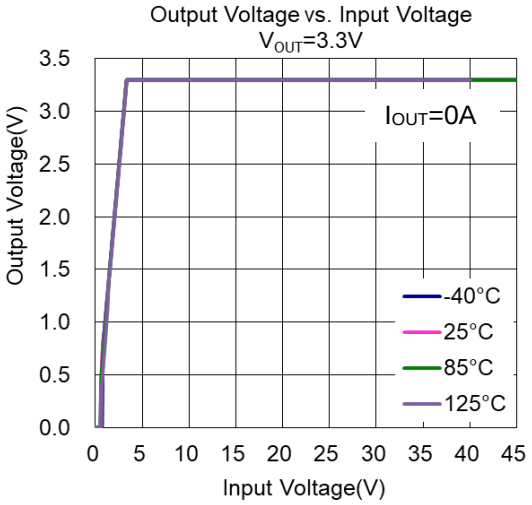


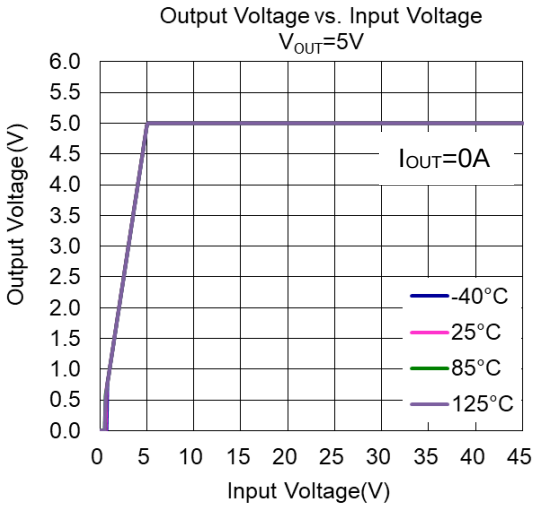


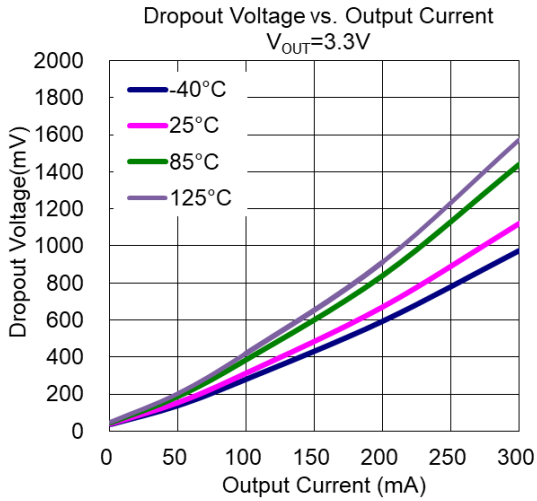


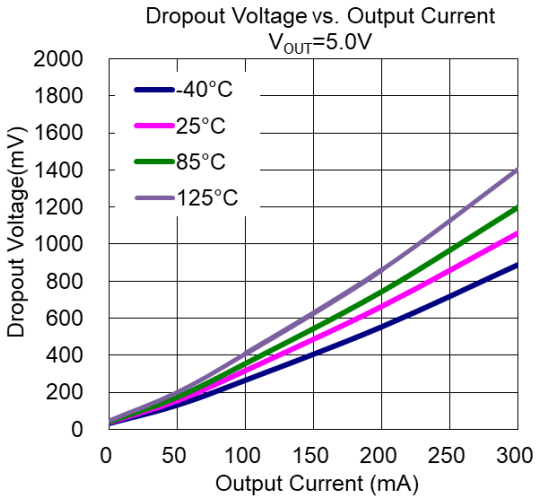


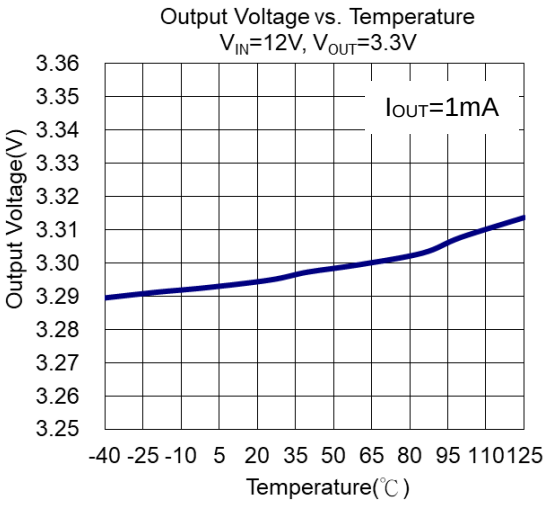
Typical Characteristics

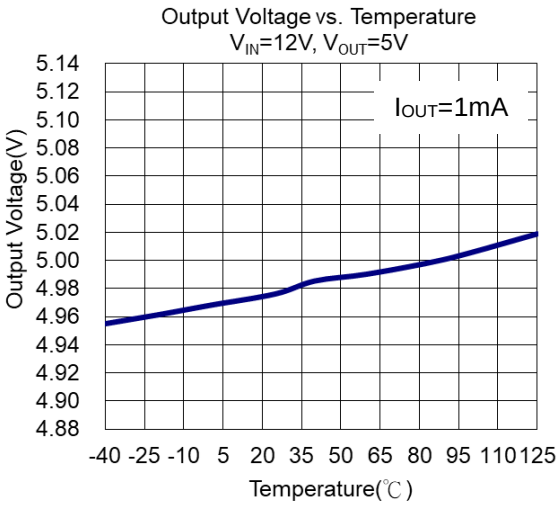












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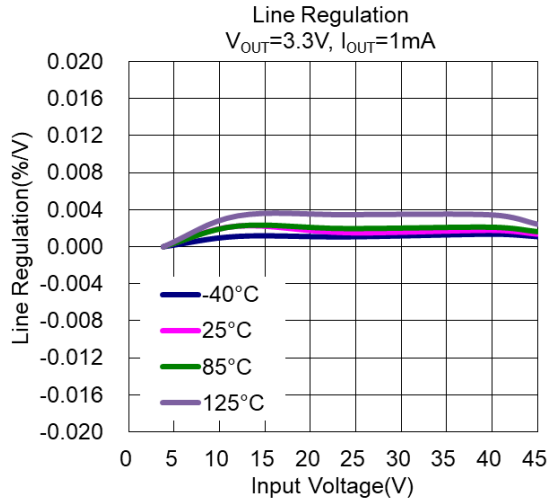

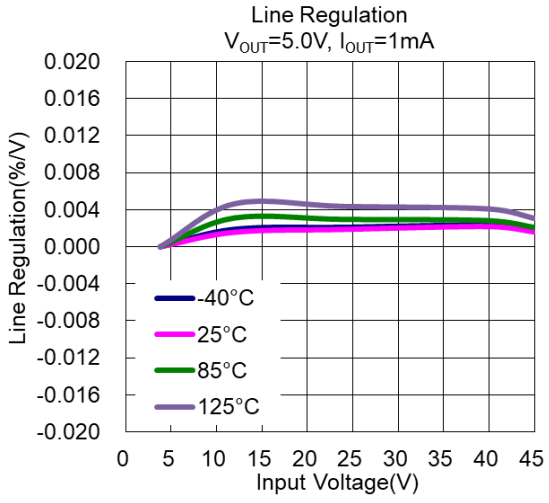

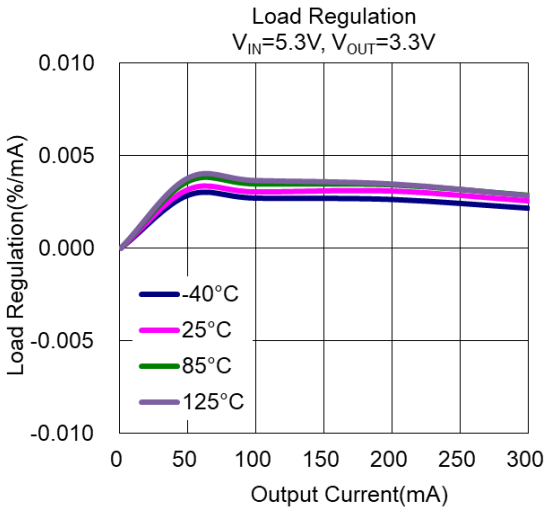

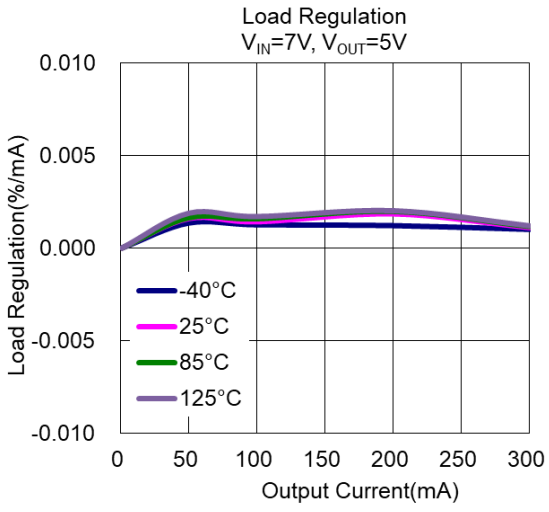

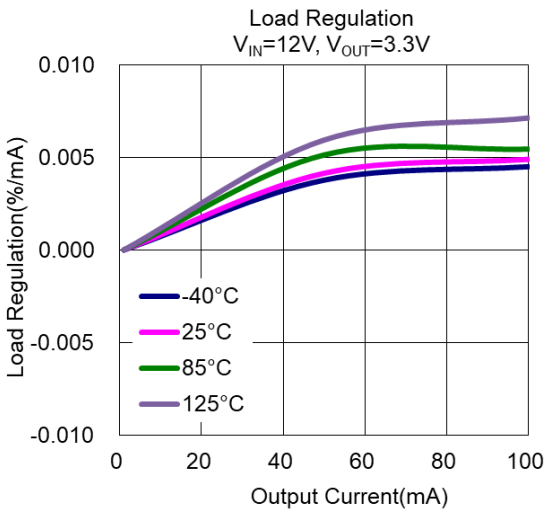

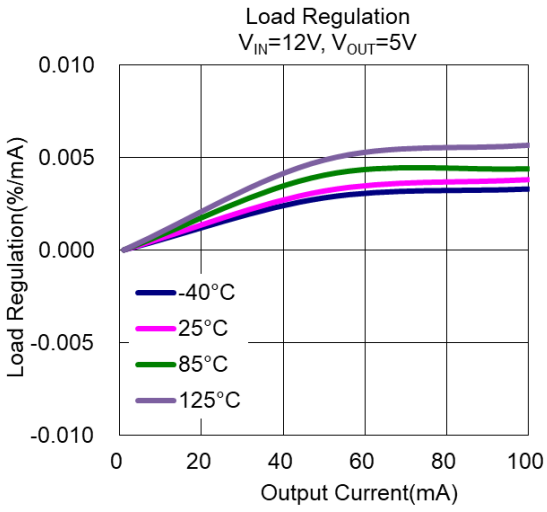

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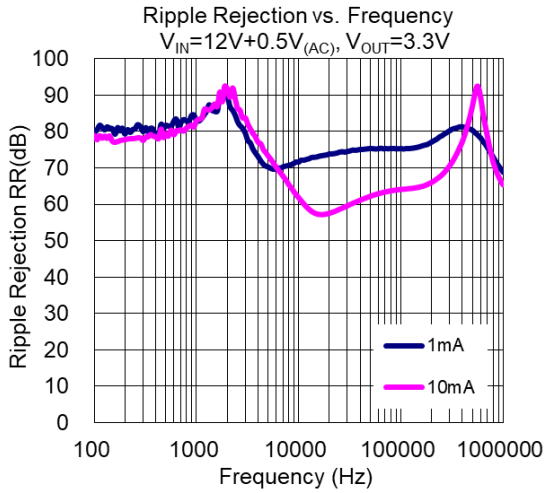
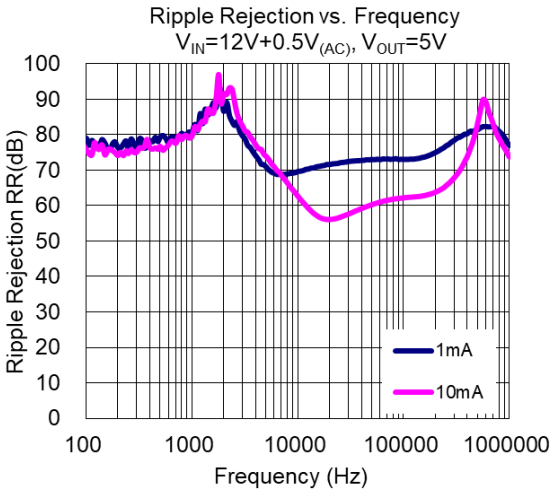
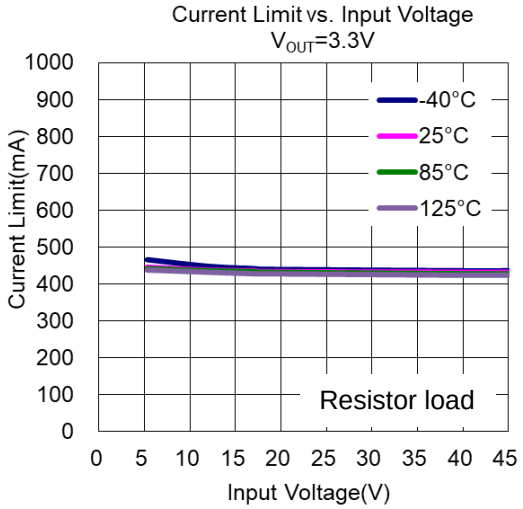
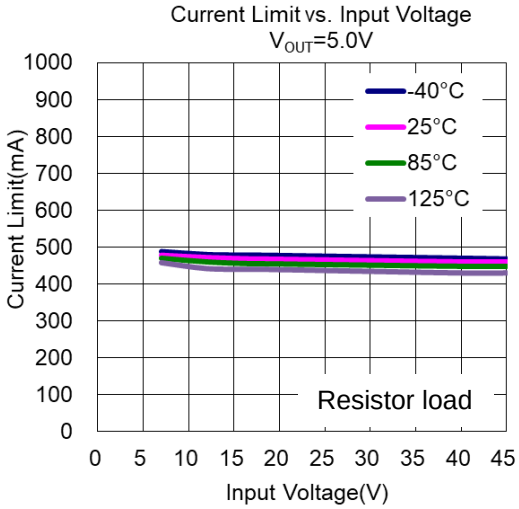
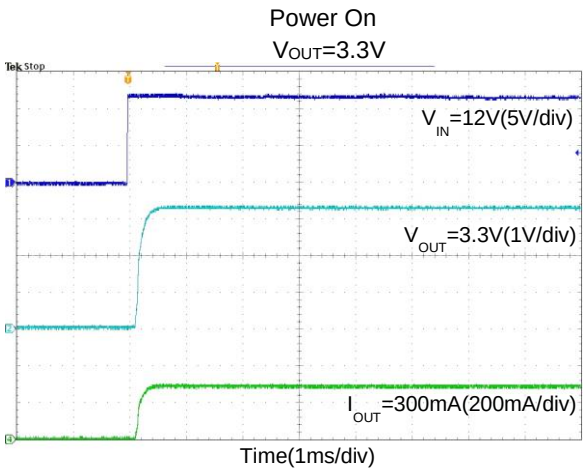
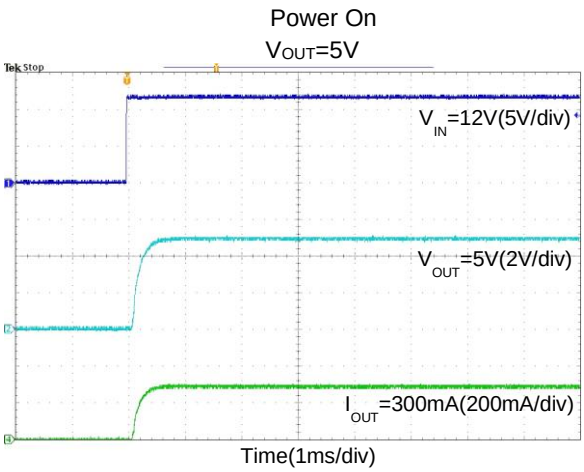






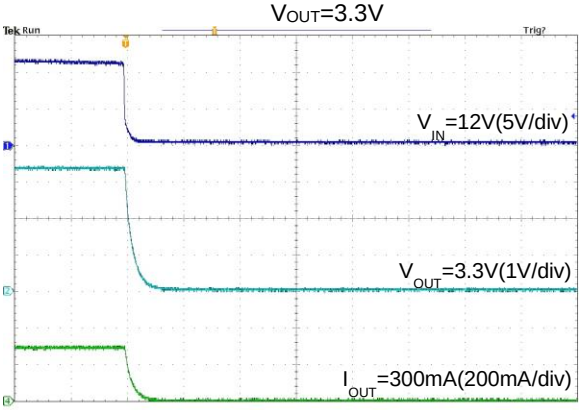






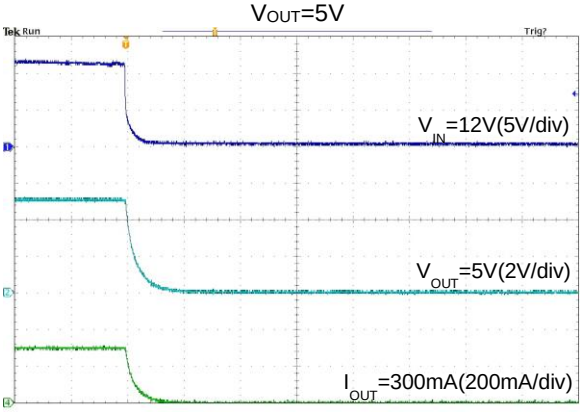
Typical Characteristics (continued)

Power Off
V_{OUT}=3.3V



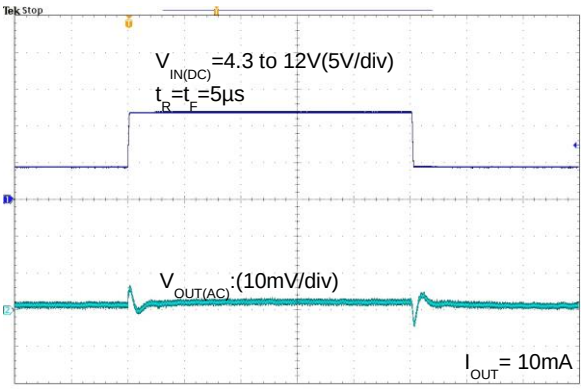
Time(1ms/div)

Power Off
V_{OUT}=5V



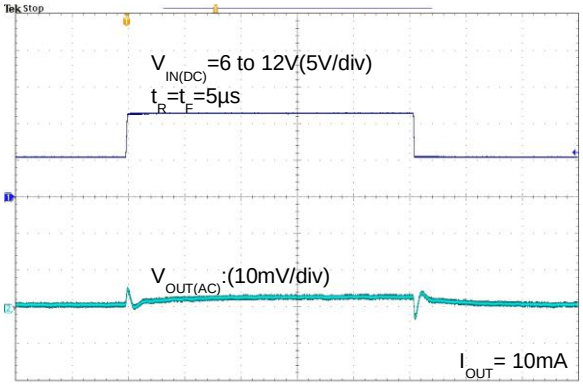
Time(1ms/div)

Line Transient Response
V_{OUT}=3.3V



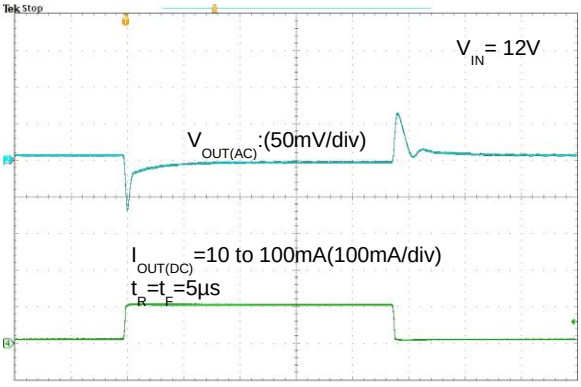
Time:200µs/div

Line Transient Response
V_{OUT}=5V



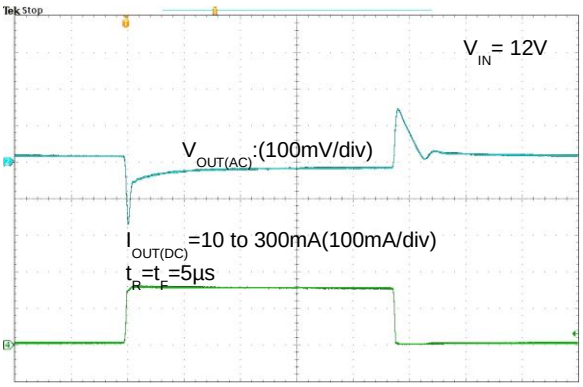
Time:200µs/div

Load Transient Response
V_{OUT}=3.3V



Time:200µs/div

Load Transient Response
V_{OUT}=3.3V

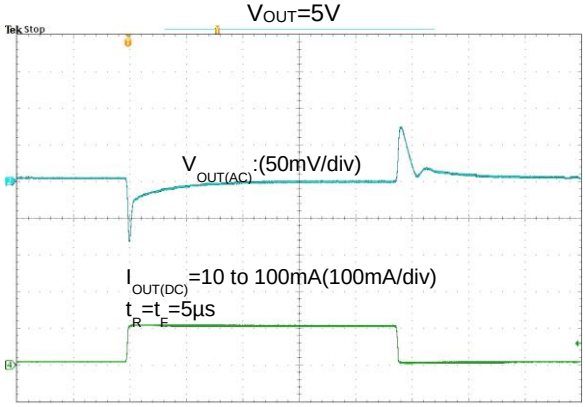


Time:200µs/div

V_{IN}= 12V

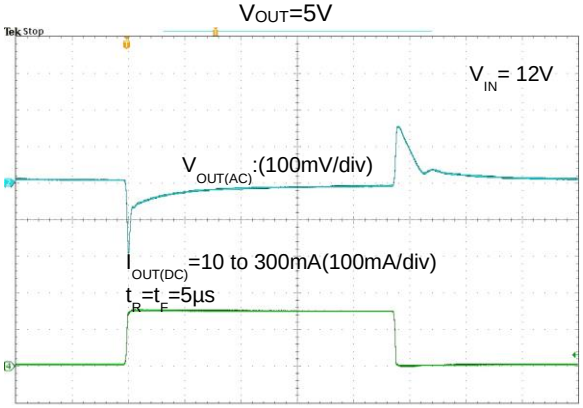
Typical Characteristics (continued)

Load Transient Response
V_{OUT}=5V



Time:200µs/div

Load Transient Response
V_{OUT}=5V



Time:200µs/div

Application Information

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended minimum output capacitance is 1µF. A ceramic capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place the output capacitor as close as possible to VOUT and GND pins.

Input Capacitor

A 1µF ceramic capacitor is recommended to connect between VIN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to ensure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

Current-Limit and Short-Circuit Protection

When output current at VOUT pin is higher than the current-limit threshold or the VOUT pin directly shorts to GND, current-limit protection will be triggered and clamp the output current at a pre-designed level to prevent overcurrent and thermal damage.

Thermal Protection

The AP7375Q has internal thermal sense and protection circuits. When excessive power dissipation happens on the device, such as short circuit at the output pin or very heavy load current with a large voltage drop across the device, the internal thermal protection circuit will be triggered, shutting down the power MOSFET to prevent the LDO from damage. As soon as the excessive thermal condition is removed and the temperature of the device drops down, the thermal protection circuit will release the control of the power MOSFET, and the LDO device returns to normal operation.

Layout Considerations

For good ground loop and stability, the input and output capacitors should be located close to the input, output, and ground pins of the device. The regulator ground pin should be connected to the external circuit ground to reduce voltage drop caused by trace impedance. Ground plane is generally used to reduce trace impedance. Wide trace should be used for large current paths from V_{IN} to V_{OUT}, and load circuit.

Ordering Information

AP7375Q - XX X - X

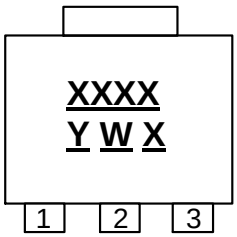
Output Voltage	Package	Packing
18 : 1.8V 30 : 3.0V 33 : 3.3V 50 : 5.0V	Y : SOT89 SP: SO-8EP W5: SOT25 WR: SOT25 FDCW: U-DFN2020-6 (SWP) (Type UXC)	7/13: Tape & Reel

Orderable Part Number	Part Number Suffix	Package Code	Package	Packing	
				Qty.	Carrier
AP7375Q-XXY-13	-13	Y	SOT89	2,500	13” Tape & Reel
AP7375Q-XXSP-13	-13	SP	SO-8EP	2,500	13” Tape & Reel
AP7375Q-XXW5-7	-7	W5	SOT25	3,000	7” Tape & Reel
AP7375Q-XXWR-7	-7	WR	SOT25	3,000	7” Tape & Reel
AP7375Q-XXFDCW-7	-7	FDCW	U-DFN2020-6 (SWP) (Type UXC)	3,000	7” Tape & Reel

Marking Information

(1) SOT89

(Top View)

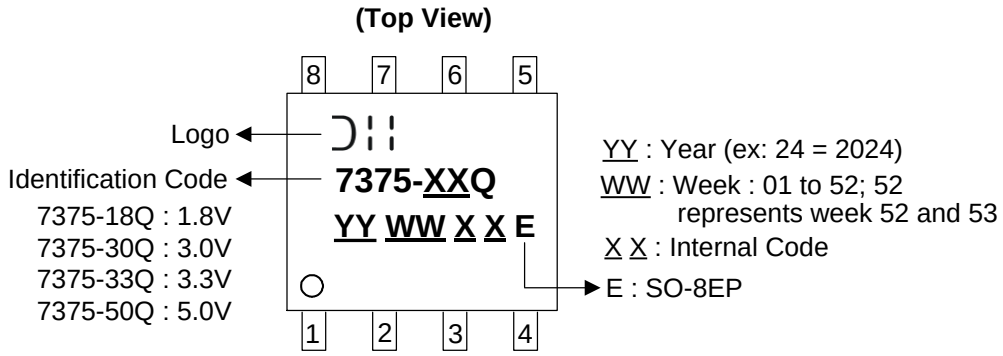


XXXX : Identification Code
Y : Year : 0 to 9 (ex: 4 = 2024)
W : Week : A to Z : week 1 to 26;
a to z : week 27 to 52;
z represents week 52 and 53
X : Internal Code

Orderable Part Number	Package	Identification Code
AP7375Q-18Y-13	SOT89	H5AQ
AP7375Q-30Y-13	SOT89	H5BQ
AP7375Q-33Y-13	SOT89	H5CQ
AP7375Q-50Y-13	SOT89	H5DQ

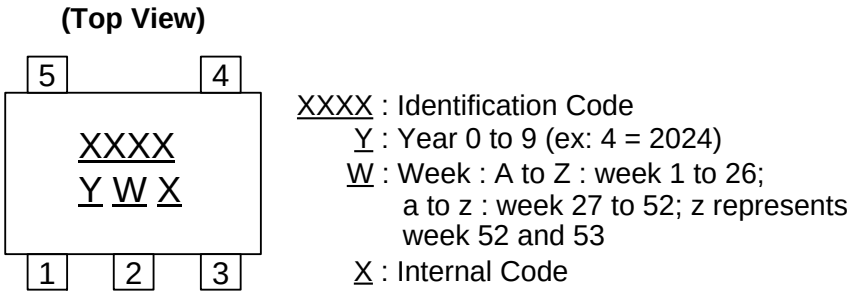
Marking Information (continued)

(2) SO-8EP



Orderable Part Number	Package	Identification Code
AP7375Q-18SP-13	SO-8EP	7375-18Q
AP7375Q-30SP-13	SO-8EP	7375-30Q
AP7375Q-33SP-13	SO-8EP	7375-33Q
AP7375Q-50SP-13	SO-8EP	7375-50Q

(3) SOT25

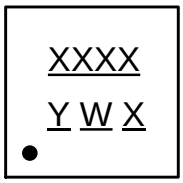


Orderable Part Number	Package	Identification Code
AP7375Q-18W5-7	SOT25	H5EQ
AP7375Q-30W5-7	SOT25	H5FQ
AP7375Q-33W5-7	SOT25	H5GQ
AP7375Q-50W5-7	SOT25	H5HQ
AP7375Q-18WR-7	SOT25	H5AQ
AP7375Q-30WR-7	SOT25	H5BQ
AP7375Q-33WR-7	SOT25	H5CQ
AP7375Q-50WR-7	SOT25	H5DQ

Marking Information (continued)

(4) U-DFN2020-6 (SWP) (Type UXC)

(Top View)



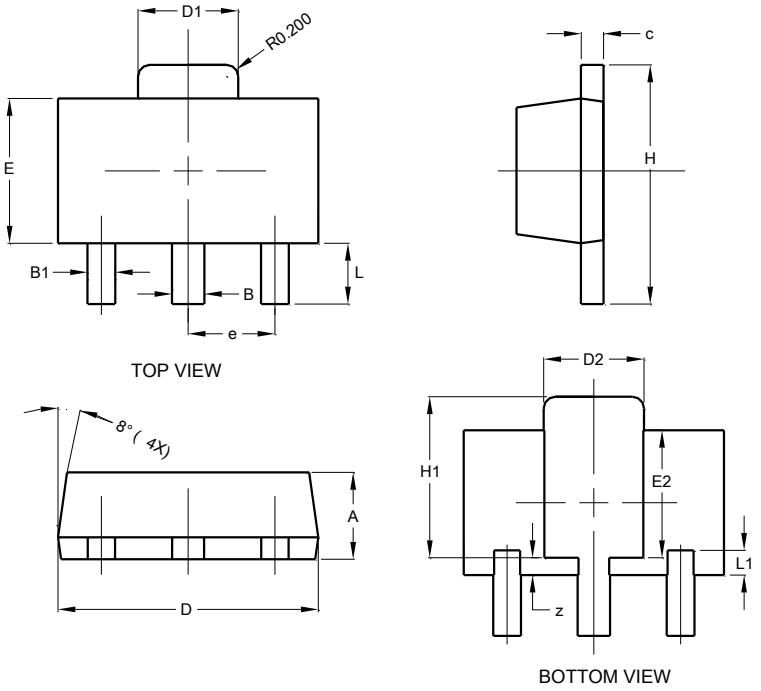
XXXX : Identification Code
Y : Year : 0 to 9 (ex: 4 = 2024)
W : Week : A to Z : week 1 to 26;
a to z : week 27 to 52; z represents week 52 and 53
X : Internal Code

Orderable Part Number	Package	Identification Code
AP7375Q-18FDCW-7	U-DFN2020-6 (SWP) (Type UXC)	H5EQ
AP7375Q-30FDCW-7	U-DFN2020-6 (SWP) (Type UXC)	H5FQ
AP7375Q-33FDCW-7	U-DFN2020-6 (SWP) (Type UXC)	H5GQ
AP7375Q-50FDCW-7	U-DFN2020-6 (SWP) (Type UXC)	H5HQ

Package Outline Dimensions

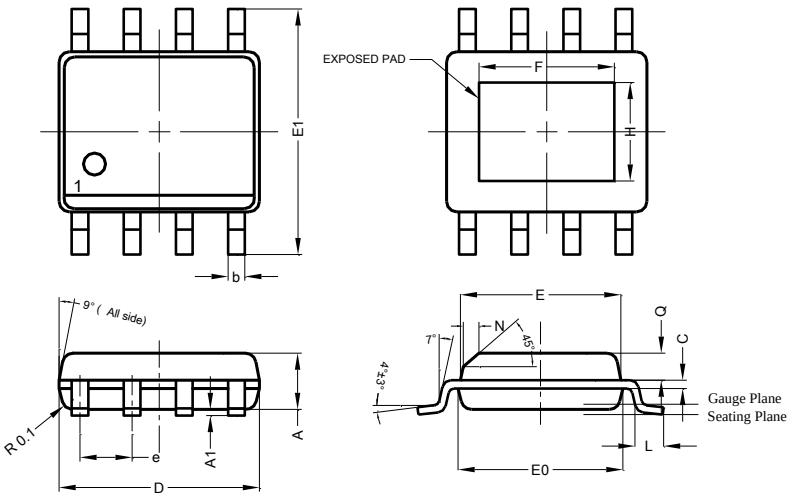
Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) SOT89



SOT89			
Dim	Min	Max	Typ
A	1.40	1.60	1.50
B	0.50	0.62	0.56
B1	0.42	0.54	0.48
c	0.35	0.43	0.38
D	4.40	4.60	4.50
D1	1.62	1.83	1.733
D2	1.61	1.81	1.71
E	2.40	2.60	2.50
E2	2.05	2.35	2.20
e	-	-	1.50
H	3.95	4.25	4.10
H1	2.63	2.93	2.78
L	0.90	1.20	1.05
L1	0.327	0.527	0.427
z	0.20	0.40	0.30
All Dimensions in mm			

(2) SO-8EP

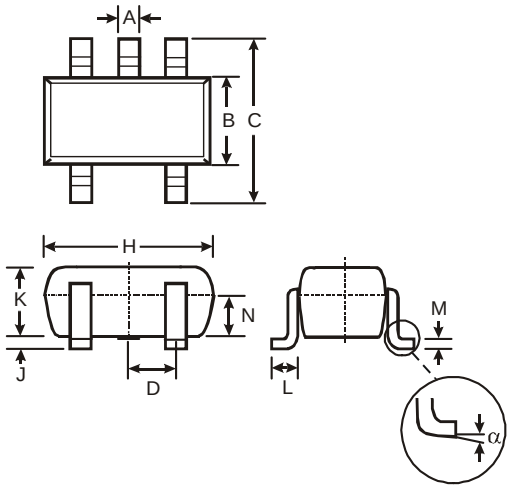


SO-8EP			
Dim	Min	Max	Typ
A	1.40	1.50	1.45
A1	0.00	0.13	-
b	0.30	0.50	0.40
C	0.15	0.25	0.20
D	4.85	4.95	4.90
E	3.80	3.90	3.85
E0	3.85	3.95	3.90
E1	5.90	6.10	6.00
e	-	-	1.27
F	2.75	3.35	3.05
H	2.11	2.71	2.41
L	0.62	0.82	0.72
N	-	-	0.35
Q	0.60	0.70	0.65
All Dimensions in mm			

Package Outline Dimensions (continued)

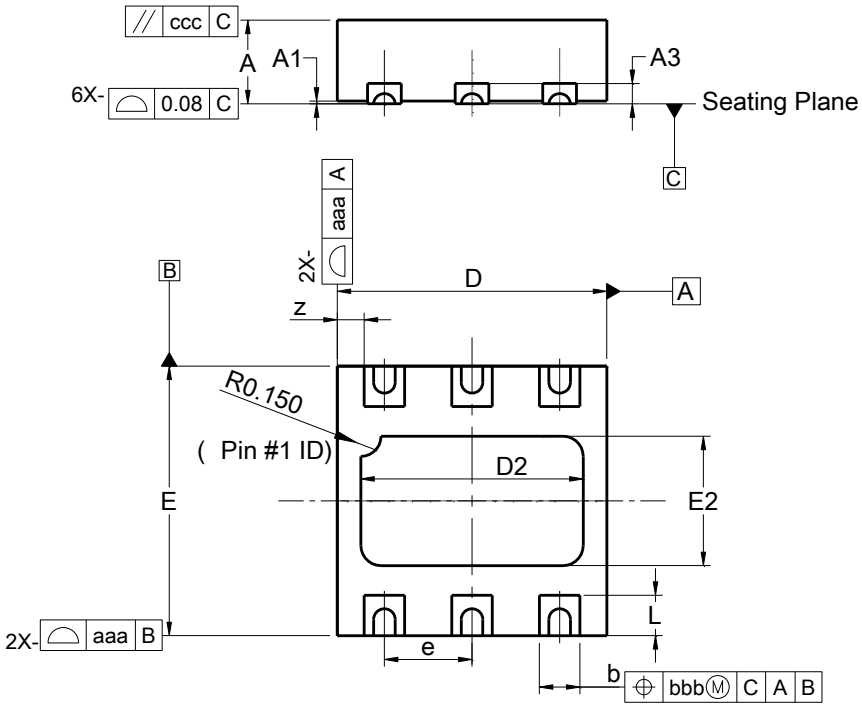
Please see http://www.diodes.com/package-outlines.html for the latest version.

(3) SOT25



SOT25			
Dim	**Min**	**Max**	**Typ**
A	0.35	0.50	0.38
B	1.50	1.70	1.60
C	2.70	3.00	2.80
D	-	-	0.95
H	2.90	3.10	3.00
J	0.013	0.10	0.05
K	1.00	1.30	1.10
L	0.35	0.55	0.40
M	0.10	0.20	0.15
N	0.70	0.80	0.75
α	0°	8°	-
All Dimensions in mm			

(4) U-DFN2020-6 (SWP) (Type UXC)

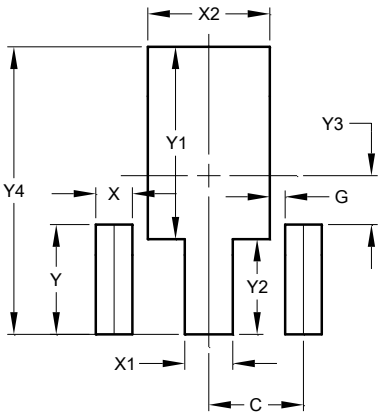


U-DFN2020-6 (SWP) (Type UXC)			
Dim	**Min**	**Max**	**Typ**
A	0.57	0.63	0.60
A1	0.00	0.05	0.02
A3	—	—	0.13
b	0.25	0.35	0.30
D	1.95	2.075	2.00
D2	1.55	1.75	1.65
E	1.95	2.075	2.00
E2	0.86	1.06	0.96
e	—	—	0.65
L	0.25	0.35	0.30
z	—	—	0.20
aaa	0.25		
bbb	0.10		
ccc	0.10		
All Dimensions in mm			

Suggested Pad Layout

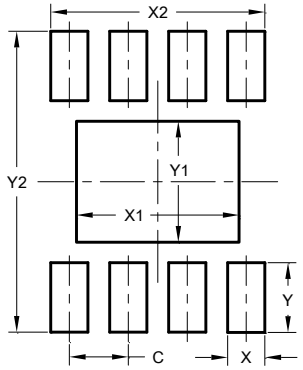
Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) SOT89



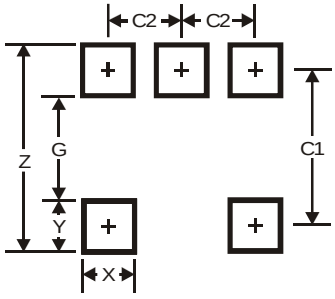
Dimensions	Value (in mm)
C	1.500
G	0.244
X	0.580
X1	0.760
X2	1.933
Y	1.730
Y1	3.030
Y2	1.500
Y3	0.770
Y4	4.530

(2) SO-8EP



Dimensions	Value (in mm)
C	1.270
X	0.802
X1	3.502
X2	4.612
Y	1.505
Y1	2.613
Y2	6.500

(3) SOT25

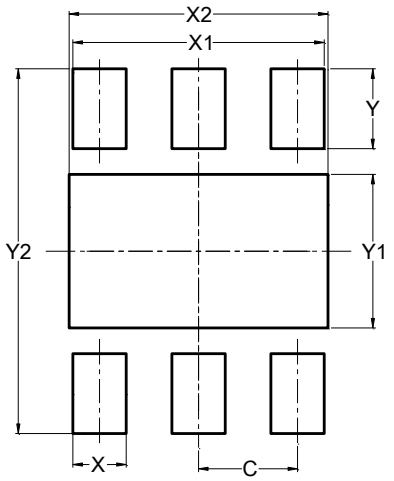


Dimensions	Value (in mm)
Z	3.20
G	1.60
X	0.55
Y	0.80
C1	2.40
C2	0.95

Suggested Pad Layout (continued)

Please see http://www.diodes.com/package-outlines.html for the latest version.

(4) U-DFN2020-6 (SWP) (Type UXC)



Dimensions	Value (in mm)
C	0.650
X	0.350
X1	1.650
X2	1.700
Y	0.525
Y1	1.010
Y2	2.400

Mechanical Data

- Moisture Sensitivity: Level 1 Per J-STD-020
- Terminals:
  - SOT89/ SO-8EP/ SOT25: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
  - U-DFN2020-6 (SWP) (Type UXC): Finish – NiPdAu over Copper Leads, Solderable per MIL-STD-202, Method 208 e4
- Weight:
  - SOT89: 0.054 grams (Approximate)
  - SO-8EP: 0.075 grams (Approximate)
  - SOT25: 0.018 grams (Approximate)
  - U-DFN2020-6 (SWP) (Type UXC): 0.007 grams (Approximate)

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