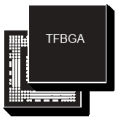
STM32MP251C/F STM32MP253C/F STM32MP255C/F STM32MP257C/F

Datasheet

Arm® based dual Cortex®-A35 1.5 GHz + Cortex®-M33 MPU, AI, 3D GPU, video enc./dec., TFT/DSI/LVDS, USB 3.0, PCIe®, crypto



VFBGA361 (10 × 10 mm) pitch 0.5 mm
VFBGA424 (14 × 14 mm) pitch 0.5 mm
TFBGA436 (18 × 18 mm) pitch 0.8 mm

Product summary	
STM32MP25xC/F	STM32MP251C, STM32MP251F, STM32MP253C, STM32MP253F, STM32MP255C, STM32MP255F, STM32MP257C, STM32MP257F

Features

Includes ST state-of-the-art patented technology.

Cores

- Up to 64-bit dual-core Arm® Cortex®-A35
  - Up to 1.5 GHz
  - 32-Kbyte I + 32-Kbyte D level 1 cache for each core
  - 512-Kbyte unified level 2 cache
  - Arm® NEON™ and Arm® TrustZone®
- 32-bit Arm® Cortex®-M33 with FPU/MPU
  - Up to 400 MHz
  - L1 16-Kbyte I / 16-Kbyte D
  - Arm® TrustZone®
- 32-bit Arm® Cortex®-M0+ in SmartRun domain
  - Up to 200 MHz (up to 16 MHz in autonomous mode)

Memories

- External DDR memory up to 4 Gbytes
  - Up to DDR3L-2133 16/32-bit
  - Up to DDR4-2400 16/32-bit
  - Up to LPDDR4-2400 16/32-bit
- 808-Kbyte internal SRAM: 256-Kbyte AXI SYSRAM, 128-Kbyte AXI video RAM or SYSRAM extension, 256-Kbyte AHB SRAM, 128-Kbyte AHB SRAM with ECC in backup domain, 8-Kbyte SRAM with ECC in backup domain, 32 Kbytes in SmartRun domain
- Two Octo-SPI memory interfaces
- Flexible external memory controller with up to 16-bit data bus: parallel interface to connect external ICs, and SLC NAND memories with up to 8-bit ECC

Security/safety

- Secure boot, TrustZone® peripherals, active tamper, environmental monitors, display secure layers, hardware accelerators
- Complete resource isolation framework

Reset and power management

- 1.71 to 1.95 V and 2.7/3.0 to 3.6 V multiple section I/O supply
- POR, PDR, PVD, and BOR
- On-chip LDO and power-switches for RETRAM, BKPSRAM, V_{SW}, and SmartRun domains
- Dedicated supplies for Cortex®-A35 and GPU/NPU (if present)
- Internal temperature sensors
- Low-power modes: Sleep, Stop, and Standby
- DDR memory retention in Standby mode

Prerelease product(s)

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- Controls for PMIC companion chip

Low-power consumption

Clock management

- Internal oscillators: 64 MHz HSI, 4/16 MHz MSI, 32 kHz LSI
- External oscillators: 16-48 MHz HSE, 32.768 kHz LSE
- Up to 8× PLLs with fractional mode

General-purpose inputs/outputs

- Up to 172 secure I/O ports with interrupt capability
  - Up to 6 wake-up inputs
  - Up to 8 tamper input pins + 8 active tampers output pins

Interconnect matrix

- Bus matrices
  - 128-, 64-, 32-bit STNoC interconnect, up to 600 MHz
  - 32-bit Arm® AMBA® AHB interconnect, up to 400 MHz

4 DMA controllers to unload the CPU

- 48 + 4 physical channels in total
- 3× dual master port, high-performance, general-purpose, direct memory access controller (HPDMA), 16 channels each
- 1× low-power DMA controller with 4 channels in SmartRun domain

Up to 51 communication peripherals

- 8× I^2C FM+ (1 Mbit/s, SMBus/PMBus®)
- 4× I^3C (12.5 Mbit/s)
- 5× UART + 4× USART (12.5 Mbit/s, ISO7816 interface, LIN, IrDA, SPI) + 1× LPUART
- 8× SPI (50 Mbit/s, including 3 with full duplex I^2S audio class accuracy via internal audio PLL or external clock)
- 4× SAI (stereo audio: I^2S, PDM, SPDIF Tx)
- SPDIF Rx with 4 inputs
- 3× SDMMC up to 8-bit (SD/e•MMC™/SDIO)
- Up to 3× CAN controllers supporting CAN FD protocol, out of which one supports time-triggered CAN (TTCAN)
- 1× USB 2.0 high-speed Host with embedded 480 Mbits/s PHY
- 1× USB 2.0/3.0 high-speed/SuperSpeed dual role data with embedded 480 Mbits/s and 5 Gbits/s PHY (5 Gbits/s PHY shared with PCI Express)
- 1× USB Type-C® Power Delivery control with two CC lines PHY
- 1 × PCI Express with embedded 5 Gbits/s PHY (PHY shared with USB 3.0 SuperSpeed)
- Up to 3× Gigabit Ethernet interfaces
  - 1× Gigabit Ethernet GMAC with one PHY interface (optional)
  - 1× Gigabit Ethernet GMAC with one external PHY interface, optionally internally connected to one embedded Ethernet switch providing two external PHY interfaces
  - TSN, IEEE 1588v2 hardware, MII/RMII/RGMII

Prerelease product(s)

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- Camera interface #1 (5 Mpixels @30 fps)
  - MIPI CSI-2®, 2× data lanes up to 2.5 Gbit/s each
  - 8- to 16-bit parallel, up to 120 MHz
  - RGB, YUV, JPG, RawBayer with basic ISP
  - Lite-ISP, demosaicing, downscaling, cropping, 3 pixel pipelines
- Camera interface #2 (1 Mpixels @15 fps)
  - 8- to 14-bit parallel, up to 80 MHz
  - RGB, YUV, JPG
  - Cropping
- Digital parallel interface up to 16-bit input or output

7 analog peripherals

- 3 × ADCs with 12-bit max. resolution (up to 5 Msps each, up to 23 channels)
- Internal temperature sensor (DTS)
- 1× multifunction digital filter (MDF) with up to 8 channels/8 filters
- 1× audio digital filter (ADF) with 1 filter and sound activity detection
- Internal (VREFBUF) or external ADC reference V_{REF+}

Graphics

- Optional 3D GPU: VeriSilicon® - Up to 900 MHz
  - OpenGL® ES 3.2.8 - Vulkan 1.2
  - OpenCL™ 3.0, OpenVX™ 1.3
  - Up to 150 Mtriangle/s, 900 Mpixel/s
- LCD-TFT controller, up to 24-bit // RGB888
  - Up to FHD (1920 × 1080) @60 fps
  - 3 layers including a secure layer
  - YUV support, 90° output rotation
- MIPI DSI®, 4× data lanes, up to 2.5 Gbit/s each
  - Up to QXGA (2048 × 1536) @60 fps
- Optional FPD-1 and OpenLDI JEIDA/VESA (LVDS), up to 2× links of 4× data lanes, up to 1.1 Gbit/s per lane
  - Up to QXGA (2048 × 1536) @60 fps

Artificial intelligence

- Optional NPU: VeriSilicon® - Up to 900 MHz
  - TensorFlowLite - ONNX - Linux NN

Video processing

- Optional hardware video encoder and decoder up to 600 MHz
  - H264/VP8 up to FHD (1920×1080) @60 fps
  - JPEG up to 500 Mpixel/s
  - 128 Kbytes of video RAM

Up to 34 timers and 7 watchdogs

- 4× 32-bit timers with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
- 3× 16-bit advanced motor control timers
- 10× 16-bit general-purpose timers (including 2 basic timers without PWM)
- 5× 16-bit low-power timers
- Secure RTC with subsecond accuracy and hardware calendar
- Up to 2× 4 Cortex®-A35 system timers (secure, non-secure, virtual, hypervisor)

Prerelease product(s)

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- 2× SysTick M33 timer (secure, non-secure)
- 1× SysTick M0+ timer
- 7× watchdogs (5× independent and 2× window)

Hardware acceleration

- AES-128, -192, -256, DES/TDES
- Secure AES-256 with SCA
- RSA, ECC, ECDSA with SCA
- HASH (SHA-1, SHA-224, SHA-256, SHA3), HMAC
- True random number generator
- CRC calculation unit
- “On-the-fly” DDR encryption/decryption (AES-128)
- “On-the-fly” OTFDEC Octo-SPI flash memory decryption (AES-128)

Debug mode

- Arm® CoreSight™ trace and debug: SWD and JTAG interfaces

12288-bit fuses including 96-bit unique ID

All packages are ECOPACK2 compliant

Prerelease product(s)

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1 Introduction

This document provides information on STM32MP25xC/F devices, such as description, functional overview, pin assignment and definition , electrical characteristics, packaging and ordering information.

It must be read in conjunction with the STM32MP25xC/F reference manual (RM0457).

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32MP25xC/F errata sheet (ES0598).

For information on the Arm® Cortex®- M33 core, refer to the Cortex®- M33 Technical Reference Manual, available from the www.arm.com website.

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2 Description

STM32MP25xC/F devices are based on the high-performance single or dual-core Arm® Cortex®-A35 64-bit RISC core operating at up to 1.5 GHz. The Cortex®-A35 processor includes a 32-Kbyte L1 instruction cache for each CPU, a 32-Kbyte L1 data cache for each CPU, and a 512-Kbyte L2 cache. The Cortex®-A35 processor uses a highly efficient 8-stage in-order pipeline that has been extensively optimized to provide full Armv8-A features while maximizing area and power efficiency.

STM32MP25xC/F devices also embed a Cortex®-M33 32-bit RISC core operating at up to 400 MHz frequency. The Cortex®-M33 core features a floating point unit (FPU) single precision which supports Arm® single-precision data-processing instructions, and data types. The Cortex®-M33 supports a full set of DSP instructions, TrustZone®, and a memory protection unit (MPU) which enhances application security.

The devices also embed a Cortex®-M0+ 32-bit RISC core operating at up to 200 MHz frequency (16 MHz when running from backup regulator). This processor is located in the SmartRun domain, and can be used to ensure very-low-power peripheral activity when all other processors and domains are stopped.

STM32MP25xC/F devices can also embed a 3D graphic processing unit (VeriSilicon®, OpenGL ES 3.2.8, Vulkan 1.2, OpenCL 3.0, OpenVX 1.3) running at up to 900 MHz, with performances up to 150 Mtriangle/s, 900 Mpixel/s.

The graphic processing unit can provide a neural processor unit (VeriSilicon®, TensorFlowLite, ONNX, Linux NN) running at up to 900 MHz.

STM32MP25xC/F devices provide an external SDRAM interface supporting external memories up to 32-Gbit density (4 Gbytes), 16- or 32-bit DDR3L up to 1066 MHz, 16- or 32-bit LPDDR4 or DDR4 up to 1200 MHz. The SDRAM content can be encrypted with AES-128.

The devices incorporate high-speed embedded memories: 808 Kbytes of internal SRAM (including 256-Kbyte AXI SYSRAM, 128-Kbyte AXI video SRAM (which can be used as general purpose), two banks of 128 Kbytes each of AHB SRAM, three banks of 8, 8, and 16 Kbytes of AHB SRAM in SmartRun domain, 128 Kbytes of AHB SRAM in backup domain, and 8 Kbytes of SRAM in backup domain), as well as an extensive range of enhanced I/Os and peripherals connected to APB buses, AHB buses, a 32-bit multi-AHB bus matrix, and a 128/64-bit multi-layer AXI interconnect supporting access to internal and external memories.

Each device offers three ADCs, a low-power secure RTC, 12 general-purpose 16-bit timers, 4 general-purpose 32-bit timers, three PWM timers for motor control, five low-power timers, and a true random number generator (RNG) , and cryptographic acceleration cells.

STM32MP25xC/F devices offer a video encoder and a video decoder.

The devices support 8 multi-function digital filters (MDF), and one dedicated audio-digital filter with sound-activity detection (ADF).

The devices feature the following standard and advanced communication interfaces.

Standard peripherals

- eight I2Cs
- four I3Cs
- four USARTs and five UARTs
- one low-power UART
- eight SPIs, three I2Ss full-duplex master/slave. The I2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock.
- four SAI serial audio interfaces
- one SPDIF Rx interface
- three SDMMC interfaces
- an USB 2.0 Host with embedded Hi-Speed PHY
- an USB 2.0/3.0 dual-role data with both Hi-Speed and 5Gbits/s SuperSpeed PHYs
- three FDCAN interfaces, including one supporting TTCAN mode (optional)
- two Gigabit Ethernet Interface, with TSN support (optional)
- one Gigabit Ethernet Switch connected to ETH1 and providing two external PHY interfaces, with TSN support (optional)

Advanced peripherals including

- a flexible memory control (FMC) interface
- two Octo-SPI flash memory interface , with on-the-fly content decryption

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- two camera interfaces for CMOS sensors, one with basic ISP, demosaicing and parallel or MIPI CSI interface
- an LCD-TFT display interface
- a MIPI DSI display interface
- an LVDS display interface (optional)

A comprehensive set of power-saving mode allows the design of low-power applications.

STM32MP25xC/F devices are proposed in various packages up to 436 balls with 0.5 mm to 0.8 mm pitch. The set of included peripherals can change with the selected device.

These features make STM32MP25xC/F devices suitable for a wide range of consumer, industrial, white goods and medical applications.

Figure 1 shows the general block diagram of STM32MP25xC/F devices.

Table 1. STM32MP25xC/F features and peripheral counts

Features			STM32MP25xC/F
Package			VFBGA361 (10×10 pitch 0.5 mm), VFBGA424 (14×14 pitch 0.5 mm), TFBGA436 (18×18 pitch 0.8 mm)(1)
CPU processor			Up to dual-core Cortex-A35 FPU Neon TrustZone, up to 1500 MHz(1)
ROM			128 Kbytes (only for Cortex-A35)
GPU			Optional VeriSilicon GC8000UL up to 900 MHz(1)
NPU			
MCU processor		-	Cortex-M33 FPU TrustZone
		Caches size	16-Kbyte data cache
			16-Kbyte instruction cache
		Frequency	400 MHz
SmartRun processor		-	Cortex-M0+
		Frequency	16 MHz
Video		Decoder (VDEC)	H264/VP8 up to 1080p60
		Encoder (VENC)	JPEG 500 Mpixel/s(1)
		Video RAM	Up to 128 Kbytes(1)
Embedded SRAM (808 Kbytes)		CPU system	Up to 384 Kbytes(1)
		MCU system	256 Kbytes (128 Kbytes tamper protected)
		MCU retention	128 Kbytes
		SmartRun domain	32 Kbytes
		Backup	8 Kbytes (tamper protected)
SDRAM	DDR3L	1066 MHz	Up to 4 Gbytes(1)
	DDR4	1200 MHz	
	LPDDR4	1200 MHz	
Backup registers			512 bytes (128 × 32-bits, tamper protected)
Timers	Advanced	16 bits	3
	General purpose	16 bits	8
		32 bits	4
	Basic	16 bits	2
	Low power	16 bits	5

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Features			STM32MP25xC/F
Timers	SysTick	24 bits	2 (Cortex-M33, secure and non-secure)
		24 bits	1 (Cortex-M0+)
	Cortex-A35 (CNT)	64 bits	Up to 2 × 4 (secure, non-secure, Virtual, Hypervisor)[1]
	RTC		1
	Watchdog		7 (5× independent, 2× window)
Communication Peripherals	SPI	Total	8
		having I2S	3
	I2C (with SMB/PMB support)		8
	I3C		4
	USART (Smartcard, SPI, IrDA, LIN) + UART (IrDA, LIN)[2]		4 + 5
	LPUART		1
	SAI		4 (up to 8 audio channels), with I2S master/ slave, PCM input, SPDIF-TX
	PCI Express (PCIE)		Yes, 1× TX + 1× RX, embedded 5 Gbit/s PHY
	USB	USB 2.0 Host (USBH)	1 port, embedded Hi-Speed PHY
		USB 2.0/3.0 Dual Role (USB3DR)[2]	Yes, embedded Hi-Speed and SuperSpeed 5 Gbps PHY
		Embedded PHYs	3 (2× Hi-Speed + 1x SuperSpeed 5 Gbps)
		Type-C support (UCPD)	Yes, includes two CC-lines embedded PHY
	SPDIFRX		4 inputs
	FDCAN		Up to 3[1]
SDMMC (SD, SDIO, *e*•MMC)[2]			3 (8 + 8 + 4 bits).
OCTOSPI[2]			2, with AES-128 (CTR) decryption (OTFDEC)
FMC	Parallel address/data 8/16 bits		4× CS, up to 4x 64 Mbytes[1]
	Parallel AD-Mux 8/16 bits		4× CS, up to 4x 64 Mbytes[1]
	NAND 8/16 bits[2]		Yes, 4 x CS, SLC, BCH4/8[1]
Gigabit Ethernet interfaces			Up to 3[1]
LCD-TFT (LTDC)		-	Up to 314 MHz pixel clock (when used with DSI or LVDS)
		Parallel interface	Up to 24-bits 150 MHz pixel clock (up to 1080p60)
Display serial interface (DSI)			4× data lanes 2.5 Gbit/s each (up to 1536p60)[1]
LVDS display interface (LVDS)			Up to dual-link of 4× data lanes 1.1 Gbit/s each (up to 1536p60)[1]
Camera interface	-		CSI-2 + RGB/RawBayer parallel
	CSI-2 serial (CSI + DCMIPP)		2× data lanes 2.5 Gbit/s each, path shared with DCMIPP
	Parallel RGB/RawBayer (DCMIPP)		Up to 120 MHz, path shared with CSI.
	Image signal processing (ISP)		Yes, embedded inside DCMIPP
	Parallel RGB (DCMI)		Up to 80 MHz

Prerelease product(s)

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Features		STM32MP25xC/F
Parallel interface (PSSI)		16-bit input or output, path shared with DCMI and DCMIPP
HPDMA		3 instances, 48 physical channels in total
LPDMA		1 instance, 4 physical channels
Cryptography	CRYP (two instances)	DES/TDES (ECB, CBC), AES-256 (ECB, CBC, CTR, GCM, GMAC, CCM)
	Secure AES (SAES)	AES-256 (ECB, CBC, CTR, GCM, GMAC, CCM), hardware attack protections, keys sharing to CRYP
	Public key accelerator (PKA)	Public key primitives for RSA, DH, and ECC over GF(p). 64-bit core
Hash (HASH)		SHA-1, SHA-2 and SHA-3 (up to 512), MD5, HMAC
Random number generator (RNG)		True-RNG. FIPS 140-2 NDRNG (NIST SP800-90B certifiable)
Fuses (one-time programming)		12288 effective bits
Multi-function digital filter (MDF)		8 input channels with 8 filters
Audio digital filter (ADF)		1 input channel with 1 filter and sound-activity detection
GPIOs	with interrupt (total count)	Up to 172[(1)]
	Wake-up pins	Up to 6[(1)]
	Tamper input/active output pins	Up to 8 inputs and 8 outputs[(1)]
Up to 12 bit ADC		3 (up to 5 Msps each)
-	ADC channels in total (differential)	Up to 23 channels (or 11 differential)[(1)]
	VREF generation (VREFBUF)	1.21 V, 1.5 V, or VREF+ input
	VREF+ input pin	Yes

1. *See next tables for details.*
2. *Can be a boot source.*

Table 2. STM32MP25xC/F differences per product lines

Feature			STM32MP251x	STM32MP253x	STM32MP255x	STM32MP257x
CPU	Cortex-A35 FPU Neon TrustZone		Single-core	Dual-core		
	Cache size	L1 data + instruction	32 + 32 Kbytes	2 x (32 + 32) Kbytes		
		L2 unified	512 Kbytes	512 Kbytes		
	Frequency	STM32MP25xC	Up to 1200 MHz			
		STM32MP25xF	Up to 1500 MHz			
GPU	For 3D graphics		No		VeriSilicon GC8000UL - Open GL ES 3.2.8 - Vulkan 1.2	
	Performance[(1)] / frequency	STM32MP25xC	-		800 MHz, up to 133 Mtriangle/s or 800 Mpixel/s	
		STM32MP25xF	-		900 MHz, up to 150 Mtriangle/s or 900 Mpixel/s	
NPU	For AI processing		No		VeriSilicon GC8000UL - TensorFlowLite - ONNX - Linux NN	
	Performance[(1)] / frequency	STM32MP25xC	-		800 MHz, 1.2 TOPS	

Prerelease product(s)

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Feature			STM32MP251x	STM32MP253x	STM32MP255x	STM32MP257x
NPU	Performance[1] / frequency	STM32MP25xF	-		900 MHz, 1.35 TOPS	
Video		Decoder (VDEC)	No		H264/VP8 up to 1080p60 - JPEG 500 Mpixel/s[2]	
		Encoder (VENC)	No			
		Frequency	-		600 MHz	
Embedded SRAM		Video RAM	No		128 Kbytes, shared between VDEC and VENC[3]	
		CPU system	256 + 128 Kbytes		256 Kbytes[3]	
Timers	A35 (CNT)	64 bits	4 (S, NS, V, H)	2x 4 (secure, non-secure, Virtual, Hypervisor)		
FDCAN			No	3 (1x TT-FDCAN), 10-Kbyte shared buffer		
Gigabit Ethernet interfaces	External interfaces		1, R(G)MII, MII	2, R(G)MII, MII		3, R(G)MII
	GMAC (ETH), TSN, PTP, EEE		1	2		
	3 ports Gigabit Switch (ETHSW)		No	No	No	2 external ports
Display serial interface (DSI)			No		4× data lanes 2.5 Gbit/s each (up to 1536p60)	
LVDS display interface (LVDS)			No		Up to dual-link of 4x data lanes 1.1 Gbit/s each (up to 1536p60)[4]	

1. *GPU and NPU share performance.*
2. *This is the performance of either VDEC or VENC running alone. VDEC and VENC share performances as they are using same video RAM.*
3. *If neither VDEC nor VENC are used, the video RAM can be used as general purpose memory, thus giving a total of 384 Kbytes for CPU system.*
4. *Single or dual-link depends on the package (see next table for details).*

Table 3. STM32MP25xC/F differences per packages

Features			STM32MP25xxAL	STM32MP25xxAK	STM32MP25xxAI
			VFBGA361	VFBGA424	TFBGA436
Packages		Body size (mm)	10×10	14×14	18×18
		Pitch (mm)	0.5	0.5	0.8
		Thickness (mm)	1	1	1.2
		Ball count	361	424	436
SDRAM	-		Up to 2 x 4.8 Gbytes/s internal buses . AES-128 encryption/decryption		
	DDR3L	16 bits 1066 MHz	Up to 1 Gbyte, single rank		
		32 bits 1066 MHz	-	Up to 2 Gbytes, single rank	
	DDR4	16 bits 1200 MHz	Up to 4 Gbytes, single rank		
		32 bits 1200 MHz	-	Up to 4 Gbytes, single rank	
	LPDDR4	16 bits 1200 MHz	Up to 2 Gbytes, single rank		
		32 bits 1200 MHz	-	Up to 4 Gbytes, dual-rank lockstep	
FMC	Parallel address.data 8/16-bits		-		4× CS, up to 4× 64 MBytes
	Parallel AD-mux 8/16-bits		4× CS, up to 4× 64 MBytes		
	NAND 8/16-bits [1]		Yes, 4× CS, SLC, BCH4/8		
LVDS display interface (LVDS)			Single-link of 4× data lanes 1.1 Gbit/s each (up to 1080p60) [2]	Dual-link of 4× data lanes 1.1 Gbit/s each (up to 1536p60)[2]	
GPIO	with interrupt (total count)		144	144	172

Prerelease product(s)

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Features		STM32MP25xxAL	STM32MP25xxAK	STM32MP25xxAI
		VFBGA361	VFBGA424	TFBGA436
GPIO	Wakeup pins	6	6	6
	Tamper input/active output pins	8 + 8	8 + 8	8 + 8
ADC	ADC channels in total (differential)	23 (11)[3]	21 (10)	23 (11)[3]

1. *Can be a boot source.*
2. *Availability depends on device.*
3. *Including 2 (or 1 differential) low-noise inputs on dedicated ANA0/ANA1 pins.*

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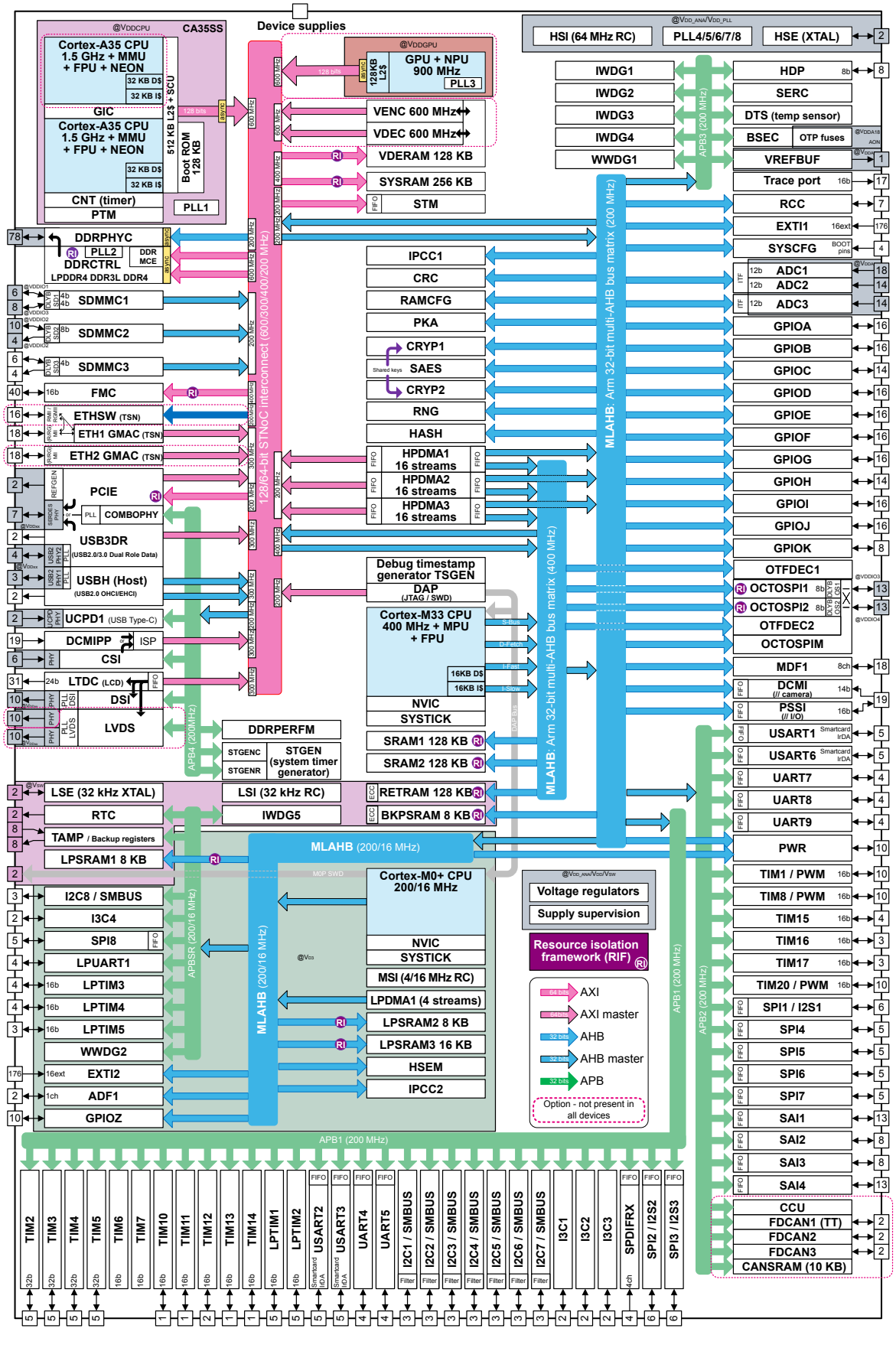
Figure 1. STM32MP25xC/F block diagram



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3 Functional overview

3.1 Dual-core Arm Cortex-A35 subsystem (CA35SS)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

3.1.1 Features

- Armv8-A architecture
- AArch32 for full backward compatibility with Armv7
- AArch64 for 64-bit support and new architectural features
- 32-Kbyte L1 instruction cache for each CPU
- 32-Kbyte L1 data cache for each CPU
- 512-Kbyte level2 cache
- Arm A64 + A32 + Thumb-2 instruction set
- Arm TrustZone security technology
- Arm NEON advanced SIMD
- DSP and SIMD extensions
- VFPv4 floating-point
- Hardware virtualization support
- Performance monitoring Uuit (PMU)
- Program trace macrocell (PTM) that supports instruction trace only
- Integrated generic interrupt controller (GIC) with 384 shared peripheral interrupts
- Integrated generic timer (CNT)

Note: The cryptographic extension is not supported.

3.1.2 Overview

The Cortex-A35 processor uses a highly-efficient 8-stage in-order pipeline that has been extensively optimized to provide full Armv8-A features while maximizing area and power efficiency.

3.1.2.1 Thumb-2 technology

Delivers the peak performance of traditional Arm code, while also providing up to a 30 % reduction in memory requirement for instructions storage.

3.1.2.2 TrustZone technology

Ensures reliable implementation of security applications ranging from digital rights management to electronic payment. Broad support from technology and industry partners.

3.1.2.3 PMU

The PMU provides six performance monitors that can be configured to gather statistics on the operation of each core and the memory system. The information can be used for debug and code profiling.

3.1.2.4 NEON and FPU

Advanced SIMD is a media and signal processing architecture that adds instructions primarily for audio, video, 3-D graphics, image, and speech processing. The floating-point architecture provides support for single-precision and double-precision floating-point operations.

All scalar floating-point instructions are available in the A64 instruction set. All VFP instructions are available in A32 and T32 instruction sets. The same advanced SIMD instructions are available in both A32 and T32 instruction sets. The A64 instruction set offers additional advanced SIMD instructions, including double-precision floating-point vector operations.

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3.1.2.5 *Hardware virtualization*

Highly-efficient hardware support for data management and arbitration, whereby multiple software environments and their applications are able to simultaneously access the system capabilities. This enables the realization of devices that are robust, with virtual environments that are well isolated from each other.

3.1.2.6 *Optimized L1 caches*

Performance and power optimized L1 caches combine minimal access latency techniques to maximize performance and minimize power consumption. There is also the option of cache coherence for enhanced inter-processor communication, or support of a rich SMP capable OS for simplified multicore software development.

3.1.2.7 *Integrated L2 cache controller*

Provides low-latency and high-bandwidth access to cached memory in high-frequency, or to reduce the power consumption associated with off-chip memory access.

3.1.2.8 *Snoop control unit (SCU)*

The SCU is responsible for managing the interconnect, arbitration, communication, cachetocache and system memory transfers, cache coherence and other capabilities for the processor.

This system coherence also reduces software complexity involved in maintaining software coherence within each OS driver.

3.1.2.9 *Generic interrupt controller (GIC)*

Implementing the standardized and architected interrupt controller, the GIC provides a rich and flexible approach to inter-processor communication, and the routing and prioritization of system interrupts.

Supporting up to 416 independent interrupts (including 384 shared interrupt), under software control, each interrupt can be distributed across Cortex-A35 cores, hardware prioritized, and routed between the operating system and TrustZone software management layer.

This routing flexibility and the support for virtualization of interrupts into the operating system, provide one of the key features required to enhance the capabilities of a solution utilizing an hypervisor.

3.2 Arm Cortex-M33 core with TrustZone and FPU (CM33)

The Arm Cortex-M33 core with TrustZone and FPU is a 32-bit RISC processor that features exceptional code-efficiency, delivering the high-performance expected from an Arm core in the memory size usually associated with 8- and 16-bit devices.

It is comprise of:

- Arm TrustZone technology, using the Armv8-M main extension supporting secure and non-secure states
- floating-point extension (FPU)
- Armv8-M DSP extension
- a nested vectored interrupt controller (NVIC) closely integrated with the processor
- a memory system with memory protection unit (MPU) with up to 16 non-secure regions and 16 secure regions
- a security attribution unit (SAU) with up to 8 regions
- an implementation defined attribution unit (IDAU)
- debug components including breakpoints (BPU), data watchpoints (DWT), instrumentation and processor trace (ITM/ETM), cross trigger interface (CTI)
- 16-Kbyte instruction and 16-Kbyte data caches (ICACHE/DCACHE)

3.3 Arm Cortex-M0+ core (CM0P)

The CortexM0+ processor is built on a highly area- and power-optimized 32bit core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32bit architecture, with a higher code density than other 8bit and 16bit microcontrollers.

The Cortex-M0+ is tightly coupled with a nested vectored interrupt controller (NVIC)

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3.4 Graphic processing unit (GPU)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

STM32MP25xC/F devices include a 3D graphics engine (VeriSilicon GC8000UL).

The GPU is a dedicated graphics processing unit accelerating numerous 3D graphics applications such as graphical user interface (GUI), menu display or animations. It works together with an optimized software stack design for industry-standard APIs with support for Android™ and Linux® embedded development platforms.

The GPU is used to accelerate parallel computing (GPGPU), via the typical OpenCL or Vulkan API, or more image-based API like OpenVX or OpenCV. This wide support guarantees to be able to accelerate any application up to the most recent ones, with graphic performances reaching 25.6 GFlops.

The GPU is built in a separate power domain, which allows the GPU to be switched off when not used in the long-term, or even to play with dynamic voltage frequency scaling (DVFS).

The GPU graphic hardware acceleration is exposed through the following API:

- OpenVG 1.2 for 2D or curve drawing
- OpenGL/ES 3.2.8 for 3D apps (backward compatible: OES2.1 and OES1.1)
- Vulkan 1.2 for modern 3D apps
- OpenCL 3.0 for parallel programming
- OpenVX 1.3 for acceleration of computer vision applications

The GPU provides the following graphic theoretical performance (values for 800 MHz):

- Vertex: 200 MVtx/s
- Triangle: 133 MTrg/s
- Texel: 800 MTex/s
- Pixel: 800 MPix/s
- Float 16bit: 25.6 GFlops
- Float 32bit: 12.8 GFlops

3.5 Neural processor unit (NPU)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

The NPU provides powerful hardware acceleration for neural network, to allow efficient artificial intelligence (AI) applications.

The NPU acceleration is implemented by hardware neural operator inserted into the GPU. As such, it benefits of both optimized hardware (the neural operator), and of the flexibility and efficiency of the existing GPU shaders.

The NPU neural hardware acceleration is exposed through the following API:

- TensorFlowLite-API
- ONNX
- Linux NN-API-Adapter

The NPU flexibility is used to optimally accelerate the following frameworks (nonexhaustive list)

- TensorFlow non-exhaustive hardware support
- TensorFlowLite full hardware support (including its SoftMax subset)
- Caffe, Caffe2
- CNTK, Torch, Theano, Darknet

The NPU provides the following neural theoretical performance, below values for 800 MHz (values for 900 MHz overdrive inside parenthesis):

- Integer operations: 1.2 (1.35) TOPS (8-bit integer)

To reduce the required DDR bandwidth during neural computations, the NPU embeds natively 128 Kbytes of memory.

3.6 Memories

3.6.1 External SDRAM

STM32MP25xC/F devices embed a controller for the external SDRAM which supports the following devices

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- DDR3L, 16- or 32-bit data, up to 2 Gbytes, up to DDR3L-2133 (1066 MHz clock)
- DDR4, 16- or 32-bit data, up to 4 Gbytes, up to DDR4-2400 (1200 MHz clock)
- LPDDR4, 16- or 32-bit data, up to 4 Gbytes, up to LPDDR4-2400 (1200 MHz clock)

3.6.2 Embedded SRAM

All devices feature:

- SYSRAM in MPU domain: 256 Kbytes with half/full hardware erase mechanism on reset
- VDERAM in MPU domain: 128 Kbytes (not usable when either VDEC or VENC is used) with hardware erase mechanism on enable as general purpose RAM
- SRAM1 in MCU domain: 128 Kbytes with hardware erase mechanism on tamper detection
- SRAM2 in MCU domain: 128 Kbytes
- LPSRAM1 in SmartRun domain: 8 Kbytes with hardware erase mechanism on reset
  The content of this area can be retained in Standby or V_{BAT} mode, and can be protected by the CRC mechanism.
- LPSRAM2 in SmartRun domain: 8 Kbytes with hardware erase mechanism on reset
- LPSRAM3 in SmartRun domain: 16 Kbytes
- RETRAM (retention RAM): 128 Kbytes with hardware erase mechanism on reset
  The content of this area can be retained in Standby or V_{BAT} mode, and can be protected by ECC and CRC mechanisms.
- BKPSRAM (backup SRAM): 8 Kbytes with hardware erase mechanism on tamper detection
  The content of this area can be protected against possible unwanted accesses, and can be retained in Standby or V_{BAT} mode. The content can also be protected by ECC mechanism.

3.7 DDR3L/DDR4/LPDDR4 controller (DDRCTRL)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

DDRCTRL combined with DDRPHYC provides a complete 16 /32-bit memory interface solution for DDR memory subsystem.

- JEDEC compliant LPDDR4 SDRAM up to 2400 MT/s
- JEDEC compliant DDR4 SDRAM up to 2400 MT/s with DLL on-range
- JEDEC compliant DDR3L SDRAM up to 2133 MT/s with DLL on-range
- Dual-rank for LPDDR4 devices.
- Dual-rank for DDR3L/DDR4 devices.
- 2 x 128-bit AXI4 ports
  - up to 16 QoS levels and up to 3 traffic classes are supported per direction.
  - CID-based firewalling function with poisoning output signaling
  - 1 port provided with AES- 128 encryption/decryption with programmable memory range (DDRMCE)

Low-power features:

- Linked with the RCC, ability to move the DDR memory subsystem in self refresh through automatic way, hardware way, or software way (ASR, HSR and SSR).

3.8 Boot modes

At startup, the boot source used by the internal boot ROM is selected by BOOT pins and OTP settings.

Table 4. Default interfaces

Unless otherwise mentioned in table below.

Boot source	When used by Cortex-A35	When used by Cortex-M33
SD-Card	SDMMC1	
e•MMC	SDMMC2	
Serial NOR, HyperFlash and serial NAND	OCTOSPIM port1	OCTOSPIM port2
SLC NAND	FMC	

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Boot source	When used by Cortex-A35	When used by Cortex-M33
USB	USB3DR (high-speed only)	-
UART	USART2/6 and UART5/8/9	-

Table 5. Boot sources

BOOT[3:0] pins	Alternate boot pins OTP value							
	0b00 (default)				0b01	0b10	0b11	
	Cortex-A35 master	Cortex-M33 master	Cortex-M33 master (1)		Cortex-A35 master	Cortex-M33 master	Cortex-M33 master (1)	
			Cortex-A35	Cortex-M33			Cortex-A35	Cortex-M33
0	UART and USB(2) (3)							
1	SD-Card	-	-	-	SD-Card	SD-Card	Serial NAND	Serial NOR
2	e•MMC	-	-	-	e•MMC	e•MMC	e•MMC	Serial NOR
3	Development boot(2)							
4	Serial NOR	-	-	-	Serial NOR	Serial NOR	SLC NAND	Serial NOR
5	-						e•MMC(4)	Serial NOR
6	-						e•MMC(4)	HyperFlash™
7	-	SD-Card	-	-	HyperFlash™	HyperFlash™	Serial NAND	HyperFlash™
8	-	e•MMC	-	-	Serial NAND	Serial NAND	e•MMC	HyperFlash™
9	-						SD-Card(5)	Serial NOR
10	-						SD-Card(5)	HyperFlash™
11	-	Serial NOR	-	-	SLC NAND	SLC NAND	SLC NAND(6)	HyperFlash™
12	Development boot(2)							
13	-	-	e•MMC	Serial NOR	SD-Card(5)	SD-Card(5)	SD-Card	Serial NOR
14	-	-	SD-Card	Serial NOR	e•MMC(4)	e•MMC(4)	SD-Card	HyperFlash™
15	UART and USB(3)							

1. *Two flash memory config. Indirect Cortex-A35 boot (from Cortex-M33) or used during Cortex-A35 D1Standby exit*
2. *Cannot be override by OTP.*
3. *Wait incoming connection on USART2/6 or UART5/8/9 on default pins and USB high-speed device on USB3DR_DP/DM.*
4. *e•MMC on SDMMC1*
5. *SD-Card on SDMMC2*
6. *Only 8-bit memory is supported as some FMC and OCTOSPIM port2 pins are shared (usage of FMC in 16-bit mode is exclusive of usage of OCTOSPIM port2).*

The default pins used during boot are described in Table 6 .

Note: There is few mutual exclusions with this default settings. SDMMC2 cannot be used with FMC. OCTOSPI Port2 cannot be used with FMC 16 bits. OCTOSPI port2 in 8-bit mode cannot be used with FMC.

Table 6. Minimum set of default pins used during boot ROM phase

Most can be changed using OTP settings. This table is for default OTP settings.

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Interface	type			Signal	Pin	IO supply domain
FMC	SLC NAND 8-bits		SLC NAND 16-bits	FMC_NOE	PE15	V_{DDIO2}[1]
				FMC_RNB	PE13	
				FMC_NWE	PE14	
				FMC_NCE1	PE12	
				FMC_ALE	PE8	
				FMC_CLE	PE11	
				FMC_D0	PE9	
				FMC_D1	PE6	
				FMC_D2	PE7	
				FMC_D3	PD15	V_{DD}
				FMC_D4	PD14	
				FMC_D5	PB13	
				FMC_D6	PD12	
				FMC_D7	PB14	
	-			FMC_D8	PB5	V_{DDIO4}[2]
				FMC_D9	PB6	
				FMC_D10	PB7	
				FMC_D11	PD13	V_{DD}
				FMC_D12	PB8	V_{DDIO4}[2]
				FMC_D13	PB9	
				FMC_D14	PB11	
				FMC_D15	PB10	
OCTOSPIM Port1	Serial NOR,	Serial NAND	HyperFlash™	OCTOSPIM_P1_CLK	PD0	V_{DDIO3}
				OCTOSPIM_P1_NCS1	PD3	
				OCTOSPIM_P1_IO0	PD4	
				OCTOSPIM_P1_IO1	PD5	
	-			OCTOSPIM_P1_IO2	PD6	
				OCTOSPIM_P1_IO3	PD7	
				OCTOSPIM_P1_IO4	PD8	
				OCTOSPIM_P1_IO5	PD9	
				OCTOSPIM_P1_IO6	PD10	
				OCTOSPIM_P1_IO7	PD11	
				OCTOSPIM_P1_NCLK	PD1	
				OCTOSPIM_P1_DQS	PD2	
OCTOSPIM Port2	Serial NOR,	Serial NAND	HyperFlash™	OCTOSPIM_P2_CLK	PB10	V_{DDIO4}[2]
				OCTOSPIM_P2_NCS1	PB8	
				OCTOSPIM_P2_IO0	PB0	
				OCTOSPIM_P2_IO1	PB1	
	-			OCTOSPIM_P2_IO2	PB2	
				OCTOSPIM_P2_IO3	PB3	

Prerelease product(s)

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Interface	type		Signal	Pin	IO supply domain
OCTOSPIM Port2	-	HyperFlash™	OCTOSPIM_P2_IO4	PB4	V_{DDIO4}[2]
			OCTOSPIM_P2_IO5	PB5	
			OCTOSPIM_P2_IO6	PB6	
			OCTOSPIM_P2_IO7	PB7	
			OCTOSPIM_P2_NCLK	PB11	
			OCTOSPIM_P2_DQS	PB9	
SDMMC1	SD-Card or eMMC		SDMMC1_CK	PE3	V_{DDIO1}
			SDMMC1_CMD	PE2	
			SDMMC1_D0 [3]	PE4	
SDMMC2	SD-Card or eMMC		SDMMC2_CK	PE14	V_{DDIO2}[1]
			SDMMC2_CMD	PE15	
			SDMMC2_D0[3]	PE13	
USART2			USART2_RX	PA8	V_{DD}
			USART2_TX	PA4	
UART5			UART5_RX	PB15	V_{DD}
			UART5_TX	PA0	
USART6			USART6_RX	PF4	V_{DD}
			USART6_TX	PF5	
UART8			UART8_RX	PF3	V_{DD}
			UART8_TX	PG3	
UART9			UART9_RX	PB14	V_{DD}
			UART9_TX	PD13	

1. *Some FMC and SDMMC2 pins are shared, this means that usage of FMC is exclusive of usage of SDMMC2.*
2. *Some FMC and OCTOSPIM port2 pins are shared, this means that usage of FMC in 16-bit mode is exclusive of usage of OCTOSPIM Port2.*
3. *Only used as input by boot ROM*

Although low-level boot is done using internal clocks, ST supplies software packages as well as major external interfaces (such as DDR or USB) require a crystal or an external oscillator to be connected on HSE pins.

See the product reference manual for constrains and recommendations regarding connection of HSE pins and supported frequencies.

3.9 Power supply management (PWR)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

3.9.1 Power supply scheme

The system requires supply on V_{DD}, $V_{DDA18AON}$, V_{DDCPU} and V_{DDCORE} to start, and to allow independent supplies for V_{DDGPU}, $V_{DDA18ADC}$, V_{BAT}, $V_{DD33USB}$, $V_{DD33UCPD}$, V_{DDIO2}, V_{DDIO3}, V_{DDIO4}, V_{DDIO1}, and V_{DDQDDR}.

- V_{DD} power supply input for I/Os (1.8 V or 3.3 V typical)
- $V_{DDA18AON}$ power supply input for system analog such as reset, power management, oscillators and OTP
- V_{BAT} optional power supply input for backup domain, and optionally D3 domain when V_{DD} is not present (VBAT mode)
- V_{DDCORE} digital core domain supply, dependent on V_{DD} supply. V_{DD} must be present before V_{DDCORE}.
  - V_{DDCSI}, V_{DDDSI}, V_{DDLVDS}, $V_{DDCOMBOPHY}$, $V_{DDCOMBOPHYTX}$, and $V_{DDPCIECLK}$ are usually connected to V_{DDCORE}.

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- V_{DDCPU} digital CPU domain supply (Cortex-A35), dependent on V_{DD} supply. V_{DD} must be present before V_{DDCPU}.
- V_{DDGPU} digital GPU domain supply, dependent on V_{DD} supply. V_{DD} must be present before V_{DDGPU}.
- V_{DDQDDR} DDR I/O supply
- $V_{DDA18ADC}$ analog power supply input for ADCs and voltage reference buffers, independent from any other supply
- V_{REF+} external reference voltage for ADCs, independent from any other supply
  - reference voltage output when the voltage reference buffer is enabled
  - independent external reference voltage input when the voltage reference buffer is disabled
- V_{SSA} separate analog and reference voltage ground
- $V_{DD33USB}$ supply input for USB HS PHY, independent from any other supply
- $V_{DD33UCPD}$ supply input for USB Type-C CC1 and CC2 pins, independent from any other supply
- V_{DDIO3} supply input, mostly for OCTOSPIM_P1 I/Os, independent from any other supply
- V_{DDIO4} supply input, mostly for OCTOSPIM_P2 I/Os, independent from any other supply
- V_{DDIO2} supply input, mostly for e.MMC I/Os, independent from any other supply
- V_{DDIO1} supply input, mostly for SD Card I/Os, independent from any other supply
- V_{SS} common ground for all supplies except for analog

3.9.2 Power-supply supervisor

The devices have an integrated power-on reset (POR) and power-down reset (PDR) circuitry, coupled with a brownout reset (BOR) circuitry:

- Power-on reset (POR)
  The POR supervisor monitors V_{DD} and $V_{DDA18AON}$ power supplies, and compares them to a fixed threshold. The devices remain in reset mode when V_{DD} and $V_{DDA18AON}$ are below this threshold.
- Power-down reset (PDR)
  The PDR supervisor monitors V_{DD} and $V_{DDA18AON}$ power supplies. A reset is generated when V_{DD} or $V_{DDA18AON}$ drops below a fixed threshold.
- Brownout reset (BOR)
  The BOR supervisor monitors V_{DD} power supply. A 2.7 V BOR thresholds can be enabled through option bytes. A reset is generated when V_{DD} drops below this threshold. The BOR must not be enabled when V_{DD} = 1.8 V typ. is used.
- Power-on reset V_{DDCORE} (POR_VDDCORE)
  The POR_VDDCORE supervisor monitors V_{DDCORE} power supply, and compares it to a fixed threshold. The V_{DDCORE} domain remains in reset mode when V_{DDCORE} is below this threshold,
- Power-down reset V_{DDCORE} (PDR_VDDCORE)
  The PDR_VDDCORE supervisor monitors V_{DDCORE} power supply. A V_{DDCORE} domain reset is generated when V_{DDCORE} drops below a fixed threshold.
- Power-on reset V_{DDCPU} (POR_VDDCPU)
  The POR_VDDCPU supervisor monitors V_{DDCPU} power supply, and compares it to a fixed threshold. The V_{DDCPU} domain remains in reset mode when V_{DDCPU} is below this threshold.
- Power-down reset V_{DDCPU} (PDR_VDDCPU)
  The PDR_VDDCPU supervisor monitors V_{DDCPU} power supply. A V_{DDCPU} domain reset is generated when V_{DDCPU} drops below a fixed threshold.
- Power-on reset V_{SW} (POR_VSW)
  The POR_VSW supervisor monitors V_{SW} power supply, and compares it to a fixed threshold. The V_{SW} domain remains in reset mode when V_{SW} is below this threshold.

The devices also include monitoring which can generate tamper events, interrupt, or wake-up:

- Programmable voltage detector (PVD)
  The PVD monitors the PVD_IN pin, and compares it to a fixed threshold. An interrupt or a wake-up can be generated when PVD_IN is below or above the threshold.

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- V_{DDCORE} monitoring
  Monitors V_{DDCORE} power supply and compares it to a fixed threshold. A tamper event, an interrupt, or a wake-up can be generated when V_{DDCORE} is below or above the threshold.
- V_{DDCPU} monitoring
  Monitors V_{DDCPU} power supply, and compares it to a configurable threshold. A tamper event, an interrupt, or a wake-up can be generated when V_{DDCPU} is below or above the threshold.
- V_{DDGPU} monitoring
  Monitors V_{DDGPU} power supply and compares it to a configurable threshold. An interrupt or a wake-up can be generated when V_{DDGPU} is below or above the threshold. A GPU reset is also generated if V_{DDGPU} is below the threshold (VDDGPURDY = 0).
- Peripheral voltage monitoring
  Monitors independently V_{DDIO2}, V_{DDIO3}, V_{DDIO4}, V_{DDIO1}, $V_{DD33UCPD}$, $V_{DD33USB}$ and $V_{DDA18ADC}$ power supplies with fixed thresholds. An interrupt or a wake-up can be generated when supplies are below or above the thresholds.

3.10 Low-power strategy

Several low-power modes are available to save power when the Cortex-A35 and/or the CortexM33 do not need to execute code (when waiting for an external event). It is up to the user to select the mode that gives the best compromise between low-power consumption, short startup time, and available wake-up sources.

- Slowing down system clocks (see RCC section in the reference manual)
- Controlling individual peripheral clocks (see RCC section in the reference manual)
- Low-power modes:
  - CSleep (CPU clock stopped)
  - CStop (CPU subsystem clock stopped)
  - D1 DStop1 (CPU subsystem clock stopped, normal mode signaled to external regulator)
  - D1 DStandby (domain power down and wake-up via reset)
  - Stop1, LP-Stop1, and LPLV-Stop1 (system clock stalled, normal or low-power mode signaled to external regulator supplying the VDDCPU and the VDDCORE)
  - Stop2, LP-Stop2, and LPLV-Stop2 (system clock stalled, powered down mode signaled to external regulator supplying the VDDCPU, and normal or low-power mode signaled to external regulator supplying the VDDCORE)
  - Standby1 (system powered down and D3 domain in autonomous mode running with local clocks)
  - Standby2 (system powered down, D3 domain also in power down)

3.11 Resource isolation framework (RIF)

The RIF is a comprehensive set of hardware blocks designed to enforce and manage the isolation of STM32 hardware resources like memory and peripherals.

Within a defined hardware execution compartment (eight are available), privileged, unprivileged, secure, and non-secure application softwares can assign their own embedded memory buffers, external memory regions, and peripherals thanks to the RIF hardware.

The RIF architectural framework extends to FMC, SYSCFG, IPCC, HSEM, DMA, RTC, TAMP, RCC, PWR, EXTI, or GPIO.

3.12 Reset and clock controller (RCC)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

The RCC manages the generation of all clocks, as well as the clock gating and the control of system and peripheral resets. It provides a high flexibility in the choice of clock sources, and allows application of clock ratios to improve the power consumption. In addition, on some communication peripherals that are capable to work with two different clock domains (either a bus interface clock or a kernel peripheral clock), the system frequency can be changed without modifying the peripheral activity rate.

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Prerelease product(s)

3.12.1 Features

- RIF aware
- Reset part:
  - Generation of local and system reset
  - Bidirectional pad reset (NRST) to reset of external devices, or to reset the device
  - Output pad reset (NRSTC1MS) to reset of external mass-storage devices used by the Cortex-A35
- Clock generation part:
  - Generation and distribution of clocks for the complete system
  - 5 separate PLLs (excluding external Cortex-A35, DDRCTRL, and GPU ones):
    - Integer or fractional mode
    - Spread-spectrum function to reduce the amount of EMI peaks
    - Possibility to change on-the-fly the fractional ratios of the PLLs
  - Smart clock gating for reduction of power dissipation
  - 2 external oscillators:
    - HSE that supports a wide range of crystals: 16 to 48 MHz
    - LSE for 32.768 kHz crystals
  - 3 Internal oscillators:
    - HSI that runs around 64 MHz
    - MSI that runs around 16 MHz or 4 MHz
    - LSI that runs around 32 kHz
  - Buffered clock outputs for external devices
- Two independent interrupt interfaces (one dedicated to Cortex-A35, and one dedicated to Cortex-M33)
- Two independent failure events (HSE and LSE)
- Two independent events to wake up processors (one dedicated to Cortex-A35 and one dedicated to Cortex-M33)

3.12.2 Clock management

The RCC provides a high flexibility to the application in the choice of the clock generators:

- from HSI, high-speed internal oscillator (~ 64 MHz)
- from HSE, high-speed external oscillator (16 to 48 MHz)
- from LSE; low-speed external oscillator (32 kHz)
- from LSI, low-speed internal oscillator (~ 32 kHz)
- from MSI, low-power internal oscillator (~ 4 MHz or ~ 16 MHz)

The RCC offers a good flexibility for the application to select the appropriate clock for CPUs and peripherals. More especially for peripherals that need a specific clock like SPI(I2S), SAI, and SDMMC.

Each clock source can be switched on or off independently in order to optimize the power consumption.

There are mainly three clock paths:

- Cortex-A35 bus matrix
- Cortex-M33 and its bus matrix
- peripheral kernel clocks

The Cortex-A35, the GPU, and DDRCTRL clocking are derived locally because of high frequency use. The RCC manages only source clocks for their related local PLLs.

3.12.3 Reset sources

There are several sources able to generate a reset:

- supply monitors (V_{DD}, V_{DDCORE}, V_{DDCPU} , V_{DDGPU} or V_{SW}) lower than expected values
- independent watchdogs timeout
- D1 domain exit from DStandby state
- exit from Standby mode
- external signals driving the NRST pin

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- software commands

The coverage (or scope) of the resets differ according to the source initiating the reset, with the following categories:

- power-on/off resets
- system resets
- local resets

An application reset can be generated from one of the following sources:

- reset from the NRST pin
- reset from low-voltage detection on VDD
- reset from the independent watchdogs
- software reset from RCC registers
- failure on HSE
- RETRAM CRC or ECC error

A system reset can be generated from one of the following sources:

- reset from application reset
- reset from low-voltage detection on V_{DDCORE}
- a reset from low-voltage detection on V_{DDCPU}

The NRST reset is activated by:

- low voltage on V_{DD}
- failure on HSE
- reset from the independent watchdogs
- software reset from RCC registers
- RETRAM CRC or ECC error
- assertion of NRST by an external source

3.13 Hardware semaphore (HSEM)

The hardware semaphore provides 16 (32-bit) register-based semaphores.

The semaphores can be used to ensure synchronization between different processes that run on a core and between different cores. The HSEM provides a non-blocking mechanism to lock semaphores in an atomic way. The following functions are provided:

- Locking a semaphore can be done in two ways:
  - 2-step lock: by writing CoreID and ProcessID to the semaphore, followed by a read check.
  - 1-step lock: by reading the CoreID from the semaphore
- Interrupt generation when a semaphore is freed
  - Each semaphore can generate an interrupt on one of the interrupt lines.
- Semaphore clear protection
  - A semaphore is only cleared when CoreID and ProcessID matches.
- Global semaphore clear per CoreID

3.14 Inter-processor communication controller (IPCC1/2)

The IPCC is used to communicate data between two processors. It provides a non-blocking signaling mechanism to post and retrieve communication data in an atomic way (signaling for 16 channels for IPPC1, and four channels for IPCC2).

The IPCC communication data must be located in a common memory, which is not part of the IPCC.

3.14.1 Main features

- Status signaling for the four channels
  - Channel occupied/free flag, also used as lock

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- Two interrupt lines per processor
  - One for RX channel occupied (communication data posted by sending processor)
  - One for TX channel free (communication data retrieved by receiving processor)
- Interrupt masking per channel
  - Channel occupied mask
  - Channel free mask
- Two channel operation modes
  - Simplex (each channel has its own communication data memory location)
  - Half duplex (a single channel in associated to a bidirectional communication data information memory location)

3.15 General-purpose input/outputs (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (with or without pull-up or pull-down), or as peripheral alternate function. Some of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

After reset, all GPIOs are in analog mode to reduce power consumption.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/O registers.

Access to each GPIO configuration bits can be restricted to secure-only and/or privileged-only. These configuration bits can also be allocated to a specific CPU.

3.16 Bus-interconnect matrix

For more details on interconnect, see the reference manual (RM0457).

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Figure 2. **AXI STNoC multi-frequency network**

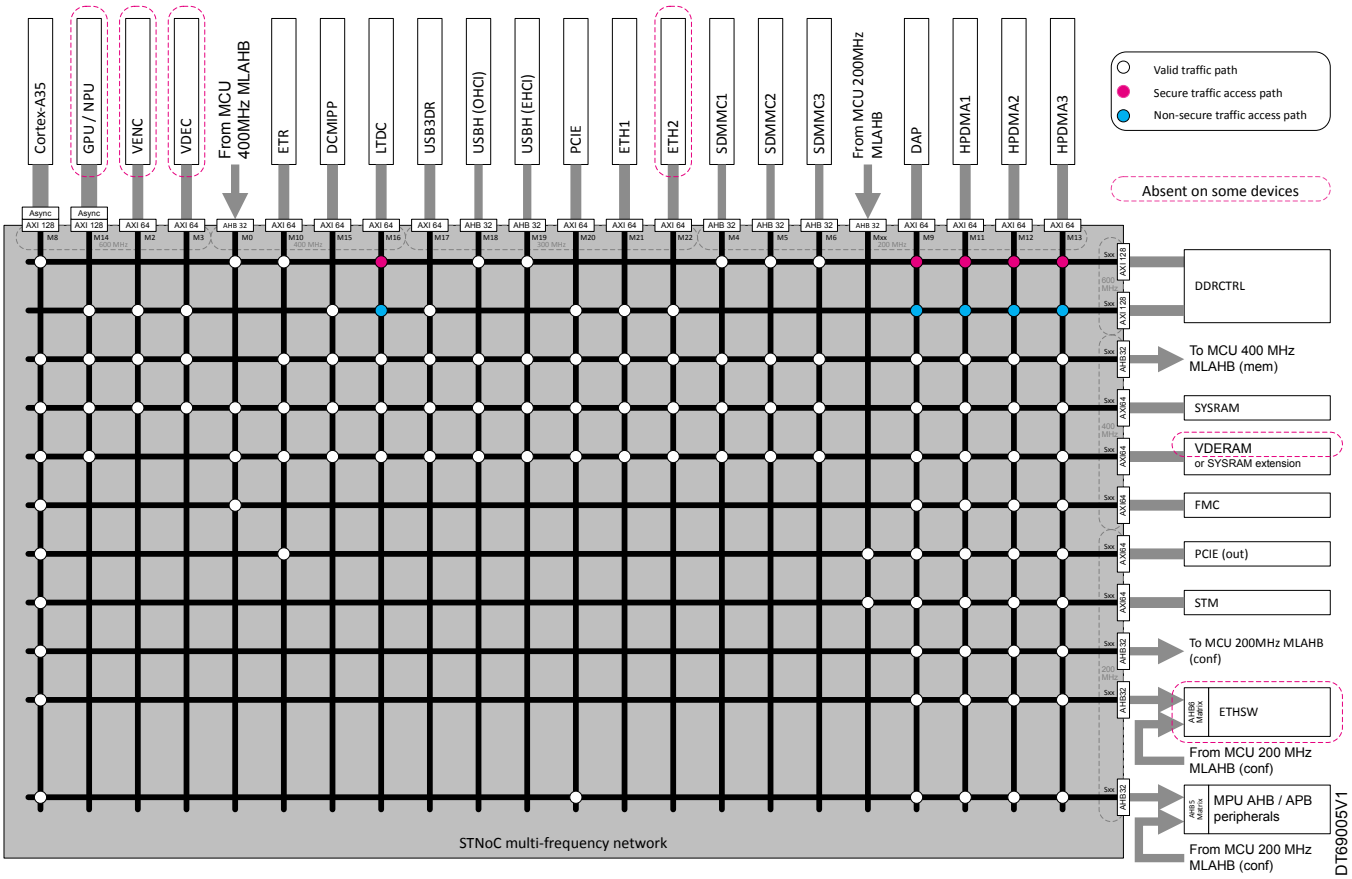

Figure 3. **MCU multi-Layer AHB 400 MHz**

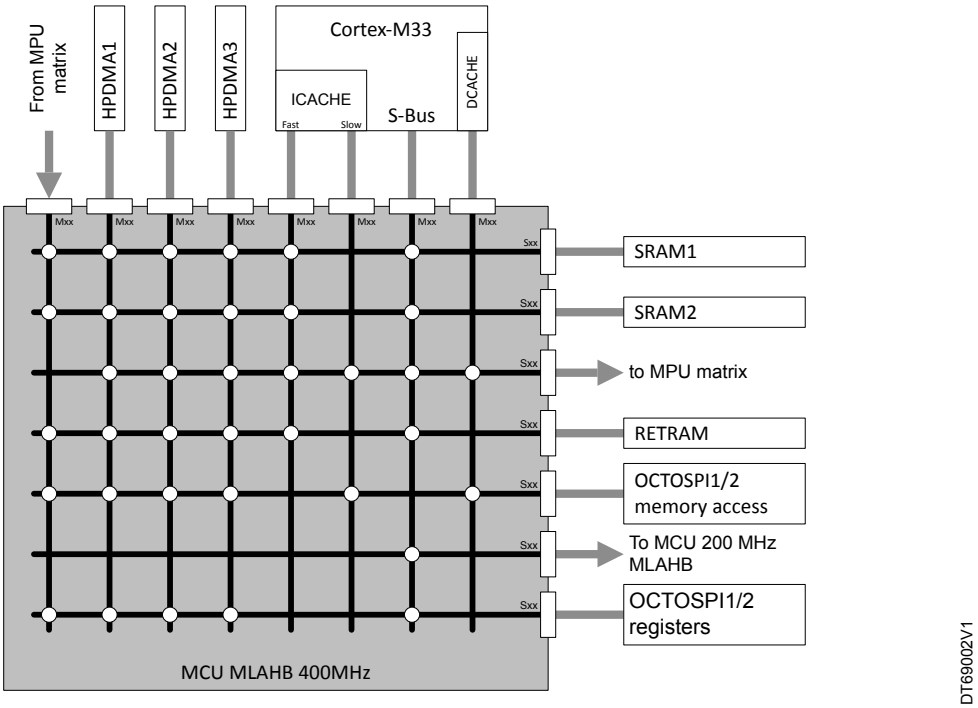

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Figure 4. MCU multi-Layer AHB 200 MHz

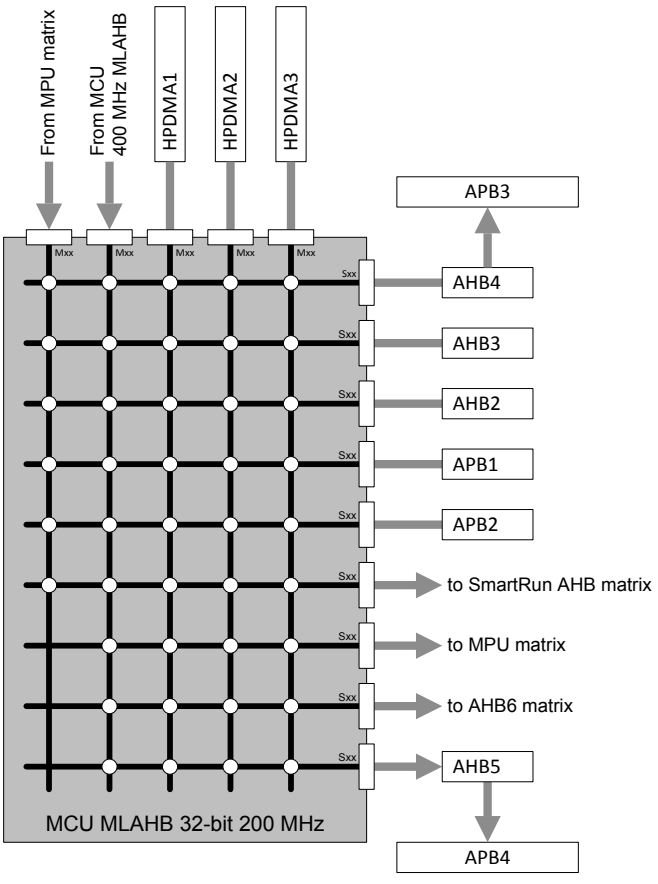

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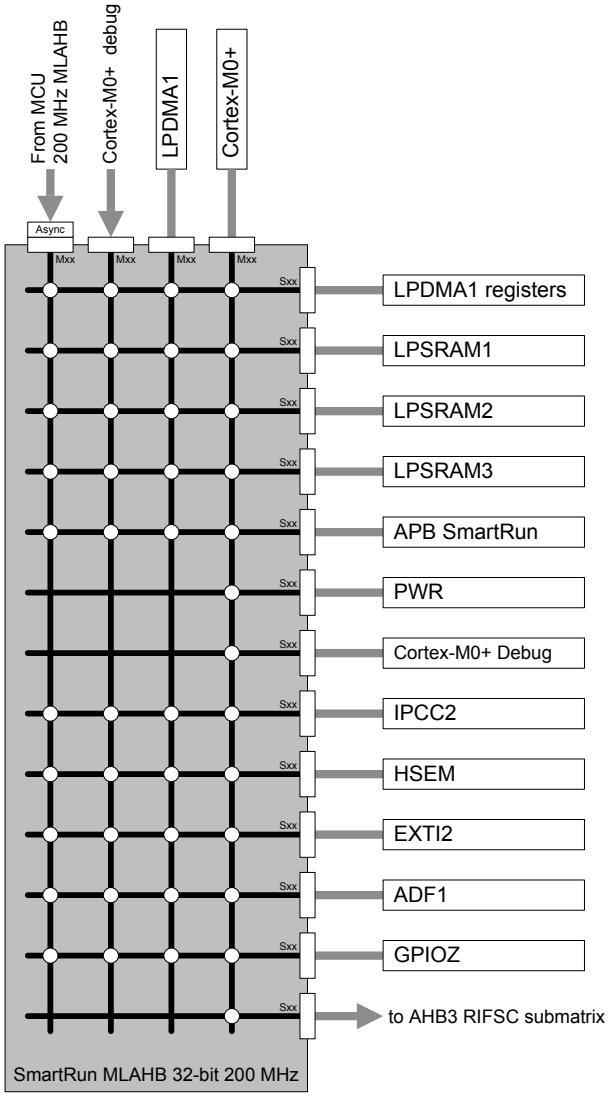
Figure 5. **SmartRun multi-Layer AHB matrix**



DT69004V3

3.17 High-performance DMA controllers (HPDMA1/2/3)

- AXI master and AHB master
- Memory-mapped data transfers from a source to a destination:
  - Peripheral-to-memory
  - Memory-to-peripheral
  - Memory-to-memory
  - Peripheral-to-peripheral
- Autonomous data transfers during Sleep and Stop modes
- Per channel event generation
- Per channel interrupt generation
- 16 concurrent DMA channels
- Per channel FIFO
- Linked-list support
- TrustZone support
- Privileged/unprivileged support
- Channel isolation support

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3.18 Low-power DMA controller (LPDMA1)

- AHB master
- Memory-mapped data transfers from a source to a destination:
  - Peripheral-to-memory
  - Memory-to-peripheral
  - Memory-to-memory
  - Peripheral-to-peripheral
- Autonomous data transfers during Sleep and Stop modes
- Per channel event generation
- Per channel interrupt generation
- 4 concurrent DMA channels
- Linked-list support
- TrustZone support
- Privileged/unprivileged support
- Channel isolation support

3.19 Cortex-M33 nested vectored interrupt controller (NVIC)

The devices embed a NIC that can support up to 320 maskable interrupt channels, not including the Cortex®-M33 interrupt lines.

- 16 programmable priority levels
- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Tail chaining
- Processor context automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

NVIC registers are banked across secure and non-secure states.

The NVIC provides flexible interrupt management features with minimum interrupt latency.

3.20 Cortex-M0+ nested vectored interrupt controller (NVIC)

The devices embeds an NVIC that can support up to 32 maskable interrupt channels, not including the Cortex-M0+ core interrupt lines.

- 4 programmable priority levels
- Closely coupled NVIC that gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor context automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This NVIC provides flexible interrupt management features with minimum interrupt latency.

3.21 Extended interrupt and event controller (EXTI1/2)

The EXTI manages individual CPU and system wake-up through configurable and direct event inputs. It provides wake-up requests to the power control, and generates an interrupt request to the CPU NVIC or GIC, and events to the CPU event inputs. For each CPU, an additional event generation block (EVG) is needed to generate the CPU event signal.

The EXTI wake-up requests allow the system to be woken up from Stop mode, and CPUs to be woken up from CStop and CStandby modes.

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The interrupt request and event request generation can also be used in Run mode.

The EXTI also includes the EXTI I/Oport selection.

Each interrupt or event can be set as secure to restrict access to secure software only.

EXTI1 is shared between Cortex-A35 and Cortex-M33 while EXTI2 is shared between all cores.

3.22 Cyclic redundancy check calculation unit (CRC)

The CRC calculation unit is used to get a CRC code using a programmable polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the flash memory integrity.

The CRC calculation unit helps computing a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.23 Flexible memory controller (FMC)

The FMC main features are the following:

- Interface with static-memory mapped devices including:
  - NOR flash memory
  - Static or pseudo-static random access memory (SRAM, PSRAM)
  - NAND flash memory with 4-bit/8-bit BCH hardware ECC
- 8-,16-bit data bus width
- Independent chip-select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO

3.24 Octo-SPI memory interface (OCTOSPI1/2)

The OCTOSPI supports two protocols used by most external serial memories such as serial PSRAMs, serial NAND and serial NOR flash memories, HyperRAMs, and HyperFlash memories:

- Indirect mode: all the operations are performed using the OCTOSPI registers.
- Automatic status-polling mode: the external memory status register is periodically read and an interrupt can be generated in case of flag setting.
- Memory-mapped mode: the external memory is memory mapped ,and is seen by the system as if it was an internal memory supporting both read and write operations.

The OCTOSPI supports multiple protocols:

- XSPI protocol and its various flavors (such as XCELLA, OCTABUS, HyperBus™ as defined by memory providers)

3.25 On-the-fly decoder (OTFDEC1/2)

The OTFDEC is used to decrypt on-the-fly AHB traffic based on the read request address information. Four independent and non-overlapping encrypted regions can be defined in the OTFDEC.

The OTFDEC uses AES-128 in counter mode to achieve the lowest possible latency. Each time the content of an encrypted region is changed, the entire region must be re-encrypted with a different cryptographic context (key or initialization vector). This constraint makes the OTFDEC suitable to decrypt read-only data or code, stored in external NOR flash memory.

3.26 Octo-SPI I/O manager (OCTOSPIM)

The OCTOSPIM is an internal multiplexer:

- Efficient OCTOSPI pin assignment by allowing pin swapping
- Multiplexing two single-, dual-, quad, or octal-SPI interfaces over the same external bus: interfaces (with for example different security attributes) share then the same memory, or access two memories embedded in a multichip package.

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3.27 Analog-to-digital converters (ADC1/2/3)

STM32MP25xC/F devices embed three analog-to-digital converters, which resolution can be configured to 12, 10, or 8 bits. Each ADC shares up to 20 channels, performing conversions in single-shot or scan mode. In scan mode, an automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- simultaneous ADC1/ADC2 conversion
- interleaved ADC1/ADC2 conversion

The ADC can be served by DMA, thus allows the automatic transfer of ADC converted values to a destination location without any software action.

In addition, an analog watchdog feature can accurately monitor the converted voltage of one, some, or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

In order to synchronize A/D conversion, the ADCs can be triggered by timers.

3.28 Digital temperature sensor (DTS)

The DTS is a high-precision low-power junction temperature sensor, based on a configurable controller plus one or multiple embedded temperature sensors. The sensor can operate in two distinct modes to provide temperature readings:

- first mode used to a provide calibrated accurate temperature
- second mode that does not require any calibration

Main features:

- Two programmable (rise or fall) hardware alarms incorporating hysteresis
- Status registers recording the minimum and maximum data values received
- A power-up timer with IRQ to support manual operation
- A calibration sequence requiring no knowledge of die temperature.

3.29 V_{BAT} operation

The V_{SW} domain supplies the RTC, the TAMP, the LSI, the LSE , the IWDG5, the backup registers , the LPSRAM1, the retention RAM, and the backup SRAM.

In order to optimize the battery duration, this power domain is supplied by V_{DD} when available, or by the voltage applied on VBAT pin (when V_{DD} supply is not present). V_{BAT} power is switched when the PDR detects that V_{DD} has dropped below the PDR level.

The voltage on VBAT pin can be provided by an external battery, by a supercapacitor, or directly by V_{DD}. In the later case, V_{BAT} mode is not functional.

V_{BAT} operation is activated when V_{DD} is not present.

Note: None of these events (external interrupts, watchdog reset, TAMP event, or RTC alarm/events) can directly restore the V_{DD} supply, and force the device out of the V_{BAT} operation. Nevertheless, watchdog reset (taken as a tamper event), TAMP events, and RTC alarm/events can be used to generate a signal to an external circuitry (typically a PMIC) that can restore the V_{DD} supply.

3.30 Voltage reference buffer (VREFBUF)

STM32MP25xC/F devices embed a voltage reference buffer which can be used as voltage reference for ADC, and as voltage reference for external components through VREF+ pin.

An external voltage reference must be provided through the VREF+ pin when the internal voltage reference buffer is off.

3.31 Multifunction digital filter (MDF1)

The MDF is a high-performance module dedicated to the connection of external sigma-delta (ΣΔ) modulators.

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3.31.1 Features

- 8 serial digital inputs:
  - configurable SPI interface to connect various digital sensors
  - configurable Manchester coded interface support
  - compatible with PDM interface to support digital microphones
- 2 common clocks input/output for ΣΔ modulator(s)
- Flexible matrix (BSMX) for connection between filters and digital inputs
- 2 inputs for connecting internal ADCs
- 8 flexible digital filter paths, including
  - A Configurable CIC filter:
    - Can be split into 2 CIC filters: high resolution filter, and out-off limit detector
    - Can be configured in $Sinc^4$ filter
    - Can be configured in $Sinc^5$ filter
    - Adjustable decimation ratio
  - A reshape filter to improve the out-off band rejection and in-band ripple
  - A high pass filter to cancel the DC offset
  - An offset error cancellation
  - Gain control
  - Saturation blocks
  - An out-off limit detector
- Short-circuit detector,
- Clock absence detector
- 16 or 24-bit signed output data resolution,
- Continuous or single conversion,
- Possibility to delay independently each bitstream
- Various trigger possibilities
- Break generation on out-of limit or short-circuit detector events
- Autonomous functionality in Stop modes
- DMA can be used to read the conversion data
- Interrupts services

Targeted applications:

- Audio: speech capture
- Motor control
- Metering

3.32 Audio digital filter (ADF1)

The audio digital filter (ADF) is a high-performance module dedicated to the connection of external ΣΔ modulators.

3.32.1 Features

- 1 serial digital input:
  - configurable SPI interface to connect various digital sensors
  - configurable Manchester coded interface support
  - compatible with PDM interface to support digital microphones
- 2 common clocks input/output for ΣΔ modulators

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- 1 flexible digital filter paths, including:
  - A MCIC filter configurable in Sinc4 or Sinc5 filter with an adjustable decimation ratio
  - A reshape filter to improve the out-off band rejection and in-band ripple
  - A high pass filter to cancel the DC offset
  - Gain control
  - Saturation blocks
- Clock absence detector
- Sound activity detector
- 4-bit signed output data resolution
- Continuous or single conversion
- Possibility to delay the selected bitstream
- One trigger input
- Autonomous functionality in Stop modes
- DMA can be used to read the conversion data
- Interrupts services

Targeted applications:

- Audio: speech capture
- Metering

3.33 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8- to 14-bit parallel interface, to receive video data. The camera interface can support a resolution of 1 Mpixels @15 fps.

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12-, or 14-bit
- 8-bit progressive video monochrome or RawBayer format, YC_bC_r 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

3.34 Parallel synchronous slave interface (PSSI)

The PSSI and the DCMI use the same circuitry.These two peripherals cannot be used at the same time: when using the PSSI, DCMI registers cannot be accessed, and vice-versa.

The PSSI and the DCMI share also the same alternate functions and interrupt vector.

The PSSI is a generic synchronous 8/16-bit parallel data input/output slave interface. It enables the transmitter to send a data valid signal that indicates when the data is valid, and the receiver to output a flow control signal that indicates when it is ready to sample the data.

Main features:

- Slave mode operation
- 8-bit or 16-bit parallel data input or output
- 8-word (32-byte) FIFO
- Data enable (PSSI_DE) alternate function input, and Ready (PSSI_RDY) alternate function output

3.35 Digital camera interface with pixel processing (DCMIPP)

- Parallel input interface:
  - Up to 16 bits @120 MHz, up to 2 Mpixels sensors @30 fps
  - Pixel format: RGB565, 888, YUV422, RawBayer/Mono 8/10/12/14

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- When connected to CSI-2 input interface:
  - Up to 200 Mpixel/s, up to 5 Mpix sensors @30 fps, supports MIPI CSI-2 v1.3
  - Pixel format: all MIPI CSI-2 v1.3: RGB565, 888, YUV422, RawBayer
  - Features: interleaved packets, 4 virtual channels
- Flow selection and frame control
- Byte-to-pixel conversion
- Statistic removal
- Bad pixel removal (automatic detection and correction of bad pixels from sensor array)
- Decimation of one pixel every 1/2/4/8
- Integrated image processing used to connect low-cost camera module without any embedded ISP
  - Color conversion to adapt to the sensor and tune the Illumination
  - Contrast enhancement
  - RawBayer to RGB conversion (demosaicing)
  - Exposure control
  - Statistics extraction
- Decimation on pipe 0 (pipe dump)
- Parallel pipelines for parallel applications:
  - Pipe0 (for data dump), for a direct dump without processing
  - Pipe1 (for main use), with downsize, color conversion, decoder, multi-planar, and image processing
  - Pipe2 (for ancillary use), with downsize, color conversion, decoder, co-planar
- Downsize
  - Box-filtering, with any decimal ratio, up to 8x8, on pipe1 and pipe2
- Gamma conversion
- RGB to YUV color conversion
- Output pixel format:
  - Pipe0: any data as is, Y/Rb: 8/10/12/14 statistics, bitstreams
  - Pipe2: RGB888, RGB565, YUV422-1, Y8, ARGB and RGBA (co-planar only)
  - Pipe1: Pipe2 formats + YUV422-2, YUV420-2, YUV420-3 (multi-planar possible)
- AXI master

3.36 Camera serial interface (CSI)

The CSI provides an interface between the system and the PHY, allowing communication with a CSI-2 compliant camera.

- Compliant with MIPI Alliance standard v1.3
- Up to two data lanes, up to 2.5 Gbit/s per lane in high-speed (HS) mode and 10 Mbit/s in low-power (LP) mode
- Data transmission in HS and LP modes
- Escape mode (ESC), and ultra-low-power state mode (ULPS)
- CSI-2 virtual channel and data type filtering supporting interleaved data
  - Up to 4 virtual channels
  - Support data formats specified into the MIPI Alliance standard for CSI-2 v1.3 (18 data formats, plus the user defined onces, up to 7 independent data types)
- Internal connection with the DCMIPP

3.37 LCD-TFT display controller (LTDC)

The LTDC handles display composition and rotation, with the following main features:

- 3 display layers with dedicated FIFO
- Input pixel flexible format, including YUV420 full-planar
- Secure layer: protected access to buffer and configuration registers
- Output rotation: 90 and 270 degrees

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- Horizontal and vertical mirror
- Color lookup-table, color keying, gamma, and dithering on output

LTDC parallel interface:

- Provides a 24-bit parallel digital RGB, and delivers all signals to interface directly to a broad range of LCD and TFT panels.
- Up to 150 Mpixel/s, which correspond up to FHD (1920 × 1080) @60 fps resolution with HDMI blankings
- Output pixel formats: RGB888, RGB666, RGB565, YUV422-16 bits

LTDC DSI interface:

- The LTDC provide pixels to the DSI interface (exclusive to other interface).

LTDC LVDS interface:

- The LTDC provide pixels to the LVDS interface (exclusive to other interface).

3.38 Display serial interface (DSI)

Note: Features may be limited or absent in some devices or packages (see Section 2: Description for details).

The DSI is part of a group of communication protocols defined by the MIPI Alliance. The MIPI DSI host controller is a digital core that implements all protocol functions defined in the MIPI DSI specification.

It provides an interface between the system and the MIPI D-PHY that allows the communication with a DSI-compliant display.

- Compliant with MIPI Alliance standards
- Interface with MIPI D-PHY
- Supports all commands defined in the MIPI Alliance specification for DCS
- Bidirectional communication and escape mode support through data lane 0
- Supports non-continuous clock in D-PHY clock lane for additional power saving
- Supports ultra-low-power mode with PLL disabled
- ECC and checksum capabilities
- Support for end of transmission packet (EoTp)
- Fault recovery schemes
- Configurable selection of system interfaces:
  - AMBA APB for control and optional support for generic and DCS commands
  - Video mode interface through LTDC
  - Adapted command mode interface through LTDC
  - Independently programmable virtual channel ID in video mode, adapted command mode and APB slave
- Video mode interfaces features:
  - LTDC interface color coding mappings into 16, 18 and 24-bit interface
  - Programmable polarity of all LTDC interface signals
- Adapted interface features:
  - Support for sending large amounts of data through the memory_write_start (WMS) and memory_write_continue (WMC) DCS commands
  - LTDC interface color coding mappings into 16, 18 and 24-bit interface
- Video mode pattern generator
- Up to 4 × data lanes, up to 2.5 Gbps each
- Up to QXGA (2048 × 1536) @60 fps

3.39 LVDS display interface (LVDS)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

The LVDS supports the following high-level features:

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- FPD-Link-I and OpenLDI (v0.95) protocols
- Single-link or dual-link operation
- Single-display or double-display (with the same content duplicated on both)
- Flexible bit-mapping, including JEIDA and VESA
- RGB888 or RGB666 output
- Up to 2 links of 4 data lanes, up to 1.1 Gbit/s per lane
  - FPD bitrate: 784 Mbit/s per lane (112 Mpixel/s per link, 224 Mpixel/s if dual Link)
  - OpenLDI bitrate: 1100 Mbit/s per lane (157 Mpixel/s per link, 314 Mpixel/s if dual link)
- Up to QXGA (2048 × 1536) @60 fps with dual link
- Up to WSXGA+ (1680 × 1050) @60 fps with single link (1080p60 supported with OpenLDI)

3.40 Video encoder (VENC)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

- Video encode
  - H264 (MPEG4_Part10/AVC, baseline/main/high up to 5.2), VP8
  - Up to 1080p60 for H264/VP8 (performance shared with the VDEC)
- Still-image encode
  - JPEG (baseline interleaved)
  - Up to 500 Mpixel/s for JPEG (performance shared with the VDEC)
- VDERAM
  - 128 Kbytes
  - Hardware handshake between VENC and VDEC
  - Can be statically assigned to CPU as additional system RAM by SYSCFG setting

3.41 Video decoder (VDEC)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

- Video decode
  - H264 (MPEG4_Part10/AVC, baseline/main/high up to 5.2), VP8
  - Up to 1080p60 for H264/VP8 (performance shared with the VENC)
- Still-image decode
  - JPEG (baseline interleaved).
  - Up to 500 Mpixel/s for JPEG (performance shared with the VENC)
- VDERAM
  - 128 Kbytes
  - Hardware handshake between VENC and VDEC
  - Can be statically assigned to CPU as additional system RAM by SYSCFG setting

3.42 True random number generator (RNG)

All devices embed an RNG that deliver s 32-bit random numbers generated by an integrated analog circuit.

3.43 Hash processor (HASH)

The HASH is a fully compliant implementation of the secure hash algorithm (SHA-1, SHA-2 family, SHA-3 family), and the HMAC (keyed-hash message authentication code) algorithm. The HMAC is suitable for applications that require a message authentication.

The HASH computes FIPS (federal information processing Standards) approved digests of 160-, 224-, 256-, 384-, and 512-bit length, for messages of any length:

- less than 2^{64} bits (for SHA-1, SHA-224, and SHA-256)
- less than 2^{128} bits (for SHA-384, SHA-512)

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3.44 Cryptographic processor (CRYP1/2)

The devices embed two cryptographic processor that can be used both to encrypt and decrypt data using the DES, triple-DES, or AES algorithms. The implementation if fully compliant with the following standards:

- DES and TDES are defined by FIPS (PUB 46-3, Oct 1999), and by the American National Standards Institute (ANSI X9.52)
- AES is defined by FIPS (FIPS PUB 197, Nov 2001)

Multiple key sizes and chaining modes are supported:

- DES/TDES chaining modes ECB and CBC, supporting standard 56-bit keys with 8-bit parity per key
- AES chaining modes ECB, CBC, CTR, GCM, GMAC, CCM for key sizes of 128, 192, or 256 bits

The CRYP in AES mode supports key sharing from SAES co-processor. It is a 32-bit AHB peripheral with DMA support for incoming and outgoing data.

The CRYP also includes input and output FIFOs (each 8 words deep) for better performance.

3.45 Secure AES (SAES)

The SAES encrypts or decrypts data, using an algorithm and implementation fully compliant with the AES standard. It implements embedded protection against differential power analysis (DPA) and related side-channel attacks.

The SAES supports CTR, GCM, GMAC, CCM, ECB, and CBC chaining modes for key sizes of 128 or 256 bits, as well as special modes such as hardware secret key encryption/decryption (wrapped-key mode) and key sharing with faster CRYP peripheral (shared-key mode).

The SAES can load directly two hardware master keys that are not directly accessible by any software. These keys can be used to encrypt random keys that are usable only on this device, and are not directly accessible by software.

The SAES supports DMA single transfers for incoming and outgoing data (two DMA channels required). It is connected by hardware to the RNG and to the CRYP1/2.

The SAES is an AMBA AHB slave peripheral.

3.46 Public key accelerator (PKA)

The PKA is intended for the computation of cryptographic public key primitives, specifically those related to RSA, Diffie-Hellmann, or ECC (elliptic curve cryptography) over GF(p) (Galois fields). To achieve high performance at a reasonable cost, these operations are executed in the Montgomery domain.

For a given operation, all needed computations are performed within the accelerator: no further hardware/software elaboration is needed to process inputs or outputs.

3.47 Boot and security and OTP control (BSEC)

The BSEC is used to control an OTP (one-time programmable) fuse box, used for embedded non-volatile storage for device configuration and security parameters.

Embedded non-volatile secrets are stored in the BSEC upper area that is only accessible while BSEC is operating in a closed state. In open state those non-volatile secrets are permanently hidden.

The BSEC use is reserved to trusted domain CPU, and boot CPU following a BSEC reset (cold/warm or hot).

3.48 Timers and watchdogs

The devices include three advanced-control timers, twelve general-purpose timers, two basic timers, five low-power timers, seven watchdogs, two SysTick timers in CortexM33 , one SysTick timer in Cortex-M0+, and four system timers in each Cortex-A35.

All timer counters can be frozen in debug mode.

The table below compares features of the different timers.

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Table 7. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary output	Max interface clock (MHz)	Max[1] timer clock (MHz)
Advanced -control	TIM1, TIM8 , TIM20	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	6	4	200	200
General purpose	TIM2, TIM3, TIM4, TIM5	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No	200	200
	TIM10, TIM11, TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	200	200
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	200	200
	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1	200	200
	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1	200	200
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	200	200
Low-power	LPTIM1, LPTIM2	16-bit	Up, Up/down	1, 2, 4, 8, 16, 32, 64, 128	Yes	2[2]	No	200	100
	LPTIM3, LPTIM4	16-bit	Up	1, 2, 4, 8, 16, 32, 64, 128	Yes	2[2]	No	200[3]	100[4]
	LPTIM5	16-bit	Up	1, 2, 4, 8, 16, 32, 64, 128	No	0	No	200[3]	100

1. *The maximum timer clock depends on RCC settings.*
2. *only compare channel.*
3. *16 MHz bus clock when supplied by the backup regulator (LP-Stop1/2, LPLV-Stop1/2 or Standby1).*
4. *32 kHz timer clock in autonomous mode (Stop1/2, LP-Stop1/2, LPLV-Stop1/2 or Standby1).*

3.48.1 Advanced-control timers (TIM1/8/20)

The advanced-control timers can be seen as three-phase PWM generators multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their four independent channels can be used for:

- input capture
- output compare
- PWM generation (edge- or center-aligned modes)
- one-pulse mode output

If configured as standard 16-bit timers, the advanced-control timers have the same features as the general-purpose timers. If configured as 16-bit PWM generators, they have full modulation capability (0 to 100%).

The advanced-control timers can work together with general-purpose timers via the timer link feature for synchronization or event chaining.

TIM1, TIM8 and TIM20 support independent DMA request generation.

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3.48.2 General-purpose timers (TIM2/3/4/5/10/11/12/13/14/15/16/17)

There are twelve synchronizable general-purpose timers embedded in STM32MP25xC/F devices (see Table 7 for differences).

- **TIM2, TIM3, TIM4, TIM5**

These timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. They feature four independent channels for input capture/output compare, PWM, or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

These timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1, TIM8 and TIM20, via the timer link feature for synchronization or event chaining.

Any of these general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 have independent DMA request generation. They can handle quadrature (incremental) encoder signals, and the digital outputs from one to four halleffect sensors.

- **TIM10, TIM11, TIM12, TIM13, TIM14, TIM15, TIM16, TIM17**

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13, TIM14, TIM16 and TIM17 feature one independent channel, whereas TIM12 and TIM15 have two independent channels for input capture/output compare, PWM, or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers or used as simple timebases.

3.48.3 Basic timers (TIM6/TIM7)

These timers are used as a generic 16-bit time base, and support independent DMA request generation.

3.48.4 Low-power timer (LPTIM1/2/3/4/5)

These low-power timers have an independent clock and run in Stop mode if they are clocked by LSE, LSI, or an external clock. They can wake up the device from Stop mode.

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/one-shot mode
- Selectable software/hardware input trigger
- Selectable clock source:
  - Internal clock source: LSE, LSI, HSI (RCC flexgen output)
  - External clock source over LPTIM input (working even with no internal clock source running, used by the pulse counter application)
- Programmable digital glitch filter
- Encoder mode (LPTIM1/2)

3.48.5 Independent watchdog (IWDG1/2/3/4/5)

The IWDG is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI). As it operates independently from the main clock, the IWDG can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

3.48.6 System window watchdog (WWDG1/2)

The WWDG is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.48.7 SysTick timer

This timer is embedded in the Cortex-M33 (two instances, secure and non-Secure) , and in the Cortex-M0+ core. It is dedicated to real-time operating systems, but can also be used as standard downcounter.

- 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0

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- Programmable clock source

3.48.8 Cortex-A35 generic timers (CNT)

The Cortex-A35 generic timers are fed by value from system timing generation (STGEN). The Cortex-A35 processor provides a set of four timers for each processor:

- Physical timer for use in secure and non-secure modes. The registers for the physical timer are banked to provide secure and non-secure copies.
- Virtual timer for use in non-secure mode
- Physical timer for use in hypervisor mode

These generic timers are not memory-mapped peripherals: they are accessible only by specific Cortex-A35 coprocessor instructions (cp15).

3.49 System timer generation (STGEN)

The STGEN generates a time-count value that provides a consistent view of time for all Cortex-A35 generic timers.

- 64-bit wide to avoid roll-over issues
- Starts from zero or a programmable value
- control APB interface (STGENC) that enables the timer to be saved and restored across powerdown events
- Read-only APB interface (STGENR) that enables the timer value to be read by nonsecure software and debug tools
- timer value incrementing that can be stopped during system debug

3.50 Real-time clock (RTC)

The RTC provides an automatic wake-up to manage all low-power modes. It is an independent BCD timer/counter that provides a time-of-day clock/calendar with programmable alarm interrupts.

The RTC includes also a periodic programmable wake-up flag with interrupt capability.

After backup domain reset, all RTC registers are protected against possible parasitic write accesses.

As long as the supply voltage remains in the operating range, the RTC never stops, regardless of the device status (Run mode, low-power mode, or under reset).

- Calendar with subseconds, seconds, minutes, hours (12 or 24 format), day (day of week), date (day of month), month, and year
- Daylight saving compensation programmable by software
- Programmable alarm with interrupt function. The alarm can be triggered by any combination of the calendar fields.
- Automatic wake-up unit that generates a periodic flag that triggers an automatic wakeup interrupt
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Accurate synchronization with an external clock using the subsecond shift feature
- Digital calibration circuit (periodic counter correction): 0.95 ppm accuracy, obtained in a calibration window of several seconds
- Timestamp function for event saving
- Maskable interrupts/events:
  - Alarm A
  - Alarm B
  - Wake-up interrupt
  - Timestamp
- TrustZone support:
  - RTC fully securable
  - Alarm A, alarm B, wake-up timer and timestamp individual secure or non-secure configuration

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Prerelease product(s)

3.51 Tamper and backup registers (TAMP)

The 128 x 32-bit backup registers are retained in all low-power modes, and in V_{BAT} mode. They can be used to store sensitive data as their content is protected by a tamper detection circuit. 16 tamper pins (eight input and eight outputs), and 14 internal tampers are available for anti-tamper detection.

The eight external tamper pins can be configured for edge detection, edge and level, level detection with filtering, or up to eight active tamper which increases the security level by auto-checking that tamper pins are not externally opened or shorted.

- 128 backup registers (TAMP_BKPxR) implemented in the RTC domain that remains powered-on by V_{BAT} when the V_{DD} power is switched off
- 8 external tamper detection events:
  - Each external event can be configured to be active or passive.
  - External passive tampers with configurable filter and internal pull-up
- 14 internal tamper events
- Any tamper detection can generate an RTC timestamp event.
- Any tamper detection erases backup registers.
- TrustZone support:
  - Tamper secure or non-secure configuration
  - Backup registers configuration in three configurable-size areas:
    - 1 read/write secure area
    - 1 write secure/read non-secure area
    - 1 read/write non-secure area
- Monotonic counter

3.52 Inter-integrated circuit interface (I2C1/2/3/4/5/6/7/8)

STM32MP251C devices embed eight I^2C interfaces, that handle communications between the device and the serial I^2C bus. Each I^2C interface controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 Kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 Kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System management bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources that allows the I^2C communication speed to be independent from the PCLK reprogramming
- Wake-up from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

3.53 Improved inter-integrated circuit (I3C1/2/3/4)

STM32MP25xC/F devices embed four I3C interfaces, that handle communication between the device and others that are all connected on an I^3C bus, like sensors and host processors.

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The I3C peripheral implements all required features of the MIPI I3C specification v1.1. It can control all I^3C bus-specific sequencing, protocol, arbitration and timing, and can be acting as controller (formerly known as master), or as target (formerly known as slave).

The I3C peripheral, acting as controller, improves the I^2C interface features still preserving some backward compatibility: it allows an I^2C target to operate on an I^3C bus in legacy I^2C fast-mode (Fm) or legacy I^2C fast-mode plus (Fm+), provided that this latter does not perform clock stretching.

The I3C peripheral can be used with DMA in order to off-load the CPU.

- MIPI I3C specification v1.1 (see I3C section in the reference manual), as:
  - I3C primary controller
  - I3C secondary controller
  - I3C target
- Registers configuration from the host application via the APB slave port
- Queued transfers:
  - Transmit FIFO (TX-FIFO) for data bytes/words to be transmitted on I^3C bus
  - Receive FIFO (RX-FIFO) for received data bytes/words on I^3C bus
  - Control FIFO (C-FIFO) for control words to be sent on I^3C bus, when controller
  - Status FIFO (S-FIFO) for status words as received on I^3C bus, when controller
  - For each FIFO, optional DMA mode with a dedicated DMA channel
- Messages:
  - Legacy I2C read/write messages to legacy I2C targets in Fm/Fm+
  - I3C SDR read/write private messages
  - I3C SDR (write) broadcast CCC messages
  - I3C SDR read/write direct CCC messages
- Frame-level management, when controller:
  - Software-triggered or hardware-triggered transfer
  - Optional C-FIFO and TX-FIFO preload
  - Multiple messages encapsulation
  - Optional arbitrable header
- Programmable bus timing, when controller
  - SCL high and low period
  - SDA hold time
  - Bus free (minimum) time (between a stop and a start)
  - Bus available/idle condition time, maximum clock stall time
  - Minimum clock stall time during 9th bit
- Target-initiated requests management:
  - In-band interrupts, with programmable IBI payload (up to 4 bytes)
  - Bus control request, with recovery flow support and hand-off delay
  - Hot-join mechanism
  - Pending read notification
- Bus error management
  - M0, M1, M2, and M3, when controller
  - S0, S1, S2, S3, S4, S5, and S6 when target
  - bus control switch error and recovery
  - target reset
- Separately programmed event/flag generation and management
  - Separated identification and clear control
  - Host application notification via event/flag polling, and/or via interrupt with a perevent programmable enable
  - Error type identification
- Autonomous mode and transfers during Sleep and Stop modes via DMA

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- Autonomous wake-up on
  - Slave request acknowledge, when controller
  - Missed start detection, when target
  - Reset pattern detection, when target

3.54 Universal synchronous asynchronous receiver transmitter (USART1/2/3/6, UART4/5/7/8/9)

STM32MP25xC/F devices embed four USART and five UART (see Table 8. USART/UART features for feature summary).

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode, and have LIN master/slave capability. They provide hardware management of CTS and RTS signals, and RS485 Driver Enable. They can communicate at speeds of up to 10 Mbit/s.

The USARTs embed a 64-bytes transmit FIFO (TXFIFO) and a 64-bytes receive FIFO (RXFIFO). The FIFO mode is enabled by software, and is disabled by default.

All USARTs provide Smartcard mode (ISO 7816 compliant) and SPI-like communication capability. They have a clock domain independent from the CPU clock: this allows the USARTx to wake up the device from Stop mode using baudrates up to 200 Kbaud. Wake-up events from Stop mode are programmable and can be one of the following:

- start bit detection
- any received data frame
- a specific programmed data frame

All USARTs can be served by the DMA controller.

Table 8. USART/UART features

Modes/features[1]	USART1/2/3/6	UART4/5/7/8/9
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode (master/slave)	X	-
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	X
LIN mode	X	X
Dual clock domain and wakeup from low power mode	X	X
Receiver timeout interrupt	X	X
Modbus communication	X	X
Auto-baudrate detection	X	X
Driver enable	X	X
Data length	7, 8, and 9 bits	

1. *X = supported.*

3.55 Low-power universal asynchronous receiver transmitter (LPUART1)

The devices embed one LPUART that supports asynchronous serial communication with minimum power consumption. The LPUART supports half-duplex single-wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART embeds a transmit FIFO (TXFIFO) and a receive FIFO (RXFIFO). The FIFO mode is enabled by software, and is disabled by default.

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The LPUART has a clock domain independent from the CPU clock, and can wake up the system from Stop mode. The wake-up from Stop mode is programmable, and can be done on one of the following:

- a start bit detection
- any received data frame
- a specific programmed data frame
- specific TXFIFO/RXFIFO status when FIFO mode is enabled

Even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low-energy consumption.

The LPUART interface can be served by the LPDMA controller.

3.56 Serial peripheral interface (SPI1/2/3/4/5/6/7/8) inter-integrated sound interfaces (I2S1/2/3)

The devices feature up to eight SPIs that allow communication at up to 50 Mbit/s in master and slave modes, in half-duplex, full-duplex, and simplex modes. The 3-bit prescaler gives eight master mode frequencies, and the frame is configurable from 4 to 16 bits.

All SPI interfaces support NSS pulse mode, TI mode, hardware CRC calculation, and eight 8-bit embedded Rx and Tx FIFOs with DMA capability.

The standard I^2S interfaces (multiplexed with SPI1, SPI2 and SPI3) can be operated in master or slave mode, in full-duplex and half-duplex communication modes. They can be configured to operate with a 16-/32-bit resolution as an input or output channel.

Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency. All I^2S interfaces support 16x 8bit embedded Rx and Tx FIFOs with DMA capability.

3.57 Serial audio interfaces (SAI1/2/3/4)

The devices embed four SAIs that are used to design many stereo or mono audio protocols such as I^2S, LSB or MSB-justified, PCM/DSP, TDM, or AC'97. An SPDIF output is available when the audio block is configured as a transmitter. To bring this level of flexibility and reconfigurability, the SAI contains two independent audio subblocks. Each block has it own clock generator and I/O line controller.

Audio sampling frequencies up to 192 kHz are supported.

Up to eight microphones can be supported thanks to an embedded PDM interface.

The SAI can work in master or slave configuration. The audio subblocks can be either receiver or transmitter, and can work synchronously or asynchronously (with respect to the other one). The SAI can be connected with other SAIs to work synchronously.

3.58 SPDIF receiver interface (SPDIFRX)

The SPDIFRX is designed to receive an S/PDIF flow compliant with IEC-60958 and IEC61937. These standards support simple stereo streams up to high sample rate, and compressed multi-channel surround sound, such as those defined by Dolby® or DTS® (up to 5.1).

- Up to 4 inputs available
- Automatic symbol rate detection
- Maximum symbol rate: 12.288 MHz
- Stereo stream from 32 to 192 kHz supported
- Supports audio IEC-60958 and IEC-61937, consumer applications
- Parity bit management
- Communication using DMA for audio samples
- Communication using DMA for control and user channel information
- Interrupt capabilities

The SPDIFRX receiver provides all necessary features to detect the symbol rate, and to decode the incoming data stream. The user can select the wanted SPDIF input, and when a valid signal is available, the SPDIFRX re-samples the incoming signal, decodes the Manchester stream, and recognizes frames, sub-frames, and blocks elements. It delivers to the CPU decoded data, and associated status flags.

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The SPDIFRX also offers a signal named spdif_frame_sync, which toggles at the S/PDIF sub-frame rate: this signal is used to compute the exact sample rate for clock drift algorithms.

3.59 Secure digital input/output MultiMediaCard interface (SDMMC1/2/3)

Three SDMMCs provide an interface between the AHB bus and SD memory cards, SDIO and e.MMC devices.

SDMMC features include the following:

- Full compliance with MultiMediaCard System Specification Version 5.1

Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit (HS200 speed limited by maximum allowed I/O speed, HS400 is not supported).

- Full compatibility with previous versions of MultiMediaCards (backward compatibility)
- Full compliance with SD memory card specifications version 6.0 (SDR104 SDMMC_CK speed limited to maximum allowed I/O speed, SPI and UHS-II modes not supported)
- Full compliance with SDIO card specification version 4.0

Card support for two different databus modes: 1-bit (default) and 4-bit (SDR104 SDMMC_CK speed limited to maximum allowed I/O speed, SPI and UHS-II modes not supported)

- Data transfer up to 208 Mbyte/s for the 8-bit mode (depending on the maximum allowed I/O speed)
- Data and command output enable signals to control external bidirectional drivers
- The SDMMC host interface embeds a dedicated DMA controller that allows high-speed transfers between the interface and the SRAM.
- IDMA linked list support

Each SDMMC is coupled with a delay block (DLYBSD) that supports an external data frequency above 100 MHz.

3.60 Controller area network (FDCAN1/2/3)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

The CAN subsystem consists of three FDCANs, a shared message RAM, and a clock calibration unit.

All FDCANs are compliant with ISO 11898-1 (CAN protocol specification version 2.0 part A, B), and CAN FD protocol specification version 1.0.

FDCAN1 supports time triggered CAN (TTCAN) specified in ISO 11898-4, including event synchronized time-triggered communication, global system time, and clock drift compensation. The FDCAN1 contains additional registers, specific to the time triggered feature. The CAN FD option can be used together with event-triggered and time-triggered CAN communication.

A 10 Kbyte message RAM implements filters, receives FIFOs, receives buffers, transmits event FIFOs, transmits buffers (and triggers for TTCAN). This message RAM is shared between all FDCANs.

The common clock calibration unit is optional. It can be used to generate a calibrated clock for FDCANs from the HSI internal RC oscillator and the PLL, by evaluating CAN messages received by the FDCAN1.

3.61 Universal serial bus Hi-Speed host (USBH)

The devices embed one USB Hi-Speed host (up to 480 Mbit/s) with one physical port. USBH supports both low, full-speed (OHCI) as well as Hi-Speed (EHCI) operations. It integrates a physical interface (PHY) which can be used for either low-speed (1.2 Mbit/s), full-speed (12 Mbit/s) ,or Hi-Speed operation (480 Mbit/s).

The USBH is compliant with the USB 2.0 specification.

3.62 USB Type-C Power Delivery controller (UCPD1)

The devices embed one controller compliant with USB Type-C Rev.1.2 and USB Power Delivery Rev. 3.1 specifications.

The UCPD use specific I/Os supporting the USB Type-C and USB Power Delivery requirements, featuring:

- USB Type-C pull-up (Rp, all values) and pull-down (Rd) resistors
- USB Power Delivery message transmission and reception

The digital controller handles notably:

- USB Type-C level detection with de-bounce, generating interrupts
- byte-level interface for USB Power Delivery payload, generating interrupts (DMA compatible)
- USB Power Delivery timing dividers (including a clock pre-scaler)

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- CRC generation/checking
- 4b5b encode/decode
- ordered sets (with a programmable ordered set mask at receive)
- frequency recovery in receiver during preamble

The interface offers low-power operation compatible with Stop mode, maintaining the capacity to detect incoming USB Power Delivery messages.

3.63 Universal serial bus 3.0 dual role data (USB3DR)

- 5 Gbit/s PHY (COMBOPHY)
- xHCI model.
- Dual Role Data. The USB3DR can be configured statically as a Host or Device port.
- OTG is not supported:
  - Dynamic switch from Host (resp. Device) to Device (resp. Host) role is not supported.
  - Host Negotiation Protocol (HNP), Role Swap Protocol (RSP), Session Request Protocol (SRP), Attach Detection Protocol (ADP) are not supported.
- USB3 SuperSpeed mode (5 Gbit/s), as well as USB2 Low-Speed/Full-Speed/Hi-Speed modes (when Host) or USB2 Full-Speed/Hi-Speed modes (when Device).
- Descriptor caching and data pre-fetching to meet system performance.
- Variable FIFO buffer allocation for each endpoint.
- Simultaneously 4 Gbps IN and 4 Gbps OUT bandwidth
- DMA engine
- Supports Battery Charging v1.2, with the exception of the Accessory Charger Adapter mode

The standards supported are:

- Universal Serial Bus 3.0 Specification, Revision 1.0, November 12, 2008
- Universal Serial Bus Specification, Revision 2.0, USB Implementers Forum, Inc., April 27, 2000
- Errata for “USB Revision 2.0 April 27 2000” as of May 28, 2002, USB-IF
- eXtensible Host Controller Interface for Universal Serial Bus (xHCI), Revision 1.1, Intel Corp., December 20, 2013
- UTMI+ Specification, Revision 1.0, ULPI Working Group, February 25, 2004
- Battery Charging Specification, Revision 1.2, December 7, 2010

3.64 PCI Express interface (PCIE)

The PCIE controller has the following features:

- one lane Generation2 PCIe
- dual-mode (RC or EP)
- PTM
- 256 byte maximum payload size
- Remote device maximum read request size 1K Byte
- Single Virtual Channel
- Single Function
- Legacy INTx support, MSI and GICv2m host support
- ASPM L0s and L1, and L1.1 substate
- AER
- internal ATU
- 5 Gbit/s PHY (COMBOPHY)

An included PCIe reference clock generator (REFGEN) provides a 100 MHz differential clock to a PCIe link partner. This can be used to eliminate the external 100 MHz clock source that is typically found in PCIe common-clock implementations.

The PCIE internal reference clock is 25 MHz (without SSC). There is also the option of an external PCIE differential reference clock 100 MHz (with SSC).

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3.65 5-Gbit/s PHY controller (COMBOPHY)

The COMBOPHY control a 5-Gbit/s multi-protocol PHY, that is used by the USB3DR or the PCIE (mutually exclusive). It supports data rates up to 5 Gbit/s for USB3.0, 5 Gbit/s for PCIe gen2, and 2.5 Gbit/s for PCIe gen1.

The COMBOPHY includes the physical coding sublayer (PCS) blocks that perform 8-/10bit encoding/decoding, and resynchronizing RX data to the local clock domain.

The COMBOPHY is single lane. The SuperSpeed lane multiplexing for USB Type-C must be managed by a switch outside the device.

3.66 Gigabit Ethernet MAC interface (ETH1/2)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

The devices embed two fully independent instances of a 10/100/1000 Ethernet MAC controller, that enable transmission and reception of data over Ethernet, in compliance with IEEE 802.3-2008.

Each Ethernet MAC controller is connected to an external Ethernet PHY via a standard media independent interface.

Features provided by the Ethernet controller include:

- 10, 100, and 1000 Mbps data transfer rates
- Full-duplex and half-duplex operations
- Standard or Jumbo Ethernet packets
- Two independent Rx queues and two independent Tx queues, with each queue associated to a (subset of) PCP code(s)
- Configurable media-independent interface to external PHY:
  - RGMII
  - MII
  - RMII
  - MDIO master interface for external PHY device configuration
  - Internal or external reference clocks
- Low-power support:
  - Energy Efficient Ethernet (EEE) compliant with IEEE 802.3az-2010;
  - Detection of LAN wake-up frames and “Magic Packet” frames
- Timing and synchronization:
  - compliance with IEEE 1588-2008 (PTP) and IEEE 802.1AS-Rev
  - hardware “auxiliary timestamp trigger” for accurate sampling of the “PTP system clock”
  - Internal or external system time
- Time-sensitive networking:
  - “Forwarding and Queuing Enhancements for Time-Sensitive Streams” compliant with IEEE 802.1Qav
  - “Enhancements to Scheduled Traffic” compliant with IEEE 802.1Qbv, with a gate control list depth up to 128
  - “Frame Preemption” compliant with IEEE 802.1Qbu and IEEE 802.3br
- Preamble and start-of-frame data insertion (for Tx) and deletion (for Rx)
- Option for automatic CRC generation (for Tx), checking and stripping (for Rx)
- Source address field insertion or replacement in transmitted packets
- Filtering options:
  - Perfect match with a given SA/DA (up to 3 MAC addresses are supported)
  - 64-bit Hash filter match
  - Several multicast/broadcast rules supported
  - Based on IEEE 802.1q ‘VLAN tag’ field (perfect match, hash filtering)
  - Support for different ‘VLAN tag’ filtering for each Rx queue
  - Based on TCP/UDP/IP address (perfect match, inverse filtering)

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- TCP/IP offloading:
  - Checksum calculation and insertion in the transmit path
  - Checksum error detection in the receive path.
  - TCP segmentation offload (automatic split of a large TCP packet into smaller Ethernet frames)

3.67 Gigabit Ethernet switch (ETHSW)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

A 3-port gigabit Ethernet switch is included. The switch supports TSN and related standards, and also includes a cut-through accelerator (called ACM) for the two external ports.

Two switch ports are available externally providing RGMII and RMII interfaces. The third port is connected internally to the ETH1 controller.

The switch can be completely bypassed. In this case, ETH1 is connected directly to a single external port.

3.68 Debug infrastructure

The devices offer a comprehensive set of debug and trace features to support software development and system integration.

- Breakpoint debugging
- Code execution tracing
- Software instrumentation
- JTAG debug port
- Serial-wire debug port
- Trigger input and output
- Serial-wire trace port
- Trace port
- Arm CoreSight debug and trace components

The debug can be controlled via a JTAG/serial-wire debug access port, using industry standard debugging tools.

A trace port allows data to be captured for logging and analysis.

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4 Pinouts/ballouts, pin description, and alternate functions

4.1 Ballout schematics

Figure 6. STM32MP25xC/F VFBGA361 pinout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	VSS	DSI_D3P	DSI_D2P	DSI_CKN	DSI_D0N	DSI_D1N	PB8	PB9	PB3	PD2	PD15	PD6	PD14	PE2	PE3	PE13	DDR_DQ11	DDR_DQ9	VSS
B	VDDCSI	DSI_D3N	DSI_D2N	DSI_CKP	DSI_D0P	DSI_D1P	PB11	PB0	PB5	PD11	PI10	PD5	PE0	PE4	PE8	PE11	DDR_DQ10	DDR_DQS1N	DDR_DQS1P
C	CSI_CKP	CSI_CKN	VSS	DSI_REXT	VDDA18DSI	VDDDSI	VSS	PB6	PB4	PD9	PD0	PD4	PE1	PE5	PE7	PE12	DDR_DQ8	DDR_DQ15	DDR_DQM1
D	CSI_D1P	CSI_D1N	VDDA18CSI	PI6	PI7	VDDIO4	PB7	PD3	PB1	VDDIO1	PD10	PD7	VSS	PE15	PE10	VDDA18DDR	DDR_DQ14	DDR_DQ13	DDR_DQ12
E	CSI_D0N	CSI_D0P	CSI_REXT	PG15	PG8	VDDIO4	PG7	VSS	PB2	VDDIO3	PD8	PB10	VDDCPU	PB12	VDDA18PLL1	VSS	DDR_RESETN	DDR_A9	DDR_A20
F	LVDS1_D0N	LVDS1_D0P	LVDS1_D1N	LVDS1_D1P	PG10	VSS	PG11	VDDIO2	PD1	VDDIO3	VSS	PI11	VSS	PE6	PE9	VDDQDDR	DDR_A0	DDR_A11	DDR_A21
G	PI4	PG9	LVDS1_D2N	LVDS1_D2P	PF15	VDDA18PLL2	PF14	VSS	PD13	VDDCORE	VSS	PH4	VDDCPU	PE14	PB13	DDR_ZQ	DDR_A1	DDR_A10	DDR_A22
H	PI0	PF13	LVDS1_D4N	LVDS1_D4P	PG14	VDDA18PLL3	PG12	VDD	PI3	VSS	VDDCORE	PG3	VSS	PD12	PB14	VSS	DDR_A25	DDR_A8	DDR_A23
J	VDDLVDS	LVDS1_D3N	LVDS1_D3P	VDDA18LVDS	PI2	VSS	PG13	VSS	PI1	VDDCORE	VSS	PA5	VDDCPU	VSS	PB15	VDDQDDR	DDR_A2	DDR_A13	DDR_A3
K	PG5	PG6	PZ6	VSS	VSS	PI9	PI5	VDD	PA8	VSS	VDDCORE	PA9	VSS	PH3	PA7	VSS	DDR_VREF	DDR_A14	DDR_A26
L	PZ7	PZ9	PZ8	PZ4	PZ0	VDD	PF12	VSS	PF10	VDDCORE	VSS	PH7	VDDCPU	PH2	PH6	VDDQDDR	DDR_A5	DDR_A15	DDR_A27
M	OSC32_OUT	OSC32_IN	PZ2	PZ1	PZ3	VSSAON	PG2	V08CAP	PH5	VSS	VDDGPU	PH8	VDDCPU	PA6	PA10	VDDQDDR	DDR_A4	DDR_A16	DDR_A28
N	PDR_ON	NRST	PZ5	PI8	VDDA18AON	VDDA18ADC	PG4	VDDCORE	PF0	VDDCORE	VSS	PA2	VSS	VDDGPU	PA1	VSS	DDR_A6	DDR_A17	DDR_A29
P	PWR_LP	PWR_CPU_ON	BOOT1	PC13	ANA1	VSSA	PF5	VSS	PF2	VSS	VDDGPU	PA4	VDDGPU	VSS	PA0	VDDQDDR	DDR_A7	DDR_A18	DDR_A30
R	OSC_IN	OSC_OUT	BOOT3	PG1	ANA0	VBAT	PC6	PA12	PA11	VDDGPU	VSS	PA3	VDDA18COMBOPHY	VDD33USB	USB3DR_TXRTUNE	VSS	DDR_A12	VSS	DDR_A31
T	NRSTC1MS	BOOT0	BOOT2	PF11	PG0	PF9	PC5	PA14	PC2	PA15	PH11	DNU	VDDA18USB	VDDCOMBOPHY	USBH_HS_TXRTUNE	VDDQDDR	DDR_DQM0	DDR_DQ5	DDR_DQ4
U	VREF-	VREF+	PWR_ON	PC3	PF6	PC8	PF8	PF1	PH13	PH10	VDD33UCPD	VDDPCIECLK	PCIE_CLKINP	PCIE_CLKOUTP	COMBOPHY_TX1P	COMBOPHY_RX1P	DDR_DQ3	DDR_DQ7	DDR_DQ6
V	JTDO-TRACESWO	NJTRST	PC4	PC12	PC11	PC9	PF7	PH12	PC0	PC1	USBH_HS_DM	USB3DR_DM	PCIE_CLKINN	PCIE_CLKOUTN	COMBOPHY_TX1N	COMBOPHY_RX1N	DDR_DQ2	DDR_DQS0N	DDR_DQS0P
W	VSS	JTMS-SWDIO	JTDI	JTCK-SWCLK	PC7	PC10	PF4	PH9	PA13	PF3	USBH_HS_DP	USB3DR_DP	UCPD1_CC1	UCPD1_CC2	COMBOPHY_REXT	VDDCOMBOPHYTX	DDR_DQ1	DDR_DQ0	VSS

DT73148V1

1. *The above figure shows the package top view.*
2. *VDDGPU, VDDA18DSI, VDDDSI, VDDA18LVDS, and VDDLVDS are DNU on product without the related feature (respectively GPU/NPU, DSI and LVDS) and must be connected to VSS. DSI_xxx and LVDSx_xxx are DNU on product without the related feature (respectively DSI and LVDS) and must be left open. See Section 2 for details on feature availability. Alternatively, for PCB compatibility purposes, those balls could be connected in same ways as for a product with enabled feature. Refer to AN5489 for additional details.*

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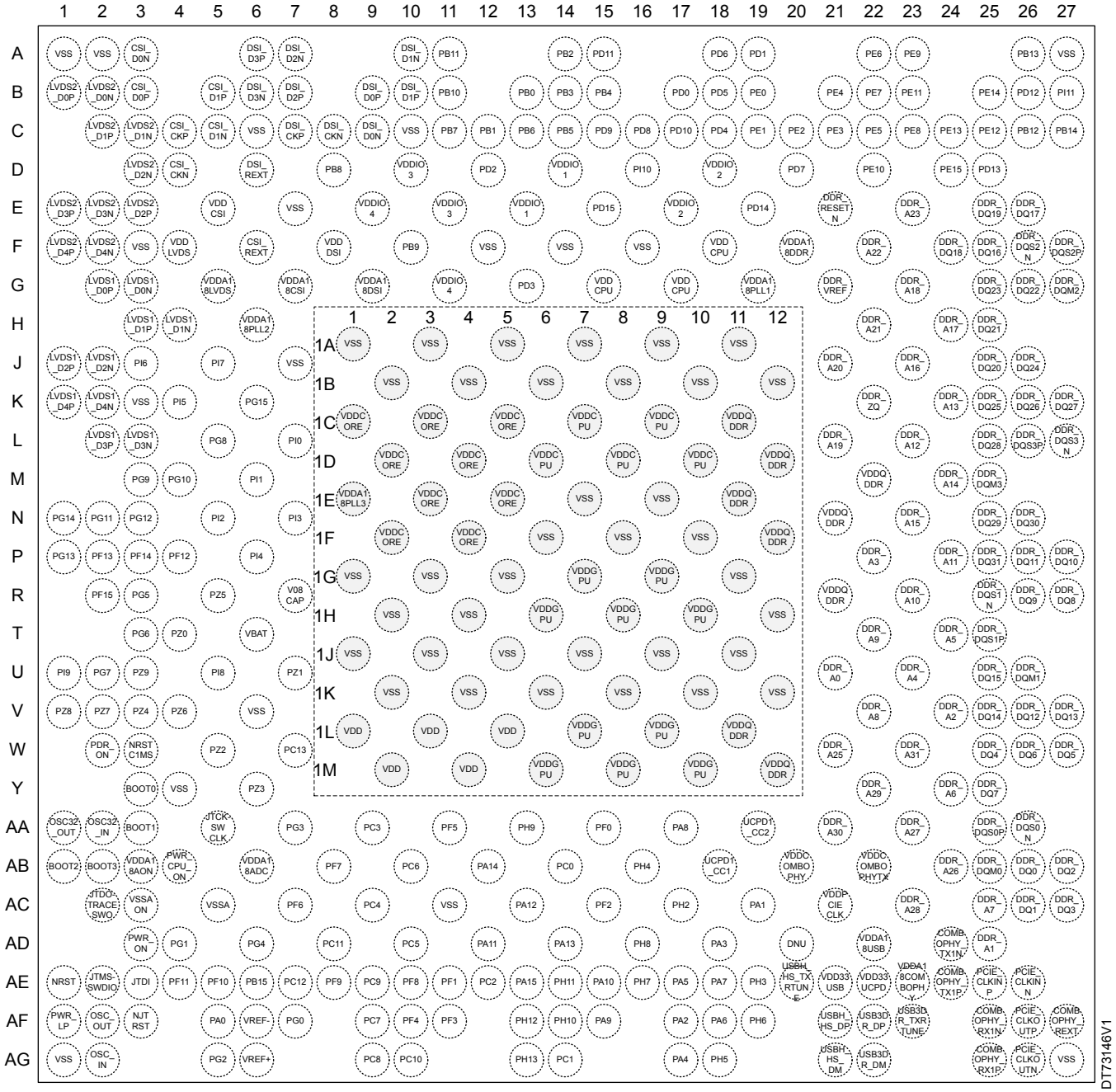
Figure 7. STM32MP25xC/F VFBGA424 pinout



1. *The above figure shows the package top view.*
2. *VDDGPU, VDDA18DSI, VDDDSI, VDDA18LVDS, and VDDLVDS are DNU on product without the related feature (respectively GPU/NPU, DSI and LVDS) and must be connected to VSS. DSI_xxx and LVDSx_xxx are DNU on product without the related feature (respectively DSI and LVDS) and must be left open. See Section 2 for details on feature availability. Alternatively, for PCB compatibility purposes, those balls could be connected in same ways as for a product with enabled feature. Refer to AN5489 for additional details.*

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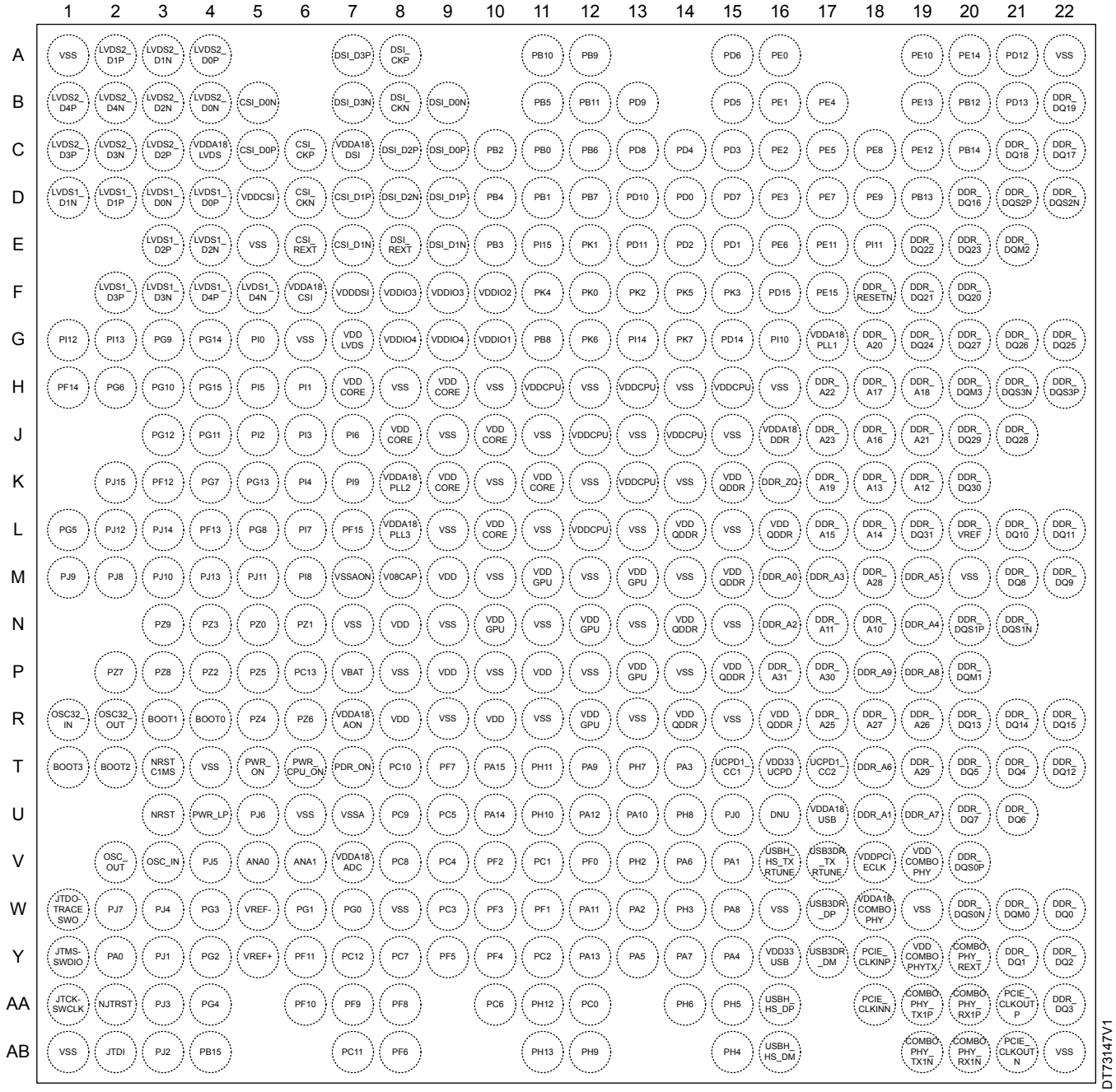
Figure 8. STM32MP25xC/F TFBGA436 pinout



1. *The above figure shows the package top view.*
2. *VDDGPU, VDDA18DSI, VDDDSI, VDDA18LVDS, and VDDLVDS are DNU on product without the related feature (respectively GPU/NPU, DSI and LVDS) and must be connected to VSS. DSI_xxx and LVDSx_xxx are DNU on product without the related feature (respectively DSI and LVDS) and must be left open. See Section 2 for details on feature availability. Alternatively, for PCB compatibility purposes, those balls could be connected in same ways as for a product with enabled feature. Refer to AN5489 for additional details.*

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Table 9. I/O power domains

Supply pin	Pin names[1]
VDD	NRSTC1MS, PA0, PA1, PA10, PA11, PA12, PA13, PA14, PA15, PA2, PA3, PA4, PA5, PA6, PA7, PA8, PA9, PB12, PB13, PB14, PB15, PC0, PC1, PC10, PC11, PC12, PC2, PC6, PC7, PC8, PC9, PD12, PD13, PD14, PD15, PF0, PF1, PF10, PF11, PF12, PF13, PF14, PF15, PF2, PF3, PF4, PF5, PF8, PF9, PG0, PG10, PG11, PG12, PG13, PG14, PG15, PG2, PG4, PG5, PG6, PG7, PG8, PG9, PH10, PH11, PH12, PH13, PH2, PH3, PH4, PH5, PH6, PH7, PH8, PH9, PI0, PI1, PI10, PI11, PI12, PI13, PI14, PI15, PI2, PI3, PI4, PI5, PI6, PI7, PI9, PJ0, PJ1, PJ10, PJ11, PJ12, PJ13, PJ14, PJ15, PJ2, PJ3, PJ4, PJ5, PJ6, PJ7, PJ8, PJ9, PK0, PK1, PK2, PK3, PK4, PK5, PK6, PK7, PWR_CPU_ON, PWR_LP, PWR_ON, PZ7, PZ8, PZ9, JTCK-SWCLK, JTDI, JTDO-TRACESWO, JTMS-SWDIO, NJTRST, NRST
VDDIO1[2]	PE0, PE1, PE2, PE3, PE4, PE5
VDDIO2[3]	PE10, PE11, PE12, PE13, PE14, PE15, PE6, PE7, PE8, PE9
VDDIO3[4]	PD0, PD1, PD10, PD11, PD2, PD3, PD4, PD5, PD6, PD7, PD8, PD9
VDDIO4[5]	PB0, PB1, PB10, PB11, PB2, PB3, PB4, PB5, PB6, PB7, PB8, PB9
VDDA18AON	OSC_IN, OSC_OUT, PDR_ON
VSW[6]	OSC32_IN, OSC32_OUT, PC13, PI8, PZ0, PZ1, PZ2, PZ3, PZ4, PZ5, PZ6
VDD/VSW[6][7]	PC3, PC4, PC5, PF6, PF7, PG1, PG3

1. *Does not includes analog peripherals which have one or more dedicated supplies (for example PHYs).*
2. *Usually used for SD-Card using SDMMC1.*
3. *Usually used for e.MMC or SD-Card using SDMMC2.*
4. *Usually used for OCTOSPIM_P1.*
5. *Usually used for OCTOSPIM_P2.*
6. *VSW is supplied by V_{BAT} in absence of V_{DD}.*
7. *Pins with two supplies: V_{SW} supply for enabled TAMP_INx additional function, V_{DD} supply for GPIO and other alternate function.*

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4.2 Ball description

Table 10. Legend/abbreviations used in the ballout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified, the function during and after reset is the same as the actual pin/ball name	
	DNU (do not use)	Represent a pin/ball that must be left unconnected (open) at application level unless otherwise noted.
Pin type	S	Supply pin
	I	Input only pin
	O	Output only pin
	I/O	Input/output pin
	A	Analog or special level pin
I/O structure	TT(U/D/PD)	3.6 V capable I/O (with fixed pull-up/pull-down/programmable pull-down)[1]
	DDR	1.35 V, 1.2 V, or 1.1 V I/O for DDR3L, DDR4 or LPDDR4 interface
	A	Analog signal
	RST	Reset pin with weak pull-up resistor
	Option for TT I/Os	
	_f[2]	I3C option
	_a[2]	Analog option (supplied by $V_{DDA18ADC}$ for the analog part of the I/O)
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

1. *3.6 V capable only if related I/O supply is 3.3 V typ. and related VDDIOxVRSEL = 0.*
2. *The related I/O structures in table below are TT_f, TT_a and TT_af.*

Note: Alternate functions listed in following tables may be absent in some devices or packages (see Section 2 for details).

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Table 11. STM32MP25xC/F ball definitions

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
R5	-	V5	ANA0	A	A	-	-	ADC1_INP0, ADC1_INN1, ADC2_INP0, ADC2_INN1, ADC3_INP0, ADC3_INN1
P5	-	V6	ANA1	A	A	-	-	ADC1_INP1, ADC2_INP1, ADC3_INP1
T2	Y3	R4	BOOT0	I	TTPD	(1)	-	-
P3	AA3	R3	BOOT1	I	TTPD	(1)	-	-
T3	AB1	T2	BOOT2	I	TTPD	(1)	-	-
R3	AB2	T1	BOOT3	I	TTPD	(1)	-	-
W13	AB18	T15	UCPD1_CC1	A	A	-	-	UCPD1_CC1
W14	AA19	T17	UCPD1_CC2	A	A	-	-	UCPD1_CC2
C2	D4	D6	CSI_CKN	A	A	-	-	-
C1	C4	C6	CSI_CKP	A	A	-	-	-
E1	A3	B5	CSI_D0N	A	A	-	-	-
E2	B3	C5	CSI_D0P	A	A	-	-	-
D2	C5	E7	CSI_D1N	A	A	-	-	-
D1	B5	D7	CSI_D1P	A	A	-	-	-
E3	F6	E6	CSI_REXT	A	A	-	-	-
F17	U21	M16	DDR_A0	O	DDR	-	-	-
G17	AD25	U18	DDR_A1	O	DDR	-	-	-
J17	V24	N16	DDR_A2	O	DDR	-	-	-
J19	P22	M17	DDR_A3	O	DDR	-	-	-
M17	U23	N19	DDR_A4	O	DDR	-	-	-
L17	T24	M19	DDR_A5	O	DDR	-	-	-
N17	Y24	T18	DDR_A6	O	DDR	-	-	-

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Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
P17	AC25	U19	DDR_A7	O	DDR	-	-	-
H18	V22	P19	DDR_A8	O	DDR	-	-	-
E18	T22	P18	DDR_A9	O	DDR	-	-	-
G18	R23	N18	DDR_A10	O	DDR	-	-	-
F18	P24	N17	DDR_A11	O	DDR	-	-	-
R17	L23	K19	DDR_A12	O	DDR	-	-	-
J18	K24	K18	DDR_A13	O	DDR	-	-	-
K18	M24	L18	DDR_A14	O	DDR	-	-	-
L18	N23	L17	DDR_A15	O	DDR	-	-	-
M18	J23	J18	DDR_A16	O	DDR	-	-	-
N18	H24	H18	DDR_A17	O	DDR	-	-	-
P18	G23	H19	DDR_A18	O	DDR	-	-	-
-	L21	K17	DDR_A19	O	DDR	-	-	-
E19	J21	G18	DDR_A20	O	DDR	-	-	-
F19	H22	J19	DDR_A21	O	DDR	-	-	-
G19	F22	H17	DDR_A22	O	DDR	-	-	-
H19	E23	J17	DDR_A23	O	DDR	-	-	-
H17	W21	R17	DDR_A25	O	DDR	-	-	-
K19	AB24	R19	DDR_A26	O	DDR	-	-	-
L19	AA23	R18	DDR_A27	O	DDR	-	-	-
M19	AC23	M18	DDR_A28	O	DDR	-	-	-
N19	Y22	T19	DDR_A29	O	DDR	-	-	-
P19	AA21	P17	DDR_A30	O	DDR	-	-	-
R19	W23	P16	DDR_A31	O	DDR	-	-	-
T17	AB25	W21	DDR_DQM0	O	DDR	-	-	-
C19	U26	P20	DDR_DQM1	O	DDR	-	-	-
-	G27	E21	DDR_DQM2	O	DDR	-	-	-

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Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
-	M25	H20	DDR_DQM3	O	DDR	-	-	-
V18	AA26	W20	DDR_DQS0N	I/O	DDR	-	-	-
B18	R25	N21	DDR_DQS1N	I/O	DDR	-	-	-
-	F26	D22	DDR_DQS2N	I/O	DDR	-	-	-
-	L27	H21	DDR_DQS3N	I/O	DDR	-	-	-
V19	AA25	V20	DDR_DQS0P	I/O	DDR	-	-	-
B19	T25	N20	DDR_DQS1P	I/O	DDR	-	-	-
-	F27	D21	DDR_DQS2P	I/O	DDR	-	-	-
-	L26	H22	DDR_DQS3P	I/O	DDR	-	-	-
V17	AB27	Y22	DDR_DQ2	I/O	DDR	-	-	-
U17	AC27	AA22	DDR_DQ3	I/O	DDR	-	-	-
W17	AC26	Y21	DDR_DQ1	I/O	DDR	-	-	-
W18	AB26	W22	DDR_DQ0	I/O	DDR	-	-	-
U18	Y25	U20	DDR_DQ7	I/O	DDR	-	-	-
U19	W26	U21	DDR_DQ6	I/O	DDR	-	-	-
T19	W25	T21	DDR_DQ4	I/O	DDR	-	-	-
T18	W27	T20	DDR_DQ5	I/O	DDR	-	-	-
D19	V26	T22	DDR_DQ12	I/O	DDR	-	-	-
C18	U25	R22	DDR_DQ15	I/O	DDR	-	-	-
D17	V25	R21	DDR_DQ14	I/O	DDR	-	-	-
D18	V27	R20	DDR_DQ13	I/O	DDR	-	-	-
A18	R26	M22	DDR_DQ9	I/O	DDR	-	-	-
C17	R27	M21	DDR_DQ8	I/O	DDR	-	-	-
A17	P26	L22	DDR_DQ11	I/O	DDR	-	-	-
B17	P27	L21	DDR_DQ10	I/O	DDR	-	-	-
-	J25	F20	DDR_DQ20	I/O	DDR	-	-	-
-	H25	F19	DDR_DQ21	I/O	DDR	-	-	-

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Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
-	G25	E20	DDR_DQ23	I/O	DDR	-	-	-
-	G26	E19	DDR_DQ22	I/O	DDR	-	-	-
-	E25	B22	DDR_DQ19	I/O	DDR	-	-	-
-	F25	D20	DDR_DQ16	I/O	DDR	-	-	-
-	F24	C21	DDR_DQ18	I/O	DDR	-	-	-
-	E26	C22	DDR_DQ17	I/O	DDR	-	-	-
-	P25	L19	DDR_DQ31	I/O	DDR	-	-	-
-	N26	K20	DDR_DQ30	I/O	DDR	-	-	-
-	L25	J21	DDR_DQ28	I/O	DDR	-	-	-
-	N25	J20	DDR_DQ29	I/O	DDR	-	-	-
-	K25	G22	DDR_DQ25	I/O	DDR	-	-	-
-	K26	G21	DDR_DQ26	I/O	DDR	-	-	-
-	K27	G20	DDR_DQ27	I/O	DDR	-	-	-
-	J26	G19	DDR_DQ24	I/O	DDR	-	-	-
K17	G21	L20	DDR_VREF	A	A	-	-	-
E17	E21	F18	DDR_RESETN	O	DDR	-	-	-
G16	K22	K16	DDR_ZQ	A	A	-	-	-
A4	C8	B8	DSI_CKN	A	A	-	-	-
B4	C7	A8	DSI_CKP	A	A	-	-	-
A5	C9	B9	DSI_D0N	A	A	-	-	-
B5	B9	C9	DSI_D0P	A	A	-	-	-
A6	A10	E9	DSI_D1N	A	A	-	-	-
B6	B10	D9	DSI_D1P	A	A	-	-	-
B3	A7	D8	DSI_D2N	A	A	-	-	-
A3	B7	C8	DSI_D2P	A	A	-	-	-
B2	B6	B7	DSI_D3N	A	A	-	-	-
A2	A6	A7	DSI_D3P	A	A	-	-	-

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Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
C4	D6	E8	DSI_REXT	A	A	-	-	-
W4	AA5	AA1	JTCK-SWCLK	I	TTD	(1)	-	-
W3	AE3	AB2	JTDI	I	TTU	(1)	-	-
V1	AC2	W1	JTDO-TRACESWO	O	TTU	(1)	-	-
W2	AE2	Y1	JTMS-SWDIO	I/O	TTU	(1)	-	-
F1	G3	D3	LVDS1_D0N	A	A	(2)	-	-
F2	G2	D4	LVDS1_D0P	A	A	(2)	-	-
F3	H4	D1	LVDS1_D1N	A	A	(2)	-	-
F4	H3	D2	LVDS1_D1P	A	A	(2)	-	-
G3	J2	E4	LVDS1_D2N	A	A	(2)	-	-
G4	J1	E3	LVDS1_D2P	A	A	(2)	-	-
J2	L3	F3	LVDS1_D3N	A	A	(2)	-	-
J3	L2	F2	LVDS1_D3P	A	A	(2)	-	-
H3	K2	F5	LVDS1_D4N	A	A	(2)	-	-
H4	K1	F4	LVDS1_D4P	A	A	(2)	-	-
-	B2	B4	LVDS2_D0N	A	A	(2)	-	-
-	B1	A4	LVDS2_D0P	A	A	(2)	-	-
-	C3	A3	LVDS2_D1N	A	A	(2)	-	-
-	C2	A2	LVDS2_D1P	A	A	(2)	-	-
-	D3	B3	LVDS2_D2N	A	A	(2)	-	-
-	E3	C3	LVDS2_D2P	A	A	(2)	-	-
-	E2	C2	LVDS2_D3N	A	A	(2)	-	-
-	E1	C1	LVDS2_D3P	A	A	(2)	-	-
-	F2	B2	LVDS2_D4N	A	A	(2)	-	-
-	F1	B1	LVDS2_D4P	A	A	(2)	-	-
V2	AF3	AA2	NJTRST	I	TTU	(1)	-	-

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Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
N2	AE1	U3	NRST	I/O	RST	(1)	-	-
T1	W3	T3	NRSTC1MS	O	TT	(3)	-	-
P15	AF5	Y2	PA0	I/O	TT_a	(1)	LPTIM1_CH2, SPI5_RDY, UART8_CTS, SAI2_MCLK_B, UART5_TX(boot), USART3_TX, TIM3_ETR, TIM5_CH2, ETH2_MII_RXD2, FMC_NL, DCMI_D9/PSSI_D9/DCMIPP_D9, EVENTOUT	WKUP1
N15	AC19	V15	PA1	I/O	TT_af	(1)	SPI6_MISO, SAI3_SD_A, USART1_RTS/USART1_DE, USART6_CK, TIM4_CH2, I2C4_SDA, I2C6_SDA, LCD_R3, DCMI_D5/PSSI_D5/DCMIPP_D5, ETH3_PHY_INTN, EVENTOUT	-
N12	AF17	W13	PA2	I/O	TT_af	(1)	LPTIM2_IN1, SPI7_MISO, MDF1_SDI7, USART1_RX, I3C1_SDA, I2C1_SDA, LCD_B0, DCMI_D3/PSSI_D3/ DCMIPP_D3, ETH3_RGMII_RX_CTL/ETH3_RMII_CRS_DV, EVENTOUT	-
R12	AD18	T14	PA3	I/O	TT_af	(1)	LPTIM2_ETR, SPI7_MOSI, MDF1_CKI7, USART1_TX, I3C1_SCL, I2C7_SMBA, I2C1_SCL, LCD_B1, DCMI_D2/ PSSI_D2/DCMIPP_D2, ETH3_RGMII_TX_CTL/ ETH3_RMII_TX_EN, EVENTOUT	-
P12	AG17	Y15	PA4	I/O	TT_a	(1)	USART2_TX(boot), FDCAN2_TX, TIM2_CH1, LCD_R1, ETH1_PTP_AUX_TS, ETH3_PPS_OUT, EVENTOUT	-
J12	AE17	Y13	PA5	I/O	TT	(1)	SPI4_MOSI, SAI2_MCLK_B, SAI2_SD_B, USART2_RTS/ USART2_DE, FDCAN2_RX, TIM2_CH4, LCD_G0, FMC_A0, DCMI_D13/PSSI_D13/DCMIPP_D13, ETH3_RGMII_RX_CLK/ ETH3_RMII_REF_CLK, EVENTOUT	-
M14	AF18	V14	PA6	I/O	TT	(1)	SPI4_SCK, SAI2_FS_B, MDF1_SDI6, USART2_CK, TIM13_CH1, TIM2_ETR, LCD_G4, FMC_NE1, DCMI_D12/ PSSI_D12/DCMIPP_D12, ETH3_RGMII_TXD0/ ETH3_RMII_TXD0, EVENTOUT	-
K15	AE18	Y14	PA7	I/O	TT	(1)	AUDIOCLK, SPI6_RDY, PCIE_CLKREQN, MDF1_CCK0, USART1_CTS/USART1_NSS, TIM4_ETR, I2C2_SMBA, I2C6_SMBA, LCD_B5, I2C3_SMBA, I2C4_SMBA, DCMI_D6/ PSSI_D6/DCMIPP_D6, ETH3_RGMII_TXD1/ ETH3_RMII_TXD1, EVENTOUT	-
K9	AA17	W15	PA8	I/O	TT_f	(1)	LPTIM2_CH2, SPI7_NSS, SAI1_FS_B, USART1_CK, USART2_RX(boot), I2C5_SCL, LCD_B2, DCMI_D4/PSSI_D4/ DCMIPP_D4, EVENTOUT	-

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Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
K12	AF15	T12	PA9	I/O	TT	(1)	SPI4_NSS, SAI2_SCK_B, USART2_CTS/USART2_NSS, LPTIM5_ETR, TIM2_CH3, ETH1_MDC, LCD_G7, PSSI_D14/ DCMIPP_D14, ETH3_RGMII_RXD0/ETH3_RMII_RXD0, EVENTOUT	-
M15	AE15	U13	PA10	I/O	TT	(1)	SPI4_MISO, SAI2_SD_B, USART2_RX, LPTIM5_IN1, TIM2_CH2, ETH1_MDIO, LCD_R6, PSSI_D15/DCMIPP_D15, ETH3_RGMII_RXD1/ETH3_RMII_RXD1, EVENTOUT	-
R9	AD12	W12	PA11	I/O	TT	(1)	SPI8_SCK, LPTIM2_CH1, SAI4_SD_B, MDF1_SDI4, ETH1_MII_RX_DV/ETH1_RGMII_RX_CTL/ ETH1_RMII_CRS_DV, EVENTOUT	-
R8	AC13	U12	PA12	I/O	TT_f	(1)	SPI6_MOSI, SAI3_FS_A, TIM4_CH1, I2C4_SCL, I2C6_SCL, ETH1_PHY_INTN, EVENTOUT	-
W9	AD14	Y12	PA13	I/O	TT	(1)	SPI8_RDY, I2S3_MCK, LPTIM2_ETR, MDF1_CKI3, USART2_CTS/USART2_NSS, I2C7_SMBA, ETH1_MII_TX_EN/ ETH1_RGMII_TX_CTL/ETH1_RMII_TX_EN, EVENTOUT	-
T8	AB12	U10	PA14	I/O	TT	(1)	SPI8_NSS, LPTIM2_CH2, SAI4_FS_B, MDF1_CCK1, ETH1_MII_RX_CLK/ETH1_RGMII_RX_CLK/ ETH1_RMII_REF_CLK, EVENTOUT	-
T10	AE13	T10	PA15	I/O	TT_f	(1)	SPI3_MISO/I2S3_SDI, USART2_RX, I2C7_SDA, ETH1_MII_TXD0/ETH1_RGMII_TXD0/ETH1_RMII_TXD0, EVENTOUT	-
B8	B13	C11	PB0	I/O	TT	(4)	SPI2_SCK/I2S2_CK, USART1_CK, TIM16_CH1, TIM20_CH4N, OCTOSPIM_P2_IO0(boot), EVENTOUT	-
D9	C12	D11	PB1	I/O	TT	(4)	SPI3_NSS/I2S3_WS, TIM16_CH1N, TIM20_CH3N, OCTOSPIM_P2_IO1(boot), FMC_NCE4, EVENTOUT	-
E9	A14	C10	PB2	I/O	TT	(4)	SPI2_MOSI/I2S2_SDO, MDF1_CKI3, TIM17_BKIN, TIM16_BKIN, TIM20_CH2N, OCTOSPIM_P2_IO2(boot), EVENTOUT	-
A9	B14	E10	PB3	I/O	TT	(4)	SPI2_NSS/I2S2_WS, MDF1_SDI3, TIM20_CH3, OCTOSPIM_P2_IO3(boot), FMC_NCE3, EVENTOUT	-
C9	B15	D10	PB4	I/O	TT_f	(4)	SPI2_RDY, UART4_CTS, SAI4_FS_B, MDF1_SDI4, TIM14_CH1, TIM20_CH2, I2C2_SDA, OCTOSPIM_P2_IO4(boot), I3C2_SDA, EVENTOUT	-
B9	C14	B11	PB5	I/O	TT_f	(4)	I2S2_MCK, UART4_RTS/UART4_DE, SAI4_SD_B, MDF1_CKI4, TIM20_CH1, I2C2_SCL, OCTOSPIM_P2_IO5(boot), FMC_AD8/FMC_D8(boot), I3C2_SCL, SDMMC3_D123DIR, EVENTOUT	-

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Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
C8	C13	C12	PB6	I/O	TT	(4)	SPI2_MISO/I2S2_SDI, UART4_RX, SAI4_SCK_B, TIM20_CH1N, OCTOSPIM_P2_IO6(boot), FMC_AD9/ FMC_D9(boot), SDMMC3_D0DIR, EVENTOUT	-
D7	C11	D12	PB7	I/O	TT	(4)	SPI3_SCK/I2S3_CK, UART4_TX, SAI4_MCLK_B, TIM20_ETR, TIM12_CH1, OCTOSPIM_P2_IO7(boot), FMC_AD10/ FMC_D10(boot), SDMMC3_CDIR, EVENTOUT	-
A7	D8	G11	PB8	I/O	TT	(4)	SPI3_MOSI/I2S3_SDO, PCIE_CLKREQN, USART1_TX, TIM17_CH1, TIM20_CH4, OCTOSPIM_P2_NCS1(boot), FMC_AD12/FMC_D12(boot), EVENTOUT	-
A8	F10	A12	PB9	I/O	TT	(4)	SPI3_RDY, USART1_RTS/USART1_DE, FDCAN1_TX, TIM20_BKIN, TIM10_CH1, OCTOSPIM_P2_DQS(boot), OCTOSPIM_P2_NCS2, FMC_AD13/FMC_D13(boot), EVENTOUT	-
E12	B11	A11	PB10	I/O	TT	(4)	SPI3_MISO/I2S3_SDI, USART1_RX, TIM17_CH1N, OCTOSPIM_P2_CLK(boot), FMC_AD15/FMC_D15(boot), EVENTOUT	-
B7	A11	B12	PB11	I/O	TT	(4)	I2S3_MCK, USART1_CTS/USART1_NSS, FDCAN1_RX, TIM20_BKIN2, TIM12_CH2, OCTOSPIM_P2_NCLK(boot), OCTOSPIM_P2_NCS2, FMC_AD14/FMC_D14(boot), OCTOSPIM_P1_NCS2, EVENTOUT	-
E14	C26	B20	PB12	I/O	TT_a	(1)	UART8_CTS, TIM13_CH1, DSI_TE, SDMMC3_D2, FMC_NWAIT, DCMI_D12/PSSI_D12/DCMIPP_D12, EVENTOUT	-
G15	A26	D19	PB13	I/O	TT_a	(1)	SPI7_SCK, SAI1_SD_B, UART8_RX, SDMMC3_CK, FMC_AD5/FMC_D5(boot), FMC_AD0/FMC_D0, EVENTOUT	-
H15	C27	C20	PB14	I/O	TT	(1)	SPI2_SCK/I2S2_CK, MDF1_CKI7, UART9_RX(boot), TIM4_CH2, SDMMC3_D0, FMC_AD7/FMC_D7(boot), FMC_AD2/FMC_D2, EVENTOUT	-
J15	AE6	AB4	PB15	I/O	TT_a	(1)	LPTIM1_IN2, SPI5_SCK, UART8_RTS/UART8_DE, SAI2_SD_B, UART5_RX(boot), TIM3_CH2, TIM5_CH1, ETH1_PPS_OUT, FMC_A18, LCD_R4, DCMI_D8/PSSI_D8/ DCMIPP_D8, EVENTOUT	ADC1_INP15, ADC3_INP5
V13	AE26	AA18	PCIE_CLKINN	A	-	-	-	-
U13	AE25	Y18	PCIE_CLKINP	A	-	-	-	-
V14	AG26	AB21	PCIE_CLKOUTN	A	-	-	-	-
U14	AF26	AA21	PCIE_CLKOUTP	A	-	-	-	-

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Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
V9	AB14	AA12	PC0	I/O	TT	(1)	LPTIM1_CH1, SPI6_SCK, SAI3_MCLK_B, USART6_TX, DCMI_D0/PSSI_D0/DCMIPP_D0, ETH2_MII_RX_CLK/ ETH2_RMII_REF_CLK, ETH1_MII_TX_CLK, ETH1_RGMII_GTX_CLK, LCD_G7, EVENTOUT	-
V10	AG14	V11	PC1	I/O	TT_f	(1)	SPI3_MOSI/I2S3_SDO, USART2_TX, I2C7_SCL, ETH1_MII_TXD1/ETH1_RGMII_TXD1/ETH1_RMII_TXD1, EVENTOUT	-
T9	AE12	Y11	PC2	I/O	TT	(1)	SPI8_MOSI, LPTIM2_IN1, SAI4_MCLK_B, MDF1_SDI3, USART2_RTS/USART2_DE, ETH1_MII_RXD1/ ETH1_RGMII_RXD1/ETH1_RMII_RXD1, EVENTOUT	-
U4	AA9	W9	PC3	I/O	TT_a	(5)	LPTIM1_IN2, SPI3_NSS/I2S3_WS, SPI6_RDY, USART6_RTS/ USART6_DE, FDCAN2_TX, ETH2_MII_RX_DV/ ETH2_RGMII_RX_CTL/ETH2_RMII_CRS_DV, ETH1_MII_RX_ER, LCD_G6, DCMI_D3/PSSI_D3/DCMIPP_D3, EVENTOUT	ADC1_INP12, ADC1_INN10, ADC2_INP12, ADC2_INN10, ADC3_INP12, ADC3_INN10, TAMP_IN3
V3	AC9	V9	PC4	I/O	TT	(5)	SPI6_MISO, SAI3_FS_B, ETH2_MII_TX_EN/ ETH2_RGMII_TX_CTL/ETH2_RMII_TX_EN, ETH1_RGMII_CLK125, LCD_R0, EVENTOUT	TAMP_IN1
T7	AD10	U9	PC5	I/O	TT_af	(5)	SPDIFRX1_IN1, MDF1_SDI1, TIM8_CH1N, I2C4_SDA, ETH2_MDIO, ETH1_MII_COL, FMC_A25, ETH1_PPS_OUT, LCD_DE, EVENTOUT	ADC1_INP10, ADC2_INP10, ADC3_INP10, TAMP_IN6
R7	AB10	AA10	PC6	I/O	TT_af	(1)	RTC_REFIN, SPDIFRX1_IN0, MDF1_CKI1, TIM8_CH1, I2C4_SCL, ETH2_MDC, ETH1_MII_CRS, FMC_A24, ETH1_PHY_INTN, LCD_CLK, EVENTOUT	ADC1_INP9, ADC1_INN5, ADC2_INP9, ADC2_INN5
W5	AF9	Y8	PC7	I/O	TT_a	(1)	SPI6_MOSI, SAI3_SD_B, TIM8_CH2N, ETH2_MII_TXD0/ ETH2_RGMII_TXD0/ETH2_RMII_TXD0, ETH1_MII_TXD2, LCD_B4, DCMI_D1/PSSI_D1/DCMIPP_D1, EVENTOUT	ADC3_INP9, ADC3_INN5
U6	AG9	V8	PC8	I/O	TT_a	(1)	LPTIM1_ETR, SPI6_NSS, SAI3_SCK_B, USART6_CTS/ USART6_NSS, TIM8_CH2, ETH2_MII_TXD1/ ETH2_RGMII_TXD1/ETH2_RMII_TXD1, ETH1_MII_TXD3, LCD_B3, DCMI_D2/PSSI_D2/DCMIPP_D2, EVENTOUT	-
V6	AE9	U8	PC9	I/O	TT_a	(1)	MCO1, SPI3_MISO/I2S3_SDI, SAI2_SCK_A, TIM13_CH1, TIM8_CH4N, USBH_HS_OVRCUR, ETH2_MII_TXD2/ ETH2_RGMII_TXD2, USB3DR_OVRCUR, FMC_A22, LCD_G2, DCMI_D7/PSSI_D7/DCMIPP_D7, EVENTOUT	ADC1_INP8, ADC1_INN4, ADC2_INP8, ADC2_INN4

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Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
W6	AG10	T8	PC10	I/O	TT_a	(1)	SPI3_MOSI/I2S3_SDO, LPTIM4_ETR, TIM8_CH4, USBH_HS_VBUSEN, ETH2_MII_TXD3/ETH2_RGMII_TXD3, USB3DR_VBUSEN, FMC_A23, LCD_G3, DCMI_D6/PSSI_D6/ DCMIPP_D6, EVENTOUT	ADC1_INP5, ADC2_INP5
V5	AD8	AB7	PC11	I/O	TT_a	(1)	LPTIM1_CH1, SPI5_NSS, SAI2_MCLK_A, UART5_RTS/ UART5_DE, USART3_RTS/USART3_DE, TIM3_CH1, TIM5_ETR, ETH2_MII_RXD3/ETH2_RGMII_RXD3, FMC_NBL1, LCD_R2, DCMI_D10/PSSI_D10/DCMIPP_D10, EVENTOUT	ADC1_INP7, ADC1_INN3, ADC2_INP7, ADC2_INN3, ADC3_INP7, ADC3_INN3
V4	AE7	Y7	PC12	I/O	TT_af	(1)	LPTIM1_CH2, I3C3_SCL, MDF1_CKI2, TIM8_CH3, I2C3_SCL, ETH2_MII_RXD1/ETH2_RGMII_RXD1/ETH2_RMII_RXD1, ETH1_MII_RXD3, LCD_G1, DCMI_D5/PSSI_D5/DCMIPP_D5, EVENTOUT	ADC1_INP17
P4	W7	P6	PC13	I/O	TT	(6)	EVENTOUT	RTC_OUT1/ RTC_LSCO/RTC_TS, TAMP_OUT1
M2	AA2	R1	OSC32_IN	I	A	(7)	-	OSC32_IN
M1	AA1	R2	OSC32_OUT	O	A	(8)	-	OSC32_OUT
N1	W2	T7	PDR_ON	I	-	(9)	-	-
C11	B17	D14	PD0	I/O	TT	(10)	TRACECLK, HDP0, SPI7_RDY, SAI1_D2, SAI4_FS_A, UART7_RX, TIM15_CH2, SDVSEL1, OCTOSPIM_P1_CLK(boot), DCMI_PIXCLK/PSSI_PDCK/ DCMIPP_PIXCLK, EVENTOUT	-
F9	A19	E15	PD1	I/O	TT	(10)	HDP1, SPI1_MISO/I2S1_SDI, SAI1_CK2, SAI4_SD_A, UART7_RTS/UART7_DE, TIM15_CH1, TIM1_BKIN, FDCAN3_RX, OCTOSPIM_P1_NCLK(boot), OCTOSPIM_P1_NCS2, OCTOSPIM_P2_NCS2, DCMI_HSYNC/PSSI_DE/DCMIPP_HSYNC, EVENTOUT	-
A10	D12	E14	PD2	I/O	TT	(10)	HDP2, SPI1_NSS/I2S1_WS, SAI1_CK1, SAI4_SCK_A, UART7_CTS, TIM15_BKIN, TIM1_ETR, FDCAN3_TX, OCTOSPIM_P1_DQS(boot), OCTOSPIM_P1_NCS2, DCMI_VSYNC/PSSI_RDY/DCMIPP_VSYNC, EVENTOUT	-
D8	G13	C15	PD3	I/O	TT	(10)	SAI1_MCLK_A, SPI2_SCK/I2S2_CK, SAI1_D1, SAI4_MCLK_A, UART7_TX, TIM15_CH1N, TIM1_BKIN2, SDVSEL2, OCTOSPIM_P1_NCS1(boot), PSSI_D15/DCMIPP_D15, EVENTOUT	-

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Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
C12	C18	C14	PD4	I/O	TT	(10)	TRACED0, SPI4_MISO, HDP3, SAI1_D3, SAI1_SD_B, TIM1_CH4N, TIM4_CH1, OCTOSPIM_P1_IO0(boot), PSSI_D14/DCMIPP_D14, EVENTOUT	-
B12	B18	B15	PD5	I/O	TT	(10)	TRACED1, SPI4_NSS, HDP4, SAI1_D4, SAI1_FS_B, TIM1_CH3N, TIM4_CH2, OCTOSPIM_P1_IO1(boot), DCMI_D13/PSSI_D13/DCMIPP_D13, EVENTOUT	-
A12	A18	A15	PD6	I/O	TT	(10)	TRACED2, SPI4_MOSI, HDP5, SAI1_SCK_B, MDF1_SDI2, TIM1_CH2N, TIM4_CH3, OCTOSPIM_P1_IO2(boot), DCMI_D12/PSSI_D12/DCMIPP_D12, EVENTOUT	-
D12	D20	D15	PD7	I/O	TT	(10)	TRACED3, SPI4_SCK, SPI1_RDY, SAI1_MCLK_B, MDF1_CKI2, TIM1_CH1N, TIM4_CH4, OCTOSPIM_P1_IO3(boot), DCMI_D11/PSSI_D11/ DCMIPP_D11, EVENTOUT	-
E11	C16	C13	PD8	I/O	TT	(10)	TRACED4, SPI4_RDY, I2S1_MCK, SAI1_FS_A, UART4_CTS, MDF1_SDI1, TIM1_CH4, TIM4_ETR, OCTOSPIM_P1_IO4(boot), SDMMC1_D7, SDMMC1_D123DIR, DCMI_D10/PSSI_D10/DCMIPP_D10, EVENTOUT	-
C10	C15	B13	PD9	I/O	TT	(10)	TRACED5, HDP6, SPI1_MOSI/I2S1_SDO, SAI1_SD_A, UART4_RTS/UART4_DE, MDF1_CKI1, TIM1_CH3, OCTOSPIM_P1_IO5(boot), SDMMC1_D6, SDMMC1_D0DIR, DCMI_D9/PSSI_D9/DCMIPP_D9, EVENTOUT	-
D11	C17	D13	PD10	I/O	TT_f	(10)	TRACED6, HDP7, SAI1_SCK_A, UART4_RX, MDF1_SDI0, I2C4_SDA, TIM1_CH2, TIM14_CH1, OCTOSPIM_P1_IO6(boot), SDMMC1_D5, SDMMC1_CDIR, DCMI_D8/PSSI_D8/DCMIPP_D8, EVENTOUT	-
B10	A15	E13	PD11	I/O	TT_f	(10)	TRACED7, SPI1_SCK/I2S1_CK, SAI1_MCLK_A, UART4_TX, MDF1_CKI0, I2C4_SCL, TIM1_CH1, SDVSEL1, OCTOSPIM_P1_IO7(boot), SDMMC1_D4, SDMMC1_CKIN, DCMI_D7/PSSI_D7/DCMIPP_D7, EVENTOUT	-
H14	B26	A21	PD12	I/O	TT_a	(1)	SPI7_MISO, SPI2_MISO/I2S2_SDI, SPDIFRX1_IN2, UART8_RTS/UART8_DE, TIM4_ETR, SDMMC3_CMD, FMC_AD6/FMC_D6(boot), FMC_AD1/FMC_D1, EVENTOUT	-
G9	D25	B21	PD13	I/O	TT_a	(1)	SPI2_NSS/I2S2_WS, MDF1_SDI7, UART9_TX(boot), TIM4_CH4, SDMMC3_D1, FMC_AD11/FMC_D11(boot), FMC_NWE, EVENTOUT	-
A13	E19	G15	PD14	I/O	TT_af	(1)	I2S1_MCK, FDCAN1_RX, TIM11_CH1, I2C7_SDA, FMC_AD4/ FMC_D4(boot), SDMMC3_D3, DCMI_D1/PSSI_D1/ DCMIPP_D1, EVENTOUT	-

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Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
A11	E15	F16	PD15	I/O	TT_af	(1)	SPI1_RDY, DSI_TE, I2C5_SDA, FDCAN1_TX, TIM1_BKIN2, TIM5_ETR, I2C7_SCL, FMC_AD3/FMC_D3(boot), SDMMC3_CKIN, DCMI_D0/PSSI_D0/DCMIPP_D0, EVENTOUT	-
B13	B19	A16	PE0	I/O	TT	(11)	TRACED2, LPTIM2_CH1, SPI1_SCK/I2S1_CK, SPI3_RDY, USART3_CK, SDMMC1_D2, EVENTOUT	-
C13	C19	B16	PE1	I/O	TT	(11)	TRACED3, LPTIM2_CH2, I2S1_MCK, I2S3_MCK, USART3_RX, SDMMC1_D3, EVENTOUT	-
A14	C20	C16	PE2	I/O	TT	(11)	LPTIM2_ETR, SPI1_MISO/I2S1_SDI, SPI3_MOSI/I2S3_SDO, SAI1_SCK_B, TIM10_CH1, SDMMC1_CMD(boot), EVENTOUT	-
A15	C21	D16	PE3	I/O	TT	(11)	TRACECLK, SPI1_RDY, SPI3_SCK/I2S3_CK, SAI1_MCLK_B, USART3_TX, TIM11_CH1, SDMMC1_CK(boot), EVENTOUT	-
B14	B21	B17	PE4	I/O	TT	(11)	TRACED0, LPTIM2_IN1, SPI1_MOSI/I2S1_SDO, SPI3_MISO/ I2S3_SDI, SAI1_SD_B, USART3_CTS/USART3_NSS, FDCAN1_TX, SDMMC1_D0(boot), EVENTOUT	-
C14	C22	C17	PE5	I/O	TT	(11)	TRACED1, LPTIM2_IN2, SPI1_NSS/I2S1_WS, SPI3_NSS/ I2S3_WS, SAI1_FS_B, USART3_RTS/USART3_DE, FDCAN1_RX, SDMMC1_D1, EVENTOUT	-
F14	A22	E16	PE6	I/O	TT	(12)	SPI4_RDY, SPDIFRX1_IN2, USART1_TX, TIM1_ETR, FMC_AD1/FMC_D1(boot), SDMMC2_D6, SDMMC2_D0DIR, EVENTOUT	-
C15	B22	D17	PE7	I/O	TT	(12)	SAI4_D4, SPDIFRX1_IN3, USART1_RX, TIM1_CH4N, TIM14_CH1, FMC_AD2/FMC_D2(boot), SDMMC2_D7, SDMMC2_D123DIR, EVENTOUT	-
B15	C23	C18	PE8	I/O	TT	(12)	SPI4_MOSI, SAI4_CK1, SAI4_MCLK_A, MDF1_CKI0, TIM1_CH1, FMC_A17/FMC_ALE(boot), SDMMC2_D2, EVENTOUT	-
F15	A23	D18	PE9	I/O	TT	(12)	SPI4_MISO, SAI4_D2, SAI4_FS_A, USART1_CK, TIM1_CH4, FMC_AD0/FMC_D0(boot), SDMMC2_D5, SDMMC2_CDIR, EVENTOUT	-
D15	D22	A19	PE10	I/O	TT	(12)	SPI4_SCK, SAI4_D1, SAI4_SD_A, USART1_CTS/ USART1_NSS, TIM1_CH3, FMC_NE3, FMC_NCE2, SDMMC2_D4, SDMMC2_CKIN, EVENTOUT	-
B16	B23	E17	PE11	I/O	TT	(12)	SPI7_SCK, SAI4_D3, SAI1_FS_A, TIM15_CH2, TIM1_CH3N, FMC_A16/FMC_CLE(boot), SDMMC2_D1, EVENTOUT	-

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Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
C16	C25	C19	PE12	I/O	TT	(12)	SPI4_NSS, SAI4_CK2, SAI4_SCK_A, MDF1_SDI0, USART1_RTS/USART1_DE, TIM1_CH2, FMC_NE2, FMC_NCE1(boot), SDMMC2_D3, EVENTOUT	-
A16	C24	B19	PE13	I/O	TT	(12)	SPI7_MISO, SAI1_SD_A, TIM15_CH1, TIM1_CH2N, FMC_RNB(boot), SDMMC2_D0(boot), EVENTOUT	-
G14	B25	A20	PE14	I/O	TT	(12)	SPI7_NSS, SAI1_MCLK_A, MDF1_CKI6, TIM15_BKIN, TIM1_BKIN, FMC_NWE(boot), SDMMC2_CK(boot), EVENTOUT	-
D14	D24	F17	PE15	I/O	TT	(12)	SPI7_MOSI, SAI1_SCK_A, MDF1_SDI6, TIM15_CH1N, TIM1_CH1N, FMC_NOE(boot), SDMMC2_CMD(boot), EVENTOUT	-
N9	AA15	V12	PF0	I/O	TT_af	(1)	SPI3_SCK/I2S3_CK, FDCAN2_RX, TIM12_CH2, I2C2_SDA, ETH1_MDC, ETH2_MII_CRS, I3C2_SDA, EVENTOUT	ADC1_INP11, ADC2_INP11, ADC3_INP11
U8	AE11	W11	PF1	I/O	TT	(1)	SPI8_MISO, LPTIM2_IN2, SAI4_SCK_B, MDF1_CKI4, USART2_CK, ETH1_MII_RXD0/ETH1_RGMII_RXD0/ ETH1_RMII_RXD0, EVENTOUT	-
P9	AC15	V10	PF2	I/O	TT_af	(1)	SPI3_RDY, I2C4_SMBA, TIM12_CH1, I2C2_SCL, ETH1_MDIO, ETH2_MII_COL, FMC_NE4, I3C2_SCL, EVENTOUT	ADC1_INP13, ADC1_INN11, ADC2_INP13, ADC2_INN11, ADC3_INP13, ADC3_INN11
W10	AF11	W10	PF3	I/O	TT_a	(1)	UART8_RX(boot), SAI2_SCK_B, MDF1_CCK0, TIM3_CH4, TIM8_BKIN2, ETH1_CLK, ETH2_PPS_OUT, FMC_A20, LCD_R6, DCMI_HSYNC/PSSI_DE/DCMIPP_HSYNC, EVENTOUT	ADC1_INP16, ADC1_INN15
W7	AF10	Y10	PF4	I/O	TT	(1)	RTC_OUT2, SPI6_NSS, SAI3_SCK_A, USART6_RX(boot), TIM4_CH4, ETH1_MDC, ETH2_CLK, ETH2_PPS_OUT, ETH1_PPS_OUT, LCD_B7, EVENTOUT	-
P7	AA11	Y9	PF5	I/O	TT	(1)	SPI6_SCK, SAI3_MCLK_A, USART6_TX(boot), TIM4_CH3, ETH1_MDIO, ETH1_CLK, ETH2_PHY_INTN, ETH1_PHY_INTN, LCD_B6, EVENTOUT	-
U5	AC7	AB8	PF6	I/O	TT	(5)	RTC_OUT2, SAI3_MCLK_B, USART6_CK, TIM12_CH1, I2C3_SMBA, ETH2_MII_RX_CLK/ETH2_RGMII_RX_CLK/ ETH2_RMII_REF_CLK, LCD_B0, EVENTOUT	TAMP_IN5

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Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
V7	AB8	T9	PF7	I/O	TT	(5)	SPDIFRX1_IN1, SPI6_SCK, SAI3_SD_A, TIM2_ETR, ETH2_RGMII_GTX_CLK, ETH2_MII_TX_CLK, LCD_R1, EVENTOUT	TAMP_IN2
U7	AE10	AA8	PF8	I/O	TT	(1)	RTC_REFIN, SAI3_SCK_B, USART3_RX, TIM12_CH2, ETH1_CLK, ETH2_RGMII_CLK125, ETH2_MII_RX_ER, ETH2_MII_RX_DV/ETH2_RMII_CRS_DV, LCD_G0, EVENTOUT	-
T6	AE8	AA7	PF9	I/O	TT	(1)	SAI3_SD_B, SAI2_SD_A, MDF1_SDI5, UART8_RTS/ UART8_DE, TIM2_CH2, ETH2_MII_RXD2/ ETH2_RGMII_RXD2, ETH2_MDIO, EVENTOUT	-
L9	AE5	AA6	PF10	I/O	TT_a	(1)	MCO2, SPI3_RDY, SAI2_MCLK_A, MDF1_CKI6, UART8_TX, TIM2_CH3, ETH2_MII_TXD2, EVENTOUT	ADC3_INP2
T4	AE4	Y6	PF11	I/O	TT_a	(1)	MCO1, SPDIFRX1_IN0, SPI6_RDY, SAI2_SCK_A, MDF1_SDI6, UART8_RX, TIM2_CH4, ETH2_MII_TXD3, EVENTOUT	ADC3_INP6, ADC3_INN2
L7	P4	K3	PF12	I/O	TT	(1)	TRACECLK, SPI5_MISO, SPI1_MISO/I2S1_SDI, UART9_RTS/ UART9_DE, TIM5_CH1, LCD_CLK, DCMI_D0/PSSI_D0/ DCMIPP_D0, EVENTOUT	-
H2	P2	L4	PF13	I/O	TT	(1)	TRACED0, HDP0, AUDIOCLK, USART6_TX, SPI2_NSS/ I2S2_WS, MDF1_CKI7, USART3_CTS/USART3_NSS, FDCAN3_TX, TIM3_CH3, LCD_R2, EVENTOUT	-
G7	P3	H1	PF14	I/O	TT	(1)	TRACED1, HDP1, USART6_RX, MDF1_SDI7, USART3_RTS/ USART3_DE, FDCAN3_RX, TIM3_CH4, LCD_R3, EVENTOUT	-
G5	R2	L7	PF15	I/O	TT	(1)	TRACED2, HDP2, SPI2_RDY, USART6_CTS/USART6_NSS, SPI2_SCK/I2S2_CK, USART3_CK, TIM2_CH2, TIM3_ETR, I2C6_SMBA, LCD_R4, EVENTOUT	-
T5	AF7	W7	PG0	I/O	TT_af	(1)	LPTIM1_IN1, I3C3_SDA, MDF1_SDI2, TIM8_CH3N, I2C3_SDA, ETH2_MII_RXD0/ETH2_RGMII_RXD0/ ETH2_RMII_RXD0, ETH1_MII_RXD2, LCD_G5, DCMI_D4/ PSSI_D4/DCMIPP_D4, EVENTOUT	ADC1_INP18, ADC1_INN17
R4	AD4	W6	PG1	I/O	TT_af	(5)	LPTIM1_IN1, I2S3_MCK, I3C3_SCL, SAI2_SD_A, UART5_CTS, USART3_CTS/USART3_NSS, TIM5_CH4, I2C3_SCL, ETH2_MII_RX_ER, ETH2_MII_RXD3, FMC_NBL0, LCD_VSYNC, DCMI_D11/PSSI_D11/DCMIPP_D11, EVENTOUT	WKUP3, ADC1_INP6, ADC1_INN2, ADC2_INP6, ADC2_INN2, TAMP_IN4

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Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
M7	AG5	Y4	PG2	I/O	TT_af	(1)	RTC_REFIN, I2S3_MCK, I3C3_SDA, SAI2_FS_A, USART3_CK, TIM5_CH3, I2C3_SDA, ETH2_MII_TX_CLK, ETH2_RGMII_CLK125, FMC_CLK, LCD_HSYNC, EVENTOUT	WKUP5, ADC1_INP2, ADC2_INP2
H12	AA7	W4	PG3	I/O	TT_a	(5)	LPTIM1_ETR, SPI5_MOSI, UART8_TX(boot), SAI2_FS_B, TIM3_CH3, TIM8_ETR, ETH2_CLK, ETH2_PHY_INTN, FMC_A19, LCD_R5, DCMI_PIXCLK/PSSI_PDCK/ DCMIPP_PIXCLK, EVENTOUT	WKUP6, ADC1_INP3, ADC2_INP3, ADC3_INP3, TAMP_IN7
N7	AD6	AA4	PG4	I/O	TT_a	(1)	SPI5_MISO, SAI3_FS_B, LPTIM4_IN1, TIM8_BKIN, ETH2_PPS_OUT, ETH2_MDC, FMC_A21, LCD_R7, DCMI_VSYNC/PSSI_RDY/DCMIPP_VSYNC, EVENTOUT	PVD_IN, ADC1_INP4, ADC2_INP4
K1	R3	L1	PG5	I/O	TT_f	(1)	TRACED3, HDP3, USART6_RTS/USART6_DE, TIM2_CH3, I2C6_SDA, LCD_R5, DCMI_PIXCLK/PSSI_PDCK/ DCMIPP_PIXCLK, EVENTOUT	-
K2	T3	H2	PG6	I/O	TT_f	(1)	TRACED4, HDP4, SPI5_SCK, SPI1_SCK/I2S1_CK, TIM2_CH4, I2C6_SCL, LCD_R6, DCMI_HSYNC/PSSI_DE/ DCMIPP_HSYNC, EVENTOUT	-
E7	U2	K4	PG7	I/O	TT	(1)	TRACED5, HDP5, SPI5_NSS, SPI1_NSS/I2S1_WS, UART9_CTS, TIM5_ETR, LCD_R7, DCMI_VSYNC/PSSI_RDY/ DCMIPP_VSYNC, EVENTOUT	-
E5	L5	L5	PG8	I/O	TT	(1)	TRACED6, HDP6, SPI5_RDY, SPI1_RDY, USART6_CK, UART5_RTS/UART5_DE, UART9_TX, TIM5_CH3, LCD_G2, DCMI_D2/PSSI_D2/DCMIPP_D2, EVENTOUT	-
G2	M3	G3	PG9	I/O	TT	(1)	TRACED7, UART5_TX, TIM5_CH4, LCD_G3, DCMI_D3/ PSSI_D3/DCMIPP_D3, EVENTOUT	-
F5	M4	H3	PG10	I/O	TT	(1)	TRACED8, HDP0, UART5_RX, TIM8_CH4N, LCD_G4, DCMI_D4/PSSI_D4/DCMIPP_D4, EVENTOUT	-
F7	N2	J4	PG11	I/O	TT	(1)	TRACED9, HDP1, SPI7_MOSI, FDCAN1_TX, TIM8_CH4, LCD_G5, DCMI_D5/PSSI_D5/DCMIPP_D5, EVENTOUT	-
H7	N3	J3	PG12	I/O	TT	(1)	TRACED10, HDP2, SPI7_MISO, FDCAN1_RX, TIM8_CH1N, LCD_G6, DCMI_D6/PSSI_D6/DCMIPP_D6, EVENTOUT	-
J7	P1	K5	PG13	I/O	TT_f	(1)	TRACED11, HDP3, SPI7_SCK, MDF1_CKI6, TIM8_CH2N, I2C1_SCL, I3C1_SCL, LCD_G7, DCMI_D7/PSSI_D7/ DCMIPP_D7, EVENTOUT	-
H5	N1	G4	PG14	I/O	TT	(1)	TRACED12, HDP4, SPI7_RDY, MDF1_CKI5, USART1_TX, TIM8_BKIN2, LCD_B1, DCMI_D9/PSSI_D9/DCMIPP_D9, EVENTOUT	-

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Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
E4	K6	H4	PG15	I/O	TT	(1)	TRACED13, HDP5, LPTIM1_CH2, MDF1_SDI5, USART1_RX, TIM8_ETR, LCD_B2, DCMI_D10/PSSI_D10/DCMIPP_D10, EVENTOUT	-
R1	AG2	V3	OSC_IN	I	A	(13)	-	OSC_IN
R2	AF2	V2	OSC_OUT	I/O	A	(14)	-	OSC_OUT
L14	AC17	V13	PH2	I/O	TT_f	(1)	LPTIM2_CH1, SPI7_RDY, SPDIFRX1_IN3, SAI1_SCK_B, I3C3_SDA, TIM16_CH1, I2C5_SDA, I2C3_SDA, ETH3_RGMII_GTX_CLK, EVENTOUT	-
K14	AE19	W14	PH3	I/O	TT_f	(1)	SPI1_NSS/I2S1_WS, UART7_RX, TIM17_CH1N, TIM5_CH3, I2C7_SCL, ETH3_RGMII_TXD3, EVENTOUT	-
G12	AB16	AB15	PH4	I/O	TT	(1)	UART7_TX, TIM17_BKIN, TIM5_CH2, LCD_R0, USB3DR_OVRCUR, USBH_HS_OVRCUR, ETH1_PTP_AUX_TS, ETH3_PPS_OUT, EVENTOUT	BOOTFAILN
M9	AG18	AA15	PH5	I/O	TT	(1)	SAI2_FS_A, UART8_CTS, TIM2_CH1, UART7_RX, LCD_G1, USB3DR_VBUSEN, USBH_HS_VBUSEN, ETH2_PTP_AUX_TS, EVENTOUT	WKUP2
L15	AF19	AA14	PH6	I/O	TT_f	(1)	LPTIM2_IN2, SAI1_MCLK_B, I3C3_SCL, TIM16_CH1N, I2C5_SCL, I2C3_SCL, I2C1_SMBA, ETH3_RGMII_TXD2, EVENTOUT	-
L12	AE16	T13	PH7	I/O	TT_f	(1)	SPI1_MOSI/I2S1_SDO, UART4_TX, UART7_RTS/UART7_DE, TIM17_CH1, TIM5_CH4, I2C7_SDA, ETH3_RGMII_RXD2, EVENTOUT	-
M12	AD16	U14	PH8	I/O	TT	(1)	SPI1_MISO/I2S1_SDI, SPDIFRX1_IN3, UART4_RX, UART7_CTS, TIM5_CH1, I2C3_SMBA, I2C5_SMBA, ETH3_RGMII_RXD3, EVENTOUT	-
W8	AA13	AB12	PH9	I/O	TT_a	(1)	SPI6_NSS, SAI3_MCLK_A, USART6_RX, TIM15_CH1N, ETH1_RGMII_CLK125, ETH1_MII_RX_ER, EVENTOUT	ADC3_INP4
U10	AF14	U11	PH10	I/O	TT_a	(1)	SPI1_SCK/I2S1_CK, SPI6_MOSI, SAI3_SCK_A, TIM15_CH1, ETH2_MDC, ETH1_MII_TXD2/ETH1_RGMII_TXD2, EVENTOUT	ADC3_INP8, ADC3_INN4
T11	AE14	T11	PH11	I/O	TT_a	(1)	SPI6_MISO, SAI3_FS_A, TIM15_CH2, ETH2_MDIO, ETH1_MII_TXD3/ETH1_RGMII_TXD3, EVENTOUT	-
V8	AF13	AA11	PH12	I/O	TT	(1)	SPI3_NSS/I2S3_WS, SPI6_MISO, TIM10_CH1, ETH1_MII_RXD2/ETH1_RGMII_RXD2, EVENTOUT	-

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Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
U9	AG13	AB11	PH13	I/O	TT	(1)	SPI3_SCK/I2S3_CK, SPI6_MOSI, TIM15_BKIN, TIM11_CH1, ETH1_MII_RXD3/ETH1_RGMII_RXD3, EVENTOUT	-
H1	L7	G5	PI0	I/O	TT	(1)	TRACED14, HDP6, LPTIM1_IN1, SAI4_MCLK_B, USART1_CK, TIM8_BKIN, LCD_B3, DCMI_D11/PSSI_D11/ DCMIPP_D11, EVENTOUT	-
J9	M6	H6	PI1	I/O	TT_f	(1)	TRACED15, HDP7, SPI7_NSS, MDF1_SDI6, TIM8_CH3N, I2C1_SDA, I3C1_SDA, LCD_B4, DCMI_D8/PSSI_D8/ DCMIPP_D8, EVENTOUT	-
J5	N5	J5	PI2	I/O	TT	(1)	LPTIM1_ETR, SAI4_SCK_B, USART1_RTS/USART1_DE, TIM8_CH1, LCD_B5, DCMI_D13/PSSI_D13/DCMIPP_D13, EVENTOUT	-
H9	N7	J6	PI3	I/O	TT	(1)	LPTIM1_IN2, SAI4_SD_B, USART1_CTS/USART1_NSS, TIM8_CH2, LCD_B6, PSSI_D14/DCMIPP_D14, EVENTOUT	-
G1	P6	K6	PI4	I/O	TT	(1)	LPTIM1_CH1, SAI4_FS_B, TIM8_CH3, LCD_B7, PSSI_D15/ DCMIPP_D15, EVENTOUT	-
K7	K4	H5	PI5	I/O	TT	(1)	SPI5_MOSI, SPI1_MOSI/I2S1_SDO, UART5_CTS, UART9_RX, TIM5_CH2, LCD_DE, DCMI_D1/PSSI_D1/ DCMIPP_D1, EVENTOUT	-
D4	J3	J7	PI6	I/O	TT	(1)	MCO1, USART3_TX, TIM2_ETR, TIM3_CH1, LCD_VSYNC, EVENTOUT	WKUP4
D5	J5	L6	PI7	I/O	TT	(1)	USART3_RX, TIM2_CH1, TIM3_CH2, LCD_HSYNC, EVENTOUT	-
N4	U5	M6	PI8	I/O	TT	(6)	EVENTOUT	RTC_OUT2/ RTC_LSCO, TAMP_IN1/ TAMP_OUT2
K6	U1	K7	PI9	I/O	TT	(1)	SPI7_MOSI, SPI2_MOSI/I2S2_SDO, FDCAN2_TX, UART9_CTS, TIM16_BKIN, SDVSEL2, FMC_NWAIT, DSI_TE, LCD_B0, EVENTOUT	-
B11	D16	G16	PI10	I/O	TT	(1)	SAI1_SCK_A, SPI1_SCK/I2S1_CK, SPDIFRX1_IN0, FDCAN2_RX, MDF1_CCK0, TIM4_CH1, SDVSEL1, FMC_AD12/FMC_D12, DSI_TE, EVENTOUT	-
F12	B27	E18	PI11	I/O	TT	(1)	I2S2_MCK, UART8_TX, UART9_RTS/UART9_DE, TIM4_CH3, SDMMC3_D3, FMC_AD15/FMC_D15, EVENTOUT	-
-	-	G1	PI12	I/O	TT	(1)	SPI4_NSS, FDCAN3_RX, TIM11_CH1, FMC_A2, LCD_G0, EVENTOUT	-

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Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
-	-	G2	PI13	I/O	TT	(1)	SPI4_MOSI, FDCAN2_RX, TIM10_CH1, FMC_A3, LCD_G1, EVENTOUT	-
-	-	G13	PI14	I/O	TT	(1)	SPI2_NSS/I2S2_WS, MDF1_SDI1, TIM20_CH3, TIM1_CH3N, FMC_NWAIT, FMC_AD10/FMC_D10, DCMI_D4/PSSI_D4/ DCMIPP_D4, EVENTOUT	-
-	-	E11	PI15	I/O	TT	(1)	I2S2_MCK, UART4_RX, MDF1_CKI2, TIM20_BKIN2, TIM1_BKIN2, SDVSEL1, SDMMC3_CDIR, DCMI_D9/PSSI_D9/ DCMIPP_D9, EVENTOUT	-
-	-	U15	PJ0	I/O	TT	(1)	SPI5_MOSI, PCIE_CLKREQN, SAI4_D2, USART6_CTS/ USART6_NSS, USBH_HS_VBUSEN, ETH2_PTP_AUX_TS, FMC_A11, ETH3_PPS_OUT, EVENTOUT	-
-	-	Y3	PJ1	I/O	TT_f	(1)	USART6_RX, TIM8_CH1N, I2C1_SCL, I3C1_SCL, FMC_A7, DCMI_VSYNC/PSSI_RDY/DCMIPP_VSYNC, EVENTOUT	-
-	-	AB3	PJ2	I/O	TT	(1)	SAI2_SD_B, UART9_RTS/UART9_DE, TIM8_CH4N, USBH_HS_OVRCUR, FMC_A14, EVENTOUT	-
-	-	AA3	PJ3	I/O	TT	(1)	SPI5_NSS, SAI2_FS_A, SAI4_D1, USART6_RTS/ USART6_DE, TIM8_CH3, FMC_A10, EVENTOUT	-
-	-	W3	PJ4	I/O	TT	(1)	SAI2_FS_B, MDF1_CCK1, USART6_CK, TIM8_CH4, I2C2_SMBA, I2C5_SMBA, EVENTOUT	-
-	-	V4	PJ5	I/O	TT	(1)	SPI5_MISO, SAI2_SCK_B, SAI4_CK1, USART6_TX, TIM8_CH1, FMC_A8, EVENTOUT	-
-	-	U5	PJ6	I/O	TT	(1)	SPI7_MOSI, SAI4_SD_A, USART2_CK, TIM20_CH1N, TIM1_CH1, I2C6_SMBA, DCMI_D7/PSSI_D7/DCMIPP_D7, EVENTOUT	-
-	-	W2	PJ7	I/O	TT	(1)	SPI5_MISO, SAI2_MCLK_B, SAI4_D3, USART6_CK, TIM8_CH2N, I2C1_SMBA, FMC_A12, DCMI_D0/PSSI_D0/ DCMIPP_D0, EVENTOUT	-
-	-	M2	PJ8	I/O	TT	(1)	SPI5_SCK, SAI4_CK2, USART6_RX, TIM8_CH2, FMC_A9, PSSI_D14/DCMIPP_D14, EVENTOUT	-
-	-	M1	PJ9	I/O	TT	(1)	SPI4_RDY, TIM12_CH1, TIM8_BKIN, FMC_A5, DCMI_PIXCLK/ PSSI_PDCK/DCMIPP_PIXCLK, EVENTOUT	-
-	-	M3	PJ10	I/O	TT_f	(1)	TIM12_CH2, TIM8_ETR, I2C1_SDA, I3C1_SDA, FMC_A6, DCMI_HSYNC/PSSI_DE/DCMIPP_HSYNC, EVENTOUT	-

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VFBGA361	VFBGA424	TFBGA436						
-	-	M5	PJ11	I/O	TT	(1)	SPI5_RDY, SAI2_SCK_A, SAI4_D4, UART9_CTS, TIM8_CH3N, FMC_A13, DCMI_D12/PSSI_D12/DCMIPP_D12, EVENTOUT	-
-	-	L2	PJ12	I/O	TT_f	(1)	SAI2_SD_A, UART9_RX, FDCAN1_TX, TIM8_BKIN2, I2C2_SCL, I3C2_SCL, FMC_A15, DCMI_D13/PSSI_D13/ DCMIPP_D13, EVENTOUT	-
-	-	M4	PJ13	I/O	TT_f	(1)	SAI2_MCLK_A, UART9_TX, FDCAN1_RX, TIM10_CH1, I2C2_SDA, I3C2_SDA, PSSI_D15/DCMIPP_D15, EVENTOUT	-
-	-	L3	PJ14	I/O	TT	(1)	SPI4_SCK, FDCAN3_TX, FMC_A1, LCD_R0, EVENTOUT	-
-	-	K2	PJ15	I/O	TT	(1)	TRACED7, HDP7, SPI4_MISO, FDCAN2_TX, TIM11_CH1, FMC_A4, LCD_R1, EVENTOUT	-
-	-	F12	PK0	I/O	TT	(1)	SPI2_MISO/I2S2_SDI, SPDIFRX1_IN2, MDF1_CCK0, TIM20_ETR, TIM1_ETR, SDMMC3_D123DIR, FMC_AD11/ FMC_D11, DCMI_D11/PSSI_D11/DCMIPP_D11, EVENTOUT	-
-	-	E12	PK1	I/O	TT	(1)	SPI2_MOSI/I2S2_SDO, MDF1_SDI2, TIM20_BKIN, TIM1_BKIN, SDVSEL2, SDMMC3_D0DIR, FMC_AD13/ FMC_D13, DCMI_D10/PSSI_D10/DCMIPP_D10, EVENTOUT	-
-	-	F13	PK2	I/O	TT_f	(1)	SPI7_NSS, SAI4_SCK_A, USART1_RTS/USART1_DE, TIM20_CH2, TIM1_CH2N, I2C6_SDA, FMC_NCE3, DCMI_D6/ PSSI_D6/DCMIPP_D6, EVENTOUT	-
-	-	F15	PK3	I/O	TT	(1)	SPI7_RDY, MDF1_CKI1, TIM20_CH3N, TIM1_CH3, FMC_AD8/ FMC_D8, DCMI_D3/PSSI_D3/DCMIPP_D3, FMC_NCE4, EVENTOUT	-
-	-	F11	PK4	I/O	TT	(1)	SPI7_MISO, UART4_TX, SAI4_FS_A, TIM20_CH1, TIM1_CH1N, SDMMC3_CKIN, FMC_AD9/FMC_D9, DCMI_D8/ PSSI_D8/DCMIPP_D8, EVENTOUT	-
-	-	F14	PK5	I/O	TT_f	(1)	SPI2_RDY, MDF1_CKI0, USART1_TX, TIM20_CH4N, TIM1_CH4, I2C5_SCL, FMC_AD5/FMC_D5, DCMI_D1/ PSSI_D1/DCMIPP_D1, EVENTOUT	-
-	-	G12	PK6	I/O	TT_f	(1)	SPI7_SCK, SAI4_MCLK_A, USART1_CTS/USART1_NSS, TIM20_CH2N, TIM1_CH2, I2C6_SCL, FMC_AD14/FMC_D14, FMC_AD7/FMC_D7, DCMI_D5/PSSI_D5/DCMIPP_D5, EVENTOUT	-
-	-	G14	PK7	I/O	TT_f	(1)	MDF1_SDI0, USART1_RX, TIM20_CH4, TIM1_CH4N, I2C5_SDA, FMC_NCE4, FMC_AD6/FMC_D6, DCMI_D2/ PSSI_D2/DCMIPP_D2, EVENTOUT	-

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Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
P2	AB4	T6	PWR_CPU_ON	O	TT	(1)	-	-
P1	AF1	U4	PWR_LP	O	TT	(1)	-	-
U3	AD3	T5	PWR_ON	O	TT	(1)	-	-
L5	T4	N5	PZ0	I/O	TT_f	(15)	LPTIM3_IN1, SPI8_MOSI, TIM8_CH1, LPUART1_TX, LPTIM5_OUT, I2C8_SDA, LPTIM3_CH2, I3C4_SDA, EVENTOUT	CPU3_SWDIO, TAMP_OUT3
M4	U7	N6	PZ1	I/O	TT_f	(15)	LPTIM3_CH1, SPI8_MISO, TIM8_CH2, LPUART1_RX, LPTIM5_ETR, I2C8_SCL, I2C8_SMBA, I3C4_SCL, EVENTOUT	CPU3_SWCLK, TAMP_OUT5
M3	W5	P4	PZ2	I/O	TT_f	(15)	LPTIM3_CH1, SPI8_SCK, ADF1_CCK0, LPUART1_RTS/ LPUART1_DE, LPTIM4_ETR, I2C8_SCL, I3C4_SCL, EVENTOUT	TAMP_IN3/ TAMP_OUT7
M5	Y6	N4	PZ3	I/O	TT_f	(15)	DBTRGI, DBTRGO, LPTIM3_ETR, SPI8_NSS, MDF1_SDI5, ADF1_SDI0, LPUART1_CTS, LPTIM4_IN1, I2C8_SDA, LPTIM4_CH2, I3C4_SDA, EVENTOUT	TAMP_OUT4
L4	V3	R5	PZ4	I/O	TT_f	(15)	DBTRGI, DBTRGO, MCO2, SPI8_RDY, MDF1_CCK1, ADF1_CCK1, LPUART1_RX, LPTIM4_CH1, I2C8_SCL, I3C4_SCL, EVENTOUT	TAMP_IN5/ TAMP_OUT6
N3	R5	P5	PZ5	I/O	TT	(15)	MCO1, LPTIM3_ETR, SPI8_SCK, ADF1_CCK0, LPUART1_RTS/LPUART1_DE, LPTIM5_IN1, LPTIM4_CH2, EVENTOUT	TAMP_OUT8
K3	V4	R6	PZ6	I/O	TT	(15)	DBTRGI, DBTRGO, SPI8_NSS, TIM8_CH3, ADF1_SDI0, LPUART1_CTS, LPTIM5_OUT, LPTIM4_CH2, EVENTOUT	TAMP_IN8
L1	V2	P2	PZ7	I/O	TT	(1)	SPI8_MOSI, MDF1_CCK1, ADF1_CCK1, LPUART1_TX, LPTIM5_IN1, LPTIM3_CH2, EVENTOUT	-
L3	V1	P3	PZ8	I/O	TT	(1)	LPTIM3_IN1, SPI8_MISO, MDF1_SDI5, ADF1_SDI0, LPUART1_RX, LPTIM4_CH1, I2C8_SMBA, LPTIM5_ETR, EVENTOUT	-
L2	U3	N3	PZ9	I/O	TT_f	(1)	MCO2, SPI8_RDY, MDF1_CKI5, LPUART1_TX, LPTIM4_ETR, I2C8_SDA, LPTIM3_CH2, I3C4_SDA, EVENTOUT	-
V11	AG21	AB16	USBH_HS_DM	A	A	-	-	-
V12	AG22	Y17	USB3DR_DM	A	A	-	-	-
W11	AF21	AA16	USBH_HS_DP	A	A	-	-	-
W12	AF22	W17	USB3DR_DP	A	A	-	-	-

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Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
T15	AE20	V16	USBH_HS_TXRTUNE	A	A	-	-	-
R15	AF23	V17	USB3DR_TXRTUNE	A	A	-	-	-
T12	AD20	U16	DNU	A	A	-	-	-
W15	AF27	Y20	COMBOPHY_REXT	A	A	-	-	-
V16	AF25	AB20	COMBOPHY_RX1N	A	A	-	-	-
U16	AG25	AA20	COMBOPHY_RX1P	A	A	-	-	-
V15	AD24	AB19	COMBOPHY_TX1N	A	A	-	-	-
U15	AE24	AA19	COMBOPHY_TX1P	A	A	-	-	-
U1	AF6	W5	VREF-	A	A	-	-	-
U2	AG6	Y5	VREF+	A	A	-	-	-
R6	T6	P7	VBAT	S	-	-	-	-
H8	1L1	M9	VDD	S	-	-	-	-
K8	1L3	N8	VDD	S	-	-	-	-
L6	1L5	P9	VDD	S	-	-	-	-
-	1M2	P11	VDD	S	-	-	-	-
-	1M4	R8	VDD	S	-	-	-	-
-	-	R10	VDD	S	-	-	-	-
N6	AB6	V7	VDDA18ADC	S	-	-	-	-
D3	G7	F6	VDDA18CSI	S	-	-	-	-
D16	F20	J16	VDDA18DDR	S	-	-	-	-
C5	G9	C7	VDDA18DSI	S	-	-	-	-
J4	G5	C4	VDDA18LVDS	S	-	(2)	-	-
E15	G19	G17	VDDA18PLL1	S	-	-	-	-
H6	1E1	L8	VDDA18PLL3	S	-	-	-	-
G6	H6	K8	VDDA18PLL2	S	-	-	-	-

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Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
R13	AE23	W18	VDDA18COMBOPHY	S	-	-	-	-
T13	AD22	U17	VDDA18USB	S	-	-	-	-
G10	1C1	H7	VDDCORE	S	-	-	-	-
H11	1C3	H9	VDDCORE	S	-	-	-	-
J10	1C5	J8	VDDCORE	S	-	-	-	-
K11	1D2	J10	VDDCORE	S	-	-	-	-
L10	1D4	K9	VDDCORE	S	-	-	-	-
N8	1E3	K11	VDDCORE	S	-	-	-	-
N10	1E5	L10	VDDCORE	S	-	-	-	-
-	1F2	-	VDDCORE	S	-	-	-	-
-	1F4	-	VDDCORE	S	-	-	-	-
E13	F18	H11	VDDCPU	S	-	-	-	-
G13	G15	H13	VDDCPU	S	-	-	-	-
J13	G17	H15	VDDCPU	S	-	-	-	-
L13	1C7	J12	VDDCPU	S	-	-	-	-
M13	1C9	J14	VDDCPU	S	-	-	-	-
-	1D6	K13	VDDCPU	S	-	-	-	-
-	1D8	L12	VDDCPU	S	-	-	-	-
-	1D10	-	VDDCPU	S	-	-	-	-
F16	1C11	K15	VDDQDDR	S	-	-	-	-
J16	1D12	L14	VDDQDDR	S	-	-	-	-
L16	1E11	L16	VDDQDDR	S	-	-	-	-
M16	M22	M15	VDDQDDR	S	-	-	-	-
P16	1F12	N14	VDDQDDR	S	-	-	-	-
T16	N21	P15	VDDQDDR	S	-	-	-	-
-	R21	R14	VDDQDDR	S	-	-	-	-
-	1L11	R16	VDDQDDR	S	-	-	-	-

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Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
-	1M12	-	VDDQDDR	S	-	-	-	-
F8	D18	F10	VDDIO2	S	-	-	-	-
-	E17	-	VDDIO2	S	-	-	-	-
M11	1G7	M11	VDDGPU	S	-	(2)	-	-
N14	1G9	M13	VDDGPU	S	-	(2)	-	-
P11	1H6	N10	VDDGPU	S	-	(2)	-	-
P13	1H8	N12	VDDGPU	S	-	(2)	-	-
R10	1H10	P13	VDDGPU	S	-	(2)	-	-
-	1L7	R12	VDDGPU	S	-	(2)	-	-
-	1L9	-	VDDGPU	S	-	(2)	-	-
-	1M6	-	VDDGPU	S	-	(2)	-	-
-	1M8	-	VDDGPU	S	-	(2)	-	-
-	1M10	-	VDDGPU	S	-	(2)	-	-
E10	D10	F8	VDDIO3	S	-	-	-	-
F10	E11	F9	VDDIO3	S	-	-	-	-
D6	E9	G8	VDDIO4	S	-	-	-	-
E6	G11	G9	VDDIO4	S	-	-	-	-
D10	D14	G10	VDDIO1	S	-	-	-	-
-	E13	-	VDDIO1	S	-	-	-	-
U11	AE22	T16	VDD33UCPD	S	-	-	-	-
B1	E5	D5	VDDCSI	S	-	-	-	-
C6	F8	F7	VDDDSI	S	-	-	-	-
J1	F4	G7	VDDLVDS	S	-	(2)	-	-
U12	AC21	V18	VDDPCIECLK	S	-	-	-	-
T14	AB20	V19	VDDCOMBOPHY	S	-	-	-	-
W16	AB22	Y19	VDDCOMBOPHYTX	S	-	-	-	-

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Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
N5	AB3	R7	VDDA18AON	S	-	-	-	-
R14	AE21	Y16	VDD33USB	S	-	-	-	-
A1	A1	AB1	VSS	S	-	-	-	-
A19	A2	AB22	VSS	S	-	-	-	-
C3	A27	A1	VSS	S	-	-	-	-
C7	AC11	A22	VSS	S	-	-	-	-
D13	AG1	E5	VSS	S	-	-	-	-
E8	AG27	G6	VSS	S	-	-	-	-
E16	C6	H8	VSS	S	-	-	-	-
F6	C10	H10	VSS	S	-	-	-	-
F11	E7	H12	VSS	S	-	-	-	-
F13	F3	H14	VSS	S	-	-	-	-
G8	F12	H16	VSS	S	-	-	-	-
G11	F14	J9	VSS	S	-	-	-	-
H10	F16	J11	VSS	S	-	-	-	-
H13	1A1	J13	VSS	S	-	-	-	-
H16	1A3	J15	VSS	S	-	-	-	-
J6	1A5	K10	VSS	S	-	-	-	-
J8	1A7	K12	VSS	S	-	-	-	-
J11	1A9	K14	VSS	S	-	-	-	-
J14	1A11	L9	VSS	S	-	-	-	-
K4	J7	L11	VSS	S	-	-	-	-
K5	1B2	L13	VSS	S	-	-	-	-
K10	1B4	L15	VSS	S	-	-	-	-
K13	1B6	M10	VSS	S	-	-	-	-
K16	1B8	M12	VSS	S	-	-	-	-
L8	1B10	M14	VSS	S	-	-	-	-

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Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
L11	1B12	M20	VSS	S	-	-	-	-
M10	K3	N7	VSS	S	-	-	-	-
N11	1E7	N9	VSS	S	-	-	-	-
N13	1E9	N11	VSS	S	-	-	-	-
N16	1F6	N13	VSS	S	-	-	-	-
P8	1F8	N15	VSS	S	-	-	-	-
P10	1F10	P8	VSS	S	-	-	-	-
P14	1G1	P10	VSS	S	-	-	-	-
R11	1G3	P12	VSS	S	-	-	-	-
R16	1G5	P14	VSS	S	-	-	-	-
R18	1G11	R9	VSS	S	-	-	-	-
W1	1H2	R11	VSS	S	-	-	-	-
W19	1H4	R13	VSS	S	-	-	-	-
-	1H12	R15	VSS	S	-	-	-	-
-	1J1	T4	VSS	S	-	-	-	-
-	1J3	U6	VSS	S	-	-	-	-
-	1J5	W8	VSS	S	-	-	-	-
-	1J7	W16	VSS	S	-	-	-	-
-	1J9	W19	VSS	S	-	-	-	-
-	1J11	-	VSS	S	-	-	-	-
-	1K2	-	VSS	S	-	-	-	-
-	1K4	-	VSS	S	-	-	-	-
-	1K6	-	VSS	S	-	-	-	-
-	1K8	-	VSS	S	-	-	-	-
-	1K10	-	VSS	S	-	-	-	-
-	1K12	-	VSS	S	-	-	-	-
-	V6	-	VSS	S	-	-	-	-

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Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA361	VFBGA424	TFBGA436						
-	Y4	-	VSS	S	-	-	-	-
P6	AC5	U7	VSSA	S	-	-	-	-
M6	AC3	M7	VSSAON	S	-	-	-	-
M8	R7	M8	V08CAP	A	-	-	-	-

1. *Power supply is V_{DD}.*
2. *ball is DNU in some part numbers.*
3. *Power supply is V_{DD} - used in open drain with external pull-up.*
4. *Power supply is V_{DDIO4}.*
5. *Power supply is V_{DD} or V_{SW} - input only in V_{SW}.*
6. *Power supply is V_{SW}.*
7. *Power supply is V_{SW} - OSC32_IN pin is also used as digital input in LSE bypass mode and tied to GPIO PC14 input (for test purpose only).*
8. *Power supply is V_{SW} - OSC32_OUT pin is also tied to GPIO PC15 input (for test purpose only).*
9. *Power supply is $V_{DDA18AON}$, must be always connected at board level to $V_{DDA18AON}$.*
10. *Power supply is V_{DDIO3}.*
11. *Power supply is V_{DDIO1}.*
12. *Power supply is V_{DDIO2}.*
13. *Power supply is $V_{DDA18AON}$ - OSC_IN pin is also used as digital input in HSE bypass mode and tied to GPIO PH0 input (for test purpose only).*
14. *Power supply is $V_{DDA18AON}$ - OSC_OUT pin is also tied to GPIO PH1 input, used by Boot ROM to autodetect HSE bypass mode.*
15. *Power supply is V_{DD} or V_{SW}.*

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4.3 Alternate functions

Table 12. Alternate functions AF0 to AF7

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		DBG	DBG / HDP / LPTIM1/2 / RTC / SAI1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/7/8 / SYS	HDP / I2S / LPTIM2/3 / SPDIFRX1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI4/5/6/7 / SYS	I3C3 / LPTIM1/2 / SAI1/2/3/4 / SPDIFRX1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/6/8 / UART4/8 / USART6	FDCAN2 / MDF1 / PCIE / SAI1/2/3/4 / SPDIFRX1 / SPI2 / I2S2 / TIM8 / UART4 / USART6	ADF1 / DSI / I3C3 / MDF1 / SAI2/4 / UART5/8 / USART1/6	FDCAN3 / I2C4/5 / LPUART1 / TIM14/17 / UART7/8/9 / USART1/2/3/6	FDCAN1/2/3 / LPTIM4/5 / TIM2/3/4/12/13/15/16/17/20
Port A	PA0	-	LPTIM1_CH2	SPI5_RDY	UART8_CTS	SAI2_MCLK_B	UART5_TX	USART3_TX	TIM3_ETR
	PA1	-	-	SPI6_MISO	-	SAI3_SD_A	USART1_RTS/ USART1_DE	USART6_CK	TIM4_CH2
	PA2	-	LPTIM2_IN1	SPI7_MISO	-	-	MDF1_SDI7	USART1_RX	-
	PA3	-	LPTIM2_ETR	SPI7_MOSI	-	-	MDF1_CKI7	USART1_TX	-
	PA4	-	-	-	-	-	-	USART2_TX	FDCAN2_TX
	PA5	-	-	-	SPI4_MOSI	SAI2_MCLK_B	SAI2_SD_B	USART2_RTS/ USART2_DE	FDCAN2_RX
	PA6	-	-	-	SPI4_SCK	SAI2_FS_B	MDF1_SDI6	USART2_CK	TIM13_CH1
	PA7	-	-	AUDIOCLK	SPI6_RDY	PCIE_CLKREQN	MDF1_CCK0	USART1_CTS/ USART1_NSS	TIM4_ETR
	PA8	-	LPTIM2_CH2	SPI7_NSS	-	SAI1_FS_B	-	USART1_CK	-
	PA9	-	-	-	SPI4_NSS	SAI2_SCK_B	-	USART2_CTS/ USART2_NSS	LPTIM5_ETR
	PA10	-	-	-	SPI4_MISO	SAI2_SD_B	-	USART2_RX	LPTIM5_IN1
	PA11	-	SPI8_SCK	LPTIM2_CH1	-	SAI4_SD_B	MDF1_SDI4	-	-
	PA12	-	-	SPI6_MOSI	-	SAI3_FS_A	-	-	TIM4_CH1
	PA13	-	SPI8_RDY	I2S3_MCK	LPTIM2_ETR	-	MDF1_CKI3	USART2_CTS/ USART2_NSS	-
	PA14	-	SPI8_NSS	LPTIM2_CH2	-	SAI4_FS_B	MDF1_CCK1	-	-
	PA15	-	-	SPI3_MISO/ I2S3_SDI	-	-	-	USART2_RX	-
Port B	PB0	-	-	SPI2_SCK/ I2S2_CK	-	-	-	USART1_CK	TIM16_CH1

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Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		DBG	DBG / HDP / LPTIM1/2 / RTC / SAI1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/7/8 / SYS	HDP / I2S / LPTIM2/3 / SPDIFRX1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI4/5/6/7 / SYS	I3C3 / LPTIM1/2 / SAI1/2/3/4 / SPDIFRX1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/6/8 / UART4/8 / USART6	FDCAN2 / MDF1 / PCIE / SAI1/2/3/4 / SPDIFRX1 / SPI2 / I2S2 / TIM8 / UART4 / USART6	ADF1 / DSI / I3C3 / MDF1 / SAI2/4 / UART5/8 / USART1/6	FDCAN3 / I2C4/5 / LPUART1 / TIM14/17 / UART7/8/9 / USART1/2/3/6	FDCAN1/2/3 / LPTIM4/5 / TIM2/3/4/12/13/15/16/17/20
Port B	PB1	-	SPI3_NSS/ I2S3_WS	-	-	-	-	-	TIM16_CH1N
	PB2	-	-	SPI2_MOSI/ I2S2_SDO	-	-	MDF1_CKI3	TIM17_BKIN	TIM16_BKIN
	PB3	-	-	SPI2_NSS/ I2S2_WS	-	-	MDF1_SDI3	-	-
	PB4	-	-	SPI2_RDY	UART4_CTS	SAI4_FS_B	MDF1_SDI4	TIM14_CH1	-
	PB5	-	-	I2S2_MCK	UART4_RTS/ UART4_DE	SAI4_SD_B	MDF1_CKI4	-	-
	PB6	-	-	SPI2_MISO/ I2S2_SDI	UART4_RX	SAI4_SCK_B	-	-	-
	PB7	-	SPI3_SCK/ I2S3_CK	-	UART4_TX	SAI4_MCLK_B	-	-	-
	PB8	-	SPI3_MOSI/ I2S3_SDO	-	-	PCIE_CLKREQN	-	USART1_TX	TIM17_CH1
	PB9	-	SPI3_RDY	-	-	-	-	USART1_RTS/ USART1_DE	FDCAN1_TX
	PB10	-	SPI3_MISO/ I2S3_SDI	-	-	-	-	USART1_RX	TIM17_CH1N
	PB11	-	I2S3_MCK	-	-	-	-	USART1_CTS/ USART1_NSS	FDCAN1_RX
	PB12	-	-	-	-	-	UART8_CTS	-	TIM13_CH1
	PB13	-	-	SPI7_SCK	-	SAI1_SD_B	UART8_RX	-	-
	PB14	-	-	SPI2_SCK/ I2S2_CK	-	-	MDF1_CKI7	UART9_RX	-
	PB15	-	LPTIM1_IN2	SPI5_SCK	UART8_RTS/ UART8_DE	SAI2_SD_B	UART5_RX	-	TIM3_CH2
Port C	PC0	-	LPTIM1_CH1	-	SPI6_SCK	SAI3_MCLK_B	USART6_TX	-	-
	PC1	-	-	SPI3_MOSI/ I2S3_SDO	-	-	-	USART2_TX	-

Prerelease product(s)
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Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		DBG	DBG / HDP / LPTIM1/2 / RTC / SAI1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/7/8 / SYS	HDP / I2S / LPTIM2/3 / SPDIFRX1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI4/5/6/7 / SYS	I3C3 / LPTIM1/2 / SAI1/2/3/4 / SPDIFRX1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/6/8 / UART4/8 / USART6	FDCAN2 / MDF1 / PCIE / SAI1/2/3/4 / SPDIFRX1 / SPI2 / I2S2 / TIM8 / UART4 / USART6	ADF1 / DSI / I3C3 / MDF1 / SAI2/4 / UART5/8 / USART1/6	FDCAN3 / I2C4/5 / LPUART1 / TIM14/17 / UART7/8/9 / USART1/2/3/6	FDCAN1/2/3 / LPTIM4/5 / TIM2/3/4/12/13/15/16/17/20
Port C	PC2	-	SPI8_MOSI	LPTIM2_IN1	-	SAI4_MCLK_B	MDF1_SDI3	USART2_RTS/ USART2_DE	-
	PC3	-	LPTIM1_IN2	SPI3_NSS/ I2S3_WS	SPI6_RDY	-	-	USART6_RTS/ USART6_DE	FDCAN2_TX
	PC4	-	-	-	SPI6_MISO	SAI3_FS_B	-	-	-
	PC5	-	-	SPDIFRX1_IN1	-	-	MDF1_SDI1	-	-
	PC6	-	RTC_REFIN	SPDIFRX1_IN0	-	-	MDF1_CKI1	-	-
	PC7	-	-	-	SPI6_MOSI	SAI3_SD_B	-	-	-
	PC8	-	LPTIM1_ETR	-	SPI6_NSS	SAI3_SCK_B	-	USART6_CTS/ USART6_NSS	-
	PC9	-	MCO1	SPI3_MISO/ I2S3_SDI	-	SAI2_SCK_A	-	-	TIM13_CH1
	PC10	-	-	SPI3_MOSI/ I2S3_SDO	-	-	-	-	LPTIM4_ETR
	PC11	-	LPTIM1_CH1	SPI5_NSS	-	SAI2_MCLK_A	UART5_RTS/ UART5_DE	USART3_RTS/ USART3_DE	TIM3_CH1
	PC12	-	LPTIM1_CH2	-	I3C3_SCL	-	MDF1_CKI2	-	-
	PC13	-	-	-	-	-	-	-	-
Port D	PD0	TRACECLK	HDP0	SPI7_RDY	SAI1_D2	-	SAI4_FS_A	UART7_RX	TIM15_CH2
	PD1	-	HDP1	SPI1_MISO/ I2S1_SDI	SAI1_CK2	-	SAI4_SD_A	UART7_RTS/ UART7_DE	TIM15_CH1
	PD2	-	HDP2	SPI1_NSS/ I2S1_WS	SAI1_CK1	-	SAI4_SCK_A	UART7_CTS	TIM15_BKIN
	PD3	-	SAI1_MCLK_A	SPI2_SCK/ I2S2_CK	SAI1_D1	-	SAI4_MCLK_A	UART7_TX	TIM15_CH1N
	PD4	TRACED0	SPI4_MISO	HDP3	SAI1_D3	SAI1_SD_B	-	-	-
	PD5	TRACED1	SPI4_NSS	HDP4	SAI1_D4	SAI1_FS_B	-	-	-
	PD6	TRACED2	SPI4_MOSI	HDP5	-	SAI1_SCK_B	MDF1_SDI2	-	-
	PD7	TRACED3	SPI4_SCK	SPI1_RDY	-	SAI1_MCLK_B	MDF1_CKI2	-	-

Prerelease product(s)
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Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		DBG	DBG / HDP / LPTIM1/2 / RTC / SAI1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/7/8 / SYS	HDP / I2S / LPTIM2/3 / SPDIFRX1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI4/5/6/7 / SYS	I3C3 / LPTIM1/2 / SAI1/2/3/4 / SPDIFRX1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/6/8 / UART4/8 / USART6	FDCAN2 / MDF1 / PCIE / SAI1/2/3/4 / SPDIFRX1 / SPI2 / I2S2 / TIM8 / UART4 / USART6	ADF1 / DSI / I3C3 / MDF1 / SAI2/4 / UART5/8 / USART1/6	FDCAN3 / I2C4/5 / LPUART1 / TIM14/17 / UART7/8/9 / USART1/2/3/6	FDCAN1/2/3 / LPTIM4/5 / TIM2/3/4/12/13/15/16/17/20
Port D	PD8	TRACED4	SPI4_RDY	I2S1_MCK	SAI1_FS_A	UART4_CTS	MDF1_SDI1	-	-
	PD9	TRACED5	HDP6	SPI1_MOSI/ I2S1_SDO	SAI1_SD_A	UART4_RTS/ UART4_DE	MDF1_CKI1	-	-
	PD10	TRACED6	HDP7	-	SAI1_SCK_A	UART4_RX	MDF1_SDI0	I2C4_SDA	-
	PD11	TRACED7	-	SPI1_SCK/ I2S1_CK	SAI1_MCLK_A	UART4_TX	MDF1_CKI0	I2C4_SCL	-
	PD12	-	SPI7_MISO	SPI2_MISO/ I2S2_SDI	SPDIFRX1_IN2	-	UART8_RTS/ UART8_DE	-	-
	PD13	-	-	SPI2_NSS/ I2S2_WS	-	-	MDF1_SDI7	UART9_TX	-
	PD14	-	-	I2S1_MCK	-	-	-	-	FDCAN1_RX
	PD15	-	SPI1_RDY	-	-	-	DSI_TE	I2C5_SDA	FDCAN1_TX
Port E	PE0	TRACED2	LPTIM2_CH1	SPI1_SCK/ I2S1_CK	SPI3_RDY	-	-	USART3_CK	-
	PE1	TRACED3	LPTIM2_CH2	I2S1_MCK	I2S3_MCK	-	-	USART3_RX	-
	PE2	-	LPTIM2_ETR	SPI1_MISO/ I2S1_SDI	SPI3_MOSI/ I2S3_SDO	SAI1_SCK_B	-	-	-
	PE3	TRACECLK	-	SPI1_RDY	SPI3_SCK/ I2S3_CK	SAI1_MCLK_B	-	USART3_TX	-
	PE4	TRACED0	LPTIM2_IN1	SPI1_MOSI/ I2S1_SDO	SPI3_MISO/ I2S3_SDI	SAI1_SD_B	-	USART3_CTS/ USART3_NSS	FDCAN1_TX
	PE5	TRACED1	LPTIM2_IN2	SPI1_NSS/ I2S1_WS	SPI3_NSS/ I2S3_WS	SAI1_FS_B	-	USART3_RTS/ USART3_DE	FDCAN1_RX
	PE6	-	SPI4_RDY	-	-	SPDIFRX1_IN2	-	USART1_TX	-
	PE7	-	-	-	SAI4_D4	SPDIFRX1_IN3	-	USART1_RX	-
	PE8	-	SPI4_MOSI	-	SAI4_CK1	SAI4_MCLK_A	MDF1_CKI0	-	-
	PE9	-	SPI4_MISO	-	SAI4_D2	SAI4_FS_A	-	USART1_CK	-
	PE10	-	SPI4_SCK	-	SAI4_D1	SAI4_SD_A	-	USART1_CTS/ USART1_NSS	-

Prerelease product(s)
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Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		DBG	DBG / HDP / LPTIM1/2 / RTC / SAI1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/7/8 / SYS	HDP / I2S / LPTIM2/3 / SPDIFRX1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI4/5/6/7 / SYS	I3C3 / LPTIM1/2 / SAI1/2/3/4 / SPDIFRX1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/6/8 / UART4/8 / USART6	FDCAN2 / MDF1 / PCIE / SAI1/2/3/4 / SPDIFRX1 / SPI2 / I2S2 / TIM8 / UART4 / USART6	ADF1 / DSI / I3C3 / MDF1 / SAI2/4 / UART5/8 / USART1/6	FDCAN3 / I2C4/5 / LPUART1 / TIM14/17 / UART7/8/9 / USART1/2/3/6	FDCAN1/2/3 / LPTIM4/5 / TIM2/3/4/12/13/15/16/17/20
Port E	PE11	-	-	SPI7_SCK	SAI4_D3	SAI1_FS_A	-	-	TIM15_CH2
	PE12	-	SPI4_NSS	-	SAI4_CK2	SAI4_SCK_A	MDF1_SDI0	USART1_RTS/ USART1_DE	-
	PE13	-	-	SPI7_MISO	-	SAI1_SD_A	-	-	TIM15_CH1
	PE14	-	-	SPI7_NSS	-	SAI1_MCLK_A	MDF1_CKI6	-	TIM15_BKIN
	PE15	-	-	SPI7_MOSI	-	SAI1_SCK_A	MDF1_SDI6	-	TIM15_CH1N
Port F	PF0	-	-	SPI3_SCK/ I2S3_CK	-	-	-	-	FDCAN2_RX
	PF1	-	SPI8_MISO	LPTIM2_IN2	-	SAI4_SCK_B	MDF1_CKI4	USART2_CK	-
	PF2	-	-	SPI3_RDY	-	-	-	I2C4_SMBA	-
	PF3	-	-	-	UART8_RX	SAI2_SCK_B	MDF1_CCK0	-	TIM3_CH4
	PF4	-	RTC_OUT2	SPI6_NSS	-	SAI3_SCK_A	-	USART6_RX	TIM4_CH4
	PF5	-	-	SPI6_SCK	-	SAI3_MCLK_A	-	USART6_TX	TIM4_CH3
	PF6	-	RTC_OUT2	-	SAI3_MCLK_B	-	-	USART6_CK	TIM12_CH1
	PF7	-	-	SPDIFRX1_IN1	SPI6_SCK	SAI3_SD_A	-	-	TIM2_ETR
	PF8	-	RTC_REFIN	-	SAI3_SCK_B	-	-	USART3_RX	TIM12_CH2
	PF9	-	-	-	SAI3_SD_B	SAI2_SD_A	MDF1_SDI5	UART8_RTS/ UART8_DE	TIM2_CH2
	PF10	-	MCO2	SPI3_RDY	-	SAI2_MCLK_A	MDF1_CKI6	UART8_TX	TIM2_CH3
	PF11	-	MCO1	SPDIFRX1_IN0	SPI6_RDY	SAI2_SCK_A	MDF1_SDI6	UART8_RX	TIM2_CH4
	PF12	TRACECLK	-	SPI5_MISO	SPI1_MISO/ I2S1_SDI	-	-	UART9_RTS/ UART9_DE	-
	PF13	TRACED0	HDP0	AUDIOCLK	USART6_TX	SPI2_NSS/ I2S2_WS	MDF1_CKI7	USART3_CTS/ USART3_NSS	FDCAN3_TX
	PF14	TRACED1	HDP1	-	USART6_RX	-	MDF1_SDI7	USART3_RTS/ USART3_DE	FDCAN3_RX
	PF15	TRACED2	HDP2	SPI2_RDY	USART6_CTS/ USART6_NSS	SPI2_SCK/ I2S2_CK	-	USART3_CK	TIM2_CH2

Prerelease product(s)
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Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		DBG	DBG / HDP / LPTIM1/2 / RTC / SAI1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/7/8 / SYS	HDP / I2S / LPTIM2/3 / SPDIFRX1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI4/5/6/7 / SYS	I3C3 / LPTIM1/2 / SAI1/2/3/4 / SPDIFRX1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/6/8 / UART4/8 / USART6	FDCAN2 / MDF1 / PCIE / SAI1/2/3/4 / SPDIFRX1 / SPI2 / I2S2 / TIM8 / UART4 / USART6	ADF1 / DSI / I3C3 / MDF1 / SAI2/4 / UART5/8 / USART1/6	FDCAN3 / I2C4/5 / LPUART1 / TIM14/17 / UART7/8/9 / USART1/2/3/6	FDCAN1/2/3 / LPTIM4/5 / TIM2/3/4/12/13/15/16/17/20
Port G	PG0	-	LPTIM1_IN1	-	I3C3_SDA	-	MDF1_SDI2	-	-
	PG1	-	LPTIM1_IN1	I2S3_MCK	I3C3_SCL	SAI2_SD_A	UART5_CTS	USART3_CTS/ USART3_NSS	-
	PG2	-	RTC_REFIN	I2S3_MCK	I3C3_SDA	SAI2_FS_A	-	USART3_CK	-
	PG3	-	LPTIM1_ETR	SPI5_MOSI	UART8_TX	SAI2_FS_B	-	-	TIM3_CH3
	PG4	-	-	SPI5_MISO	SAI3_FS_B	-	-	-	LPTIM4_IN1
	PG5	TRACED3	HDP3	-	USART6_RTS/ USART6_DE	-	-	-	TIM2_CH3
	PG6	TRACED4	HDP4	SPI5_SCK	SPI1_SCK/ I2S1_CK	-	-	-	TIM2_CH4
	PG7	TRACED5	HDP5	SPI5_NSS	SPI1_NSS/ I2S1_WS	-	-	UART9_CTS	-
	PG8	TRACED6	HDP6	SPI5_RDY	SPI1_RDY	USART6_CK	UART5_RTS/ UART5_DE	UART9_TX	-
	PG9	TRACED7	-	-	-	-	UART5_TX	-	-
	PG10	TRACED8	HDP0	-	-	-	UART5_RX	-	-
	PG11	TRACED9	HDP1	SPI7_MOSI	-	-	-	-	FDCAN1_TX
	PG12	TRACED10	HDP2	SPI7_MISO	-	-	-	-	FDCAN1_RX
	PG13	TRACED11	HDP3	SPI7_SCK	-	-	MDF1_CKI6	-	-
	PG14	TRACED12	HDP4	SPI7_RDY	-	-	MDF1_CKI5	USART1_TX	-
	PG15	TRACED13	HDP5	-	LPTIM1_CH2	-	MDF1_SDI5	USART1_RX	-
Port H	PH2	-	LPTIM2_CH1	SPI7_RDY	SPDIFRX1_IN3	SAI1_SCK_B	I3C3_SDA	-	TIM16_CH1
	PH3	-	-	SPI1_NSS/ I2S1_WS	-	-	-	UART7_RX	TIM17_CH1N
	PH4	-	-	-	-	-	-	UART7_TX	TIM17_BKIN

Prerelease product(s)
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Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		DBG	DBG / HDP / LPTIM1/2 / RTC / SAI1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/7/8 / SYS	HDP / I2S / LPTIM2/3 / SPDIFRX1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI4/5/6/7 / SYS	I3C3 / LPTIM1/2 / SAI1/2/3/4 / SPDIFRX1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/6/8 / UART4/8 / USART6	FDCAN2 / MDF1 / PCIE / SAI1/2/3/4 / SPDIFRX1 / SPI2 / I2S2 / TIM8 / UART4 / USART6	ADF1 / DSI / I3C3 / MDF1 / SAI2/4 / UART5/8 / USART1/6	FDCAN3 / I2C4/5 / LPUART1 / TIM14/17 / UART7/8/9 / USART1/2/3/6	FDCAN1/2/3 / LPTIM4/5 / TIM2/3/4/12/13/15/16/17/20
Port H	PH5	-	-	-	-	SAI2_FS_A	-	UART8_CTS	TIM2_CH1
	PH6	-	LPTIM2_IN2	-	-	SAI1_MCLK_B	I3C3_SCL	-	TIM16_CH1N
	PH7	-	-	SPI1_MOSI/ I2S1_SDO	-	UART4_TX	-	UART7_RTS/ UART7_DE	TIM17_CH1
	PH8	-	-	SPI1_MISO/ I2S1_SDI	SPDIFRX1_IN3	UART4_RX	-	UART7_CTS	-
	PH9	-	-	-	SPI6_NSS	SAI3_MCLK_A	-	USART6_RX	TIM15_CH1N
	PH10	-	-	SPI1_SCK/ I2S1_CK	SPI6_MOSI	SAI3_SCK_A	-	-	TIM15_CH1
	PH11	-	-	-	SPI6_MISO	SAI3_FS_A	-	-	TIM15_CH2
	PH12	-	-	SPI3_NSS/ I2S3_WS	SPI6_MISO	-	-	-	-
	PH13	-	-	SPI3_SCK/ I2S3_CK	SPI6_MOSI	-	-	-	TIM15_BKIN
Port I	PI0	TRACED14	HDP6	-	LPTIM1_IN1	SAI4_MCLK_B	-	USART1_CK	-
	PI1	TRACED15	HDP7	SPI7_NSS	-	-	MDF1_SDI6	-	-
	PI2	-	-	-	LPTIM1_ETR	SAI4_SCK_B	-	USART1_RTS/ USART1_DE	-
	PI3	-	-	-	LPTIM1_IN2	SAI4_SD_B	-	USART1_CTS/ USART1_NSS	-
	PI4	-	-	-	LPTIM1_CH1	SAI4_FS_B	-	-	-
	PI5	-	-	SPI5_MOSI	SPI1_MOSI/ I2S1_SDO	-	UART5_CTS	UART9_RX	-
	PI6	-	MCO1	-	-	-	-	USART3_TX	TIM2_ETR
	PI7	-	-	-	-	-	-	USART3_RX	TIM2_CH1
	PI8	-	-	-	-	-	-	-	-
	PI9	-	SPI7_MOSI	SPI2_MOSI/ I2S2_SDO	-	FDCAN2_TX	-	UART9_CTS	-

Prerelease product(s)
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Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		DBG	DBG / HDP / LPTIM1/2 / RTC / SAI1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/7/8 / SYS	HDP / I2S / LPTIM2/3 / SPDIFRX1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI4/5/6/7 / SYS	I3C3 / LPTIM1/2 / SAI1/2/3/4 / SPDIFRX1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/6/8 / UART4/8 / USART6	FDCAN2 / MDF1 / PCIE / SAI1/2/3/4 / SPDIFRX1 / SPI2 / I2S2 / TIM8 / UART4 / USART6	ADF1 / DSI / I3C3 / MDF1 / SAI2/4 / UART5/8 / USART1/6	FDCAN3 / I2C4/5 / LPUART1 / TIM14/17 / UART7/8/9 / USART1/2/3/6	FDCAN1/2/3 / LPTIM4/5 / TIM2/3/4/12/13/15/16/17/20
Port I	PI10	-	SAI1_SCK_A	SPI1_SCK/ I2S1_CK	SPDIFRX1_IN0	FDCAN2_RX	MDF1_CCK0	-	-
	PI11	-	-	I2S2_MCK	-	-	UART8_TX	UART9_RTS/ UART9_DE	-
	PI12	-	-	SPI4_NSS	-	-	-	-	FDCAN3_RX
	PI13	-	-	SPI4_MOSI	-	FDCAN2_RX	-	-	-
	PI14	-	-	SPI2_NSS/ I2S2_WS	-	-	MDF1_SDI1	-	TIM20_CH3
	PI15	-	-	I2S2_MCK	UART4_RX	-	MDF1_CKI2	-	TIM20_BKIN2
Port J	PJ0	-	-	SPI5_MOSI	-	PCIE_CLKREQN	SAI4_D2	USART6_CTS/ USART6_NSS	-
	PJ1	-	-	-	-	-	-	USART6_RX	-
	PJ2	-	-	-	-	SAI2_SD_B	-	UART9_RTS/ UART9_DE	-
	PJ3	-	-	SPI5_NSS	SAI2_FS_A	-	SAI4_D1	USART6_RTS/ USART6_DE	-
	PJ4	-	-	-	SAI2_FS_B	-	MDF1_CCK1	USART6_CK	-
	PJ5	-	-	SPI5_MISO	SAI2_SCK_B	-	SAI4_CK1	USART6_TX	-
	PJ6	-	-	SPI7_MOSI	-	SAI4_SD_A	-	USART2_CK	TIM20_CH1N
	PJ7	-	-	SPI5_MISO	-	SAI2_MCLK_B	SAI4_D3	USART6_CK	-
	PJ8	-	-	SPI5_SCK	-	-	SAI4_CK2	USART6_RX	-
	PJ9	-	-	SPI4_RDY	-	-	-	-	TIM12_CH1
	PJ10	-	-	-	-	-	-	-	TIM12_CH2
	PJ11	-	-	SPI5_RDY	SAI2_SCK_A	-	SAI4_D4	UART9_CTS	-
	PJ12	-	-	-	SAI2_SD_A	-	-	UART9_RX	FDCAN1_TX
	PJ13	-	-	-	SAI2_MCLK_A	-	-	UART9_TX	FDCAN1_RX
	PJ14	-	-	SPI4_SCK	-	-	-	-	FDCAN3_TX
	PJ15	TRACED7	HDP7	SPI4_MISO	-	FDCAN2_TX	-	-	-

Prerelease product(s)
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Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		DBG	DBG / HDP / LPTIM1/2 / RTC / SAI1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/7/8 / SYS	HDP / I2S / LPTIM2/3 / SPDIFRX1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI4/5/6/7 / SYS	I3C3 / LPTIM1/2 / SAI1/2/3/4 / SPDIFRX1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/6/8 / UART4/8 / USART6	FDCAN2 / MDF1 / PCIE / SAI1/2/3/4 / SPDIFRX1 / SPI2 / I2S2 / TIM8 / UART4 / USART6	ADF1 / DSI / I3C3 / MDF1 / SAI2/4 / UART5/8 / USART1/6	FDCAN3 / I2C4/5 / LPUART1 / TIM14/17 / UART7/8/9 / USART1/2/3/6	FDCAN1/2/3 / LPTIM4/5 / TIM2/3/4/12/13/15/16/17/20
Port K	PK0	-	-	SPI2_MISO/ I2S2_SDI	SPDIFRX1_IN2	-	MDF1_CCK0	-	TIM20_ETR
	PK1	-	-	SPI2_MOSI/ I2S2_SDO	-	-	MDF1_SDI2	-	TIM20_BKIN
	PK2	-	-	SPI7_NSS	-	SAI4_SCK_A	-	USART1_RTS/ USART1_DE	TIM20_CH2
	PK3	-	-	SPI7_RDY	-	-	MDF1_CKI1	-	TIM20_CH3N
	PK4	-	-	SPI7_MISO	UART4_TX	SAI4_FS_A	-	-	TIM20_CH1
	PK5	-	-	SPI2_RDY	-	-	MDF1_CKI0	USART1_TX	TIM20_CH4N
	PK6	-	-	SPI7_SCK	-	SAI4_MCLK_A	-	USART1_CTS/ USART1_NSS	TIM20_CH2N
	PK7	-	-	-	-	-	MDF1_SDI0	USART1_RX	TIM20_CH4
Port Z	PZ0	-	-	LPTIM3_IN1	SPI8_MOSI	TIM8_CH1	-	LPUART1_TX	LPTIM5_OUT
	PZ1	-	-	LPTIM3_CH1	SPI8_MISO	TIM8_CH2	-	LPUART1_RX	LPTIM5_ETR
	PZ2	-	-	LPTIM3_CH1	SPI8_SCK	-	ADF1_CCK0	LPUART1_RTS/ LPUART1_DE	LPTIM4_ETR
	PZ3	DBTRGI	DBTRGO	LPTIM3_ETR	SPI8_NSS	MDF1_SDI5	ADF1_SDI0	LPUART1_CTS	LPTIM4_IN1
	PZ4	DBTRGI	DBTRGO	MCO2	SPI8_RDY	MDF1_CCK1	ADF1_CCK1	LPUART1_RX	LPTIM4_CH1
	PZ5	-	MCO1	LPTIM3_ETR	SPI8_SCK	-	ADF1_CCK0	LPUART1_RTS/ LPUART1_DE	LPTIM5_IN1
	PZ6	DBTRGI	DBTRGO	-	SPI8_NSS	TIM8_CH3	ADF1_SDI0	LPUART1_CTS	LPTIM5_OUT
	PZ7	-	-	-	SPI8_MOSI	MDF1_CCK1	ADF1_CCK1	LPUART1_TX	LPTIM5_IN1
	PZ8	-	-	LPTIM3_IN1	SPI8_MISO	MDF1_SDI5	ADF1_SDI0	LPUART1_RX	LPTIM4_CH1
	PZ9	-	MCO2	-	SPI8_RDY	MDF1_CKI5	-	LPUART1_TX	LPTIM4_ETR

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Table 13. Alternate functions AF8 to AF15

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/4/5/8 / I3C1 / TIM1/2/3/4/5/8/10/11/12/16/20 / UART7 / USART2	DCMI / PSSI / DCMIPP / DSI / ETH1/2 / FDCAN3 / I2C1/2/3/4/5/6/7/8 / LPTIM5 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/3/5/7 / I3C1/2 / LCD / LPTIM3/4 / OCTOSPIM_P1/2 / SDMMC1/3 / TIM14	ETH1/2 / FMC / I2C3/5 / I3C4 / LCD / OCTOSPIM_P1/2 / SDMMC1 / USB3DR	DSI / ETH1/2 / FMC / I2C4 / LCD / OCTOSPIM_P2 / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / DSI / ETH1/2/3 / I3C2 / LCD / OCTOSPIM_P1 / SDMMC2	DCMI / PSSI / DCMIPP / ETH3 / FMC / LCD / SDMMC3	SYS
Port A	PA0	TIM5_CH2	-	ETH2_MII_RXD2	-	FMC_NL	-	DCMI_D9/PSSI_D9/ DCMIPP_D9	EVENTOUT
	PA1	I2C4_SDA	I2C6_SDA	-	LCD_R3	-	DCMI_D5/PSSI_D5/ DCMIPP_D5	ETH3_PHY_INTN	EVENTOUT
	PA2	I3C1_SDA	-	I2C1_SDA	LCD_B0	-	DCMI_D3/PSSI_D3/ DCMIPP_D3	ETH3_RGMII_RX_CTL/ ETH3_RMII_CRS_DV	EVENTOUT
	PA3	I3C1_SCL	I2C7_SMBA	I2C1_SCL	LCD_B1	-	DCMI_D2/PSSI_D2/ DCMIPP_D2	ETH3_RGMII_TX_CTL/ ETH3_RMII_TX_EN	EVENTOUT
	PA4	TIM2_CH1	-	LCD_R1	-	-	ETH1_PTP_AUX_TS	ETH3_PPS_OUT	EVENTOUT
	PA5	TIM2_CH4	-	LCD_G0	-	FMC_A0	DCMI_D13/PSSI_D13/ DCMIPP_D13	ETH3_RGMII_RX_CLK/ ETH3_RMII_REF_CLK	EVENTOUT
	PA6	TIM2_ETR	-	LCD_G4	-	FMC_NE1	DCMI_D12/PSSI_D12/ DCMIPP_D12	ETH3_RGMII_TXD0/ ETH3_RMII_TXD0	EVENTOUT
	PA7	I2C2_SMBA	I2C6_SMBA	LCD_B5	I2C3_SMBA	I2C4_SMBA	DCMI_D6/PSSI_D6/ DCMIPP_D6	ETH3_RGMII_TXD1/ ETH3_RMII_TXD1	EVENTOUT
	PA8	USART2_RX	I2C5_SCL	-	-	LCD_B2	DCMI_D4/PSSI_D4/ DCMIPP_D4	-	EVENTOUT
	PA9	TIM2_CH3	-	ETH1_MDC	-	LCD_G7	PSSI_D14/DCMIPP_D14	ETH3_RGMII_RXD0/ ETH3_RMII_RXD0	EVENTOUT
	PA10	TIM2_CH2	-	ETH1_MDIO	-	LCD_R6	PSSI_D15/DCMIPP_D15	ETH3_RGMII_RXD1/ ETH3_RMII_RXD1	EVENTOUT
	PA11	-	-	ETH1_MII_RX_DV/ETH1_RGMII_RX_CTL/ ETH1_RMII_CRS_DV	-	-	-	-	EVENTOUT
	PA12	I2C4_SCL	I2C6_SCL	ETH1_PHY_INTN	-	-	-	-	EVENTOUT
	PA13	-	I2C7_SMBA	ETH1_MII_TX_EN/ETH1_RGMII_TX_CTL/ ETH1_RMII_TX_EN	-	-	-	-	EVENTOUT
	PA14	-	-	ETH1_MII_RX_CLK/ETH1_RGMII_RX_CLK/ ETH1_RMII_REF_CLK	-	-	-	-	EVENTOUT
	PA15	-	I2C7_SDA	ETH1_MII_TXD0/ETH1_RGMII_TXD0/ ETH1_RMII_TXD0	-	-	-	-	EVENTOUT
Port B	PB0	TIM20_CH4N	-	OCTOSPIM_P2_IO0	-	-	-	-	EVENTOUT
	PB1	TIM20_CH3N	-	OCTOSPIM_P2_IO1	-	FMC_NCE4	-	-	EVENTOUT
	PB2	TIM20_CH2N	-	OCTOSPIM_P2_IO2	-	-	-	-	EVENTOUT
	PB3	TIM20_CH3	-	OCTOSPIM_P2_IO3	-	FMC_NCE3	-	-	EVENTOUT
	PB4	TIM20_CH2	I2C2_SDA	OCTOSPIM_P2_IO4	-	-	I3C2_SDA	-	EVENTOUT

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Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/4/5/8 / I3C1 / TIM1/2/3/4/5/8/10/11/12/16/20 / UART7 / USART2	DCMI / PSSI / DCMIPP / DSI / ETH1/2 / FDCAN3 / I2C1/2/3/4/5/6/7/8 / LPTIM5 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/3/5/7 / I3C1/2 / LCD / LPTIM3/4 / OCTOSPIM_P1/2 / SDMMC1/3 / TIM14	ETH1/2 / FMC / I2C3/5 / I3C4 / LCD / OCTOSPIM_P1/2 / SDMMC1 / USB3DR	DSI / ETH1/2 / FMC / I2C4 / LCD / OCTOSPIM_P2 / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / DSI / ETH1/2/3 / I3C2 / LCD / OCTOSPIM_P1 / SDMMC2	DCMI / PSSI / DCMIPP / ETH3 / FMC / LCD / SDMMC3	SYS
Port B	PB5	TIM20_CH1	I2C2_SCL	OCTOSPIM_P2_IO5	-	FMC_AD8/FMC_D8	I3C2_SCL	SDMMC3_D123DIR	EVENTOUT
	PB6	TIM20_CH1N	-	OCTOSPIM_P2_IO6	-	FMC_AD9/FMC_D9	-	SDMMC3_D0DIR	EVENTOUT
	PB7	TIM20_ETR	TIM12_CH1	OCTOSPIM_P2_IO7	-	FMC_AD10/FMC_D10	-	SDMMC3_CDIR	EVENTOUT
	PB8	TIM20_CH4	-	OCTOSPIM_P2_NCS1	-	FMC_AD12/FMC_D12	-	-	EVENTOUT
	PB9	TIM20_BKIN	TIM10_CH1	OCTOSPIM_P2_DQS	OCTOSPIM_P2_NCS2	FMC_AD13/FMC_D13	-	-	EVENTOUT
	PB10	-	-	OCTOSPIM_P2_CLK	-	FMC_AD15/FMC_D15	-	-	EVENTOUT
	PB11	TIM20_BKIN2	TIM12_CH2	OCTOSPIM_P2_NCLK	OCTOSPIM_P2_NCS2	FMC_AD14/FMC_D14	OCTOSPIM_P1_NCS2	-	EVENTOUT
	PB12	-	DSI_TE	SDMMC3_D2	FMC_NWAIT	-	-	DCMI_D12/PSSI_D12/ DCMIPP_D12	EVENTOUT
	PB13	-	-	SDMMC3_CK	FMC_AD5/FMC_D5	FMC_AD0/FMC_D0	-	-	EVENTOUT
	PB14	-	TIM4_CH2	SDMMC3_D0	FMC_AD7/FMC_D7	FMC_AD2/FMC_D2	-	-	EVENTOUT
	PB15	TIM5_CH1	-	ETH1_PPS_OUT	-	FMC_A18	LCD_R4	DCMI_D8/PSSI_D8/ DCMIPP_D8	EVENTOUT
Port C	PC0	-	DCMI_D0/PSSI_D0/ DCMIPP_D0	ETH2_MII_RX_CLK/ETH2_RMII_REF_CLK	ETH1_MII_TX_CLK	ETH1_RGMII_GTX_CLK	LCD_G7	-	EVENTOUT
	PC1	-	I2C7_SCL	ETH1_MII_TXD1/ETH1_RGMII_TXD1/ ETH1_RMII_TXD1	-	-	-	-	EVENTOUT
	PC2	-	-	ETH1_MII_RXD1/ETH1_RGMII_RXD1/ ETH1_RMII_RXD1	-	-	-	-	EVENTOUT
	PC3	-	-	ETH2_MII_RX_DV/ETH2_RGMII_RX_CTL/ ETH2_RMII_CRS_DV	ETH1_MII_RX_ER	-	LCD_G6	DCMI_D3/PSSI_D3/ DCMIPP_D3	EVENTOUT
	PC4	-	-	ETH2_MII_TX_EN/ETH2_RGMII_TX_CTL/ ETH2_RMII_TX_EN	-	ETH1_RGMII_CLK125	LCD_R0	-	EVENTOUT
	PC5	TIM8_CH1N	I2C4_SDA	ETH2_MDIO	ETH1_MII_COL	FMC_A25	ETH1_PPS_OUT	LCD_DE	EVENTOUT
	PC6	TIM8_CH1	I2C4_SCL	ETH2_MDC	ETH1_MII_CRS	FMC_A24	ETH1_PHY_INTN	LCD_CLK	EVENTOUT
	PC7	TIM8_CH2N	-	ETH2_MII_TXD0/ETH2_RGMII_TXD0/ ETH2_RMII_TXD0	ETH1_MII_TXD2	-	LCD_B4	DCMI_D1/PSSI_D1/ DCMIPP_D1	EVENTOUT
	PC8	TIM8_CH2	-	ETH2_MII_TXD1/ETH2_RGMII_TXD1/ ETH2_RMII_TXD1	ETH1_MII_TXD3	-	LCD_B3	DCMI_D2/PSSI_D2/ DCMIPP_D2	EVENTOUT
	PC9	TIM8_CH4N	USBH_HS_OVRCUR	ETH2_MII_TXD2/ETH2_RGMII_TXD2	USB3DR_OVRCUR	FMC_A22	LCD_G2	DCMI_D7/PSSI_D7/ DCMIPP_D7	EVENTOUT
	PC10	TIM8_CH4	USBH_HS_VBUSEN	ETH2_MII_TXD3/ETH2_RGMII_TXD3	USB3DR_VBUSEN	FMC_A23	LCD_G3	DCMI_D6/PSSI_D6/ DCMIPP_D6	EVENTOUT

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Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/4/5/8 / I3C1 / TIM1/2/3/4/5/8/10/11/12/16/20 / UART7 / USART2	DCMI / PSSI / DCMIPP / DSI / ETH1/2 / FDCAN3 / I2C1/2/3/4/5/6/7/8 / LPTIM5 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/3/5/7 / I3C1/2 / LCD / LPTIM3/4 / OCTOSPIM_P1/2 / SDMMC1/3 / TIM14	ETH1/2 / FMC / I2C3/5 / I3C4 / LCD / OCTOSPIM_P1/2 / SDMMC1 / USB3DR	DSI / ETH1/2 / FMC / I2C4 / LCD / OCTOSPIM_P2 / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / DSI / ETH1/2/3 / I3C2 / LCD / OCTOSPIM_P1 / SDMMC2	DCMI / PSSI / DCMIPP / ETH3 / FMC / LCD / SDMMC3	SYS
Port C	PC11	TIM5_ETR	-	ETH2_MII_RXD3/ETH2_RGMII_RXD3	-	FMC_NBL1	LCD_R2	DCMI_D10/PSSI_D10/ DCMIPP_D10	EVENTOUT
	PC12	TIM8_CH3	I2C3_SCL	ETH2_MII_RXD1/ETH2_RGMII_RXD1/ ETH2_RMII_RXD1	ETH1_MII_RXD3	-	LCD_G1	DCMI_D5/PSSI_D5/ DCMIPP_D5	EVENTOUT
	PC13	-	-	-	-	-	-	-	EVENTOUT
Port D	PD0	-	SDVSEL1	OCTOSPIM_P1_CLK	-	-	DCMI_PIXCLK/PSSI_PDCK/ DCMIPP_PIXCLK	-	EVENTOUT
	PD1	TIM1_BKIN	FDCAN3_RX	OCTOSPIM_P1_NCLK	OCTOSPIM_P1_NCS2	OCTOSPIM_P2_NCS2	DCMI_HSYNC/PSSI_DE/ DCMIPP_HSYNC	-	EVENTOUT
	PD2	TIM1_ETR	FDCAN3_TX	OCTOSPIM_P1_DQS	OCTOSPIM_P1_NCS2	-	DCMI_VSYNC/PSSI_RDY/ DCMIPP_VSYNC	-	EVENTOUT
	PD3	TIM1_BKIN2	SDVSEL2	OCTOSPIM_P1_NCS1	-	-	PSSI_D15/DCMIPP_D15	-	EVENTOUT
	PD4	TIM1_CH4N	TIM4_CH1	OCTOSPIM_P1_IO0	-	-	PSSI_D14/DCMIPP_D14	-	EVENTOUT
	PD5	TIM1_CH3N	TIM4_CH2	OCTOSPIM_P1_IO1	-	-	DCMI_D13/PSSI_D13/ DCMIPP_D13	-	EVENTOUT
	PD6	TIM1_CH2N	TIM4_CH3	OCTOSPIM_P1_IO2	-	-	DCMI_D12/PSSI_D12/ DCMIPP_D12	-	EVENTOUT
	PD7	TIM1_CH1N	TIM4_CH4	OCTOSPIM_P1_IO3	-	-	DCMI_D11/PSSI_D11/ DCMIPP_D11	-	EVENTOUT
	PD8	TIM1_CH4	TIM4_ETR	OCTOSPIM_P1_IO4	SDMMC1_D7	SDMMC1_D123DIR	DCMI_D10/PSSI_D10/ DCMIPP_D10	-	EVENTOUT
	PD9	TIM1_CH3	-	OCTOSPIM_P1_IO5	SDMMC1_D6	SDMMC1_D0DIR	DCMI_D9/PSSI_D9/ DCMIPP_D9	-	EVENTOUT
	PD10	TIM1_CH2	TIM14_CH1	OCTOSPIM_P1_IO6	SDMMC1_D5	SDMMC1_CDIR	DCMI_D8/PSSI_D8/ DCMIPP_D8	-	EVENTOUT
	PD11	TIM1_CH1	SDVSEL1	OCTOSPIM_P1_IO7	SDMMC1_D4	SDMMC1_CKIN	DCMI_D7/PSSI_D7/ DCMIPP_D7	-	EVENTOUT
	PD12	-	TIM4_ETR	SDMMC3_CMD	FMC_AD6/FMC_D6	FMC_AD1/FMC_D1	-	-	EVENTOUT
	PD13	-	TIM4_CH4	SDMMC3_D1	FMC_AD11/FMC_D11	FMC_NWE	-	-	EVENTOUT
	PD14	TIM11_CH1	-	I2C7_SDA	FMC_AD4/FMC_D4	SDMMC3_D3	DCMI_D1/PSSI_D1/ DCMIPP_D1	-	EVENTOUT
	PD15	TIM1_BKIN2	TIM5_ETR	I2C7_SCL	FMC_AD3/FMC_D3	SDMMC3_CKIN	DCMI_D0/PSSI_D0/ DCMIPP_D0	-	EVENTOUT
Port E	PE0	-	-	SDMMC1_D2	-	-	-	-	EVENTOUT
	PE1	-	-	SDMMC1_D3	-	-	-	-	EVENTOUT
	PE2	TIM10_CH1	-	SDMMC1_CMD	-	-	-	-	EVENTOUT

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Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/4/5/8 / I3C1 / TIM1/2/3/4/5/8/10/11/12/16/20 / UART7 / USART2	DCMI / PSSI / DCMIPP / DSI / ETH1/2 / FDCAN3 / I2C1/2/3/4/5/6/7/8 / LPTIM5 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/3/5/7 / I3C1/2 / LCD / LPTIM3/4 / OCTOSPIM_P1/2 / SDMMC1/3 / TIM14	ETH1/2 / FMC / I2C3/5 / I3C4 / LCD / OCTOSPIM_P1/2 / SDMMC1 / USB3DR	DSI / ETH1/2 / FMC / I2C4 / LCD / OCTOSPIM_P2 / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / DSI / ETH1/2/3 / I3C2 / LCD / OCTOSPIM_P1 / SDMMC2	DCMI / PSSI / DCMIPP / ETH3 / FMC / LCD / SDMMC3	SYS
Port E	PE3	TIM11_CH1	-	SDMMC1_CK	-	-	-	-	EVENTOUT
	PE4	-	-	SDMMC1_D0	-	-	-	-	EVENTOUT
	PE5	-	-	SDMMC1_D1	-	-	-	-	EVENTOUT
	PE6	TIM1_ETR	-	-	FMC_AD1/FMC_D1	SDMMC2_D6	SDMMC2_D0DIR	-	EVENTOUT
	PE7	TIM1_CH4N	-	TIM14_CH1	FMC_AD2/FMC_D2	SDMMC2_D7	SDMMC2_D123DIR	-	EVENTOUT
	PE8	TIM1_CH1	-	-	FMC_A17/FMC_ALE	SDMMC2_D2	-	-	EVENTOUT
	PE9	TIM1_CH4	-	-	FMC_AD0/FMC_D0	SDMMC2_D5	SDMMC2_CDIR	-	EVENTOUT
	PE10	TIM1_CH3	-	FMC_NE3	FMC_NCE2	SDMMC2_D4	SDMMC2_CKIN	-	EVENTOUT
	PE11	TIM1_CH3N	-	-	FMC_A16/FMC_CLE	SDMMC2_D1	-	-	EVENTOUT
	PE12	TIM1_CH2	-	FMC_NE2	FMC_NCE1	SDMMC2_D3	-	-	EVENTOUT
	PE13	TIM1_CH2N	-	-	FMC_RNB	SDMMC2_D0	-	-	EVENTOUT
	PE14	TIM1_BKIN	-	-	FMC_NWE	SDMMC2_CK	-	-	EVENTOUT
	PE15	TIM1_CH1N	-	-	FMC_NOE	SDMMC2_CMD	-	-	EVENTOUT
Port F	PF0	TIM12_CH2	I2C2_SDA	ETH1_MDC	ETH2_MII_CRS	-	I3C2_SDA	-	EVENTOUT
	PF1	-	-	ETH1_MII_RXD0/ETH1_RGMII_RXD0/ ETH1_RMII_RXD0	-	-	-	-	EVENTOUT
	PF2	TIM12_CH1	I2C2_SCL	ETH1_MDIO	ETH2_MII_COL	FMC_NE4	I3C2_SCL	-	EVENTOUT
	PF3	TIM8_BKIN2	ETH1_CLK	ETH2_PPS_OUT	-	FMC_A20	LCD_R6	DCMI_HSYNC/PSSI_DE/ DCMIPP_HSYNC	EVENTOUT
	PF4	ETH1_MDC	ETH2_CLK	ETH2_PPS_OUT	ETH1_PPS_OUT	-	LCD_B7	-	EVENTOUT
	PF5	ETH1_MDIO	ETH1_CLK	ETH2_PHY_INTN	ETH1_PHY_INTN	-	LCD_B6	-	EVENTOUT
	PF6	-	I2C3_SMBA	ETH2_MII_RX_CLK/ETH2_RGMII_RX_CLK/ ETH2_RMII_REF_CLK	-	-	LCD_B0	-	EVENTOUT
	PF7	-	-	ETH2_RGMII_GTX_CLK	ETH2_MII_TX_CLK	-	LCD_R1	-	EVENTOUT
	PF8	-	ETH1_CLK	ETH2_RGMII_CLK125	ETH2_MII_RX_ER	ETH2_MII_RX_DV/ETH2_RMII_CRS_DV	LCD_G0	-	EVENTOUT

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Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/4/5/8 / I3C1 / TIM1/2/3/4/5/8/10/11/12/16/20 / UART7 / USART2	DCMI / PSSI / DCMIPP / DSI / ETH1/2 / FDCAN3 / I2C1/2/3/4/5/6/7/8 / LPTIM5 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/3/5/7 / I3C1/2 / LCD / LPTIM3/4 / OCTOSPIM_P1/2 / SDMMC1/3 / TIM14	ETH1/2 / FMC / I2C3/5 / I3C4 / LCD / OCTOSPIM_P1/2 / SDMMC1 / USB3DR	DSI / ETH1/2 / FMC / I2C4 / LCD / OCTOSPIM_P2 / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / DSI / ETH1/2/3 / I3C2 / LCD / OCTOSPIM_P1 / SDMMC2	DCMI / PSSI / DCMIPP / ETH3 / FMC / LCD / SDMMC3	SYS
Port F	PF9	-	-	ETH2_MII_RXD2/ETH2_RGMII_RXD2	ETH2_MDIO	-	-	-	EVENTOUT
	PF10	-	-	ETH2_MII_TXD2	-	-	-	-	EVENTOUT
	PF11	-	-	ETH2_MII_TXD3	-	-	-	-	EVENTOUT
	PF12	TIM5_CH1	-	-	-	-	LCD_CLK	DCMI_D0/PSSI_D0/ DCMIPP_D0	EVENTOUT
	PF13	TIM3_CH3	-	-	-	-	LCD_R2	-	EVENTOUT
	PF14	TIM3_CH4	-	-	-	-	LCD_R3	-	EVENTOUT
	PF15	TIM3_ETR	I2C6_SMBA	-	-	-	LCD_R4	-	EVENTOUT
Port G	PG0	TIM8_CH3N	I2C3_SDA	ETH2_MII_RXD0/ETH2_RGMII_RXD0/ ETH2_RMII_RXD0	ETH1_MII_RXD2	-	LCD_G5	DCMI_D4/PSSI_D4/ DCMIPP_D4	EVENTOUT
	PG1	TIM5_CH4	I2C3_SCL	ETH2_MII_RX_ER	ETH2_MII_RXD3	FMC_NBL0	LCD_VSYNC	DCMI_D11/PSSI_D11/ DCMIPP_D11	EVENTOUT
	PG2	TIM5_CH3	I2C3_SDA	ETH2_MII_TX_CLK	ETH2_RGMII_CLK125	FMC_CLK	LCD_HSYNC	-	EVENTOUT
	PG3	TIM8_ETR	ETH2_CLK	ETH2_PHY_INTN	-	FMC_A19	LCD_R5	DCMI_PIXCLK/PSSI_PDCK/ DCMIPP_PIXCLK	EVENTOUT
	PG4	TIM8_BKIN	-	ETH2_PPS_OUT	ETH2_MDC	FMC_A21	LCD_R7	DCMI_VSYNC/PSSI_RDY/ DCMIPP_VSYNC	EVENTOUT
	PG5	-	I2C6_SDA	-	-	-	LCD_R5	DCMI_PIXCLK/PSSI_PDCK/ DCMIPP_PIXCLK	EVENTOUT
	PG6	-	I2C6_SCL	-	-	-	LCD_R6	DCMI_HSYNC/PSSI_DE/ DCMIPP_HSYNC	EVENTOUT
	PG7	TIM5_ETR	-	-	-	-	LCD_R7	DCMI_VSYNC/PSSI_RDY/ DCMIPP_VSYNC	EVENTOUT
	PG8	TIM5_CH3	-	-	-	-	LCD_G2	DCMI_D2/PSSI_D2/ DCMIPP_D2	EVENTOUT
	PG9	TIM5_CH4	-	-	-	-	LCD_G3	DCMI_D3/PSSI_D3/ DCMIPP_D3	EVENTOUT
	PG10	TIM8_CH4N	-	-	-	-	LCD_G4	DCMI_D4/PSSI_D4/ DCMIPP_D4	EVENTOUT
	PG11	TIM8_CH4	-	-	-	-	LCD_G5	DCMI_D5/PSSI_D5/ DCMIPP_D5	EVENTOUT
	PG12	TIM8_CH1N	-	-	-	-	LCD_G6	DCMI_D6/PSSI_D6/ DCMIPP_D6	EVENTOUT
	PG13	TIM8_CH2N	I2C1_SCL	I3C1_SCL	-	-	LCD_G7	DCMI_D7/PSSI_D7/ DCMIPP_D7	EVENTOUT
	PG14	TIM8_BKIN2	-	-	-	-	LCD_B1	DCMI_D9/PSSI_D9/ DCMIPP_D9	EVENTOUT

Prerelease product(s)
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Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/4/5/8 / I3C1 / TIM1/2/3/4/5/8/10/11/12/16/20 / UART7 / USART2	DCMI / PSSI / DCMIPP / DSI / ETH1/2 / FDCAN3 / I2C1/2/3/4/5/6/7/8 / LPTIM5 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/3/5/7 / I3C1/2 / LCD / LPTIM3/4 / OCTOSPIM_P1/2 / SDMMC1/3 / TIM14	ETH1/2 / FMC / I2C3/5 / I3C4 / LCD / OCTOSPIM_P1/2 / SDMMC1 / USB3DR	DSI / ETH1/2 / FMC / I2C4 / LCD / OCTOSPIM_P2 / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / DSI / ETH1/2/3 / I3C2 / LCD / OCTOSPIM_P1 / SDMMC2	DCMI / PSSI / DCMIPP / ETH3 / FMC / LCD / SDMMC3	SYS
Port G	PG15	TIM8_ETR	-	-	-	-	LCD_B2	DCMI_D10/PSSI_D10/ DCMIPP_D10	EVENTOUT
Port H	PH2	I2C5_SDA	I2C3_SDA	-	-	-	-	ETH3_RGMII_GTX_CLK	EVENTOUT
	PH3	-	TIM5_CH3	I2C7_SCL	-	-	-	ETH3_RGMII_TXD3	EVENTOUT
	PH4	-	TIM5_CH2	LCD_R0	USB3DR_OVRCUR	USBH_HS_OVRCUR	ETH1_PTP_AUX_TS	ETH3_PPS_OUT	EVENTOUT
	PH5	UART7_RX	-	LCD_G1	USB3DR_VBUSEN	USBH_HS_VBUSEN	ETH2_PTP_AUX_TS	-	EVENTOUT
	PH6	I2C5_SCL	I2C3_SCL	I2C1_SMBA	-	-	-	ETH3_RGMII_TXD2	EVENTOUT
	PH7	-	TIM5_CH4	I2C7_SDA	-	-	-	ETH3_RGMII_RXD2	EVENTOUT
	PH8	-	TIM5_CH1	I2C3_SMBA	I2C5_SMBA	-	-	ETH3_RGMII_RXD3	EVENTOUT
	PH9	-	-	ETH1_RGMII_CLK125	ETH1_MII_RX_ER	-	-	-	EVENTOUT
	PH10	-	ETH2_MDC	ETH1_MII_TXD2/ETH1_RGMII_TXD2	-	-	-	-	EVENTOUT
	PH11	-	ETH2_MDIO	ETH1_MII_TXD3/ETH1_RGMII_TXD3	-	-	-	-	EVENTOUT
	PH12	TIM10_CH1	-	ETH1_MII_RXD2/ETH1_RGMII_RXD2	-	-	-	-	EVENTOUT
	PH13	TIM11_CH1	-	ETH1_MII_RXD3/ETH1_RGMII_RXD3	-	-	-	-	EVENTOUT
Port I	PI0	TIM8_BKIN	-	-	-	-	LCD_B3	DCMI_D11/PSSI_D11/ DCMIPP_D11	EVENTOUT
	PI1	TIM8_CH3N	I2C1_SDA	I3C1_SDA	-	-	LCD_B4	DCMI_D8/PSSI_D8/ DCMIPP_D8	EVENTOUT
	PI2	TIM8_CH1	-	-	-	-	LCD_B5	DCMI_D13/PSSI_D13/ DCMIPP_D13	EVENTOUT
	PI3	TIM8_CH2	-	-	-	-	LCD_B6	PSSI_D14/DCMIPP_D14	EVENTOUT
	PI4	TIM8_CH3	-	-	-	-	LCD_B7	PSSI_D15/DCMIPP_D15	EVENTOUT
	PI5	TIM5_CH2	-	-	-	-	LCD_DE	DCMI_D1/PSSI_D1/ DCMIPP_D1	EVENTOUT
	PI6	TIM3_CH1	-	-	-	-	LCD_VSYNC	-	EVENTOUT
	PI7	TIM3_CH2	-	-	-	-	LCD_HSYNC	-	EVENTOUT

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Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/4/5/8 / I3C1 / TIM1/2/3/4/5/8/10/11/12/16/20 / UART7 / USART2	DCMI / PSSI / DCMIPP / DSI / ETH1/2 / FDCAN3 / I2C1/2/3/4/5/6/7/8 / LPTIM5 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/3/5/7 / I3C1/2 / LCD / LPTIM3/4 / OCTOSPIM_P1/2 / SDMMC1/3 / TIM14	ETH1/2 / FMC / I2C3/5 / I3C4 / LCD / OCTOSPIM_P1/2 / SDMMC1 / USB3DR	DSI / ETH1/2 / FMC / I2C4 / LCD / OCTOSPIM_P2 / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / DSI / ETH1/2/3 / I3C2 / LCD / OCTOSPIM_P1 / SDMMC2	DCMI / PSSI / DCMIPP / ETH3 / FMC / LCD / SDMMC3	SYS
Port I	PI8	-	-	-	-	-	-	-	EVENTOUT
	PI9	TIM16_BKIN	SDVSEL2	FMC_NWAIT	-	DSI_TE	LCD_B0	-	EVENTOUT
	PI10	TIM4_CH1	SDVSEL1	-	-	FMC_AD12/FMC_D12	DSI_TE	-	EVENTOUT
	PI11	-	TIM4_CH3	SDMMC3_D3	FMC_AD15/FMC_D15	-	-	-	EVENTOUT
	PI12	TIM11_CH1	-	-	-	FMC_A2	LCD_G0	-	EVENTOUT
	PI13	TIM10_CH1	-	-	-	FMC_A3	LCD_G1	-	EVENTOUT
	PI14	TIM1_CH3N	-	FMC_NWAIT	-	FMC_AD10/FMC_D10	DCMI_D4/PSSI_D4/ DCMIPP_D4	-	EVENTOUT
	PI15	TIM1_BKIN2	SDVSEL1	SDMMC3_CDIR	-	-	DCMI_D9/PSSI_D9/ DCMIPP_D9	-	EVENTOUT
Port J	PJ0	-	USBH_HS_VBUSEN	-	ETH2_PTP_AUX_TS	FMC_A11	ETH3_PPS_OUT	-	EVENTOUT
	PJ1	TIM8_CH1N	I2C1_SCL	I3C1_SCL	-	FMC_A7	-	DCMI_VSYNC/PSSI_RDY/ DCMIPP_VSYNC	EVENTOUT
	PJ2	TIM8_CH4N	USBH_HS_OVRCUR	-	-	FMC_A14	-	-	EVENTOUT
	PJ3	TIM8_CH3	-	-	-	FMC_A10	-	-	EVENTOUT
	PJ4	TIM8_CH4	I2C2_SMBA	I2C5_SMBA	-	-	-	-	EVENTOUT
	PJ5	TIM8_CH1	-	-	-	FMC_A8	-	-	EVENTOUT
	PJ6	TIM1_CH1	I2C6_SMBA	-	-	-	DCMI_D7/PSSI_D7/ DCMIPP_D7	-	EVENTOUT
	PJ7	TIM8_CH2N	I2C1_SMBA	-	-	FMC_A12	-	DCMI_D0/PSSI_D0/ DCMIPP_D0	EVENTOUT
	PJ8	TIM8_CH2	-	-	-	FMC_A9	-	PSSI_D14/DCMIPP_D14	EVENTOUT
	PJ9	TIM8_BKIN	-	-	-	FMC_A5	-	DCMI_PIXCLK/PSSI_PDCK/ DCMIPP_PIXCLK	EVENTOUT
	PJ10	TIM8_ETR	I2C1_SDA	I3C1_SDA	-	FMC_A6	-	DCMI_HSYNC/PSSI_DE/ DCMIPP_HSYNC	EVENTOUT
	PJ11	TIM8_CH3N	-	-	-	FMC_A13	-	DCMI_D12/PSSI_D12/ DCMIPP_D12	EVENTOUT
	PJ12	TIM8_BKIN2	I2C2_SCL	I3C2_SCL	-	FMC_A15	-	DCMI_D13/PSSI_D13/ DCMIPP_D13	EVENTOUT
	PJ13	TIM10_CH1	I2C2_SDA	I3C2_SDA	-	-	-	PSSI_D15/DCMIPP_D15	EVENTOUT

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Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/4/5/8 / I3C1 / TIM1/2/3/4/5/8/10/11/12/16/20 / UART7 / USART2	DCMI / PSSI / DCMIPP / DSI / ETH1/2 / FDCAN3 / I2C1/2/3/4/5/6/7/8 / LPTIM5 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/3/5/7 / I3C1/2 / LCD / LPTIM3/4 / OCTOSPIM_P1/2 / SDMMC1/3 / TIM14	ETH1/2 / FMC / I2C3/5 / I3C4 / LCD / OCTOSPIM_P1/2 / SDMMC1 / USB3DR	DSI / ETH1/2 / FMC / I2C4 / LCD / OCTOSPIM_P2 / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / DSI / ETH1/2/3 / I3C2 / LCD / OCTOSPIM_P1 / SDMMC2	DCMI / PSSI / DCMIPP / ETH3 / FMC / LCD / SDMMC3	SYS
Port J	PJ14	-	-	-	-	FMC_A1	LCD_R0	-	EVENTOUT
	PJ15	TIM11_CH1	-	-	-	FMC_A4	LCD_R1	-	EVENTOUT
Port K	PK0	TIM1_ETR	-	SDMMC3_D123DIR	-	FMC_AD11/FMC_D11	DCMI_D11/PSSI_D11/DCMIPP_D11	-	EVENTOUT
	PK1	TIM1_BKIN	SDVSEL2	SDMMC3_D0DIR	-	FMC_AD13/FMC_D13	DCMI_D10/PSSI_D10/DCMIPP_D10	-	EVENTOUT
	PK2	TIM1_CH2N	I2C6_SDA	-	-	FMC_NCE3	DCMI_D6/PSSI_D6/DCMIPP_D6	-	EVENTOUT
	PK3	TIM1_CH3	-	-	-	FMC_AD8/FMC_D8	DCMI_D3/PSSI_D3/DCMIPP_D3	FMC_NCE4	EVENTOUT
	PK4	TIM1_CH1N	-	SDMMC3_CKIN	-	FMC_AD9/FMC_D9	DCMI_D8/PSSI_D8/DCMIPP_D8	-	EVENTOUT
	PK5	TIM1_CH4	-	I2C5_SCL	-	FMC_AD5/FMC_D5	DCMI_D1/PSSI_D1/DCMIPP_D1	-	EVENTOUT
	PK6	TIM1_CH2	I2C6_SCL	-	FMC_AD14/FMC_D14	FMC_AD7/FMC_D7	DCMI_D5/PSSI_D5/DCMIPP_D5	-	EVENTOUT
	PK7	TIM1_CH4N	-	I2C5_SDA	FMC_NCE4	FMC_AD6/FMC_D6	DCMI_D2/PSSI_D2/DCMIPP_D2	-	EVENTOUT
Port Z	PZ0	I2C8_SDA	-	LPTIM3_CH2	I3C4_SDA	-	-	-	EVENTOUT
	PZ1	I2C8_SCL	I2C8_SMBA	-	I3C4_SCL	-	-	-	EVENTOUT
	PZ2	I2C8_SCL	-	-	I3C4_SCL	-	-	-	EVENTOUT
	PZ3	I2C8_SDA	-	LPTIM4_CH2	I3C4_SDA	-	-	-	EVENTOUT
	PZ4	I2C8_SCL	-	-	I3C4_SCL	-	-	-	EVENTOUT
	PZ5	-	-	LPTIM4_CH2	-	-	-	-	EVENTOUT
	PZ6	-	-	LPTIM4_CH2	-	-	-	-	EVENTOUT
	PZ7	-	-	LPTIM3_CH2	-	-	-	-	EVENTOUT
	PZ8	I2C8_SMBA	LPTIM5_ETR	-	-	-	-	-	EVENTOUT
	PZ9	I2C8_SDA	-	LPTIM3_CH2	I3C4_SDA	-	-	-	EVENTOUT

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5 Memory mapping

Refer to the product line reference manual (RM0457) for details on the memory mapping as well as the boundary addresses for all peripherals.

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6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of junction temperature, supply voltage and frequencies by tests in production on 100% of the devices with an junction temperature at T_J = 25 ° C and T_J = T_{Jmax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_J = 25 °C, V_{DD} = 3.3 V, V_{DDCORE} = 0.82 V, V_{DDCPU} = 0.8 V, V_{DDGPU} = 0.8 V. They are given only as design guidelines and are not tested in production.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure 9 .

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in Figure 10 .

Figure 9. Pin loading conditions

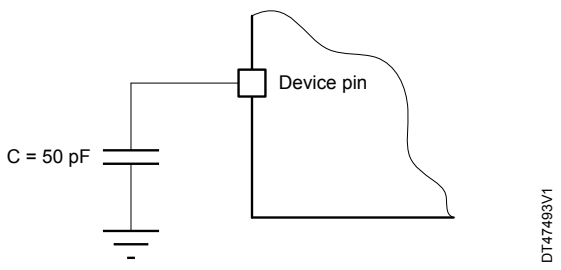
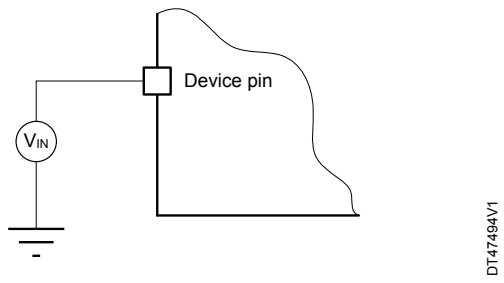


Figure 10. Pin input voltage



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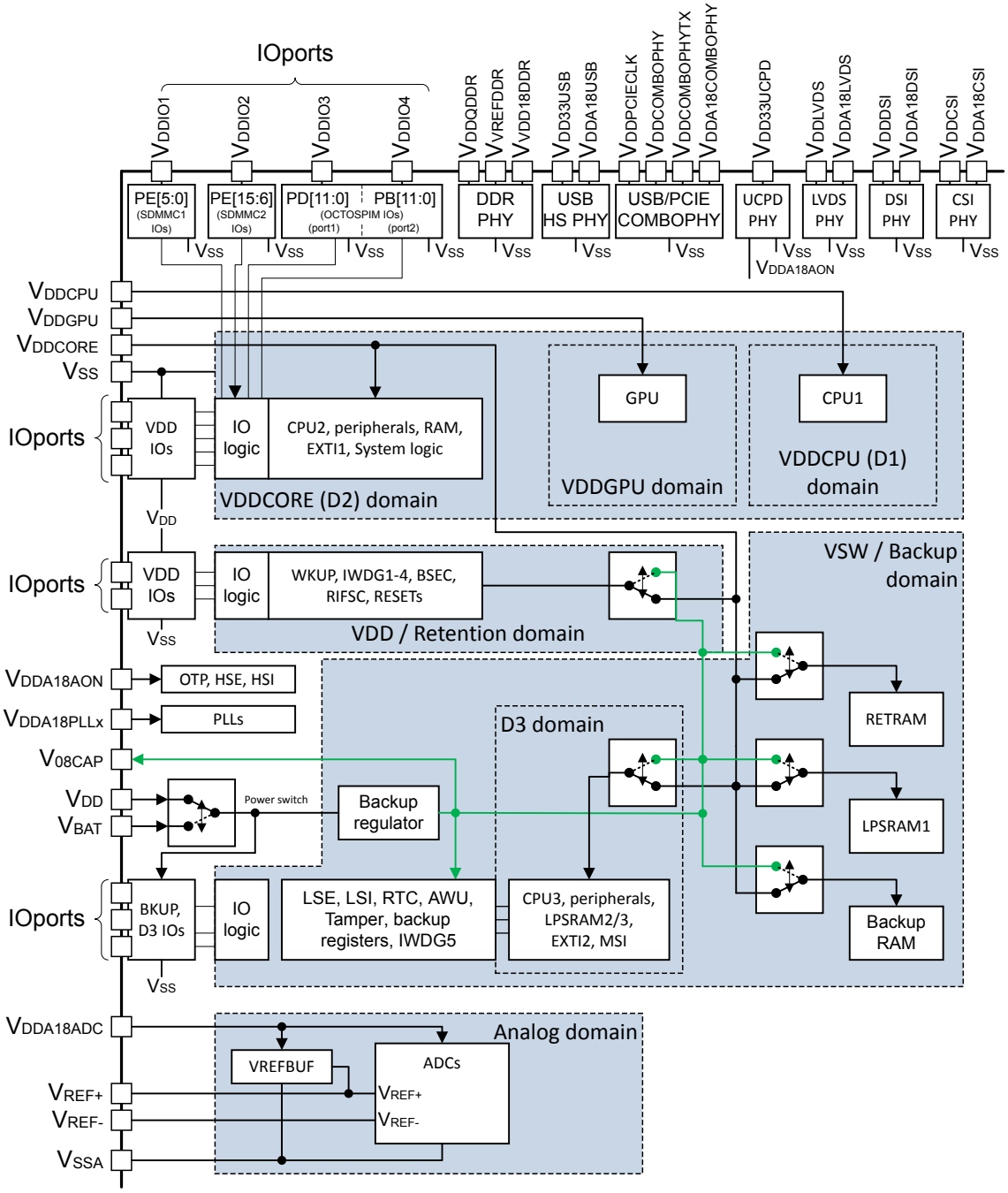
6.1.6 Power supply scheme

Figure 11. Power supply scheme



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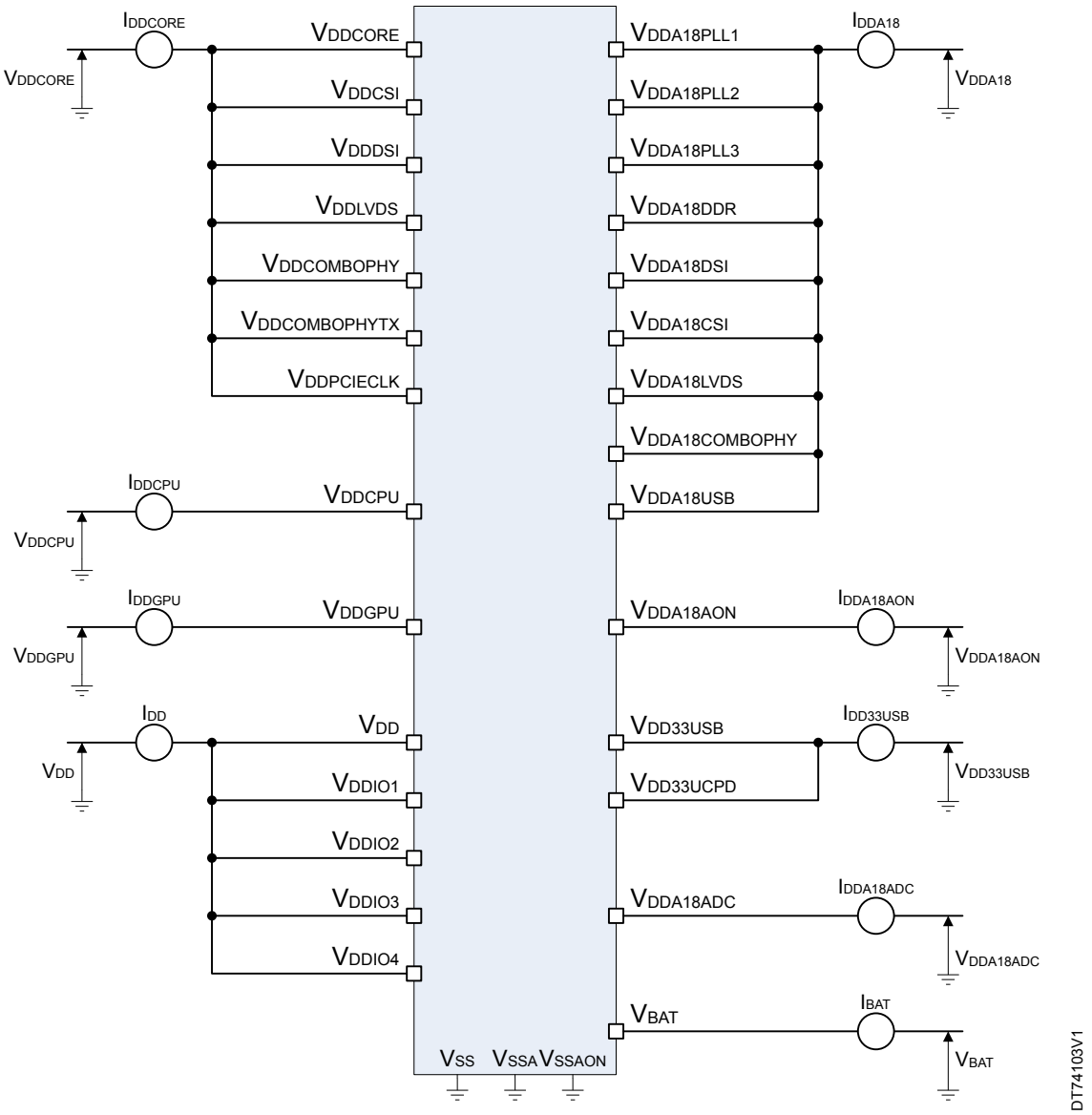
Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDCORE}/V_{SS}, V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

The number of needed capacitances and their values are provided in AN5489 "Getting started with STM32MP25x lines hardware development" available from the ST website www.st.com.

6.1.7 Current consumption measurement

Figure 12. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 14. Voltage characteristics, Table 15. Current characteristics, and Table 16. Thermal characteristics may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 qualification standard, extended mission profiles are available on demand.

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Table 14. Voltage characteristics

Specified by design, not tested in production.
All powers and grounds pins must always be connected to an external power supply, in the permitted range.

Symbols	Ratings	Min	Max	Unit
V_{DDX} - V_{SS} range 1.8 V	External supply voltage (including V_{DD}, V_{DDIOx}, V_{BAT})	-0.3	2	V
V_{DDX} - V_{SS} range 3.3 V	External supply voltage (including V_{DD}, V_{DDIOx}, V_{BAT}, $V_{DD33USB}$, $V_{DD33UCPD}$)	-0.3	3.7	
V_{DDCORE} – V_{SS}	External core supply voltage (including V_{DDCORE}, V_{DDCPU}, V_{DDGPU}, V_{DDCSI}, V_{DDDSI}, V_{DDLVDS}, $V_{DDCOMBOPHY}$, $V_{DDCOMBOPHYTX}$, $V_{DDPCIECLK}$)	-0.3	0.99	
V_{DDQDDR} – V_{SS}	DDR IO supply voltage	-0.3	1.575	
V_{DDA18} – V_{SS}	1.8 V supply voltage (including $V_{DDA18AON}$, $V_{DDA18PLL1}$, $V_{DDA18PLL2}$, $V_{DDA18PLL3}$, $V_{DDA18DSI}$, $V_{DDA18CSI}$, $V_{DDA18LVDS}$, $V_{DDA18COMBOPHY}$, $V_{DDA18DDR}$, $V_{DDA18USB}$, $V_{DDA18ADC}$)	-0.3	1.98	
V_{IN}	Input voltage on TT_xx pins (VDDIOxVRSEL = 0)	V_{SS} - 0.3	3.6	
	Input voltage on TT_xx pins (VDDIOxVRSEL = 1)		1.98	
	Input voltage on UCPD pins		V_{DD3V3_UCPD} + 1.935	
$\lvert\Delta V_{DDx}\rvert$	Variations between different VDDX power pins of the same domain	-	50	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins	-	50	

1. *V_{IN} maximum must always be respected. Refer to next table for the maximum allowed injected current values.*

Table 15. Current characteristics

Specified by design, not tested in production.

Symbols	Ratings	Condition	Max	Unit
I_{IO}	Output current sunk/source by any I/O and control pin	T_J > 110 °C	4	mA
		90 °C < T_J ≤ 110 °C	10	
		-40 °C < T_J ≤ 90 °C	20	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/Os and control pins)		±25	

1. *When several inputs are submitted to a current injection, the maximum ∑IINJ(PIN) is the absolute sum of the positive and negative injected currents (instantaneous values).*

Table 16. Thermal characteristics

Specified by design, not tested in production.

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature (suffix 3)	125	

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6.3 Operating conditions

6.3.1 General operating conditions

Table 17. General operating conditions

Voltages in this table represent DC value at ball level.

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
F_{cpu1}	Clock frequency of Cortex-A35		0	-	1200	MHz
$F_{cpu1_overdrive}$[1]	Clock frequency of Cortex-A35 in overdrive	STM32MP25xF only	0	-	1500	MHz
F_{gpu}[1]	Clock frequency of GPU/NPU		0	-	800	MHz
$F_{gpu_overdrive}$[1]	Clock frequency of GPU/NPU in overdrive	STM32MP25xF only	0	-	900	MHz
$F_{ddrctrl}$	Clock frequency of DDR memory[2]	DDR3L DLL ON	300	-	1066	MHz
		DDR3L DLL OFF	0	-	125	MHz
		DDR4 DLL ON	625	-	1200	MHz
		DDR4 DLL OFF	20	-	125	MHz
		LPDDR4	10	-	1200	MHz
$F_{ck_icn_hs_mcu}$	Clock frequency of Cortex-M33, MCU MLAHB memory		0	-	400	MHz
$F_{ck_icn_m_gpu}$[1]	Clock frequency of GPU/NPU bus		0	-	600	MHz
$F_{ck_icn_ddr}$	Clock frequency of Cortex-A35 AXI buses, DDRCTRL AXI buses		0	-	600	MHz
$F_{ck_icn_hsl}$	Clock frequency of PCIE, USB3DR, USBH, ETH1, ETH2 buses		0	-	300	MHz
$F_{ck_icn_ls_mcu}$	Clock frequency of MCU MLAHB, Cortex-M0+, MCU and SmartRun domain peripherals buses	In Run mode	0	-	200	MHz
	Clock frequency of Cortex-M0+ and SmartRun domain peripherals buses	In D3 autonomous mode	0	-	16	MHz
$F_{ck_icn_sdmmc}$	Clock frequency of MPU AHB5		0	-	200	MHz
$F_{ck_icn_nic}$	Clock frequency of MPU GIC and BOOTROM		0	-	400	MHz
$F_{ck_icn_vid}$[1]	Clock frequency of MPU VDEC and VENC bus		0	-	600	MHz
$V_{DDA18AON}$[3]	Internal analog supply voltage		1.71	1.8	1.89[4]	V
V_{DD}[3]	I/Os supply voltage	1.8 V range	1.71	1.8	1.89[4]	V
		3.3 V range[5]	3	3.3	3.6	V
V_{DDIO1}, V_{DDIO2}, V_{DDIO3}, V_{DDIO4}[6]	Specific I/Os supply voltage	1.8 V range	1.71	1.8	1.89[4]	V
		3 V / 3.3 V range[7] .	2.7	3.3	3.6	V
V_{DDCORE}, V_{DDCSI}, V_{DDDSI}, V_{DDLVDS}, $V_{DDCOMBOPHY}$, $V_{DDCOMBOPHYTX}$, $V_{DDPCIECLK}$[8]	Main digital logic supply voltage	Run1/2 mode	0.79	0.82	0.842	V
		Stop1/2, LP-Stop1/2 mode	0.79	0.82	0.842	V
		LPLV-Stop1/2 mode	0.64	0.67	0.842[9]	V
		Standby1/2 mode	0	0	0.48	V

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Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
V_{DDCPU}	Cortex-A35 supply voltage	Run1, Stop1 or LP-Stop1 mode, $F_{cpu1_overdrive}$ range[1]	0.87	0.91	0.935	V
		Run1, Stop1 or LP-Stop1 mode, F_{cpu1} range	0.765	0.8	0.842	V
		LPLV-Stop1 (LPCFG_D1 = 0)	0.64	0.67	0.842[9]	V
		Run2, Stop2, LP-Stop2 , LPLV-Stop2 or Standby1/2 mode	0	0	0.48	V
V_{DDGPU}[1]	GPU supply voltage	$F_{gpu1_overdrive}$ range	0.86	0.9	0.961	V
		F_{gpu1} range	0.76	0.8	0.839	V
$V_{DDA18PLL1}$, $V_{DDA18PLL2}$, $V_{DDA18PLL3}$, $V_{DDA18DSI}$, $V_{DDA18CSI}$, $V_{DDA18LVDS}$, $V_{DDA18COMBOPHY}$[8][10]	1.8 V analog supply for PLLs, DSI/CSI/LVDS PHYs and COMBOPHY		1.71	1.8	1.89[4]	V
$V_{DDA18DDR}$[11]	1.8 V analog supply for DDRPHY		1.71	1.8	1.89	V
$V_{DDA18USB}$[11]	1.8 V analog supply for USBPHY		1.75	1.8	1.89[4]	V
$V_{DD33USB}$, $V_{DD33UCPD}$	3.3V USB supply		3.07	3.3	3.6	V
$V_{DDA18ADC}$	ADC operating voltage		1.62	1.8	1.89[4]	V
V_{REF+}	ADC reference voltage		1.1	-	$V_{DDA18ADC}$	V
V_{BAT}	Backup operating voltage		2.3[12]	-	3.6	V
V_{DDQDDR}	DDR PHY supply voltage[2]	DDR3L memory	1.283	1.35	1.45	V
		DDR4 memory	1.14	1.2	1.26	
		LPDDR4 memory	1.06	1.1	1.17	
V_{08CAP}	Backup regulator output voltage[13]		0.72	0.8	0.88	V
VIN	I/O Input voltage	I/O	-0.3	-	V_{DDxx} + 0.3 [14]	V
		I/O when ADC is used			$V_{DDA18ADC}$ + 0.3	
		ANA0/ANA1				
		I/O when PVD_IN is used			$V_{DDA18AON}$ + 0.3	
		UCPD IOs			V_{DD3V3_UCPD} + 1.935	
		DDR I/O			V_{DDQDDR}	
T_J	Junction temperature range	Suffix 3 version	-40	-	125	° C

1. *Feature might be limited or absent in some devices or packages. See Table 1 for details.*
2. *Values depend on the external memory device choice.*
3. *$V_{DDA18AON}$ and V_{DD} must be present before any other supply.*

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4. *Static condition. 1.98 V allowed during transients.*
5. *Requires $V_{DDIOVRSEL}$ = 0.*
6. *These supplies are independent, that means each one could be in any of the following voltage ranges: 0 V (OFF), 1.8 V, 3 V or 3.3 V.*
7. *Requires $V_{DDIOxVRSEL}$ = 0*
8. *All these supplies are usually connected together.*
9. *This is the max allowed voltage, however LPLV-Stop mode is relevant only to save power, so requires voltage as low as possible (that is external regulator set for typical value, then the maximum voltage is few percent above the typical due to regulator accuracy).*
10. *The $V_{DDA18PLLx}$ must be connected together.*
11. *Could be connected to other $V_{DDA18xx}$ supplies if min/max range fullfilled.*
12. *Except when connected to V_{DD} where lower limit is then 1.71 V.*
13. *This pin is used only to connect a decoupling capacitor for internal backup regulator, this pin must never be used externally for other purposes.*
14. *V_{DDxx} stands for V_{DD}, V_{DDIO1}, V_{DDIO2}, V_{DDIO3} or V_{DDIO4}.*

6.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions.

Table 18. Operating conditions at power-up / power-down

$V_{DDA18AON}$ and V_{DD} must be present before other supplies.

Symbol	Parameter	Operating conditions	Min	Max	Unit
$t_{VDDA18AON}$[1]	$V_{DDA18AON}$ transitions	Rise time rate	20	1500	µs/V
		Fall time rate	20	1500	
t_{VDD}[1]	$V_{DD/VDDIOx}$ transitions	Rise time rate	20	1500	
		Fall time rate	20	1500	
$t_{VDDCORE}$	V_{DDCORE} transitions	Rise time rate	20	1500	
		Fall time rate	25	1500	
t_{VDDCPU}, t_{VDDGPU}, t_{VDDCSI}, t_{VDDSI}, $t_{VDDLVDS}$, $t_{VDDCOMBOPHY}$, $t_{VDDCOMBOPHYTX}$, $t_{VDDPCIECLK}$	V_{DDCPU}, V_{DDGPU}, V_{DDCSI}, V_{DDDSI}, V_{DDLVDS}, $V_{DDCOMBOPHY}$, $V_{DDCOMBOPHYTX}$, $V_{DDPCIECLK}$ transitions	Rise time rate	10	1500	
		Fall time rate	10	1500	
t_{VDDA18}	$V_{DDA18PLL1}$, $V_{DDA18PLL2}$, $V_{DDA18PLL3}$, $V_{DDA18DSI}$, $V_{DDA18CSI}$, $V_{DDA18LVDS}$, $V_{DDA18COMBOPHY}$, $V_{DDA18DDR}$, $V_{DDA18USB}$, $V_{DDA18ADC}$ transitions	Rise time rate	10	1500	
		Fall time rate	10	1500	
t_{VDD33}	$V_{DD33USB}$, $V_{DD33UCPD}$ transitions	Rise time rate	10	1500	
		Fall time rate	10	1500	
$t_{VDDQDDR}$	V_{DDQDDR} transitions	Rise time rate	10	1500	
		Fall time rate	10	1500	
t_{VBAT}	V_{BAT} transitions	Rise time rate	20	∞	
		Fall time rate	10	1500	

1. *$V_{DDA18AON}$ and V_{DD} must be present before any other supply.*

6.3.3 Embedded reset and power control block characteristics

The parameters given in Table 19 are derived from tests performed under ambient temperature and supply voltage conditions summarized in Table 17. General operating conditions.

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Table 19. Embedded reset and power control block characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Paramete	Conditions		Min	Typ	Max	Unit
$t_{RSTTEMPO}$	Reset temporization	After POR released		200	-	500	µs
$V_{DDA18AON}$ thresholds							
V_{POR_ANA}[1]	Power-on reset threshold	Rising edge		1.62	1.67	1.71	V
V_{PDR_ANA}[1]	Power-down reset threshold	Falling edge		1.58	1.63	1.67	
$V_{hyst_POR_ANA}$	Hysteresis voltage of POR/PDR	-		-	41.5	-	mV
$I_{POR_PDR(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	Always ON		-	1.25	-	µA
V_{DD} thresholds							
V_{POR}[1]	Power-on reset threshold	Rising edge		1.62	1.67	1.71	V
V_{PDR}[1]	Power-down reset threshold	Falling edge		1.58	1.63	1.67	
V_{hyst_POR}	Hysteresis voltage of POR/PDR	-		-	41.5	-	mV
$I_{POR_PDR(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	Always ON		-	0.75	-	µA
$I_{POR_PDR(VDD)}$	Supply current on V_{DD}	Always ON	V_{DD} = 1.8 V	-	0.5	-	µA
			V_{DD} = 3.3 V	-	0.92	-	
V_{BOR0}[1]	Brown-out reset threshold 0	Rising edge		1.62	1.67	1.71	V
		Falling edge		1.58	1.63	1.67	
V_{BOR1}[1]	Brown-out reset threshold 1	Falling edge		2.62	2.66	2.97	V
V_{hyst_BOR0}	Hysteresis voltage of BOR0	-		-	40	-	mV
V_{hyst_BOR1}	Hysteresis voltage of BOR1	-		-	115	-	mV
$I_{BOR(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	BOR enabled in OTP		-	0.75	-	µA
V_{DDCPU} thresholds							
V_{RDY_VDDCPU}[1]	Threshold on rising edge	Normal modes		0.61	0.66	0.71	V
		LPLV modes		0.5	0.55	0.61	
V_{hyst_VDDCPU}	Hysteresis on falling edge	-		-	26.5	-	mV
T_{delay_VDDCPU}	Delay after detection	Rising edge		190	340	510	µs
		Falling edge		-	0	-	
$I_{RDY_VDDCPU(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	Always ON		-	1.2	-	µA
V_{DDCORE} thresholds							
$V_{RDY_VDDCORE}$[1]	Threshold on rising edge	Normal modes		0.61	0.66	0.71	V
		LPLV modes		0.5	0.55	0.61	
$V_{hyst_VDDCORE}$	Hysteresis on falling edge	-		-	20	-	mV
$T_{delay_VDDCORE}$	Delay after detection	Rising edge		190	340	510	µs
		Falling edge		-	0	-	
$I_{RDY_VDDCORE(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	Always ON		-	1.2	-	µA

1. *Guaranteed by test in production.*

6.3.4 Embedded reference voltage

The parameters given in Table 20 and Table 21 are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 17. General operating conditions .

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Table 20. Embedded reference voltage characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}[1]	Internal reference voltages	-40 °C < T_J < 125 °C	0.792	0.8	0.808	V
$t_{S_VREFINT}$[2]	ADC sampling time when reading the internal reference voltage	-	34	-	-	ns
DV_{REFINT}	Internal reference voltage spread over the temperature range	-40 °C < T_J < 125 °C	-	TBD	TBD	mV
T_{coeff}	Average temperature coefficient	Average temperature coefficient	-	TBD	TBD	ppm/°C
A_{coeff}	Long term stability	1000 hours, T_J = 25 °C	-	-	TBD	ppm/°C
$V_{DDcoeff}$	Average voltage coefficient	XXV < V_{DDX} < XXV	-	TBD	TBD	ppm/V

1. *Guaranteed by test in production.*
2. *Specified by design, not tested in production.*

Table 21. Embedded reference voltage calibration value

Symbol	Parameter	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C, $V_{DDA18ADC}$ = V_{REF+} = 1.8 V	0x4400 01B8[11:0][1][2]

1. *This address is located inside BSEC which must be enabled in RCC to allow access.*
2. *Must be read in 32-bit words and relevant masking and shifting must be performed to isolate the required bits.*

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in Figure 12. Current consumption measurement scheme.

All the Run mode current consumption measurements given in this section are performed with a CoreMark code unless otherwise specified.

Supply current characteristics are evaluated by characterization, not tested in production unless otherwise specified.

6.3.5.1 Typical and maximum current consumption

The device is placed under the following conditions:

- All I/O pins are in analog input mode except when explicitly mentioned
- All peripherals are disabled except when explicitly mentioned
- RTC/LSE are disabled, unless otherwise specified
- BKPSRAM, RETRAM, LPSRAM1 backup supplies in low-power modes (such as LPLV-Stop, Standby and VBAT modes) are disabled, unless otherwise specified

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- Unless otherwise specified, the typical values are obtained for:
  - V_{DD} / V_{DDIOx}/V_{BAT} = 3.3 V
  - V_{DDCORE} = 0.82 V
  - V_{DDCPU} = 0.8 V
  - V_{DDGPU} = 0.8 V
  - V_{DDA18} / $V_{DDA18AON}$ = 1.8 V
    and the maximum values are obtained for:
  - V_{DD} / V_{DDIOx} / V_{BAT} = 3.6 V
  - V_{DDCORE} = 0.842 V
  - V_{DDCPU} = 0.842 V
  - V_{DDGPU} = 0.839 V
  - V_{DDA18} / $V_{DDA18AON}$ = 1.89 V

The parameters given in Table 22 to Table 34 are derived from tests performed under supply voltage conditions summarized in Table 17. General operating conditions .

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Table 22. Current consumption (I_{DDCORE}) in Run modes

Evaluated by characterization, not tested in production unless otherwise specified.
Except otherwise noted, typical values given with V_{DDCORE} = 0.82 V, V_{DDCPU} = 0.8 V and V_{DDGPU} = 0.8 V, maximum values given with V_{DDCORE} = 0.842 V, V_{DDCPU} = 0.842 V and V_{DDGPU} = 0.839 V.

Symbol	Parameter	Conditions										Typ	Max				Unit
		-	D1 (CPU1)[1] mode	D2 (CPU2) mode	D3 (CPU3) mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) [2]	CPU2 clk (MHz)	CPU3 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCORE}[3]	Supply current in Run mode	All peripherals Enabled[4]	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[5]	600	400	200	900[6]	235	300	530	740	960	mA
							1200	600	400	200	800	235	300	530	720	950	
							750	600	400	200	800	235	300	530	700	950	
							600	600	400	200	800	235	300	530	700	950	
I_{DDCORE}[7]	Supply current in Run mode	All peripherals Enabled[4]	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[5]	600	400	200	900[6]	180	240	470	650	890	mA
							1200	600	400	200	800	180	240	470	640	890	
							750	600	400	200	800	180	240	470	640	890	
							600	600	400	200	800	180	240	470	640	890	
I_{DDCORE}[8]	Supply current in Run mode	All peripherals Enabled[4]	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[5]	600	400	200	-	180	240	470	640	890	mA
							1200	600	400	200	-	180	240	470	640	880	
							750	600	400	200	-	180	240	470	640	880	
							600	600	400	200	-	180	240	470	640	880	
I_{DDCORE}[9]	Supply current in Run mode	All peripherals Enabled[4]	DRun (CRun: P0)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[5]	600	400	200	-	175	240	460	630	880	mA
							1200	600	400	200	-	175	240	460	630	880	
							750	600	400	200	-	175	240	460	630	870	
							600	600	400	200	-	175	240	460	630	870	
I_{DDCORE}[3]	Supply current in Run mode	All peripherals Enabled[4]	DRun (CRun: P0&P1)	Run1 (Cstop)	SRun1 (CStop)	HSE + HSI + PLL	1500[5]	600	-	-	900[6]	210	280	500	670	930	mA
							1200	600	-	-	800	210	280	500	670	920	
							750	600	-	-	800	210	280	500	670	920	
							600	600	-	-	800	210	280	500	670	920	
I_{DDCORE}[7]	Supply current in Run mode	All peripherals Enabled[4]	DRun (CRun: P0&P1)	Run1 (Cstop)	SRun1 (CStop)	HSE + HSI + PLL	1500[5]	600	-	-	900[6]	160	220	440	620	860	mA
							1200	600	-	-	800	155	220	440	610	860	
							750	600	-	-	800	155	220	440	620	860	

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Symbol	Parameter	Conditions										Typ	Max				Unit
		-	D1 (CPU1)[1] mode	D2 (CPU2) mode	D3 (CPU3) mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) [2]	CPU2 clk (MHz)	CPU3 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCORE}[7]	Supply current in Run mode	All peripherals Enabled[4]	DRun (CRun: P0&P1)	Run1 (Cstop)	SRun1 (CStop)	HSE + HSI + PLL	600	600	-	-	800	155	220	440	610	860	mA
I_{DDCORE}[8]	Supply current in Run mode	All peripherals Enabled[4]	DRun (CRun: P0&P1)	Run1 (Cstop)	SRun1 (CStop)	HSE + HSI + PLL	1500[5]	600	-	-	-	155	220	440	610	860	mA
							1200	600	-	-	-	155	220	440	610	850	
							750	600	-	-	-	155	220	440	610	850	
							600	600	-	-	-	155	220	440	610	850	
I_{DDCORE}[9]	Supply current in Run mode	All peripherals Enabled[4]	DRun (CRun: P0)	Run1 (Cstop)	SRun1 (CStop)	HSE + HSI + PLL	1500[5]	600	-	-	-	150	210	430	600	850	mA
							1200	600	-	-	-	150	210	430	600	850	
							750	600	-	-	-	150	210	430	600	840	
							600	600	-	-	-	150	210	430	600	840	
I_{DDCORE}[10]	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[5]	600	400	200	900[6]	89	140	360	530	780	mA
							1200	600	400	200	800	88.5	140	360	530	780	
							750	600	400	200	800	88.5	140	360	530	780	
							600	600	400	200	800	88.5	140	360	530	780	
I_{DDCORE}[11]	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[5]	600	400	200	-	89	140	360	530	780	mA
							1200	600	400	200	-	88.5	140	360	530	770	
							750	600	400	200	-	88.5	140	360	530	770	
							600	600	400	200	-	88.5	140	360	530	770	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[5]	600	400	200	-	89	140	360	530	780	mA
							1200	600	400	200	-	88.5	140	360	530	770	
							750	600	400	200	-	88.5	140	360	530	770	
							600	600	400	200	-	88.5	140	360	530	770	
I_{DDCORE}[11]	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (Cstop)	SRun1 (CStop)	HSE + HSI + PLL	1500[5]	600	-	-	-	42.5	85	310	480	720	mA
							1200	600	-	-	-	42	84	310	470	720	
							750	600	-	-	-	42	84	310	470	720	
							600	600	-	-	-	42	84	310	470	720	
							300	300	-	-	-	37	79	300	470	710	

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Symbol	Parameter	Conditions										Typ	Max				Unit
		-	D1 (CPU1)[1] mode	D2 (CPU2) mode	D3 (CPU3) mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) [2]	CPU2 clk (MHz)	CPU3 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCORE}[11]	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (Cstop)	SRun1 (CStop)	HSE + HSI + PLL	150	150	-	-	-	35	76	300	460	710	mA
						HSI	HSI 64	HSI 64	-	-	-	30.5	71	290	460	700	
						HSE + HSI	HSE 40	HSE 40	-	-	-	29	70	290	460	700	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0)	Run1 (Cstop)	SRun1 (CStop)	HSE + HSI + PLL	1500[5]	600	-	-	-	42.5	85	310	470	720	mA
							1200	600	-	-	-	42	84	310	470	720	
							750	600	-	-	-	42	84	310	470	720	
							600	600	-	-	-	42	84	310	470	720	
							300	300	-	-	-	37	79	300	470	710	
							150	150	-	-	-	35	76	300	460	710	
						HSI	HSI 64	HSI 64	-	-	-	30.5	71	290	460	700	
						HSE + HSI	HSE 40	HSE 40	-	-	-	29	70	290	460	700	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DStop1 (CStop)	Run1 (CRun)	SRun1 (CStop)	HSE + HSI + PLL	-	HSI 64	400	-	-	76	130	350	510	760	mA
							-	HSI 64	200	-	-	50	93	320	480	730	
							-	HSI 64	100	-	-	37	79	300	470	710	
						HSI	-	HSI 64	HSI 64	-	-	32.5	74	300	460	710	
						HSE + HSI	-	HSI 64	HSE 40	-	-	28.5	69	290	460	700	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DStandby[12] [13] (CStandby)	Run2 (CRun)	SRun1 (CStop)	HSE + HSI + PLL	-	HSI 64	400	-	-	76	130	340	510	760	mA
							-	HSI 64	200	-	-	50	93	310	480	730	
							-	HSI 64	100	-	-	37	79	300	470	710	
						HSI	-	HSI 64	HSI 64	-	-	32.5	74	290	460	700	
						HSE + HSI	-	HSI 64	HSE 40	-	-	28.5	69	290	460	700	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DStandby (CStandby)[12] [13]	Run2 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	-	HSI 64	400	200	-	77.5	130	350	510	760	mA
							-	HSI 64	200	100	-	51	94	320	480	730	

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Symbol	Parameter	Conditions										Typ	Max				Unit
		-	D1 (CPU1)[1] mode	D2 (CPU2) mode	D3 (CPU3) mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) [2]	CPU2 clk (MHz)	CPU3 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DStandby (CStandby)[12] [13]	Run2 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	-	HSI 64	100	50	-	37.5	79	300	470	710	mA
						HSI	-	HSI 64	HSI 64	HSI 64	-	33.5	75	300	460	710	
						HSE + HSI	-	HSI 64	HSE 40	HSE 40	-	29	70	290	460	700	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DRun (CSleep)	Run1 (Cstop)	SRun1 (CStop)	HSE + HSI + PLL	1500[5]	600	-	-	-	42	84	310	470	720	mA
							1200	600	-	-	-	42	84	310	470	720	
							750	600	-	-	-	42	84	310	470	720	
							600	600	-	-	-	42	84	310	470	720	
							300	300	-	-	-	37	79	300	470	710	
							150	150	-	-	-	35	76	300	460	710	
						HSI	HSI 64	HSI 64	-	-	-	30.5	71	290	460	700	
						HSE + HSI	HSE 40	HSE 40	-	-	-	29	70	290	460	700	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DRun[14] (eCSleep)	Run1 (Cstop)	SRun1 (CStop)	HSE + HSI + PLL	1500[5]	600	-	-	-	TBD	TBD	TBD	TBD	TBD	mA
							1200	600	-	-	-	TBD	TBD	TBD	TBD	TBD	
							750	600	-	-	-	TBD	TBD	TBD	TBD	TBD	
							600	600	-	-	-	TBD	TBD	TBD	TBD	TBD	
							300	300	-	-	-	TBD	TBD	TBD	TBD	TBD	
							150	150	-	-	-	TBD	TBD	TBD	TBD	TBD	
						HSI	HSI 64	HSI 64	-	-	-	TBD	TBD	TBD	TBD	TBD	
						HSE + HSI	HSE 40	HSE 40	-	-	-	TBD	TBD	TBD	TBD	TBD	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DStop1 (CStop)	Run1 (CSleep)	SRun1 (CStop)	HSE + HSI + PLL	-	HSI 64	400	-	-	57	110	320	490	730	mA
							-	HSI 64	200	-	-	40.5	83	300	470	720	
							-	HSI 64	100	-	-	32.5	74	290	460	710	
						HSI	-	HSI 64	HSI 64	-	-	29.5	71	290	460	700	

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Symbol	Parameter	Conditions										Typ	Max				Unit
		-	D1 (CPU1)(1) mode	D2 (CPU2) mode	D3 (CPU3) mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) (2)	CPU2 clk (MHz)	CPU3 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DStop1 (CStop)	Run1 (CSleep)	SRun1 (CStop)	HSE + HSI	-	HSI 64	HSE 40	-	-	26.5	67	290	450	700	mA
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DStandby (CStandby)(12) (13)	Run2 (CSleep)	SRun1 (CStop)	HSE + HSI + PLL	-	HSI 64	400	-	-	57	100	320	490	730	mA
							-	HSI 64	200	-	-	40.5	83	300	470	710	
							-	HSI 64	100	-	-	32.5	73	290	460	700	
						HSI	-	HSI 64	HSI 64	-	-	29.5	70	290	460	700	
						HSE + HSI	-	HSI 64	HSE 40	-	-	26.5	67	290	450	700	

1. *P0 and P1 are state of cores inside CPU1 when in CRun state. 'P0&P1' indicate that both cores are executing a test software. 'P0' indicate that only P0 is executing a test software while other core is clock gated (either in WFI or WFE or not present in the device).*
2. *ck_icn_ddr.*
3. *Values for STM32MP257x.*
4. *Activity on peripherals and bus masters other than processors, could lead to additional power consumption above these values, largely dependent on the amount of initialized peripherals and their activity.*
5. *Typical value given with V_{DDCPU} = 0.91 V, maximum values given with V_{DDCPU} = 0.935 V.*
6. *Typical value given with V_{DDGPU} = 0.9 V, maximum values given with V_{DDGPU} = 0.961 V.*
7. *Values for STM32MP255x.*
8. *Values for STM32MP253x.*
9. *Values for STM32MP251x.*
10. *Values for STM32MP257x and STM32MP255x.*
11. *Not relevant for STM32MP251x.*
12. *CStandby = CStop and PDDS_D1 = 1.*
13. *V_{DDCPU} is shutdown..*
14. *eCSleep mean CPU1 in enhanced CSleep with PLL1 automatically stopped (RCC_C1SREQSETR.ESLPREQ=1).*

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Table 23. Current consumption (I_{DDCPU}) in Run modes

Evaluated by characterization, not tested in production unless otherwise specified.
Except otherwise noted, typical values given with V_{DDCORE} = 0.82 V, V_{DDCPU} = 0.8 V and V_{DDGPU} = 0.8 V, maximum values given with V_{DDCORE} = 0.842 V, V_{DDCPU} = 0.842 V and V_{DDGPU} = 0.839 V.

Symbol	Parameter	Conditions										Typ	Max				Unit
		-	D1 (CPU1) (1) mode	D2 (CPU2) mode	D3 (CPU3) mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) (2)	CPU2 clk (MHz)	CPU3 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCPU}(3)	Supply current in Run mode	All peripherals Enabled(4)	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500(5)	600	400	200	900(6)	245	290	360	430	520	mA
							1200	600	400	200	800	165	200	280	360	420	
							750	600	400	200	800	105	130	200	260	340	
							600	600	400	200	800	84	110	180	230	320	
I_{DDCPU}(7)	Supply current in Run mode	All peripherals Enabled(4)	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500(5)	600	400	200	900(6)	245	290	360	430	520	mA
							1200	600	400	200	800	165	200	280	330	420	
							750	600	400	200	800	105	130	200	260	340	
							600	600	400	200	800	84	110	180	230	320	
I_{DDCPU}(8)	Supply current in Run mode	All peripherals Enabled(4)	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500(5)	600	400	200	-	245	290	360	430	520	mA
							1200	600	400	200	-	165	200	280	330	420	
							750	600	400	200	-	105	130	200	260	340	
							600	600	400	200	-	84	110	180	230	320	
I_{DDCPU}(9)	Supply current in Run mode	All peripherals Enabled(4)	DRun (CRun: P0)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500(5)	600	400	200	-	130	160	230	290	380	mA
							1200	600	400	200	-	89	120	180	240	320	
							750	600	400	200	-	56.5	75	150	200	280	
							600	600	400	200	-	46	62	130	190	270	
I_{DDCPU}(3)	Supply current in Run mode	All peripherals Enabled(4)	DRun (CRun: P0&P1)	Run1 (Cstop)	SRun1 (CStop)	HSE + HSI + PLL	1500(5)	600	-	-	900(6)	245	290	360	470	520	mA
							1200	600	-	-	800	165	200	280	330	420	
							750	600	-	-	800	105	130	200	260	340	
							600	600	-	-	800	84	110	180	230	320	
I_{DDCPU}(7)	Supply current in Run mode	All peripherals Enabled(4)	DRun (CRun: P0&P1)	Run1 (Cstop)	SRun1 (CStop)	HSE + HSI + PLL	1500(5)	600	-	-	900(6)	245	290	360	470	520	mA
							1200	600	-	-	800	165	200	280	330	420	
							750	600	-	-	800	105	130	200	260	340	
							600	600	-	-	800	84	110	180	230	320	

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Symbol	Parameter	Conditions										Typ	Max				Unit
		-	D1 (CPU1) [1] mode	D2 (CPU2) mode	D3 (CPU3) mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) [2]	CPU2 clk (MHz)	CPU3 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCPU}[8]	Supply current in Run mode	All peripherals Enabled[4]	DRun (CRun: P0&P1)	Run1 (Cstop)	SRun1 (CStop)	HSE + HSI + PLL	1500[5]	600	-	-	-	245	290	360	430	520	mA
							1200	600	-	-	-	165	200	280	330	420	
							750	600	-	-	-	105	130	200	260	340	
							600	600	-	-	-	84	110	180	230	320	
I_{DDCPU}[9]	Supply current in Run mode	All peripherals Enabled[4]	DRun (CRun: P0)	Run1 (Cstop)	SRun1 (CStop)	HSE + HSI + PLL	1500[5]	600	-	-	-	130	160	230	290	380	mA
							1200	600	-	-	-	89	120	180	240	320	
							750	600	-	-	-	56.5	74	150	200	280	
							600	600	-	-	-	46	62	130	190	270	
I_{DDCPU}[3]	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[5]	600	400	200	900[6]	245	290	360	500	520	mA
							1200	600	400	200	800	165	200	280	360	450	
							750	600	400	200	800	105	130	200	260	340	
							600	600	400	200	800	84	110	180	230	320	
I_{DDCPU}[10]	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[5]	600	400	200	-	245	290	360	430	520	mA
							1200	600	400	200	-	165	200	280	330	420	
							750	600	400	200	-	105	130	200	260	340	
							600	600	400	200	-	84	110	180	230	320	
I_{DDCPU}[9]	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[5]	600	400	200	-	130	160	230	290	380	mA
							1200	600	400	200	-	89	120	180	240	320	
							750	600	400	200	-	56.5	74	150	200	280	
							600	600	400	200	-	46	62	130	190	270	
I_{DDCPU}[10]	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (Cstop)	SRun1 (CStop)	HSE + HSI + PLL	1500[5]	600	-	-	-	245	290	360	470	520	mA
							1200	600	-	-	-	165	200	280	330	420	
							750	600	-	-	-	105	130	200	260	340	
							600	600	-	-	-	84	110	180	230	320	
							300	300	-	-	-	43	58	130	180	270	
							150	150	-	-	-	22.5	35	100	160	240	
						HSI	HSI 64	HSI 64	-	-	-	11	22	86	140	230	

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Symbol	Parameter	Conditions										Typ	Max				Unit
		-	D1 (CPU1) (1) mode	D2 (CPU2) mode	D3 (CPU3) mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) (2)	CPU2 clk (MHz)	CPU3 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCPU} (10)	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (Cstop)	SRun1 (CStop)	HSE + HSI	HSE 40	HSE 40	-	-	-	7.6	18	82	140	220	mA
I_{DDCPU}	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0)	Run1 (Cstop)	SRun1 (CStop)	HSE + HSI + PLL	1500 (5)	600	-	-	-	130	160	230	290	380	mA
							1200	600	-	-	-	89	120	180	240	320	
							750	600	-	-	-	56.5	74	150	200	280	
							600	600	-	-	-	45.5	62	130	190	270	
							300	300	-	-	-	24	37	110	160	240	
							150	150	-	-	-	13	24	89	150	230	
						HSI	HSI 64	HSI 64	-	-	-	6.8	17	81	140	220	
						HSE + HSI	HSE 40	HSE 40	-	-	-	4.95	15	79	140	220	
I_{DDCPU}	Supply current in Run mode	All peripherals Disabled	DStop1 (CStop)	Run1 (CRun)	SRun1 (CStop)	HSE + HSI + PLL	-	HSI 64	400	-	-	2.05	11	75	130	210	mA
							-	HSI 64	200	-	-	2.05	11	75	130	210	
							-	HSI 64	100	-	-	2.05	11	75	130	210	
							-	HSI 64	HSI 64	-	-	2.05	11	75	130	210	
							-	HSI 64	HSE 40	-	-	2.05	11	75	130	210	
I_{DDCPU}	Supply current in Run mode	All peripherals Disabled	DRun (CSleep)	Run1 (Cstop)	SRun1 (CStop)	HSE + HSI + PLL	1500 (5)	600	-	-	-	18.5	30	98	160	260	mA
							1200	600	-	-	-	13	24	89	150	240	
							750	600	-	-	-	8.95	19	84	140	230	
							600	600	-	-	-	7.65	18	82	140	220	
							300	300	-	-	-	4.8	14	79	140	220	
							150	150	-	-	-	3.5	13	77	130	220	
						HSI	HSI 64	HSI 64	-	-	-	2.7	12	76	130	210	
						HSE + HSI	HSE 40	HSE 40	-	-	-	2.45	12	76	130	210	
I_{DDCPU}	Supply current in Run mode	All peripherals Disabled	DRun (11) (eCSleep)	Run1 (Cstop)	SRun1 (CStop)	HSE + HSI + PLL	1500 (5)	600	-	-	-	TBD	TBD	TBD	TBD	TBD	mA
							1200	600	-	-	-	TBD	TBD	TBD	TBD	TBD	
							750	600	-	-	-	TBD	TBD	TBD	TBD	TBD	

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Symbol	Parameter	Conditions										Typ	Max				Unit
		-	D1 (CPU1) (1) mode	D2 (CPU2) mode	D3 (CPU3) mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) (2)	CPU2 clk (MHz)	CPU3 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCPU}	Supply current in Run mode	All peripherals Disabled	DRun(11) (eCSleep)	Run1 (Cstop)	SRun1 (CStop)	HSE + HSI + PLL	600	600	-	-	-	TBD	TBD	TBD	TBD	TBD	mA
							300	300	-	-	-	TBD	TBD	TBD	TBD	TBD	
							150	150	-	-	-	TBD	TBD	TBD	TBD	TBD	
						HSI	HSI 64	HSI 64	-	-	-	TBD	TBD	TBD	TBD	TBD	
						HSE + HSI	HSE 40	HSE 40	-	-	-	TBD	TBD	TBD	TBD	TBD	
I_{DDCPU}	Supply current in Run mode	All peripherals Disabled	DStop1 (CStop)	Run1 (CSleep)	SRun1 (CStop)	HSE + HSI + PLL	-	HSI 64	400	-	-	2.1	11	75	130	210	mA
							-	HSI 64	200	-	-	2.05	11	75	130	210	
							-	HSI 64	100	-	-	2.1	11	75	130	210	
						HSI	-	HSI 64	HSI 64	-	-	2.05	11	75	130	210	
						HSE + HSI	-	HSI 64	HSE 40	-	-	2.05	11	75	130	210	

1. *P0 and P1 are state of cores inside CPU1 when in CRun state. 'P0&P1' indicate that both cores are executing a test software. 'P0' indicate that only P0 is executing a test software while other core is clock gated (either in WFI or WFE or not present in the device).*
2. *ck_icn_ddr.*
3. *Values for STM32MP257x.*
4. *Activity on peripherals and bus masters other than processors, could lead to additional power consumption above these values, largely dependent on the amount of initialized peripherals and their activity.*
5. *Typical value given with V_{DDCPU} = 0.91 V, maximum values given with V_{DDCPU} = 0.935 V.*
6. *Typical value given with V_{DDGPU} = 0.9 V, maximum values given with V_{DDGPU} = 0.961 V.*
7. *Values for STM32MP255x.*
8. *Values for STM32MP253x.*
9. *Values for STM32MP251x.*
10. *Not relevant for STM32MP251x.*
11. *eCSleep mean CPU1 in enhanced CSleep (RCC_C1SREQSETR.ESLPREQ = 1).*

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Table 24. Current consumption (I_{DDGPU}) in Run modes

Evaluated by characterization, not tested in production unless otherwise specified.
Except otherwise noted, typical values given with V_{DDCORE} = 0.82 V, V_{DDCPU} = 0.8 V and V_{DDGPU} = 0.8 V, maximum values given with V_{DDCORE} = 0.842 V, V_{DDCPU} = 0.842 V and V_{DDGPU} = 0.839 V.
Not relevant for STM32MP251x and STM32MP253x.
Value are without GPU activity.

Symbol	Parameter	Conditions										Typ	Max				Unit
		-	D1 (CPU1)[1] mode	D2 (CPU2) mode	D3 (CPU3) mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) [2]	CPU2 clk (MHz)	CPU3 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDGPU}[3]	Supply current in Run mode	All peripherals Enabled[4]	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[5]	600	400	200	900[6]	14.5	43	200	310	480	mA
							1200	600	400	200	800	12.5	38	190	300	450	
							750	600	400	200	800	12.5	38	190	290	450	
							600	600	400	200	800	12.5	38	190	290	450	
I_{DDGPU}[7]	Supply current in Run mode	All peripherals Enabled[4]	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[5]	600	400	200	900[6]	14.5	43	200	310	480	mA
							1200	600	400	200	800	12.5	38	190	290	450	
							750	600	400	200	800	12.5	38	190	290	450	
							600	600	400	200	800	12.5	38	190	290	450	
I_{DDGPU}	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[5]	600	400	200	900[6]	8.1	42	200	310	480	mA
							1200	600	400	200	800	7.45	38	190	290	450	
							750	600	400	200	800	7.4	38	180	290	450	
							600	600	400	200	800	7.4	38	180	290	450	

1. *P0 and P1 are state of cores inside CPU1 when in CRun state. 'P0&P1' indicate that both cores are executing a test software. 'P0' indicate that only P0 is executing a test software while other core is clock gated (either in WFI or WFE or not present in the device).*
2. *ck_icn_ddr.*
3. *Values for STM32MP257x.*
4. *Activity on peripherals and bus masters other than processors, could lead to additional power consumption above these values, largely dependent on the amount of initialized peripherals and their activity.*
5. *Typical value given with V_{DDCPU} = 0.91 V, maximum values given with V_{DDCPU} = 0.935 V.*
6. *Typical value given with V_{DDGPU} = 0.9 V, maximum values given with V_{DDGPU} = 0.961 V.*
7. *Values for STM32MP255x.*

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Table 25. Current consumption (I_{DD}) in Run modes

Evaluated by characterization, not tested in production unless otherwise specified.
Except otherwise noted, typical values given with V_{DDCORE} = 0.82 V, V_{DDCPU} = 0.8 V and V_{DDGPU} = 0.8 V, maximum values given with V_{DDCORE} = 0.842 V, V_{DDCPU} = 0.842 V and V_{DDGPU} = 0.839 V.

Symbol	Parameter	Conditions										Typ	Max				Unit
		-	D1 (CPU1)[1] mode	D2 (CPU2) mode	D3 (CPU3) mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) [2]	CPU2 clk (MHz)	CPU3 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
$I_{DD\ (3V3)}$[3]	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[4]	600	400	200	900[5]	2.6	3.2	3.3	3.7	3.9	mA
							1200	600	400	200	800	2.6	3.2	3.3	3.7	3.9	
							750	600	400	200	800	2.6	3.2	3.3	3.7	3.9	
							600	600	400	200	800	2.6	3.2	3.3	3.7	3.9	
$I_{DD\ (1V8)}$[6]						HSE + HSI + PLL	1500[4]	600	400	200	900[5]	1.25	1.6	1.6	1.7	1.7	mA
							1200	600	400	200	800	1.25	1.6	1.6	1.7	1.7	
							750	600	400	200	800	1.25	1.6	1.6	1.7	1.7	
							600	600	400	200	800	1.25	1.6	1.6	1.7	1.7	
$I_{DD\ (3V3)}$[3]	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[4]	600	400	200	-	2.6	3.2	3.3	3.7	3.9	mA
							1200	600	400	200	-	2.6	3.2	3.3	3.7	3.9	
							750	600	400	200	-	2.6	3.2	3.3	3.7	3.9	
							600	600	400	200	-	2.6	3.2	3.3	3.7	3.9	
$I_{DD\ (1V8)}$[6]						HSE + HSI + PLL	1500[4]	600	400	200	-	1.25	1.6	1.6	1.7	1.7	mA
							1200	600	400	200	-	1.25	1.6	1.6	1.7	1.7	
							750	600	400	200	-	1.25	1.6	1.6	1.7	1.7	
							600	600	400	200	-	1.25	1.6	1.6	1.7	1.7	
$I_{DD\ (3V3)}$[3]	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0)	Run1 (CStop)	SRun1 (CStop)	HSI	HSI 64	HSI 64	-	-	-	2.55	3.2	3.3	3.6	3.9	mA
						HSE + HSI	HSE 40	HSE 40	-	-	-	2.55	3.2	3.3	3.6	3.9	
$I_{DD\ (1V8)}$[6]						HSI	HSI 64	HSI 64	-	-	-	1.2	1.5	1.6	1.6	1.7	mA
						HSE + HSI	HSE 40	HSE 40	-	-	-	1.2	1.5	1.6	1.6	1.7	
$I_{DD\ (3V3)}$[3]	Supply current in Run mode	All peripherals Disabled	DStandby[7] [8] (CStandby)	Run2 (CRun)	SRun1 (CRun)	HSI	-	HSI 64	HSI 64	HSI 64	-	2.6	3.2	3.3	3.4	3.5	mA
$I_{DD\ (1V8)}$[6]						HSI	-	HSI 64	HSI 64	HSI 64	-	1.25	1.5	1.6	1.6	1.6	mA

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1. *P0 and P1 are state of cores inside CPU1 when in CRun state. 'P0&P1' indicate that both cores are executing a test software. 'P0' indicate that only P0 is executing a test software while other core is clock gated (either in WFI or WFE or not present in the device).*
2. *ck_icn_ddr.*
3. *Typical value given with V_{DD} = 3.3 V, maximum value given with V_{DD} = 3.6 V.*
4. *Typical value given with V_{DDCPU} = 0.91 V, maximum values given with V_{DDCPU} = 0.935 V.*
5. *Typical value given with V_{DDGPU} = 0.9 V, maximum values given with V_{DDGPU} = 0.961 V.*
6. *Typical value given with V_{DD} = 1.8 V, maximum value given with V_{DD} = 1.89 V.*
7. *CStandby = CStop and PDDS_D1 = 1.*
8. *V_{DDCPU} is shutdown.*

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Table 26. Current consumption (I_{DDA18}) in Run modes

Evaluated by characterization, not tested in production unless otherwise specified.
Except otherwise noted, typical values given with V_{DDCORE} = 0.82 V, V_{DDCPU} = 0.8 V and V_{DDGPU} = 0.8 V, maximum values given with V_{DDCORE} = 0.842 V, V_{DDCPU} = 0.842 V and V_{DDGPU} = 0.839 V.

Symbol	Parameter	Conditions										Typ	Max				Unit
		-	D1 (CPU1)[1] mode	D2 (CPU2) mode	D3 (CPU3) mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) [2]	CPU2 clk (MHz)	CPU3 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDA18}	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[3]	600	400	200	900[4]	4.3	6.1	6.2	6.3	6.4	mA
							1200	600	400	200	800	3.85	5.5	5.6	5.6	5.8	
							750	600	400	200	800	3.25	4.8	4.9	5	5.1	
							600	600	400	200	800	3.1	4.6	4.7	4.8	5	
I_{DDA18}	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[3]	600	400	200	-	4.35	5.3	5.6	5.8	6.1	mA
							1200	600	400	200	-	3.9	4.9	5.1	5.3	5.5	
							750	600	400	200	-	3.3	4.2	4.5	4.7	4.9	
							600	600	400	200	-	3.15	4	4.3	4.5	4.7	
I_{DDA18}	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0)	Run1 (CStop)	SRun1 (CStop)	HSI	HSI 64	HSI 64	-	-	-	1.25	2	2.4	2.6	2.8	mA
						HSE + HSI	HSE 40	HSE 40	-	-	-	1.25	2	2.4	2.6	2.8	
I_{DDA18}	Supply current in Run mode	All peripherals Disabled	DStandby[5] [6] (CStandby)	Run2 (CRun)	SRun1 (CRun)	HSI	-	HSI 64	HSI 64	HSI 64	-	1.15	1.8	2.2	2.5	2.9	mA

1. *P0 and P1 are state of cores inside CPU1 when in CRun state. 'P0&P1' indicate that both cores are executing a test software. 'P0' indicate that only P0 is executing a test software while other core is clock gated (either in WFI or WFE or not present in the device).*
2. *ck_icn_ddr.*
3. *Typical value given with V_{DDCPU} = 0.91 V, maximum values given with V_{DDCPU} = 0.935 V.*
4. *Typical value given with V_{DDGPU} = 0.9 V, maximum values given with V_{DDGPU} = 0.961 V.*
5. *CStandby = CStop and PDDS_D1 = 1.*
6. *V_{DDCPU} is shutdown.*

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Table 27. Current consumption ($I_{DDA18AON}$) in Run modes

Evaluated by characterization, not tested in production unless otherwise specified.
Except otherwise noted, typical values given with V_{DDCORE} = 0.82 V, V_{DDCPU} = 0.8 V and V_{DDGPU} = 0.8 V, maximum values given with V_{DDCORE} = 0.842 V, V_{DDCPU} = 0.842 V and V_{DDGPU} = 0.839 V.

Symbol	Parameter	Conditions										Typ	Max				Unit
		-	D1 (CPU1)[1] mode	D2 (CPU2) mode	D3 (CPU3) mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) [2]	CPU2 clk (MHz)	CPU3 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
$I_{DDA18AON}$	Supply current in Run mode (V_{DD} = 1.8 V)	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[3]	600	400	200	900[4]	735	TBD	840	880	830	µA
							1200	600	400	200	800	735	TBD	840	860	830	
							750	600	400	200	800	735	TBD	840	830	830	
							600	600	400	200	800	735	TBD	840	830	830	
$I_{DDA18AON}$	Supply current in Run mode (V_{DD} = 3.3 V)	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[3]	600	400	200	900[4]	700	TBD	790	780	790	µA
							1200	600	400	200	800	700	TBD	790	780	820	
							750	600	400	200	800	700	TBD	790	780	790	
							600	600	400	200	800	700	TBD	790	780	790	
$I_{DDA18AON}$	Supply current in Run mode (V_{DD} = 1.8 V)	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[3]	600	400	200	-	730	TBD	840	830	830	µA
							1200	600	400	200	-	730	TBD	840	830	830	
							750	600	400	200	-	730	TBD	840	830	830	
							600	600	400	200	-	730	TBD	840	830	830	
$I_{DDA18AON}$	Supply current in Run mode (V_{DD} = 3.3 V)	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[3]	600	400	200	-	700	TBD	790	780	780	µA
							1200	600	400	200	-	700	TBD	790	780	780	
							750	600	400	200	-	700	TBD	790	780	780	
							600	600	400	200	-	700	TBD	790	780	780	
$I_{DDA18AON}$	Supply current in Run mode (V_{DD} = 1.8 V)	All peripherals Disabled	DRun (CRun: P0)	Run1 (CStop)	SRun1 (CStop)	HSI	HSI 64	HSI 64	-	-	-	470	560	590	600	620	µA
						HSE + HSI	HSE 40	HSE 40	-	-	-	730	TBD	840	830	830	
$I_{DDA18AON}$	Supply current in Run mode (V_{DD} = 3.3 V)	All peripherals Disabled	DRun (CRun: P0)	Run1 (CStop)	SRun1 (CStop)	HSI	HSI 64	HSI 64	-	-	-	435	500	540	550	570	µA
						HSE + HSI	HSE 40	HSE 40	-	-	-	700	TBD	790	780	780	
$I_{DDA18AON}$	Supply current in Run mode (V_{DD} = 1.8 V)	All peripherals Disabled	DStandby[5][6] (CStandby)	Run2 (CRun)	SRun1 (CRun)	HSI	-	HSI 64	HSI 64	HSI 64	-	470	560	590	600	620	µA

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Symbol	Parameter	Conditions										Typ	Max				Unit
		-	D1 (CPU1)[1] mode	D2 (CPU2) mode	D3 (CPU3) mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) [2]	CPU2 clk (MHz)	CPU3 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
$I_{DDA18AON}$	Supply current in Run mode (V_{DD} = 3.3 V)	All peripherals Disabled	DStandby (CStandby)[5] [6]	Run2 (CRun)	SRun1 (CRun)	HSI	-	HSI 64	HSI 64	HSI 64	-	435	500	540	550	570	µA

1. *P0 and P1 are state of cores inside CPU1 when in CRun state. 'P0&P1' indicate that both cores are executing a test software. 'P0' indicate that only P0 is executing a test software while other core is clock gated (either in WFI or WFE or not present in the device).*
2. *ck_icn_ddr.*
3. *Typical value given with V_{DDCPU} = 0.91 V, maximum values given with V_{DDCPU} = 0.935 V.*
4. *Typical value given with V_{DDGPU} = 0.9 V, maximum values given with V_{DDGPU} = 0.961 V.*
5. *CStandby = CStop and PDDS_D1 = 1.*
6. *V_{DDCPU} is shutdown.*

Table 28. Current consumption (I_{BAT}) in Run modes

Evaluated by characterization, not tested in production unless otherwise specified.
V_{SW} supplied by V_{DD}.

Symbol	Parameter	Conditions	Typ	Max				Unit
		V_{BAT} voltage	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{BAT}	Supply current in Run mode (V_{DD} = 1.8 V)	V_{BAT} = 3.0 V	TBD	5.3	6.3	7.6	11	µA
		V_{BAT} = 3.3 V	TBD	6.1	7.1	8.5	12	
I_{BAT}	Supply current in Run mode (V_{DD}= 3.3 V)	V_{BAT} = 3.0 V	TBD	5.2	4.5	3.7	2	µA
		V_{BAT} = 3.3 V	TBD	6	6.1	6.1	6.3	

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Table 29. Current consumption in Stop modes

Evaluated by characterization, not tested in production unless otherwise specified.
Except otherwise noted, typical values given with V_{DDCORE} = 0.82 V, V_{DDCPU} = 0.8 V and V_{DDGPU} = 0.8 V, maximum values given with V_{DDCORE} = 0.842 V, V_{DDCPU} = 0.842 V and V_{DDGPU} = 0.839 V

Symbol	Parameter	Conditions					Typ				Max				Unit
		D1 (CPU1) mode	D2 (CPU2) mode	D3 (CPU3) mode	CPU3 clk (MHz)	V_{DD} voltage	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCORE}	Supply current in Stop1 mode	DStop1 (CStop)	Stop1 (CStop)	SSTop1 (CStop)	-	-	11	74.5	125	205	47	230	370	570	mA
I_{DDCPU}							2.05	23.5	42.5	74.5	11	75	130	220	mA
I_{DDGPU} (1)							TBD	TBD	TBD	TBD	29	150	240	370	mA
I_{DD}						V_{DD} = 3.3 V (2)	2.5	2.55	2.6	2.7	3.1	3.3	3.6	3.9	mA
						V_{DD} = 1.8 V (3)	1.15	1.2	1.2	1.25	1.5	1.5	1.6	1.7	mA
I_{DDA18}						-	1.25	1.35	1.4	1.5	1.8	2	2.1	2.2	mA
$I_{DDA18AON}$						V_{DD} = 3.3 (2)	39	TBD	56	64	72	98	120	130	µA
						V_{DD} = 1.8 V (3)	72	81	86.5	94	130	150	160	180	µA
I_{DDCORE}	Supply current in Stop2 mode	DStandby (4) (5) (CStandby)	Stop2 (CStop)	SRun2 (CRun)	HSI 64	-	19	82.5	135	215	56	240	380	570	mA
I_{DDCPU}							- (6)								-
I_{DDGPU} (1)							- (6)								-
I_{DD}						V_{DD} = 3.3 V (2)	2.55	2.6	2.6	2.65	3.2	3.3	3.4	3.5	mA
						V_{DD} = 1.8 V (3)	1.2	1.25	1.2	1.25	1.5	1.5	1.5	1.6	mA
I_{DDA18}						-	1.2	1.35	1.4	1.5	1.8	2.2	2.5	2.9	mA
$I_{DDA18AON}$						V_{DD} = 3.3 V (2)	240	260	260	270	290	320	330	350	µA
						V_{DD} = 1.8 V (3)	270	290	290	300	340	370	380	400	µA
I_{DDCORE}					MSI 4	-	19	82.5	135	215	56	240	380	570	mA
I_{DDCPU}							- (6)								-

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Symbol	Parameter	Conditions					Typ				Max				Unit
		D1 (CPU1) mode	D2 (CPU2) mode	D3 (CPU3) mode	CPU3 clk (MHz)	V_{DD} voltage	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDGPU}[1]	Supply current in Stop2 mode	DStandby[4] [5] (CStandby)	Stop2 (CStop)	SRun2 (CRun)	MSI 4	-	-[6]								-
I_{DD}						V_{DD} = 3.3 V[2]	2.55	2.6	2.6	2.65	3.2	3.3	3.4	3.5	mA
						V_{DD} = 1.8 V[3]	1.2	1.2	1.2	1.25	1.5	1.5	1.5	1.6	mA
I_{DDA18}						-	1.2	1.35	1.4	1.5	1.8	2.2	2.5	2.9	mA
$I_{DDA18AON}$						V_{DD} = 3.3 V[2]	240	260	260	270	290	320	330	350	µA
						V_{DD} = 1.8 V[3]	270	290	290	300	340	370	380	400	µA
I_{DDCORE}	Supply current in Stop2 mode	DStandby (CStandby)[4][5]	Stop2 (CStop)	SRun2 (CSleep)	HSI 64	-	18.5	82	135	215	55	240	380	570	mA
I_{DDCPU}							-[6]								-
I_{DDGPU}[1]							-[6]								-
I_{DD}						V_{DD} = 3.3 V[2]	2.55	2.6	2.6	2.65	3.2	3.3	3.4	3.5	mA
						V_{DD} = 1.8 V[3]	1.2	1.2	1.2	1.25	1.5	1.5	1.5	1.6	mA
I_{DDA18}						-	1.2	1.35	1.4	1.5	1.8	2.2	2.5	2.8	mA
$I_{DDA18AON}$						V_{DD} = 3.3 V[2]	240	260	260	270	290	320	330	350	µA
						V_{DD} = 1.8 V[3]	270	290	290	300	340	370	380	400	µA
I_{DDCORE}					MSI 4	-	18.5	82	135	215	55	240	380	570	mA
I_{DDCPU}							-[6]								-
I_{DDGPU}[1]							-[6]								-
I_{DD}						V_{DD} = 3.3 V[2]	2.55	2.6	2.6	2.65	3.2	3.3	3.4	3.5	mA
						V_{DD} = 1.8 V[3]	1.2	1.2	1.2	1.25	1.5	1.5	1.5	1.6	mA
I_{DDA18}						-	1.2	1.35	1.4	1.5	1.8	2.2	2.5	2.9	mA

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Symbol	Parameter	Conditions					Typ				Max				Unit
		D1 (CPU1) mode	D2 (CPU2) mode	D3 (CPU3) mode	CPU3 clk (MHz)	V_{DD} voltage	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
$I_{DDA18AON}$	Supply current in Stop2 mode	DStandby (CStandby)(4)(5)	Stop2 (CStop)	SRun2 (CSleep)	MSI 4	V_{DD} = 3.3 V(2)	240	260	260	270	290	320	330	350	µA
						V_{DD} = 1.8 V(3)	270	290	290	300	340	370	380	400	µA
I_{DDCORE}	Supply current in Stop2 mode	DStandby (CStandby)(4)(5)	Stop2 (CStop)	SSTop1 (CStop)	-	-	11	74.5	125	205	46	230	370	570	mA
I_{DDCPU}							-(6)								-
I_{DDGPU}(1)							-(6)								-
I_{DD}						V_{DD} = 3.3 V(2)	2.55	2.6	2.6	2.65	3.2	3.3	3.4	3.5	mA
						V_{DD} = 1.8 V(3)	1.2	1.2	1.2	1.25	1.5	1.5	1.5	1.6	mA
I_{DDA18}						-	1.2	1.3	1.4	1.5	1.8	2.2	2.5	2.9	mA
$I_{DDA18AON}$						V_{DD} = 3.3 V(2)	37.5	49	54.5	62.5	71	97	110	130	µA
						V_{DD} = 1.8 V(3)	70	79.5	85	92	130	150	160	180	µA

1. *Not relevant for STM32MP251x.*
2. *typical values given for V_{DD} = 3.3 V, maximum values for V_{DD} = 3.6 V.*
3. *typical values given for V_{DD} = 1.8 V, maximum values for V_{DD} = 1.89 V.*
4. *CStandby = CStop and PDDS_D1 = 1.*
5. *V_{DDCPU} is shutdown.*
6. *Supply is OFF.*

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Table 30. Current consumption in LPLV-Stop modes

Evaluated by characterization, not tested in production unless otherwise specified.
Except otherwise noted, typical values given with V_{DDCORE} = 0.82 V, V_{DDCPU} = 0.8 V and V_{DDGPU} = 0.8 V, maximum values given with V_{DDCORE} = 0.842 V, V_{DDCPU} = 0.842 V and V_{DDGPU} = 0.839 V.

Symbol	Parameter	Conditions					Typ				Max				Unit
		D1 (CPU1) mode	D2 (CPU2) mode	D3 (CPU3) (1) mode	CPU3 clk (MHz)	V_{DD} voltage	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCORE}	Supply current in LPLV-Stop1 mode	DStop3(2) (CStop)	LPLV-Stop1(2) (CStop)	SStop2 (CStop)	-	-	11.5	80.5	140	230	51	270	430	670	mA
I_{DDCPU}							2.05	23.5	42.5	74.5	11	75	130	220	mA
I_{DDGPU}(3)							-(4)								-
I_{DD}						V_{DD} = 3.3 V(5)	2.8	4.85	6.75	9.9	4	9.6	15	22	mA
						V_{DD} = 1.8 V(6)	1.5	3.55	5.4	8.5	2.4	7.9	13	20	mA
I_{DDA18}						-	-(4)								-
$I_{DDA18AON}$						V_{DD} = 3.3 V(5)	38.5	TBD	56	64	71	98	120	130	µA
						V_{DD} = 1.8 V(6)	71	TBD	88	100	130	150	170	220	µA
I_{DDCORE}	Supply current in LPLV-Stop2 mode	DStandby (CStandby)	LPLV-Stop2(2) (CStop)	SRun3 (CRun)	MSI 4	-	11.5	80.5	135	230	51	270	430	660	mA
I_{DDCPU}							-(4)								-
I_{DDGPU}(3)							-(4)								-
I_{DD}						V_{DD} = 3.3 V(5)	3.1	5.2	7.1	10	4.3	10	15	23	mA
						V_{DD} = 1.8 V(6)	1.8	3.85	5.75	8.85	2.7	8.3	13	21	mA
I_{DDA18}						-	-(4)								-
$I_{DDA18AON}$						V_{DD} = 3.3 V(5)	38.5	TBD	56	64	72	98	120	130	µA
						V_{DD} = 1.8 V(6)	71.5	TBD	88	100	130	160	170	230	µA
I_{DDCORE}					LSE 0.032768	-	11.5	80.5	135	230	51	270	430	660	mA
I_{DDCPU}							-(4)								-

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Symbol	Parameter	Conditions					Typ				Max				Unit
		D1 (CPU1) mode	D2 (CPU2) mode	D3 (CPU3) (1) mode	CPU3 clk (MHz)	V_{DD} voltage	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDGPU}(3)	Supply current in LPLV-Stop2 mode	DStandby (CStandby)	LPLV-Stop2(2) (CStop)	SRun3 (CRun)	LSE 0.032768	-	-(4)								-
I_{DD}						V_{DD} = 3.3 V(5)	2.8	4.85	6.75	9.9	3.9	9.5	15	22	mA
						V_{DD} = 1.8 V(6)	1.5	3.55	5.4	8.5	2.4	7.9	13	20	mA
I_{DDA18}						-	-(4)								-
$I_{DDA18AON}$						V_{DD} = 3.3 V(5)	38.5	TBD	56	64	72	98	120	130	µA
						V_{DD} = 1.8 V(6)	71	TBD	88	100	130	160	170	230	µA
I_{DDCORE}	Supply current in LPLV-Stop2 mode	DStandby (CStandby)(7)	LPLV-Stop2(2) (CStop)	SRun3 (CSleep)	MSI 4	-	11.5	80.5	135	230	51	270	430	660	mA
I_{DDCPU}							-(4)								-
I_{DDGPU}(3)							-(4)								-
I_{DD}						V_{DD} = 3.3 V(5)	2.95	5.1	6.95	10	4.1	9.8	15	22	mA
						V_{DD} = 1.8 V(6)	1.65	3.7	5.55	8.65	2.6	8.2	13	21	mA
I_{DDA18}						-	-(4)								-
$I_{DDA18AON}$						V_{DD} = 3.3 V(5)	38.5	TBD	56	64	72	98	120	130	µA
						V_{DD} = 1.8 V(6)	71.5	TBD	88	100	130	160	170	230	µA
I_{DDCORE}					LSE 0.032768	-	11.5	80.5	135	230	51	270	430	660	mA
I_{DDCPU}							-(4)								-
I_{DDGPU}(3)							-(4)								-
I_{DD}						V_{DD} = 3.3 V(5)	2.8	4.9	6.7	9.85	3.9	9.5	15	22	mA
						V_{DD} = 1.8 V(6)	1.5	3.5	5.35	8.45	2.3	7.9	13	20	mA
I_{DDA18}						-	-(4)								-

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Symbol	Parameter	Conditions					Typ				Max				Unit
		D1 (CPU1) mode	D2 (CPU2) mode	D3 (CPU3) (1) mode	CPU3 clk (MHz)	V_{DD} voltage	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
$I_{DDA18AON}$	Supply current in LPLV-Stop2 mode	DStandby (CStandby)(7)	LPLV-Stop2(2) (CStop)	SRun3 (CSleep)	LSE 0.032768	V_{DD} = 3.3 V(5)	38.5	TBD	56	64	72	98	120	130	µA
						V_{DD} = 1.8 V(6)	71	TBD	88	99.5	130	160	170	220	µA
I_{DDCORE}	Supply current in LPLV-Stop2 mode	DStandby (CStandby)(7)	LPLV-Stop2 (CStop)(2)	SStop2 (CStop)	-	-	11.5	80.5	140	230	51	270	430	660	mA
I_{DDCPU}							-(4)								-
I_{DDGPU}(3)							-(4)								-
I_{DD}						V_{DD} = 3.3 V(5)	2.8	4.85	6.75	9.9	3.9	9.5	15	22	mA
						V_{DD} = 1.8 V(6)	1.5	3.55	5.4	8.5	2.3	7.9	13	20	mA
I_{DDA18}						-	-(4)								-
$I_{DDA18AON}$						V_{DD} = 3.3 V(5)	38.5	TBD	56	64	72	98	120	130	µA
						V_{DD} = 1.8 V(6)	71	TBD	88	100	130	160	170	230	µA

1. *Domain clocked by MSI 4 MHz.*
2. *Typical value given with V_{DDCORE} = 0.67 V, maximum values given with V_{DDCORE} = 0.71 V.*
3. *Not relevant for STM32MP251x.*
4. *Supply is OFF.*
5. *Typical values given for V_{DD} = 3.3 V, maximum values for V_{DD} = 3.6 V.*
6. *Typical values given for V_{DD} = 1.8 V, maximum values for V_{DD} = 1.89 V.*
7. *CStandby = CStop and PDDS_D1 = 1.*

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Table 31. Current consumption in Standby1 mode

Evaluated by characterization, not tested in production unless otherwise specified.
V_{DDCORE}, V_{DDCPU} and V_{DDGPU} are shutdown.

Symbol	Parameter	Conditions			Typ				Max				Unit
		D3 (CPU3) mode	CPU3 clk (MHz)	V_{DD} voltage	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DD}	Supply current in Standby1 mode	SRun3 (CRun)	MSI 4	V_{DD} = 3.3 V(1)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
				V_{DD} = 1.8 V(2)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
I_{DDA18}				-	-(3)								-
$I_{DDA18AON}$				V_{DD} = 3.3 V(1)	40	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
				V_{DD} = 1.8 V(2)	60	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
I_{DD}	Supply current in Standby1 mode	SRun3 (CRun)	LSE 0.032768	V_{DD} = 3.3 V(1)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
				V_{DD} = 1.8 V(2)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
I_{DDA18}				-	-(3)								-
$I_{DDA18AON}$				V_{DD} = 3.3 V(1)	40	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
				V_{DD} = 1.8 V(2)	70	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
I_{DD}	Supply current in Standby1 mode	SRun3 (CSleep)	MSI 4	V_{DD} = 3.3 V(1)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
				V_{DD} = 1.8 V(2)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
I_{DDA18}				-	-(3)								-
$I_{DDA18AON}$				V_{DD} = 3.3 V(1)	40	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
				V_{DD} = 1.8 V(2)	60	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
I_{DD}	Supply current in Standby1 mode	SRun3 (CSleep)	LSE 0.032768	V_{DD} = 3.3 V(1)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
				V_{DD} = 1.8 V(2)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
I_{DDA18}				-	-(3)								-
$I_{DDA18AON}$				V_{DD} = 3.3 V(1)	40	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
				V_{DD} = 1.8 V(2)	60	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
I_{DD}	Supply current in Standby1 mode	SStop2 (CStop)	-	V_{DD} = 3.3 V(1)	2.45	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
				V_{DD} = 1.8 V(2)	960	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
I_{DDA18}				-	-(3)								-
$I_{DDA18AON}$				V_{DD} = 3.3 V(1)	40	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA

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Symbol	Parameter	Conditions			Typ				Max				Unit
		D3 (CPU3) mode	CPU3 clk (MHz)	V_{DD} voltage	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
$I_{DDA18AON}$	Supply current in Standby1 mode	SStop2 (CStop)	-	V_{DD} = 1.8 V(2)	60	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA

1. *typical values given for V_{DD} = 3.3 V, maximum values for V_{DD} = 3.6 V.*
2. *typical values given for V_{DD} = 1.8 V, maximum values for V_{DD} = 1.89 V.*
3. *Supply is OFF.*

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Table 32. Current consumption in Standby2 mode

Evaluated by characterization, not tested in production unless otherwise specified.
V_{DDCORE}, V_{DDCPU} and V_{DDGPU} are shutdown.
D3 (CPU3) in CStop (SStandby).

Symbol	Parameter	Conditions					Typ				Max				Unit
		RTC/LSE	BKPSRAM	RETRAM	LPSRAM1	V_{DD} voltage	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DD}	Supply current in Standby2 mode	OFF	OFF	OFF	OFF	V_{DD} = 3.3 V(1)	2.05	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
		RTC ON, LSE ON(2)					2.1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
			ON				2.1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
			OFF	ON			2.1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
				OFF	ON		2.1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
			ON	ON			2.1	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	Supply current in Standby2 mode	OFF	OFF	OFF	OFF	V_{DD} = 1.8 V(3)	960	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
		RTC ON, LSE ON(2)					960	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			ON				960	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			OFF	ON			960	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
				OFF	ON		960	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			ON	ON			960	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
$I_{DDA18AON}$	Supply current in Standby2 mode	OFF	OFF	OFF	OFF	V_{DD} = 3.3 V(1)	40	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
						V_{DD} = 1.8 V(3)	60	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
		RTC ON, LSE ON(2)	ON	ON	ON	V_{DD} = 3.3 V(1)	40	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
						V_{DD} = 1.8 V(3)	60	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA

1. *Typical values given for V_{DD} = 3.3 V, maximum values for V_{DD} = 3.6 V.*
2. *LSE is set to medium-high drive.*
3. *typical values given for V_{DD} = 1.8 V, maximum values for V_{DD} = 1.89 V.*

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Table 33. Current consumption in VBAT1 mode

Evaluated by characterization, not tested in production unless otherwise specified.
D3 (CPU3) in SRun3 (DRun).

Symbol	Parameter	Conditions					Typ				Max				Unit
		RTC/LSE	BKPSRAM	RETRAM	LPSRAM1	V_{BAT} voltage	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{BAT}	Supply current in VBAT1 mode (D3 clocked by MSI 4 MHz)	RTC ON, LSE ON[1]	OFF	OFF	ON	V_{BAT} = 2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
						V_{BAT} = 3.0 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
						V_{BAT} = 3.3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
						V_{BAT} = 3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
I_{BAT}	Supply current in VBAT1 mode (D3 clocked by MSI 16 MHz)	RTC ON, LSE ON[1]	OFF	OFF	ON	V_{BAT} = 2.4 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
						V_{BAT} = 3.0 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
						V_{BAT} = 3.3 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	
						V_{BAT} = 3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	

1. *LSE is set to medium-high drive.*

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Table 34. Current consumption in VBAT2 mode

Evaluated by characterization, not tested in production unless otherwise specified.
D3 (CPU3) in CStop (SStandby).

Symbol	Parameter	Conditions					Typ				Max				Unit
		RTC/LSE	BKPSRAM	RETRAM	LPSRAM1	V_{BAT} voltage	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{BAT}	Supply current in VBAT2 mode	OFF	OFF	OFF	OFF	V_{BAT} = 2.4 V	16	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
		RTC ON, LSE ON[1]					16	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			ON				18	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			OFF	ON			35	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
				OFF	ON		16	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			ON	ON			40	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
I_{BAT}	Supply current in VBAT2 mode	OFF	OFF	OFF	OFF	V_{BAT} = 3.0 V	18	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
		RTC ON, LSE ON[1]					18	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			ON				20	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			OFF	ON			39	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
				OFF	ON		20	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			ON	ON			44	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
I_{BAT}	Supply current in VBAT2 mode	OFF	OFF	OFF	OFF	V_{BAT} = 3.3 V	20	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
		RTC ON, LSE ON[1]					20	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			ON				22	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			OFF	ON			41	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
				OFF	ON		22	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			ON	ON			45	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
I_{BAT}	Supply current in VBAT2 mode	OFF	OFF	OFF	OFF	V_{BAT} = 3.6 V	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
		RTC ON, LSE ON[1]					TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			ON				TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			OFF	ON			TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
				OFF	ON		TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			ON	ON			TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA

1. *LSE is set to medium-high drive.*

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6.3.5.2 *I/O system current consumption*

The current consumption of the I/O system has two components: static and dynamic.

6.3.5.3 *I/O static current consumption*

All the I/Os used as inputs with pull-up generate a current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in Table 62. I/O static characteristics.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

An additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid a current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

6.3.5.4 *I/O dynamic current consumption*

The I/Os used by an application contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin.

The theoretical formula is provided below:

$$I_{SW} = V_{DD} \times f_{SW} \times C_L$$

where

- I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load
- V_{DDx} is the MCU supply voltage
- f_{SW} is the I/O switching frequency
- C_L is the total capacitance seen by the I/O pin: C = CINT + CEXT

6.3.6 Wakeup time from low-power modes

The wakeup times given in Table 35 , Table 36 and Table 37 are measured starting from the wakeup event trigger up to the first instruction executed by the CPU1, CPU2 or CPU3:

- the CPU1, CPU2 or CPU3 goes in low-power mode after WFI (wait for interrupt) instruction.
- For CSleep modes:
  - Interrupt to GIC or NVIC is used to wakeup from low-power modes.
- For CStop modes (except Standby and VBAT):
  - For CPU1 and CPU2: EXTI1[x] is used to wakeup from low-power modes.
  - For CPU3: EXTI2[x] is used to wakeup from low-power modes.
- For Standby modes:
  - WKUPx is used to wakeup from low-power modes.
- For VBAT modes
  - TAMP_INx is used to wakeup from low-power modes.
- System mode is equal to D2 domain mode

All timings are derived from tests performed under ambient temperature and V_{DD} = 3.3 V.

General conditions unless otherwise noted:

- CPU1 software in SYSRAM
- CPU2 software in SRAMx
- CPU3 software in LPSRAMx
- HSE is 40 MHz
- When HSI is used, HSIKERON = 0

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- PWRLP_DLY = 0
- LPLVDLY_D2 = 187 µs
- $t_{WUCSleep}$ values are measured with internal interrupt
- $t_{WUCStop}$ and $t_{WULPLV-Stop}$ values are measured with EXTI pin
- $t_{WUStandby}$ values are measured with WKUP pin through PWR
- When V_{DDCORE} or V_{DDCPU} are shutdown or reduces, wakeup time value depend on supply characteristics.
  - Wakeup time in following tables are measured with 200 µs V_{DDCORE} and V_{DDCPU} setup time
  - Longer V_{DDCPU} or V_{DDCORE} startup time than 200 µs should be added to the wakeup time value
  - When voltage is reduced, V_{DDCORE} is assumed to be back to nominal value before LPLVDLY_D2 expiration. Otherwise, LPLVDLY_D2 value should be increased accordingly and this directly impact wakeup time value.

Table 35. D1 (CPU1) low-power mode wakeup timings

Evaluated by characterization, not tested in production. Unless otherwise noted.

Symbol	D1 (CPU1) mode	D2 (CPU2) mode	D3 (CPU3) mode	Conditions for wakeup domain	Typ	Max	Unit
$t_{WUCSleep_CPU1}$	DRun (CSleep)	Run1 (CStop)	(Reset)	SEV between CPU1 cores	-	15	CPU1 clock cycles
				HSI	-	12 + 20	$T_{ck_icn_nic}$ + $T_{ck_cpu1_ext2f}$
				HSE + PLL1	-	12 + 20	$T_{ck_icn_nic}$ + T_{PLL1}
	DRun (eCSleep)[1]	Run1 (CStop)	(Reset)	HSE + PLL1	-	12 + 20	$T_{ck_icn_nic}$ + $T_{ck_cpu1_ext2f}$
$t_{WUCStop_CPU1}$	DStop1 (CStop)	Run1 (CRun)	(Reset)	HSI 64 MHz	TBD	TBD	µs
				HSE + PLL1 1200 MHz	TBD	TBD	µs
	DStop1 (CStop)[2]	Stop1 (CStop)[2]	(Reset)	HSI 64 MHz[3]	3.3	TBD	µs
				HSI 64 MHz	8.2	TBD	µs
				HSE + PLL1 1200 MHz	180	TBD	µs
	DStandby (CStop)[4]	Stop2 (CStop)[2]	(Reset)	HSI 64 MHz[3][5]	660	TBD	µs
$t_{WULPLV-Stop_CPU1}$	DStop3 (CStop)[2][6]	LPLV-Stop1 (CStop)[2][6]	(Reset)	HSI 64 MHz, PWRLP_DLY = 100 us	1000	TBD	µs
	DStandby (CStop)[4][6]	LPLV-Stop2 (CStop)[2][6]	(Reset)	HSI 64 MHz[5]	1500 (1000)	TBD	µs[7]

1. *eCSleep mean CPU1 in enhanced CSleep with PLL1 automatically stopped (RCC_C1SREQSETR.ESLPREQ = 1). In this mode, CPU1 wake on ck_cpu1_ext2f, then CPU1 switch back automatically to PLL1 after PLL lock time.*
2. *PDDS_Dx = 0.*
3. *HSI active (HSIKERON = 1).*
4. *PDDS_Dx = 1.*
5. *CPU1 wake-up address register points to SYSRAM code.*
6. *LPDS_Dx=1 and LVDS_Dx = 1.*
7. *Value in parenthesis is for wakeup using WKUP pin through PWR.*

Table 36. D2 (CPU2) low-power mode wakeup timings

Evaluated by characterization, not tested in production. Unless otherwise noted.

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Symbol	D1 (CPU1) mode	D2 (CPU2) mode	D3 (CPU3) mode	Conditions for wakeup domain	Typ	Max	Unit
$t_{WUCSleep_CPU2}$[1]	DStop1 (CStop)	Run1 (CSleep)	(Reset)	-	-	14	CPU2 clock cycles
$t_{WUCStop_CPU2}$	DRun (CRun)	Run1 (CStop)	(Reset)	HSI 64 MHz	TBD	TBD	µs
				HSE + PLL 400 MHz	TBD	TBD	µs
	DStop1 (CStop)[2]	Stop1 (CStop)[2]	(Reset)	HSI 64 MHz[3]	2.7	TBD	µs
				HSI 64 MHz	7.6	TBD	µs
				HSE + PLL 400 MHz	180	TBD	µs
$t_{WULPLV\text{-}Stop_CPU2}$	DStop3 (CStop)[2][4]	LPLV-Stop1 (CStop)[2][4]	(Reset)	HSI 64 MHz[5]	900	TBD	µs
				HSI 64 MHz[6]	1000	TBD	µs
	DStandby (CStop)[4][7]	LPLV-Stop2 (CStop)[2][4]	(Reset)	HSI 64 MHz	1500 (900)[8]	TBD	µs
$t_{WUStandby_CPU2}$	DStandby (CStop)[9]	Standby2 (CStop)[9]	(Reset)[9]	HSI 64 MHz, RETRAM	1700 (800)[10]	TBD	µs

1. *Specified by design, not tested in production.*
2. *PDDS_Dx = 0.*
3. *HSI active (HSIKERON = 1).*
4. *LPDS_Dx = 1 and LVDS_Dx = 1.*
5. *CPU2TMPSKP = 1 or PWRLP_DLY = 0.*
6. *CPU2TMPSKP = 0 and PWRLP_DLY = 100 µs.*
7. *PDDS_Dx = 1*
8. *Value in parenthesis is for wakeup using WKUP pin through PWR or wakeup using EXTI without simultaneous CPU1 wakeup.*
9. *PDDS_Dx = 1.*
10. *Value in parenthesis is for RAMCFG_RETRAMCCR1.CRCBS[2:0] = 0 (only 16 Kbytes RETRAM CRC check).*

Table 37. D3 (CPU3) low-power mode wakeup timings

Evaluated by characterization, not tested in production. Unless otherwise noted.

Symbol	D1 (CPU1) mode	D2 (CPU2) mode	D3 (CPU3) mode	Conditions for wakeup domain	Typ	Max	Unit
$t_{WUCSleep_CPU3}$[1]	DRun (CSleep)	Run1 (CSleep)	SRun1 (CSleep)	-	-	8	CPU3 clock cycles
$t_{WUCStop_CPU3}$	DRun (CRun)	Run1 (CStop)	SRun1 (CStop)	HSI 64 MHz	TBD	TBD	µs
				HSE + PLL 200 MHz	TBD	TBD	µs
	DStop1 (CStop)[2]	Stop1 (CStop)[2]	SStop1 (CStop)[2]	HSI 64 MHz[3]	TBD	TBD	µs
				HSI 64 MHz	TBD	TBD	µs
				HSE + PLL 200 MHz	TBD	TBD	µs
$t_{WULPLV\text{-}Stop_CPU3}$	DStop3 (CStop)[2][4]	LPLV-Stop1 (CStop)[2][4]	SStop2 (CStop)[2]	MSI 16 MHz	TBD	TBD	µs
$t_{WUStandby_CPU3}$	DStandby (CStop)[5]	Standby2 (CStop)[5]	SStandby (CStop)[5]	MSI 4 MHz, LPSRAM1	TBD	TBD	ms
$t_{WUVBAT2_CPU3}$	OFF[6]		SStandby (CStop)[5][7]	MSI 4 MHz, LPSRAM1	TBD	TBD	ms

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1. *Specified by design, not tested in production.*
2. *PDDS_Dx = 0.*
3. *HSI active (HSIKERON = 1).*
4. *LPDS_Dx = 1 and LVDS_Dx = 1.*
5. *PDDS_Dx = 1.*
6. *All supplies OFF except V_{BAT}.*
7. *TAMP_WKUEN_D3 = 1.*

Table 38. Wakeup time using USART/LPUART

Specified by design, not tested in production.

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$ $t_{WULPUART}$	Wakeup time needed to calculate the maximum USART/ LPUART baud rate allowing the wakeup from low-power mode	Stop1/2 HSI clock with HSIKERON = 0	-	6.4	µs
$t_{WULPUART_LPLV}$	Wakeup time needed to calculate the maximum LPUART baud rate allowing the wakeup from low-power mode	LPLV-Stop1/2 MSI clock with MSIKERON = 0	-	580	µs

6.3.7 External clock source characteristics

6.3.7.1 High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O.

Digital and analog bypass modes are available.

The external clock signal has to respect the Table 62. I/O static characteristics . However, the recommended clock input waveform is shown in Figure 13 for digital bypass mode and in Figure 14 for analog bypass mode. In analog bypass mode the clock can be a sinusoidal waveform.

Table 39. High-speed external (HSE) user clock characteristics (digital bypass)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	-	16	40	48	MHz
V_{HSEH}	OSC_IN input pin high level voltage	-	-	$0.7 \times V_{DDA18}AON$	-	$V_{DDA18AON}$	V
V_{HSEL}	OSC_IN input pin low level voltage	-	-	V_{SS}	-	$0.3 \times V_{DDA18AON}$	
$t_{W(HSE)}$	OSC_IN high or low time	-	-	7	-	-	ns

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Figure 13. High-speed external clock source AC timing diagram (digital bypass)

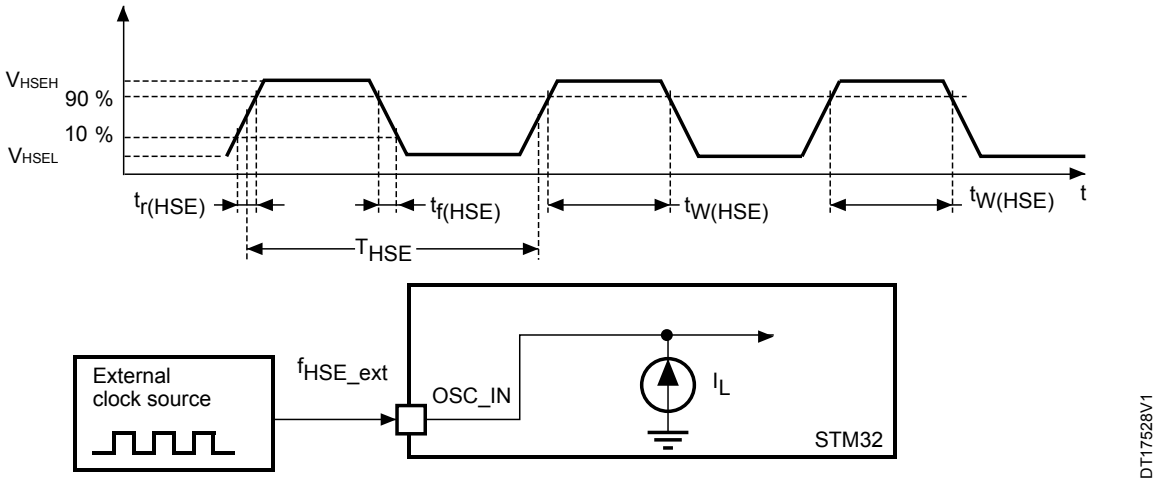

Table 40. High-speed external (HSE) user clock characteristics (analog bypass)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	16	40	48	MHz
	duty cycle (Square wave)	-	45	50	55	%
	duty cycle deterioration(1)	-	-	± 10(2)	±20(3)	%
V_{HSE}	Absolute input range	-	0	-	V_{DDA1}8AON	V
V_{PP}	OSC_IN peak-to-peak amplitude	-	0.2(4)	-	0.67 × V_{DD18}AON	
$t_{SU(HSE)}$	Time to start(5)	-	-	1	10(6)	µs
$tr/tf_{(HSE)}$	Rise and Fall time (10% to 90% threshold levels of the input peak-to-peak amplitude)	-	0.05 × T_{HSE}	-	0.3 × T_{HSE}	ns

1. *Specified by design, not tested in production.*
2. *With a square wave signal (@25 °C, VDDA18AON = 1.8 V / VPP = 400 mV / VDC = 0.8 V) where VDC is the DC component of the input signal.*
3. *With a square wave signal (@25 °C, VDDA18AON = 1.71 V / VPP = 200 mV / VDC = 0.8 V) where VDC is the DC component of the input signal.*
4. *Minimum peak-to-peak amplitude (@25 °C, 0.1 < VDC < VDDA18AON - 0.1 V) where VDC is the DC component of the input signal.*
5. *Startup time measured from the moment it is enabled (by software) to a stabilized analog bypass clock interface is reached.*
6. *Maximum start-up time is obtained with 200 mV peak-to-peak amplitude.*

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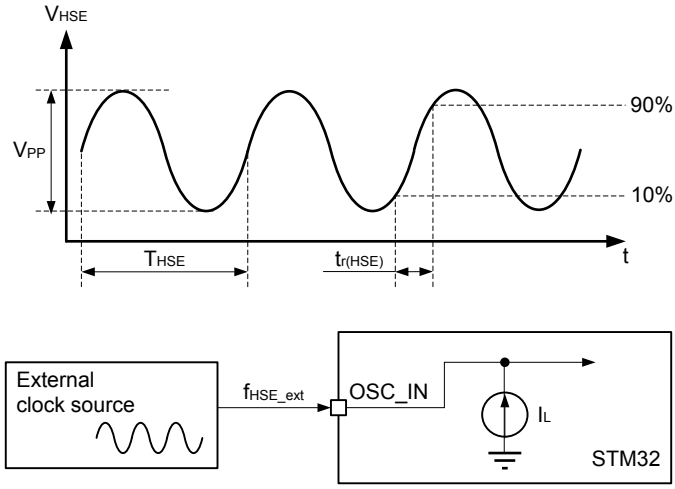
Figure 14. High-speed external clock source AC timing diagram (analog bypass)



6.3.7.2 *Low-speed external user clock generated from an external source*

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the Table 62. I/O static characteristics . However, the recommended clock input waveform is shown in Figure 15 for digital bypass and Figure 16 for analog bypass.

Table 41. Low-speed external (LSE) user clock characteristics (digital bypass)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}(1)	User external clock source frequency	-	-	32.768	-	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.7 × V_{SW}	-	V_{SW}(2)	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.3 × V_{SW}	
$t_{W(LSE)}$	OSC32_IN high or low time	-	250	-	-	ns

1. *Specified by design, not tested in production.*
2. *V_{SW} is equal to V_{DD} when present or V_{BAT} otherwise.*

Figure 15. Low-speed external clock source AC timing diagram (digital bypass)

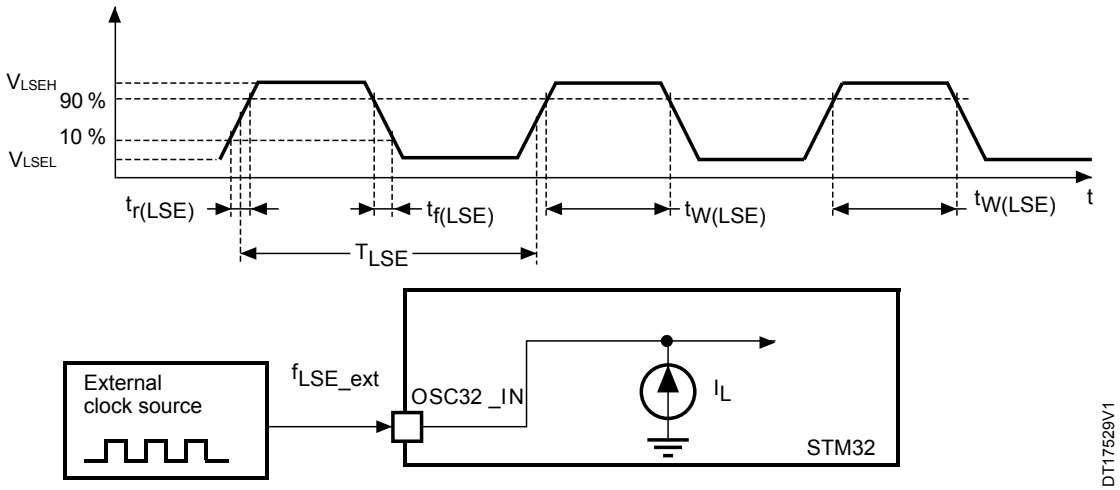


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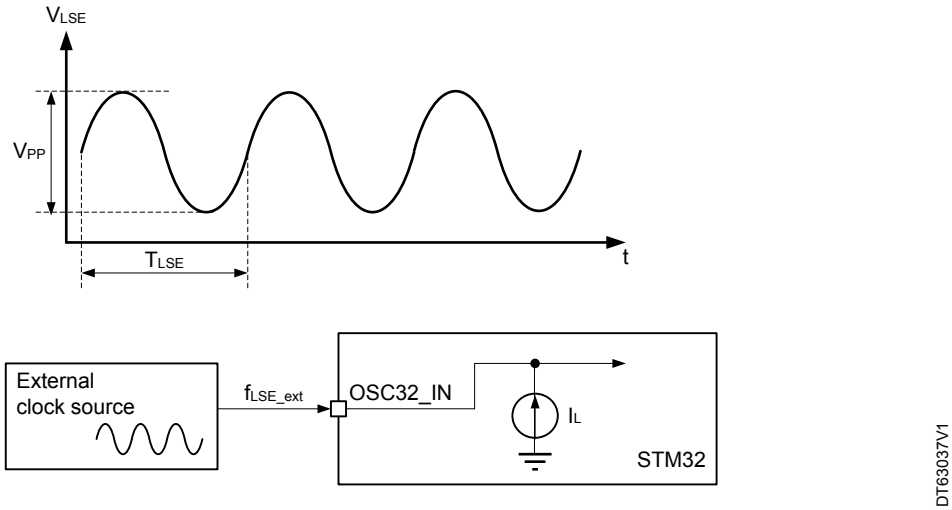
Table 42. Low-speed external (LSE) user clock characteristics (analog bypass)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}[1]	User external clock source frequency	-	-	32.768	-	kHz
V_{LSE}	Absolute input range	-	0	-	V_{SW}[2]	V
V_{PP}	OSC32_IN peak-to-peak amplitude	-	0.2[3]	1	-	

1. *Specified by design, not tested in production.*
2. *V_{SW} is equal to V_{DD} when present or V_{BAT} otherwise.*
3. *Minimum peak-to-peak amplitude (@25 °C, 0.1 < VDC < V_{SW} - 0.1 V) where VDC is the DC component of the input signal.*

Figure 16. Low-speed external clock source AC timing diagram (analog bypass)



6.3.7.3 *High-speed external clock generated from a crystal/ceramic resonator*

The high-speed external (HSE) clock can be supplied with a 16 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in Table 43 . In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 43. High-speed external (HSE) oscillator characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}[1]	Crystal frequency	-	16	40	48	MHz
R_F[1]	Internal feedback equivalent resistor	-	-	250	-	kΩ
$I_{VDDA18AON(HSE)}$	HSE current consumption on $V_{DDA18AON}$	During startup	-	-	10	mA
		Rm = 80 Ω, CL = 6 pF at 40 MHz[3]	-	TBD	-	
$Gm_{critmax}$[1]	Maximum critical crystal gm	Startup	-	-	2.5	mA/V
t_{SU}	Start-up time[4]	-	-	2	-	ms

1. *Specified by design, not tested in production.*
2. *This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.*
3. *Resonator characteristics given by the crystal/ceramic resonator manufacturer.*

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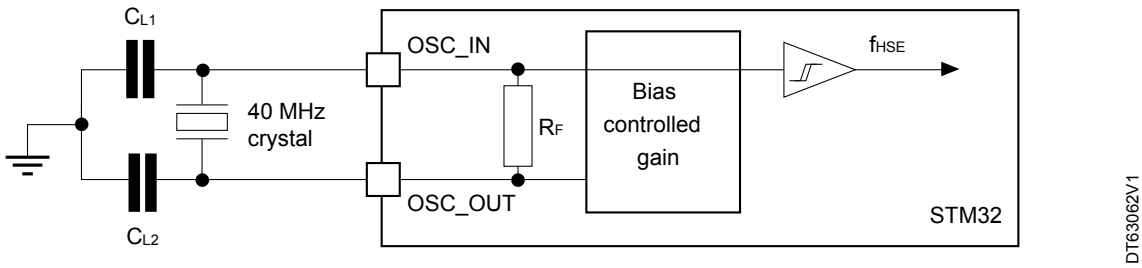
4. *Measured from the moment it is enabled (by software) to a stabilized 40 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.*

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typical), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see Figure 17). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. The PCB and pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs" available from the ST website www.st.com.

Figure 17. Typical application with a 40 MHz crystal



6.3.7.4 *Low-speed external clock generated from a crystal/ceramic resonator*

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in Table 44 . In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 44. Low-speed external (LSE) oscillator characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}(1)	Oscillator frequency	-	-	32.768	-	kHz
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00, Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01, Medium Low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10, Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11, High drive capability	-	-	2.7	
t_{SU}(2)	Startup time	V_{SW} is stabilized	-	2	-	s

1. *Specified by design, not tested in production.*
2. *t_{SU} is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.*

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs" available from the ST website www.st.com.

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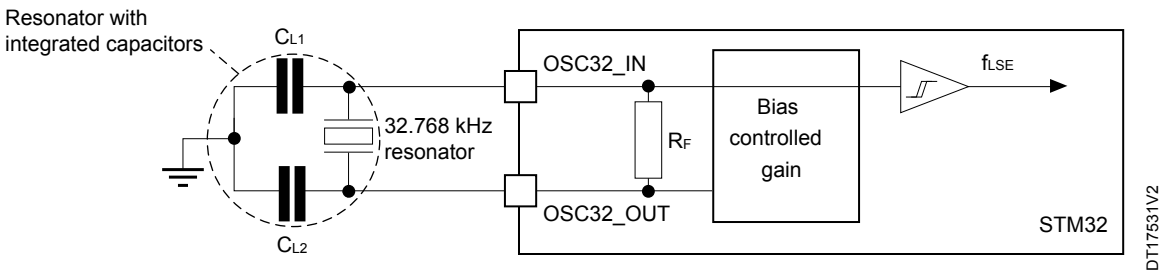
Figure 18. Typical application with a 32.768 kHz crystal



1. *Adding an external resistor between OSC32_IN and OSC32_OUT is forbidden.*

6.3.8 External clock source security characteristics

Table 45. High-speed external user clock security system (HSE CSS)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{DCM(HSE_CSS)}$	Time to detect clock missing	f_{HSE} = 48 MHz	-	1	2	µs

Table 46. Low-speed external user clock security system (LSE CSS)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{DCM(LSE_CSS)}$	Time to detect clock missing	-	-	-	300	µs
$f_{MAX(LSE_CSS)}$	Cut-off frequency	-	-	-	2	MHz

6.3.9 Internal clock source characteristics

The parameters given in Table 47 , Table 48 and Table 49 are derived from tests performed under ambient temperature and supply voltage conditions summarized in Table 17. General operating conditions .

6.3.9.1 64 MHz high-speed internal RC oscillator (HSI)

Table 47. HSI oscillator characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}[(1)]	HSI frequency	$V_{DDA18AON}$ = 1.8 V, T_J = 30 °C	63.68	64	64.32	MHz
TRIM	HSI trimming step	-	-	0.25	0.5	%
DuCy(HSI)	Duty Cycle	-	40	-	60	%
$\Delta V_{DDA18AON(HSI)}$ + ΔT_J(HSI)	HSI oscillator frequency drift over voltage and temperature variation (after factory calibration)	T_J = -40 to 125 °C	-4	-	+4	%
$t_{su(HSI)}$	HSI oscillator start-up time (Time between Enable rising and First output clock edge.)	-	-	-	3	µs
$t_{stab(HSI)}$	HSI oscillator stabilization time	At 1% of target frequency	-	-	5	µs
$I_{VDDCORE(HSI)}$	HSI supply current on V_{DDCORE}	-	-	-	10	µA
$I_{VDD18AON(HSI)}$	HSI supply current on $V_{DDA18AON}$	-	-	300	400	µA

1. *Guaranteed by test in production.*

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6.3.9.2 *4/16 MHz low-power internal RC oscillator (MSI)*

Table 48. MSI oscillator characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{MSI}	CSI frequency	V_{DDCORE} = 0.82 V, T_J = 30 °C	MSIFREQSEL=0[1]	3.956	4	4.044	MHz
			MSIFREQSEL=1	15.824	16	16.176	
TRIM	MSI trimming step	Trimming Code is not a multiple of 32		-	0.8	1.1	%
		Trimming Code is a multiple of 32		-	-2.5	-3.8	
DuCy(MSI)	Duty Cycle	At trimmed frequency		45	-	55	%
ΔT_J(MSI)	MSI oscillator frequency drift over temperature	T_J = -40 °C to 70 °C		-5	-	+5	%
		T_J = -40 °C to 125 °C		-6	-	+6	
$t_{su(MSI)}$	MSI oscillator start-up time	-		-	-	3.5	µs
$t_{stab(MSI)}$	MSI oscillator stabilization time	To reach ±5% of f_{MSI}		-	TBD	-	cycle
$I_{VDDCORE(MSI)}$	MSI Supply current on V_{DDCORE}	at 4 MHz	MSIFREQSEL = 0	-	20	22	µA
		at 16 MHz	MSIFREQSEL = 1	-	60	68	

1. *Guaranteed by test in production.*

6.3.9.3 *32 kHz low-speed internal (LSI) RC oscillator*

Table 49. LSI oscillator characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI Frequency	T_J = 30 °C[1]	30.5	32	33.5	kHz
		T_J= -40 to 125° C	28.8	32	33.6	
$t_{su(LSI)}$	LSI oscillator start-up time (time between enable rising and first output clock edge.)	-	-	-	180	µs
$t_{stab(LSI)}$	LSI oscillator stabilisation time (5% of final value)	-	-	-	TBD	µs
$I_{VSW(LSI)}$	LSI supply current on V_{SW}[2]	-	-	250	500	nA

1. *Guaranteed by test in production.*
2. *V_{SW} is equal to V_{DD} when present or V_{BAT} otherwise.*

6.3.10 PLL characteristics

The parameters given in Table 50 , Table 51 , Table 52 and Table 53. PLL_LVDS characteristics are derived from tests performed under temperature and supply voltage conditions summarized in Table 17. General operating conditions .

Table 50. PLL1 to PLL8 characteristics

Specified by design, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	Normal mode	5	-	64	MHz
		Sigma delta mode	10	-	64	
-	PLL input clock duty cycle	-	TBD	-	TBD	%

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PFD}	PFD input clock	Normal mode		5	f_{PLL_IN}/ FREFDIV	50	MHz
		Sigma delta mode		10	-	min(50, f_{VCO}/20)	
$f_{FOUTPOSTDIV}$	Divided output clock	-		16.32	-	3200	MHz
	Divided output clock duty cycle	Division by 1		48	50	52	%
		Even Division		48	50	52	
		Odd Division		47	50	53	
f_{VCO}	PLL VCO output	-		800	-	3200	MHz
t_{LOCK}	PLL lock time	Frequency lock		-	-	400	1/f_{PFD} cycles
		f_{PFD} = 40 MHz (f_{PLL_IN} = 40 MHz, FREFDIV = 1)		-	-	10	µs
Jitter	RMS period jitter	f_{VCO} = 3200 MHz		-	-	0.26	+/_ps
	RMS integrated jitter (10 kHz - 20 MHz)	f_{VCO} = 3200 MHz, F_{PFD} = 25 MHz	Integer divider	-	±2.7	±6.6	ps
			fracN divider	-	-	±11.9	
$I_{VDDA18PLL}$[1]	PLL supply current on $V_{DDA18PLL}$ (Analog)	f_{VCO} = 3200 MHz	FBDIV < 256	-	5750	6850	µA
			FBDIV > 255	-	7050	8450	
		f_{VCO} = 800 MHz	FBDIV < 256	-	715	860	
$I_{VDDCORE(PLL)}$[1]	PLL supply current on V_{DDCORE} (Digital)	f_{VCO} = 3200 MHz	V_{DDCORE} = 0.82 V	-	1200	3650	
		f_{VCO} = 800 MHz		-	295	910	

1. *Evaluated by characterization, not tested in production.*

Table 51. PLL_USB characteristics

Specified by design, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	Only those 3 values (min, typ or max) are possible	19.2	20	38.4	MHz
f_{PLL_OUT}	PLL output clock	-	-	480	-	MHz

Table 52. PLL_DSI characteristics

Specified by design, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-	-	2	-	64	MHz
f_{PLL_INFIN}	PFD input clock	-	-	2	-	24	
f_{PLL_OUT}	PLL output clock	-	-	40	-	1250	
f_{VCO_OUT}	PLL VCO output	-	-	320	-	1250	
t_{LOCK}	PLL lock time[1]	-	-	-	-	150	µs
t_{PDN}	PLL power down time	-	-	0.1	-	-	

1. *Evaluated by characterization, not tested in production.*

Table 53. PLL_LVDS characteristics

Specified by design, not tested in production unless otherwise specified.

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-	-	3	-	24	MHz
f_{PLL_INFIN}	PFD input clock	-	-	3	-	24	
f_{PLL_OUT}	PLL output clock	-	-	-	-	1100	
f_{VCO_OUT}	PLL VCO output	-	-	1800	2200	3000	
t_{LOCK}(1)	PLL lock time	-	-	-	-	355	µs
f_{Mod}	Modulation frequency	-	-	-	33	-	kHz
md	Modulation depth	-	-	-	0.25	5	%
$I_{VDDA18LVDS}$(1)	PLL supply current on $V_{DDA18LVDS}$	-	-	-	4.9	-	mA
$I_{VDDLVDS}$(1)	PLL supply current on V_{DDLVDS}	-	-	-	1.4	-	mA

1. *Evaluated by characterization, not tested in production.*

6.3.11 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows the reduction of electromagnetic interferences (see Section 6.3.13.4). It is available only on the PLL2 to PLL8.

Table 54. PLL2 to PLL8 SSCG parameters constraints

Specified by design, not tested in production.

Symbol	Parameter	Min	Typ	Max	Unit
F_{MOD}	Modulation frequency	5.2	-	391	kHz
M_D	Peak modulation depth	0.1	-	3.1	%

6.3.12 Memory characteristics

6.3.12.1 OTP characteristics

The characteristics are given at T_J = -40 to 125 °C unless otherwise specified.

Table 55. OTP characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{OTP(VDDA18AON)}$	OTP supply current on $V_{DDA18AON}$	Programming	-	3.8	10	mA
		Reading	-	0.66	1.13	
		PowerDown	-	5	132	µA
$I_{OTP(VDDCORE)}$	OTP supply current on V_{DDCORE}	Programming	-	0.09	0.45	mA
		Reading	-	1.8	3.6	
		PowerDown	-	8	500	µA

6.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

6.3.13.1 Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.

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- **FTB**: a burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in Table 56 . They are based on the EMS levels and classes defined in application note AN1709 available from the ST website www.st.com.

Table 56. EMS characteristics

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, TA = +25 °C, TFBGA436 package, F_{PLL1} = 1200 or 1500 MHz, $F_{ck_icn_hs_mcu}$ = 400 MHz, M33/M0+ cores not running, conforms to IEC 61000-4-2	2B
V_{FTB}	Fast transient voltage burst limits to be applied through 100 pF on VDD and VSS pins to induce a functional disturbance		5A

As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the device pins exposed to noise (connected to tracks longer than 50 mm on PCB).

6.3.13.2 *Designing hardened software to avoid noise problems*

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

6.3.13.3 *Software recommendations*

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (such as control registers)

See also application note AN1015.

6.3.13.4 *Electromagnetic Interference (EMI)*

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 57. EMI characteristics for f_{HSE} = 40 MHz and F_{PLL1} = 1200 MHz

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions	Monitored frequency band	Value	Unit
S_{EMI}	Peak[1]	V_{DD} = 3.6 V, TA = 25 °C, TFBGA436 package, $F_{ck_icn_hs_mcu}$ = 400 MHz, M33/M0+ cores not running, conforming to IEC61967-2	0.1 MHz to 30 MHz	14	dBµV
			30 MHz to 130 MHz	9	
			130 MHz to 1 GHz	21	
			1 GHz to 2 GHz	8	
	Level[2]		0.1 MHz to 2 GHz	3	-

1. *Refer to AN1709 "EMI radiated test" section.*
2. *Refer to AN1709 "EMI level classification" section.*

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Table 58. EMI characteristics for f_{HSE} = 40 MHz and F_{PLL1} = 1500 MHz

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions	Monitored frequency band	Value	Unit
S_{EMI}	Peak[1]	V_{DD} = 3.6 V, TA = 25 °C, TFBGA436 package, $F_{ck_icn_hs_mcu}$ = 400 MHz, M33/M0+ cores not running, conforming to IEC61967-2	0.1 MHz to 30 MHz	-	dBµV
			30 MHz to 130 MHz	-	
			130 MHz to 1 GHz	-	
			1 GHz to 2 GHz	-	
	Level[2]		0.1 MHz to 2 GHz	-	-

1. *Refer to AN1709 "EMI radiated test" section.*
2. *Refer to AN1709 "EMI level classification" section.*

6.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

6.3.14.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse) are applied to the pins of each sample according to each pin combination. This test conforms to the ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 standards.

Table 59. ESD absolute maximum ratings

Evaluated by characterization, not tested in production.

Symbol	Ratings	Conditions	Packages	Class	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-001	All	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-002	All	C1	250	V

6.3.14.2 Static latchup

Two complementary static tests are required on three parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with JESD78 IC latchup standard.

Table 60. Electrical sensitivities

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions	Class
LU	Static latchup class	T_A = +25 °C conforming to JESD78	II level A

6.3.15 I/O current injection characteristics

As a general rule, a current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} should be avoided during the normal product operation. However, in order to give an indication of the robustness of the device in cases when an abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during the device characterization.

Prerelease product(s)

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6.3.15.1 *Functional susceptibility to I/O current injection*

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter:

- ADC error above a certain limit: higher than 5 LSB total unadjusted error (TUE),
- Out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range)
- Other functional failure (for example reset, oscillator frequency deviation).

The following tables are the compilation of the SIC1/SIC2 and functional ESD results.

Negative induced A negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

Table 61. I/O current injection susceptibility

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Description	Negative Injection	Positive Injection	Unit
IINJ	ANA0, ANA1	5	0	mA
	OSC32_IN, OSC32_OUT, PC13, PI8, PZ0, PZ1, PZ2, PZ3, PZ4, PZ5, PZ6, PC3, PC4, PC5, PF6, PF7, PG1, PG3	0	NA	
	All other digital I/Os	5	NA	

6.3.16 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 62. I/O static characteristics are derived from tests performed under the conditions summarized in Table 17. General operating conditions . All I/Os are CMOS and TTL compliant.

Table 62. I/O static characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL} (1)	I/O input low voltage	2.7 < V_{DDx} < 3.6 V	-	-	0.3 × V_{DDx}	V
		1.71 <V_{DDx} < 1.89 V	-	-	0.35 × V_{DDx}	V
V_{IH} (1)	I/O input high voltage	2.7 < V_{DDx} < 3.6 V	0.7 × V_{DDx}	-	-	V
		1.71 < V_{DDx} < 1.89 V	0.65 × V_{DDx}	-	-	V
V_{IL} (2)	I/O input low voltage	2.7 < V_{DDx} < 3.6 V	-	-	0.4 × V_{DDx} - 0.27	V
		1.71 < V_{DDx} < 1.89 V	-	-	0.36 × V_{DDx}	V
V_{IH} (2)	I/O input high voltage	2.7 <V_{DDx} < 3.6 V	0.52 × V_{DDx} - 0.11	-	-	V
		1.71 < V_{DDx} < 1.89 V	0.62 × V_{DDx}	-	-	V
VHYS	I/O input hysteresis	2.7 < V_{DDx} < 3.6 V	-	0.44	-	V
		1.71 <V_{DDx} < 1.89 V	-	0.44	-	V
I_{leak}	TT_x input leakage		-	50	1000	nA
I_{VDDx}	Static current consumption on V_{DDx}		-	40	2000	nA
$I_{VDDA18AON}$	Static current consumption on $V_{DDA18AON}$		-	2	80	nA
$I_{VDDCORE}$	Static current consumption on V_{DDCORE}		-	1	180	nA
R_{PU}	Weak pull-up equivalent resistor (3)	2.7 < V_{DDx} < 3.6 V	30	40	50	kΩ
		1.71 < V_{DDx} < 1.89 V	30	40	50	kΩ

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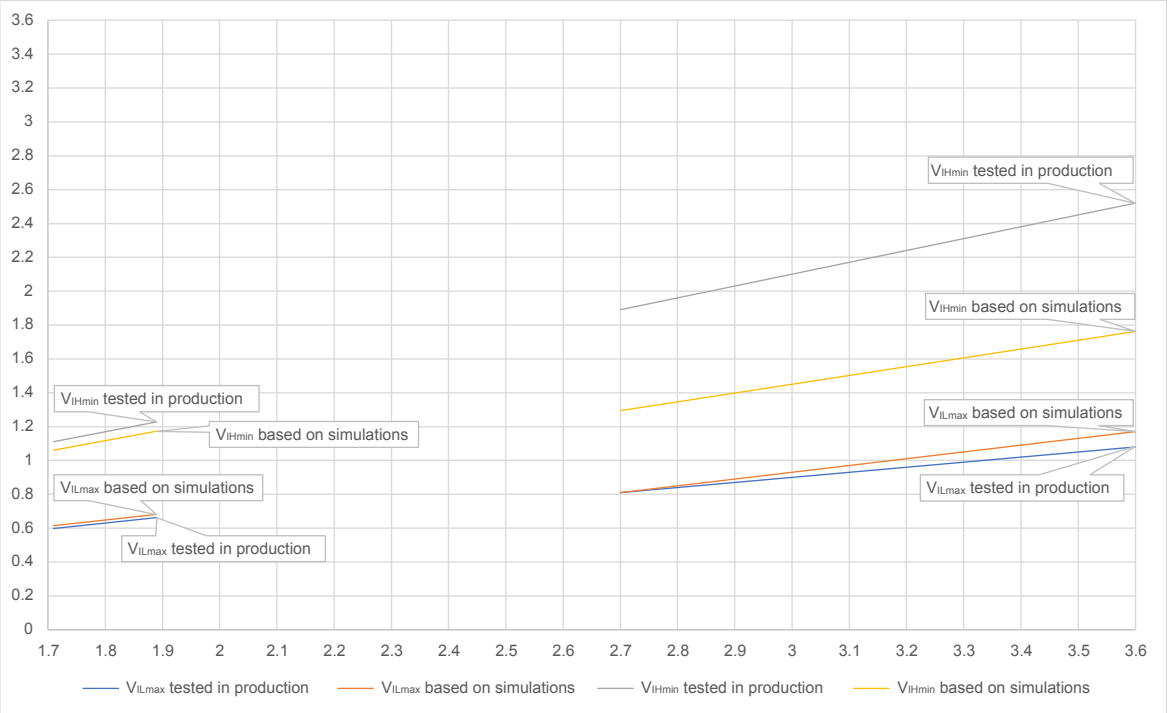
Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{PD}	Weak pull-down equivalent resistor[3]	$2.7 < V_{DDx} < 3.6$ V	30	40	50	kΩ
		$1.71 < V_{DDx} < 1.89$ V	30	40	50	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. *Guaranteed by testing.*
2. *Specified by design, not tested in production.*
3. *The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).*

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for TT I/Os is shown in Figure 19 .

Figure 19. V_{IL}/V_{IH} for TT I/Os



6.3.16.1 *Output driving current*

The GPIOs (general purpose input/outputs) can sink or source up to ±20 mA (depending on speed setup, supply voltage range and temperature).

In the user application, I/O drive current must be limited to respect the absolute maximum rating specified in Section 6.2 , in particular:

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum Run mode consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see Table 15).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run mode consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see Table 15).

6.3.16.2 *Output voltage levels*

Unless otherwise specified, the parameters given in Table 63 are derived from tests performed under ambient temperature and supply voltage conditions summarized in Table 17. General operating conditions . All I/Os are CMOS and TTL compliant.

Prerelease product(s)

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Table 63. Output voltage characteristics for all I/Os except those on V_{SW}

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions[1] [2] [3] [4]	Min	Max	Unit
V_{OL}	Output low level voltage (3.3 V range, 2.7 < V_{DDx} < 3.6 V)	I_{IO} = 6.5 mA, Speed = 0b00	-	0.4	V
		I_{IO} = 10 mA, Speed = 0b01	-	0.4	
		I_{IO} = 13 mA, Speed = 0b10	-	0.4	
		I_{IO} = 20 mA, Speed = 0b11	-	0.4	
V_{OH}	Output high level voltage (3.3 V range, 2.7 < V_{DDx} < 3.6 V)	I_{IO} = 6.5 mA, Speed = 0b00	V_{DDx} - 0.4	-	V
		I_{IO} = 10 mA, Speed = 0b01	V_{DDx} - 0.4	-	V
		I_{IO} = 13 mA, Speed = 0b10	V_{DDx} - 0.4	-	V
		I_{IO} = 20 mA, Speed = 0b11	V_{DDx} - 0.4	-	V
V_{OL}	Output low level voltage (1.8 V range, 1.71 < V_{DDx} < 1.89 V)	I_{IO} = 5.5 mA, Speed = 0b00	-	0.4	V
		I_{IO} = 8 mA, Speed = 0b01	-	0.4	V
		I_{IO} = 11 mA, Speed = 0b10	-	0.4	V
		I_{IO} = 16 mA, Speed = 0b11	-	0.4	V
V_{OH}	Output high level voltage (1.8 V range, 1.71 < V_{DDx} < 1.89 V)	I_{IO} = 5.5 mA, Speed = 0b00	V_{DDx} - 0.4	-	V
		I_{IO} = 8m A, Speed = 0b01	V_{DDx} - 0.4	-	V
		I_{IO} = 11 mA, Speed = 0b10	V_{DDx} - 0.4	-	V
		I_{IO} = 16 mA, Speed = 0b11	V_{DDx} - 0.4	-	V

1. *110 <T_J < 120: 4 mA.*
2. *90 < T_J < 110: 10 mA.*
3. *T_J < 90: 20 mA.*
4. *Maximum current depend on temperature.*

Table 64. Output voltage characteristics for I/Os supplied by V_{SW}

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
TBD	TBD	-	-	-	TBD

6.3.16.3 *Output buffer timing characteristics*

Table 65. Output timing characteristics (V_{DD} = 3.0 - 3.6 V or V_{DDIOx} = 2.7 - 3.6 V, VDDIOxVRSEL = 0)

Evaluated by characterization, not tested in production unless otherwise specified.

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
0b00	Fmax[1]	Maximum frequency	C = 50 pF	-	30	MHz
			C = 40 pF	-	35	
			C = 30 pF	-	45	
			C = 20 pF	-	67	
			C = 10 pF	-	110	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	11.7	ns
			C = 40 pF	-	9.5	
			C = 30 pF	-	7.3	

Prerelease product(s)

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Speed	Symbol	Parameter	Conditions	Min	Max	Unit
0b00	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 20 pF	-	5.2	ns
			C = 10 pF	-	3	
0b01	Fmax[1]	Maximum frequency	C = 50 pF	-	45	MHz
			C = 40 pF	-	55	
			C = 30 pF	-	70	
			C = 20 pF	-	100	
			C = 10 pF	-	166	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	8.1	ns
			C = 40 pF	-	6.7	
			C = 30 pF	-	5.2	
			C = 20 pF	-	3.6	
			C = 10 pF	-	2.2	
0b10[3]	Fmax[1]	Maximum frequency	C = 50 pF	-	60	MHz
			C = 40 pF	-	75	
			C = 30 pF	-	100	
			C = 20 pF	-	133	
			C = 10 pF	-	190	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	6.3	ns
			C = 40 pF	-	5.1	
			C = 30 pF	-	4	
			C = 20 pF	-	2.9	
			C = 10 pF	-	1.8	
0b11[3]	Fmax[1]	Maximum frequency	C = 50 pF	-	80	MHz
			C = 40 pF	-	100	
			C = 30 pF	-	120	
			C = 20 pF	-	166	
			C = 10 pF	-	220	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	4.4	ns
			C = 40 pF	-	3.7	
			C = 30 pF	-	2.9	
			C = 20 pF	-	2.2	
			C = 10 pF	-	1.5	

1. *The maximum frequency is defined with the following conditions : (Tr + Tf) ≤ 2/3 T and Skew ≤ 1/20 T and 45% < Duty cycle < 55%.*
2. *The fall and rise time are defined respectively between 90% and 10%, and between 10% and 90% of the output waveform.*
3. *IO compensation enabled.*

Table 66. Output timing characteristics (V_{DD}/V_{DDIOx} = 1.71 - 1.89 V, VDDIOxVRSEL = 1)

Evaluated by characterization, not tested in production unless otherwise specified.

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
0b00	Fmax[1]	Maximum frequency	C = 50 pF	-	30	MHz
			C = 40 pF	-	35	

Prerelease product(s)

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Speed	Symbol	Parameter	Conditions	Min	Max	Unit
0b00	Fmax[1]	Maximum frequency	C = 30 pF	-	45	MHz
			C = 20 pF	-	67	
			C = 10 pF	-	110	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	11	ns
			C = 40 pF	-	9	
			C = 30 pF	-	7	
			C = 20 pF	-	5	
			C = 10 pF	-	3	
0b01	Fmax[1]	Maximum frequency	C = 50 pF	-	45	MHz
			C = 40 pF	-	55	
			C = 30 pF	-	70	
			C = 20 pF	-	100	
			C = 10 pF	-	166	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	7.4	ns
			C = 40 pF	-	6.1	
			C = 30 pF	-	4.7	
			C = 20 pF	-	3.4	
			C = 10 pF	-	2.1	
0b10[3]	Fmax[1]	Maximum frequency	C = 50 pF	-	60	MHz
			C = 40 pF	-	75	
			C = 30 pF	-	100	
			C = 20 pF	-	133	
			C = 10 pF	-	200	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	5.7	ns
			C = 40 pF	-	4.7	
			C = 30 pF	-	3.7	
			C = 20 pF	-	2.7	
			C = 10 pF	-	1.7	
0b11[3]	Fmax[1]	Maximum frequency	C = 50 pF	-	80	MHz
			C = 40 pF	-	100	
			C = 30 pF	-	120	
			C = 20 pF	-	166	
			C = 10 pF	-	250	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	4.1	ns
			C = 40 pF	-	3.4	
			C = 30 pF	-	2.7	
			C = 20 pF	-	2	
			C = 10 pF	-	1.3	

1. *The maximum frequency is defined with the following conditions : (Tr + Tf) ≤ 2/3 T and Skew ≤ 1/20 T and 45% < Duty cycle < 55%.*
2. *The fall and rise time are defined respectively between 90% and 10%, and between 10% and 90% of the output waveform.*
3. *IO compensation enabled.*

Prerelease product(s)

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Table 67. Output timing characteristics (V_{DD}/V_{DDIOx} = 1.71 - 1.89 V, VDDIOxVRSEL = 0 degraded mode)

Evaluated by characterization, not tested in production unless otherwise specified.

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
0b00	Fmax(1)	Maximum frequency	C 50 pF	-	10	MHz
			C = 40 pF	-	15	
			C = 30 pF	-	20	
			C = 20 pF	-	33	
			C = 10 pF	-	45	
	Tr/Tf(2)	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	30.2	ns
			C = 40 pF	-	24.4	
			C = 30 pF	-	18.7	
			C = 20 pF	-	13	
			C = 10 pF	-	7.4	
0b01	Fmax(1)	Maximum frequency	C = 50 pF	-	15	MHz
			C = 40 pF	-	20	
			C = 30 pF	-	25	
			C = 20 pF	-	37	
			C = 10 pF	-	60	
	Tr/Tf(2)	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	21.1	ns
			C = 40 pF	-	17.2	
			C = 30 pF	-	13.3	
			C = 20 pF	-	9.4	
			C = 10 pF	-	5.5	
0b10(3)	Fmax(1)	Maximum frequency	C = 50 pF	-	20	MHz
			C = 40 pF	-	25	
			C = 30 pF	-	30	
			C = 20 pF	-	45	
			C = 10 pF	-	75	
	Tr/Tf(2)	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	17	ns
			C = 40 pF	-	13.9	
			C = 30 pF	-	10.8	
			C = 20 pF	-	7.8	
			C = 10 pF	-	4.5	
0b11(3)	Fmax(1)	Maximum frequency	C = 50 pF	-	30	MHz
			C = 40 pF	-	35	
			C = 30 pF	-	45	
			C = 20 pF	-	60	
			C = 10 pF	-	85	
	Tr/Tf(2)	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	11.8	ns
			C = 40 pF	-	9.8	
			C = 30 pF	-	7.9	
			C = 20 pF	-	5.8	

Prerelease product(s)

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Speed	Symbol	Parameter	Conditions	Min	Max	Unit
0b11[3]	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 10 pF	-	3.8	ns

1. *The maximum frequency is defined with the following conditions : (Tr + Tf) ≤ 2/3 T and Skew ≤ 1/20 T and 45% < Duty cycle < 55%.*
2. *The fall and rise time are defined respectively between 90% and 10%, and between 10% and 90% of the output waveform.*
3. *IO compensation enabled.*

Table 68. GPIO advance config delay characteristics (WARNING: DUMMY DATA TBD)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{init}	Initial delay	-	0	-	0.05	ps
t_{Δ}	Unit Delay	-	-	0.25	-	

6.3.17 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see Table 62. I/O static characteristics).

Unless otherwise specified, the parameters given in Table 69 are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Table 17. General operating conditions .

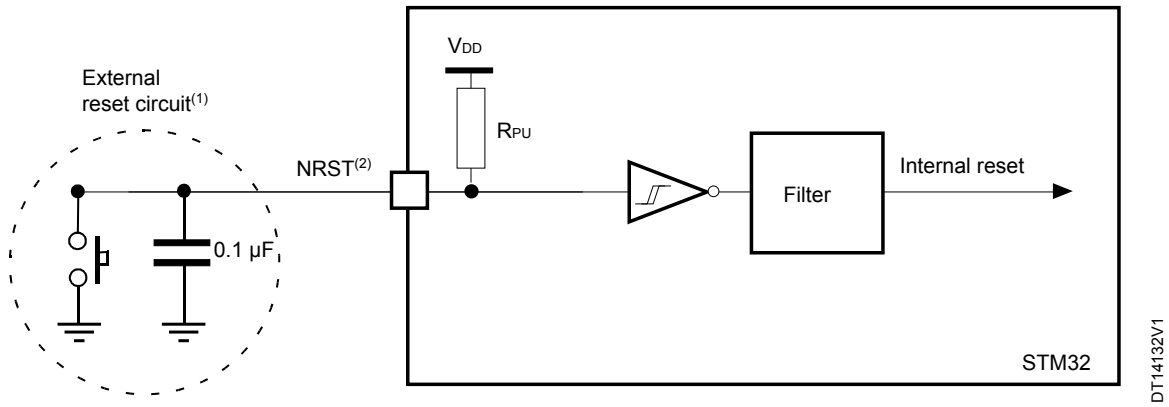
Table 69. NRST pin characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RPU[1]	Weak pull-up equivalent resistor	-	30	40	50	kΩ
tGEN	NRST minimum generated output pulse	-	17.5	-	-	µs
TFILT	NRST input filtered pulse	-	-	-	50	ns
TNFILT	NRST input not filtered pulse	-	150	-	-	ns

1. *The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).*

Figure 20. Recommended NRST pin protection



1. *The reset network protects the device against parasitic resets.*
2. *The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in Table 69 . Otherwise the reset is not taken into account by the device.*

Prerelease product(s)

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6.3.18 DDR IOs characteristics

Refer to JEDEC standards for more details and characteristics

- DDR3L: JESD79-3F with addendum JESD79-3-1A
- DDR4: JESD79-4D
- LPDDR4: JESD209-4D

6.3.19 FMC characteristics

Unless otherwise specified, the parameters given in Table 70 to Table 83. NAND flash write timings for the FMC interface are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in Table 17. General operating conditions , with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: 0.5 × V_{DD}

Refer to I/O port characteristics for more details on the input/output characteristics.

6.3.19.1 Asynchronous waveforms and timings

Figure 21 through Figure 24 represent asynchronous waveforms and Table 70 through Table 77 provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- DataHoldTime = 0x1 (1 × $T_{fmc_ker_ck}$ for read operations and 2 × $T_{fmc_ker_ck}$ for write operations)
- ByteLaneSetup = 0x1
- BusTurnAroundDuration = 0x0
- Capacitive load C_L = 30 pF

In all the timing tables, the $T_{fmc_ker_ck}$ is the fmc_ker_ck clock period.

Table 70. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{fmc_ker_ck}$ - 1	-	$3T_{fmc_ker_ck}$ + 0.5	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	0	-	1	
$t_{w(NOE)}$	FMC_NOE low time	$2T_{fmc_ker_ck}$ - 1	-	$2T_{fmc_ker_ck}$ + 1	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	$T_{fmc_ker_ck}$ - 0.5	-	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	-	1	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	Address held until next read operation			
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	$2T_{fmc_ker_ck}$ + 14	-	-	
$t_{su(Data_NOE)}$	Data to FMC_NOEx high setup time	15	-	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	-	0.5	
$t_{w(NADV)}$	FMC_NADV low time	-	-	$T_{fmc_ker_ck}$ + 0.5	

Table 71. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings

Evaluated by characterization, not tested in production unless otherwise specified.
NWAIT pulse width is equal to 1 clock cycle.

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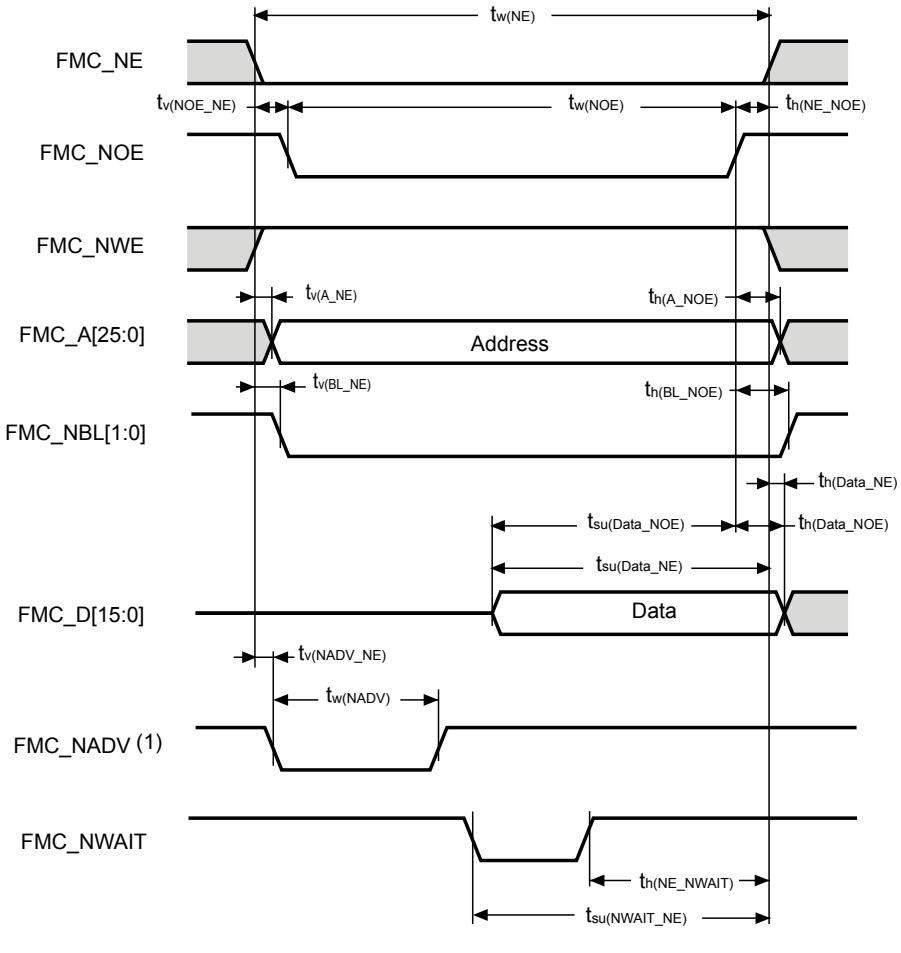
Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{fmc_ker_ck}$ - 0.5	-	$8T_{fmc_ker_ck}$ + 0.5	ns
$t_{w(NOE)}$	FMC_NWE low time	$7T_{fmc_ker_ck}$ - 0.5	-	$7T_{fmc_ker_ck}$ + 0.5	
$t_{w(NWAIT)}$	FMC_NWAIT low time	$T_{fmc_ker_ck}$	-	-	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc_ker_ck}$ + 15	-	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc_ker_ck}$ + 13	-	-	

Figure 21. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. *Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.*

Table 72. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{fmc_ker_ck}$ - 1	-	$3T_{fmc_ker_ck}$ + 1	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc_ker_ck}$ - 1	-	$T_{fmc_ker_ck}$ + 0.5	
$t_{w(NWE)}$	FMC_NWE low time	$T_{fmc_ker_ck}$ - 0.5	-	$T_{fmc_ker_ck}$ + 0.5	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc_ker_ck}$ - 0.5	-	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	-	0	

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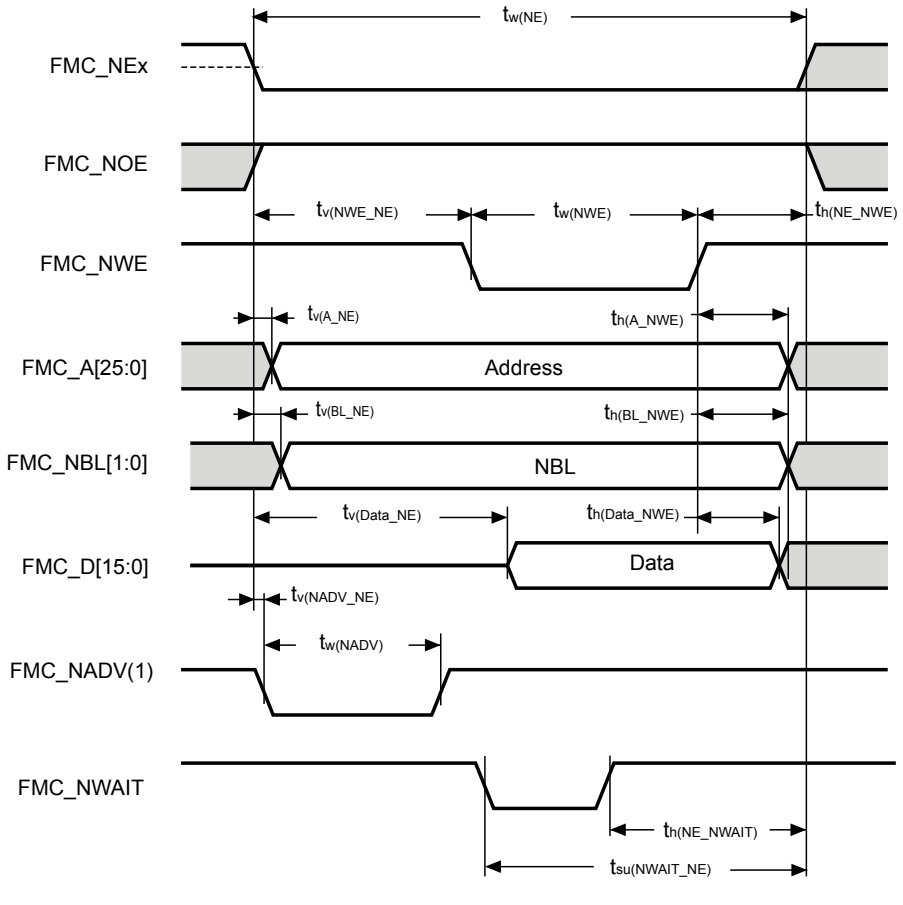
Symbol	Parameter	Min	Typ	Max	Unit
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	$3T_{fmc_ker_ck}$ - 1	-	-	ns
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	-	0.5	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$3T_{fmc_ker_ck}$ + 1	-	-	
$t_{v(Data_NE)}$	Data to FMC_NEx low to Data valid	-	-	2	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	$3T_{fmc_ker_ck}$ - 1	-	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	-	0.5	
$t_{w(NADV)}$	FMC_NADV low time	-	-	$T_{fmc_ker_ck}$ + 1	

Table 73. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings

Evaluated by characterization, not tested in production unless otherwise specified.
NWAIT pulse width is equal to 1 clock cycle.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{fmc_ker_ck}$ - 1	-	$8T_{fmc_ker_ck}$ + 0.5	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{fmc_ker_ck}$ - 1	-	$6T_{fmc_ker_ck}$ + 0.5	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc_ker_ck}$ + 15	-	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc_ker_ck}$ + 13	-	-	

Figure 22. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



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1. *Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.*

Table 74. Asynchronous multiplexed PSRAM/NOR read timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{fmc_ker_ck} - 1$	-	$4T_{fmc_ker_ck} + 0.5$	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{fmc_ker_ck} - 1$	-	$2T_{fmc_ker_ck} + 0.5$	
$t_{tw(NOE)}$	FMC_NOE low time	$T_{fmc_ker_ck} - 1$	-	$T_{fmc_ker_ck} + 0.5$	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	$T_{fmc_ker_ck}$	-	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	-	2	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	-	0.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc_ker_ck} - 1$	-	$T_{fmc_ker_ck} + 0.5$	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{fmc_ker_ck} - 3$	-	-	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	Address held until next read operation			
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	$T_{fmc_ker_ck} + 14$	-	-	
$t_{su(Data_NOE)}$	Data to FMC_NOE high setup time	15	-	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	-	

Table 75. Asynchronous multiplexed PSRAM/NOR read - NWAIT timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{fmc_ker_ck} - 1$	-	$9T_{fmc_ker_ck} + 0.5$	ns
$t_{w(NOE)}$	FMC_NWE low time	$6T_{fmc_ker_ck} - 1$	-	$6T_{fmc_ker_ck} + 0.5$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc_ker_ck} + 15$	-	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc_ker_ck} + 13$	-	-	

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Figure 23. Asynchronous multiplexed PSRAM/NOR read waveforms

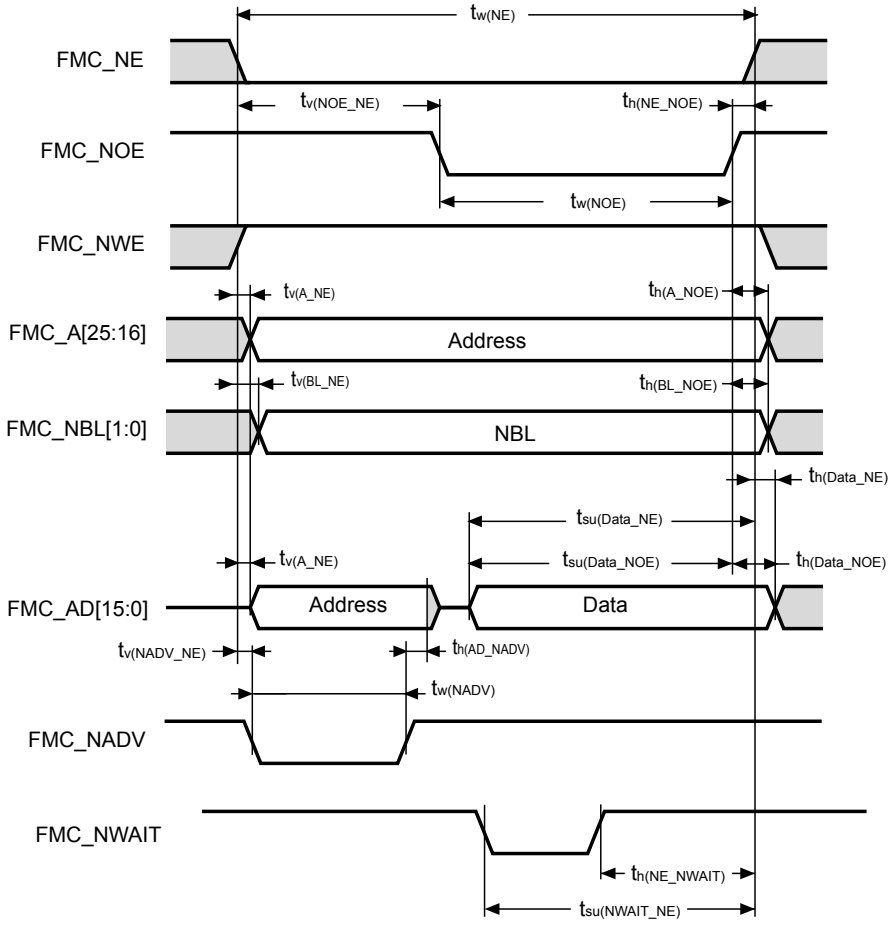

Table 76. Asynchronous multiplexed PSRAM/NOR write timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{fmc_ker_ck}$ - 1	-	$4T_{fmc_ker_ck}$ + 1	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc_ker_ck}$ - 1	-	$T_{fmc_ker_ck}$ + 0.5	
$t_{w(NWE)}$	FMC_NWE low time	$2T_{fmc_ker_ck}$ - 0.5	-	$2T_{fmc_ker_ck}$ + 0.5	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc_ker_ck}$ - 0.5	-	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	-	1.5	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	-	0.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc_ker_ck}$ - 1	-	$T_{fmc_ker_ck}$ + 1	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{fmc_ker_ck}$ - 1	-	-	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	$3T_{fmc_ker_ck}$ - 1	-	-	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$3T_{fmc_ker_ck}$ + 1	-	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	-	0	
$t_{v(Data_NADV)}$	FMC_NADV high to Data valid	-	-	$T_{fmc_ker_ck}$ + 1	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	$3T_{fmc_ker_ck}$ - 1	-	-	

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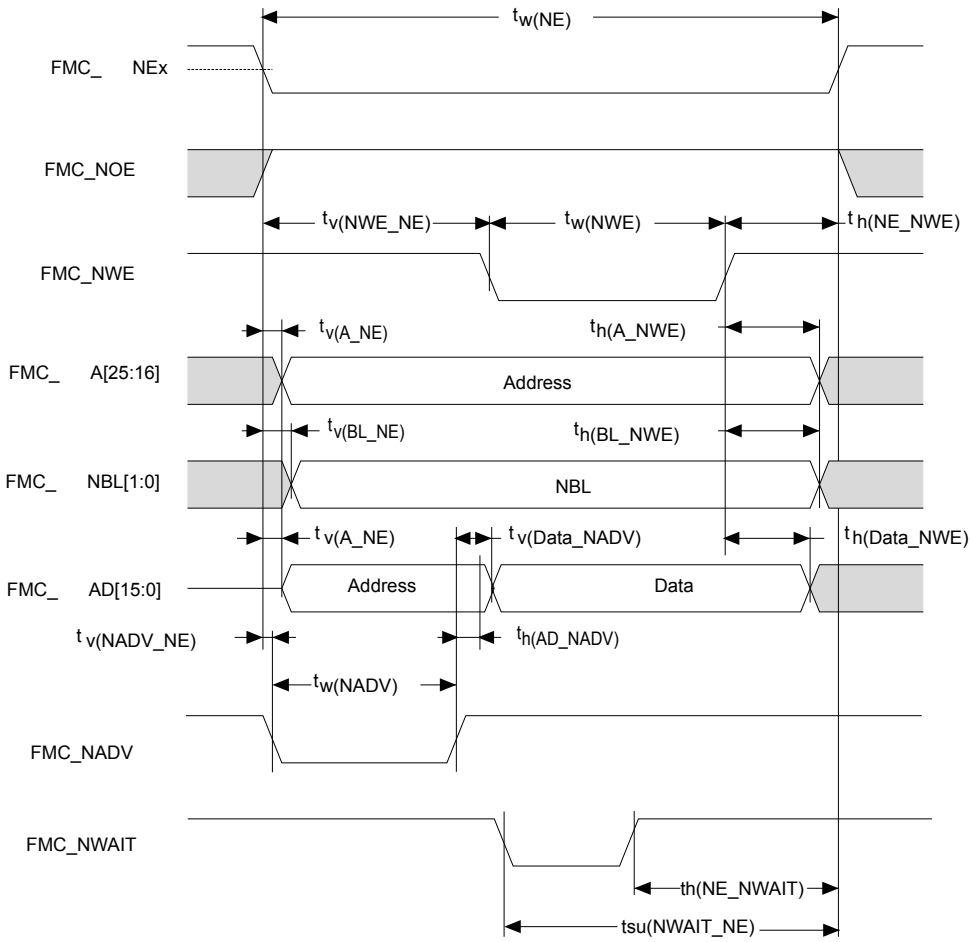
Table 77. Asynchronous multiplexed PSRAM/NOR write - NWAIT timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{fmc_ker_ck}$ - 1	-	$9T_{fmc_ker_ck}$ + 0.5	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{fmc_ker_ck}$ - 1	-	$7T_{fmc_ker_ck}$ + 0.5	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc_ker_ck}$ + 15	-	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$6T_{fmc_ker_ck}$ + 13	-	-	

Figure 24. Asynchronous multiplexed PSRAM/NOR write waveforms



6.3.19.2 *Synchronous waveforms and timings*

Figure 25 through Figure 28 represent synchronous waveforms and Table 78 through Table 81 provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR flash; DataLatency = 0 for PSRAM

In all the timing tables, the $T_{fmc_ker_ck}$ is the fmc_ker_ck clock period, with the following FMC_CLK maximum values:

- For 3.0 V < V_{DD} < 3.6 V, FMC_CLK = 70 MHz at 20 pF

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- For 1.71 V < V_{DD} < 1.89 V, FMC_CLK = 70 MHz at 20 pF

Table 78. Synchronous non-multiplexed NOR/PSRAM read timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	R × $T_{fmc_ker_ck}$ - 0.5[1]	-	-	ns
$t_{(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x = 0..2)	-	-	2.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x = 0..2)	R × $T_{fmc_ker_ck}$ / 2 + 1.5[1]	-	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	-	2.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0.5	-	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x = 16..25)	-	-	0	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x = 16..25)	R × $T_{fmc_ker_ck}$ / 2 + 0.5[1]	-	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	-	0	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	R × $T_{fmc_ker_ck}$ / 2 + 1[1]	-	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	3.5	-	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	2	-	-	
$t_{(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	4	-	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1	-	-	

1. Clock ratio R = (FMC_CLK period / fmc_ker_ck period).

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Figure 25. Synchronous non-multiplexed NOR/PSRAM read timings

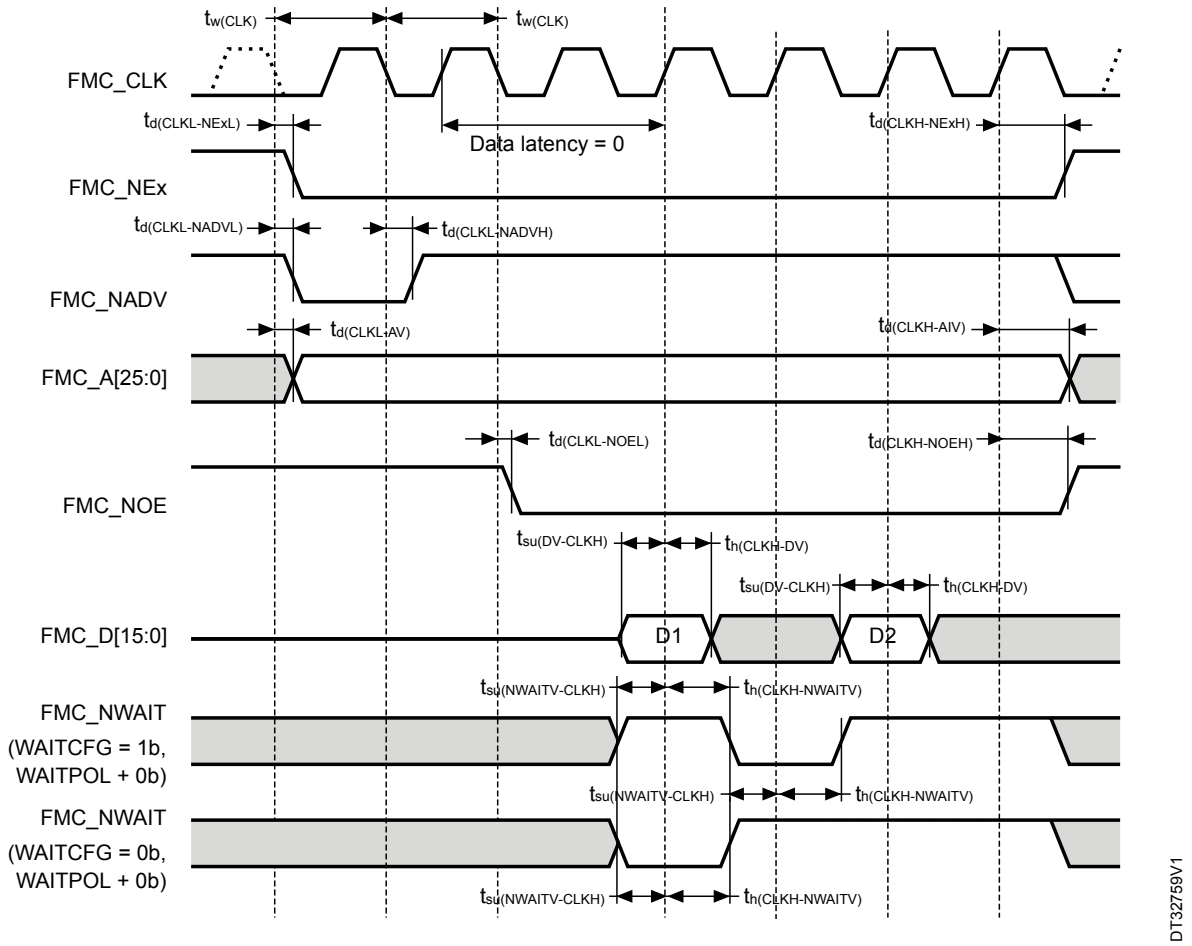

Table 79. Synchronous non-multiplexed PSRAM write timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{(CLK)}$	FMC_CLK period	$R \times T_{fmc_ker_ck}$ -0.5[(1)]	-	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x = 0..2)	-	-	1.5	
$t_{(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x = 0..2)	$R \times T_{fmc_ker_ck} / 2 + 0.5$[(1)]	-	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	-	1.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0.5	-	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x = 16..25)	-	-	0	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x = 16..25)	$R \times T_{fmc_ker_ck} / 2 + 0.5$[(1)]	-	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	-	1	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$R \times T_{fmc_ker_ck} / 2$[(1)]	-	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	-	3	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	-	0	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$R \times T_{fmc_ker_ck} / 2 + 2$[(1)]	-	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	4	-	-	

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Symbol	Parameter	Min	Typ	Max	Unit
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1	-	-	ns

1. *Clock ratio R = (FMC_CLK period / fmc_ker_ck period).*

Figure 26. Synchronous non-multiplexed PSRAM write timings

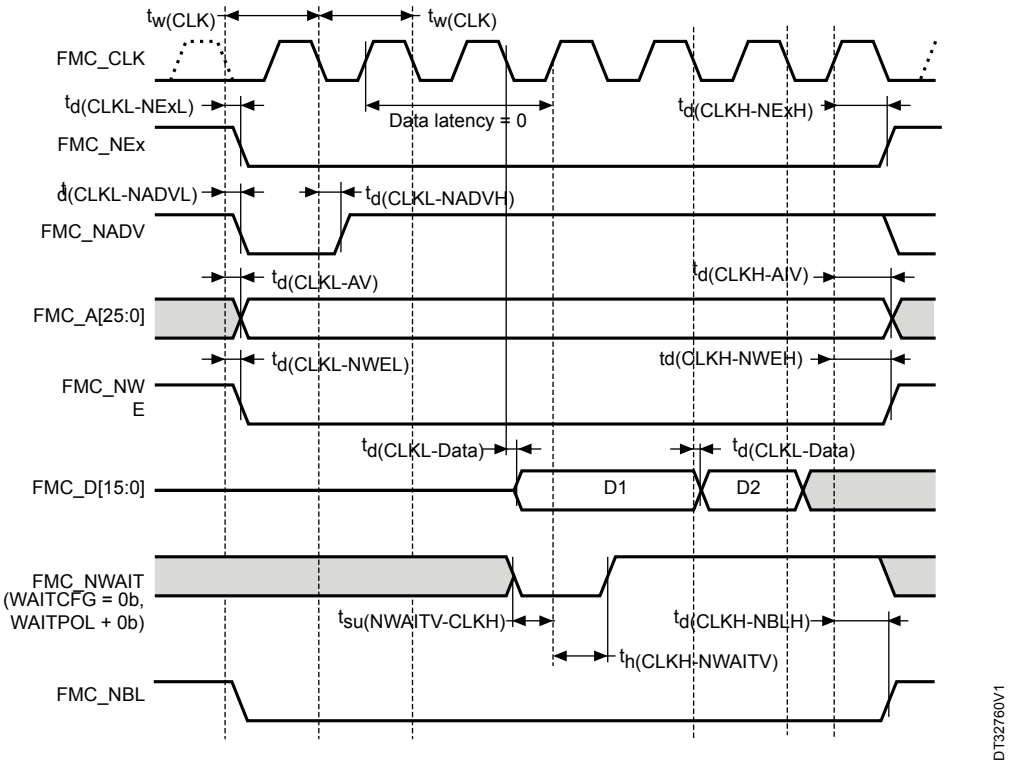

Table 80. Synchronous multiplexed NOR/PSRAM read timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$R \times T_{fmc_ker_ck} - 0.5$[1]	-	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x = 0..2)	-	-	2.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x = 0..2)	$R \times T_{fmc_ker_ck} / 2 + 1.5$[1]	-	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	-	2.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0.5	-	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x = 16..25)	-	-	0	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x = 16..25)	$R \times T_{fmc_ker_ck} / 2 + 0.5$[1]	-	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	-	0	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$R \times T_{fmc_ker_ck} / 2 + 1$[1]	-	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0.5	-	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	3.5	-	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	2	-	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	4	-	-	

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Symbol	Parameter	Min	Typ	Max	Unit
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1	-	-	ns

1. *Clock ratio R = (FMC_CLK period / fmc_ker_ck period).*

Figure 27. Synchronous multiplexed NOR/PSRAM read timings

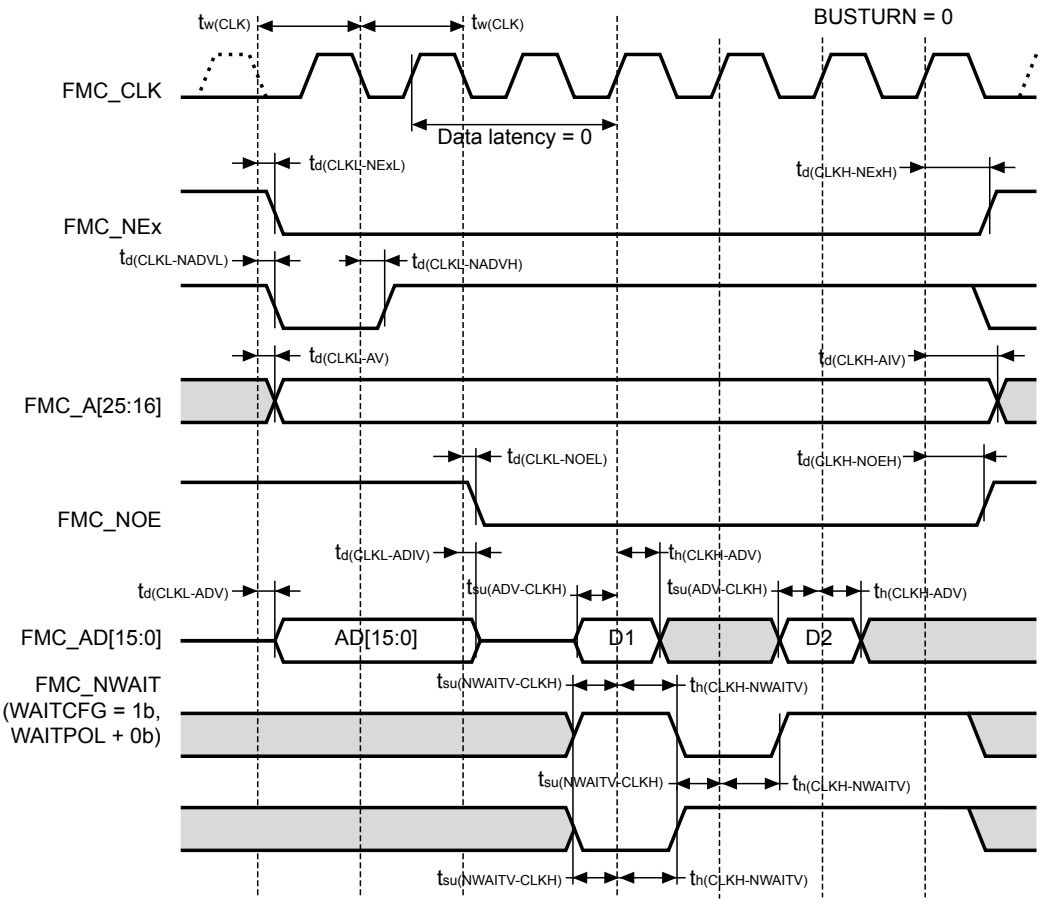

Table 81. Synchronous multiplexed PSRAM write timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(CLK)}$	FMC_CLK period, V_{DD} range = 2.7 to 3.6 V	R × $T_{fmc_ker_ck}$ - 0.5[(1)]	-	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x = 0..2)	-	-	1.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x = 0..2)	R × $T_{fmc_ker_ck}$ / 2 + 0.5[(1)]	-	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	-	2	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0.5	-	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x = 16..25)	-	-	0	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x = 16..25)	R × $T_{fmc_ker_ck}$ / 2 + 0.5[(1)]	-	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	-	1	
$t_{(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	R × $T_{fmc_ker_ck}$ / 2[(1)]	-	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	-	3	

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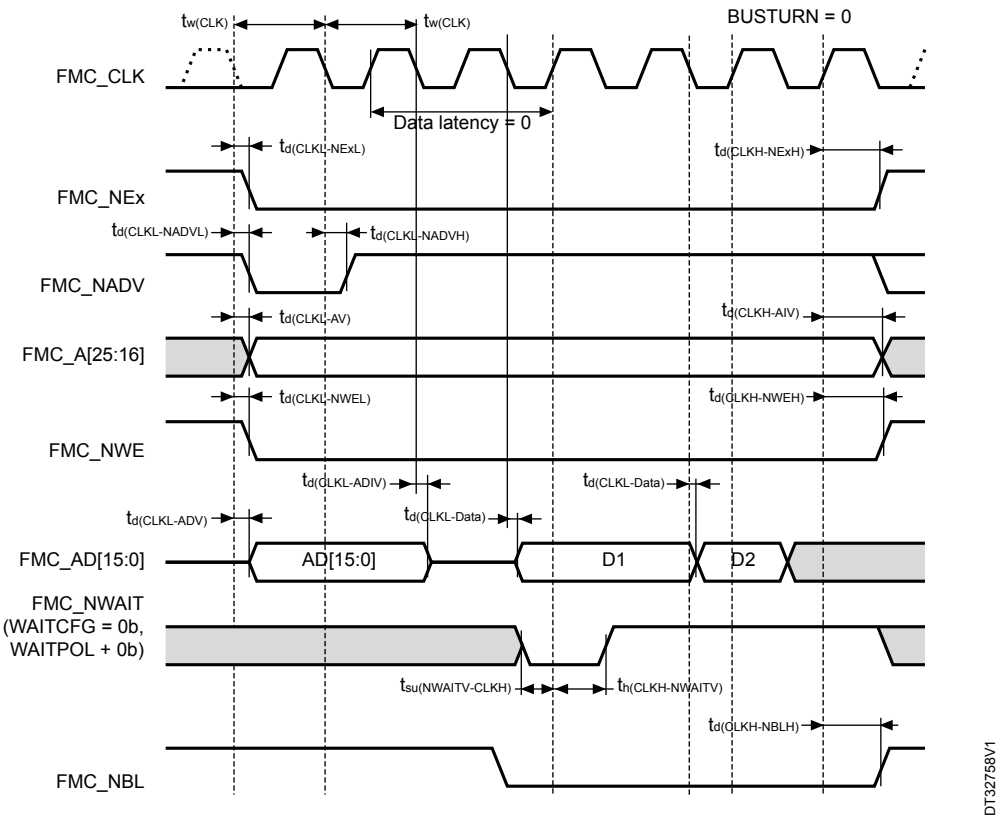
Symbol	Parameter	Min	Typ	Max	Unit
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0.5	-	-	ns
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	-	3	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	0	-	-	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$R \times T_{fmc_ker_ck} / 2 + 2$[1]	-	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	4	-	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1	-	-	

1. *Clock ratio R = (FMC_CLK period / fmc_ker_ck period).*

Figure 28. Synchronous multiplexed PSRAM write timings



6.3.19.3 *NAND controller waveforms and timings*

Figure 29 and Figure 30 represent synchronous waveforms, and Table 82 and Table 83 provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- FMC_SetupTime = 0x01
- FMC_WaitSetupTime = 0x03
- FMC_HoldSetupTime = 0x02
- FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0

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- C_L = 30-pF

In all timing tables, the $T_{fmc_ker_ck}$ is the fmc_ker_ck clock period.

Table 82. NAND flash read timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(N0E)}$	FMC_NOE low width	$4T_{fmc_ker_ck}$ - 0.5	-	$4T_{fmc_ker_ck}$ + 0.5	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	12.5	-	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	-	
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	-	$2T_{fmc_ker_ck}$ + 1.5	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$3T_{fmc_ker_ck}$ - 1	-	-	

Figure 29. NAND controller waveforms for read access

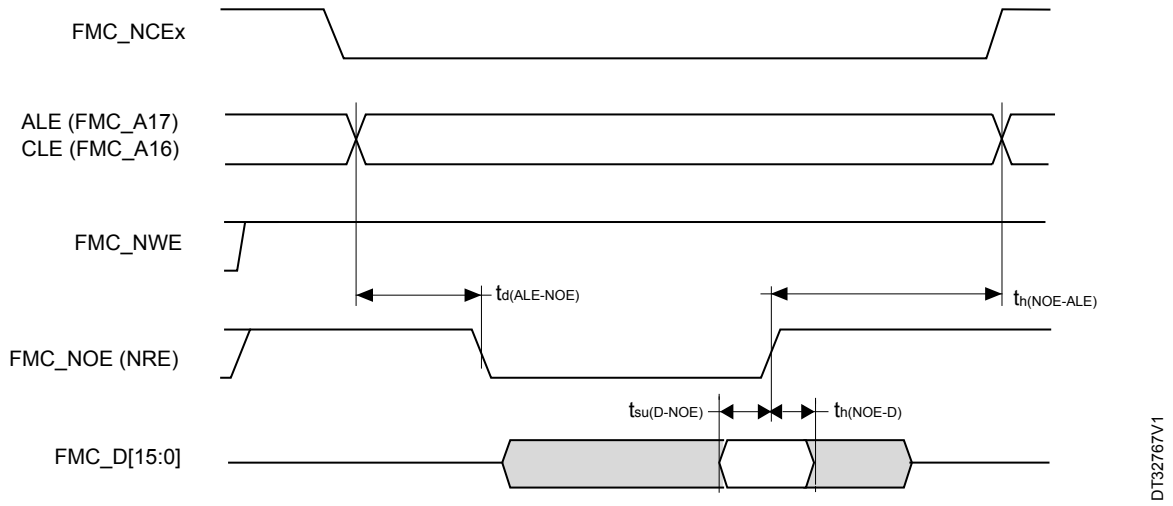

Table 83. NAND flash write timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(NWE)}$	FMC_NWE low width	$4T_{fmc_ker_ck}$ - 1	-	$4T_{fmc_ker_ck}$ + 1	
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	0	-	-	
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$5T_{fmc_ker_ck}$ - 1	-	-	
$t_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$4T_{fmc_ker_ck}$ - 1	-	-	
$t_{d(ALE-NWE)}$	FMC_ALE valid before FMC_NWE low	-	-	$2T_{fmc_ker_ck}$ + 1.5	
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$3T_{fmc_ker_ck}$ - 1	-	-	

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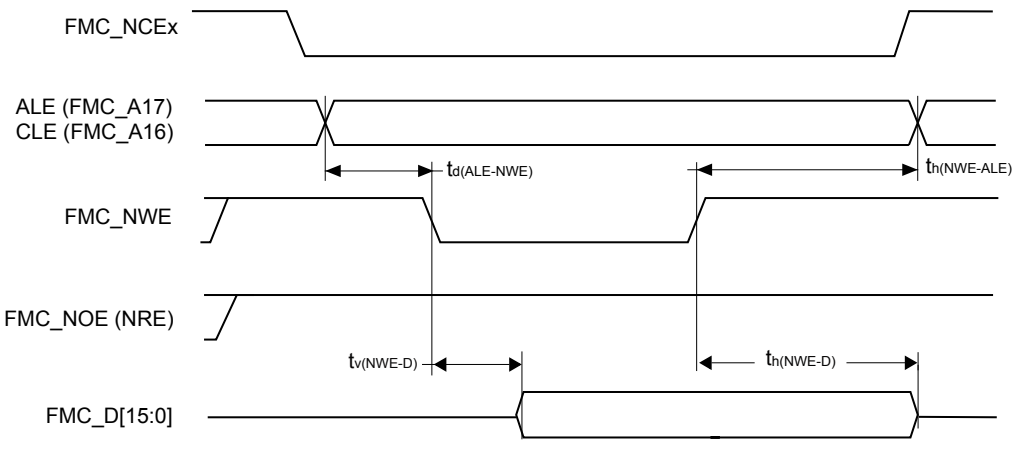
Figure 30. NAND controller waveforms for write access



6.3.20 OCTOSPI interface characteristics

Unless otherwise specified, the parameters given in Table 84 , Table 85 and Table 86 for OCTOSPI are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions , with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- or DTR(with DQS)/HyperBus the delay resister is set to DLYCFGR[3:0]=4

Refer to Section 6.3.16: I/O port characteristics for more details on the input/output alternate function characteristics.

Table 84. OCTOSPI characteristics in SDR mode (WARNING: DUMMY DATA TBD)

Evaluated by characterization, not tested in production unless otherwise specified.
Values in the table applies to octal and quad SPI mode.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{(CLK)}$	Clock frequency	$2.7 < V_{DDIOx} < 3.6$, C_L = 15 pF	-	-	175	MHz
		$1.31 < V_{DDIOx} < 1.89$, C_L = 15p F	-	-	150	
$t_{w(CLKH)}$	Clock high and low time - Even division	PRESCALER[7:0] = n = 0,1,3,5	$t_{(CLK)}$ / 2	-	$t_{(CLK)}$/2 +1	ns
$t_{w(CLKL)}$			$t_{(CLK)}$/2 - 1	-	$t_{(CLK)}$/2	
$t_{w(CLKH)}$	Clock high and low time - Odd division	PRESCALER[7:0] = n = 2,4,6,8	(n/2) × $t_{(CLK)}$ / (n+1)	-	(n/2) × $t_{(CLK)}$ / (n+1) + 1	
$t_{w(CLKL)}$			(n/2+1) × $t_{(CLK)}$ / (n+1) - 1	-	(n/2+1) × $t_{(CLK)}$ / (n+1)	
$t_{s(IN)}$	Data input setup time	-	0.5	-	-	
$t_{h(IN)}$	Data input hold time	-	1.5	-	-	
$t_{v(OUT)}$	Data output valid time	-	-	0.5	1	

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Figure 31. OCTOSPI timing diagram - SDR mode

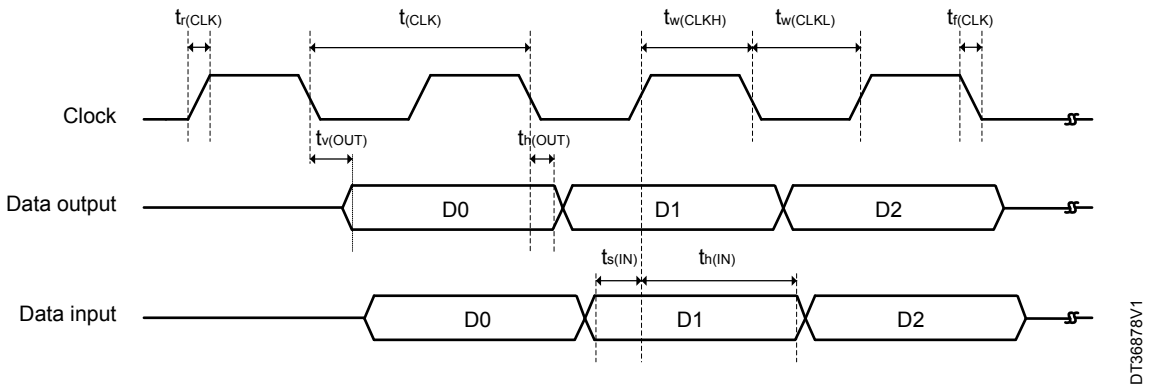

Table 85. OCTOSPI characteristics in DTR mode (without DQS) (WARNING: DUMMY DATA TBD)

Evaluated by characterization, not tested in production unless otherwise specified.
Values in the table applies to octal and quad SPI mode.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{(CLK)}$	Clock frequency	$2.7 < V_{DDIOx} < 3.6$, C_L = 15 pF	-	-	170	MHz
		$1.31 < V_{DDIOx} < 1.89$, C_L = 15 pF	-	-	130	
$t_{w(CLKH)}$	Clock high and low time - Even division	PRESCALER[7:0] = n = 0,1,3,5	$t_{(CLK)}$ / 2	-	$t_{(CLK)}$ / 2 + 1	ns
$t_{w(CLKL)}$			$t_{(CLK)}$/ 2 - 1	-	$t_{(CLK)}$ / 2	
$t_{w(CLKH)}$	Clock high and low time - Odd division	PRESCALER[7:0] = n = 2,4,6,8	(n/2) × $t_{(CLK)}$ / (n+1)	-	(n/2) × $t_{(CLK)}$ / (n+1) + 1	
$t_{w(CLKL)}$			(n/2+1) × $t_{(CLK)}$ / (n+1) - 1	-	(n/2+1) × $t_{(CLK)}$ / (n+1)	
$t_{sr(IN)}$, $t_{sf(IN)}$	Data input setup time	-	0.5	-	-	
$t_{hr(IN)}$, $t_{hf(IN)}$	Data input hold time	-	2.5	-	-	
$t_{vr(OUT)}$, $t_{vf(OUT)}$	Data output valid time	-	-	0.5 + $t_{(CLK)}$ / 4	1 + $t_{(CLK)}$ / 4	
			-	8.5[(1)]	9[(1)]	
$t_{hr(OUT)}$, $t_{hf(OUT)}$	Data output hold time	-	$t_{(CLK)}$ / 4 - 0.5	-	-	
			6.5[(1)]	-	-	

1. *With prescaler = 0 and F(CLK) < 40 MHz.*

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Figure 32. OCTOSPI timing diagram - DTR mode

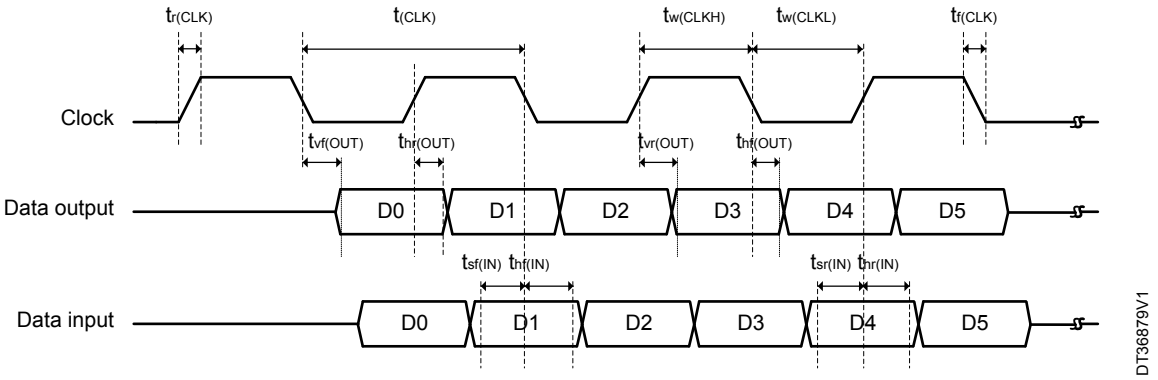

Table 86. OCTOSPI characteristics in DTR mode (with DQS or HyperBus) (WARNING: DUMMY DATA TBD)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{(CLK)}$	Clock frequency	2.7 < V_{DDIOx} < 3.6, C_L = 15 pF	-	-	195	MHz
		1.31 < V_{DDIOx} < 1.89, C_L = 15 pF	-	-	190	
$t_{w(CLKH)}$	Clock high and low time - Even division	PRESCALER[7:0] = n = 0,1,3,5	$t_{(CLK)}$ / 2	-	$t_{(CLK)}$ / 2 + 1	ns
$t_{w(CLKL)}$			$t_{(CLK)}$ / 2 - 1	-	$t_{(CLK)}$ / 2	
$t_{w(CLKH)}$	Clock high and low time - Odd division	PRESCALER[7:0] = n = 2,4,6,8	(n/2) × $t_{(CLK)}$ / (n+1)	-	(n/2) × $t_{(CLK)}$ / (n+1) + 1	
$t_{w(CLKL)}$			(n/2+1) × $t_{(CLK)}$ / (n+1) - 1	-	(n/2+1) × $t_{(CLK)}$ / (n+1)	
$t_{w(CS)}$	Chip select high time	-	3 × $t_{(CLK)}$	-	-	
$t_{v(CK)}$	CS to Clock valid time	-	-	-	$t_{(CLK)}$ + 1	
$t_{h(CK)}$	Clock to CS high hold time	-	$t_{(CLK)}$ / 2	-	-	
$V_{ODr(CK)}$	CK,CK# crossing level on CK rising edge	V_{DDIOx} = 1.8 V	1045	-	1365	
$V_{ODf(CK)}$	CK,CK# crossing level on CK falling edge	V_{DDIOx} = 1.8 V	958	-	1234	
$t_{sr(DQ)}$, $t_{sf(DQ)}$	Data input setup time	-	1.5 - $t_{(CLK)}$ / 4	-	-	
			-6[(1)]			
$t_{hrDQN)}$, $t_{hf(DQ)}$	Data input hold time	-	2 + $t_{(CLK)}$ / 4	-	-	
			9[(1)]			
$t_{v(DS)}$	Data strobe input valid time	-	0	-	-	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{h(DS)}$	Data strobe input hold time	-	0	-	-	ns
$t_{v(RWDS)}$	Data strobe output valid time	-	-	-	$3 \times t_{(CLK)}$	
$t_{vr(OUT)}$, $t_{vf(OUT)}$	Data output valid time	-	-	$0.5 + t_{(CLK)} / 4$	$1 + t_{(CLK)} / 4$	
				8.5[1]	9[1]	
$t_{hr(OUT)}$, $t_{hf(OUT)}$	Data output hold time	-	$t_{(CLK)} / 4 - 0.5$	-	-	
			6.5[1]			

1. *With prescaler = 0 and F(CLK) < 40 MHz.*

Figure 33. OCTOSPI HyperBus clock

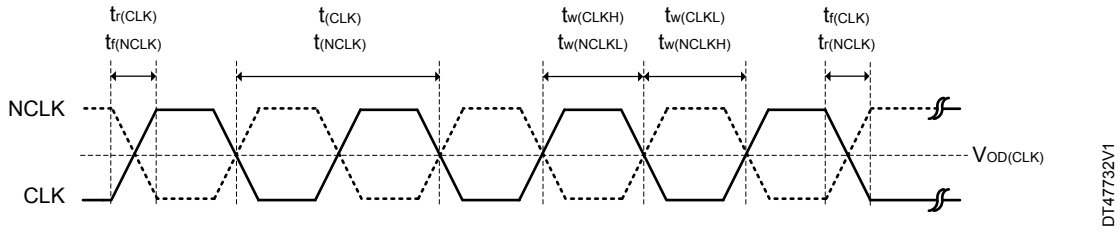

Figure 34. OCTOSPI HyperBus read

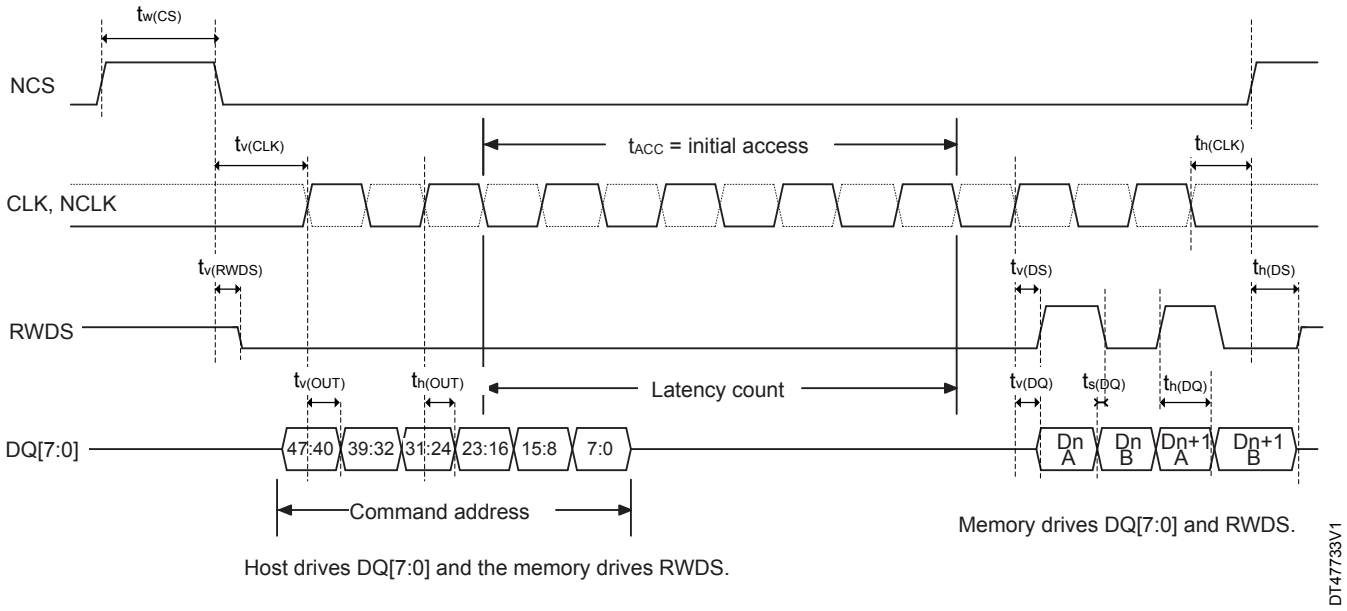

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Figure 35. OCTOSPI HyperBus read with double latency

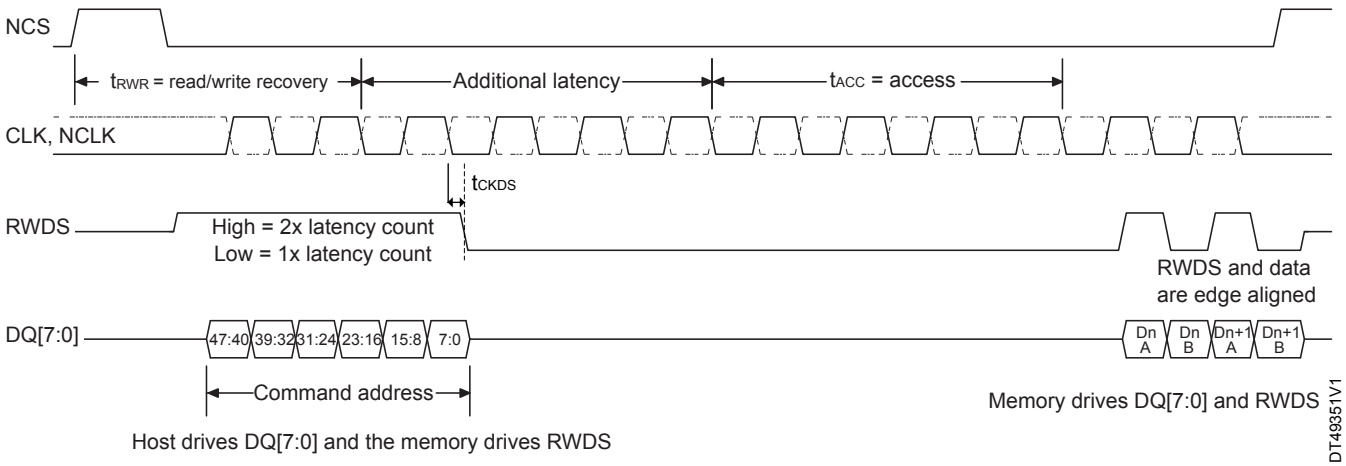
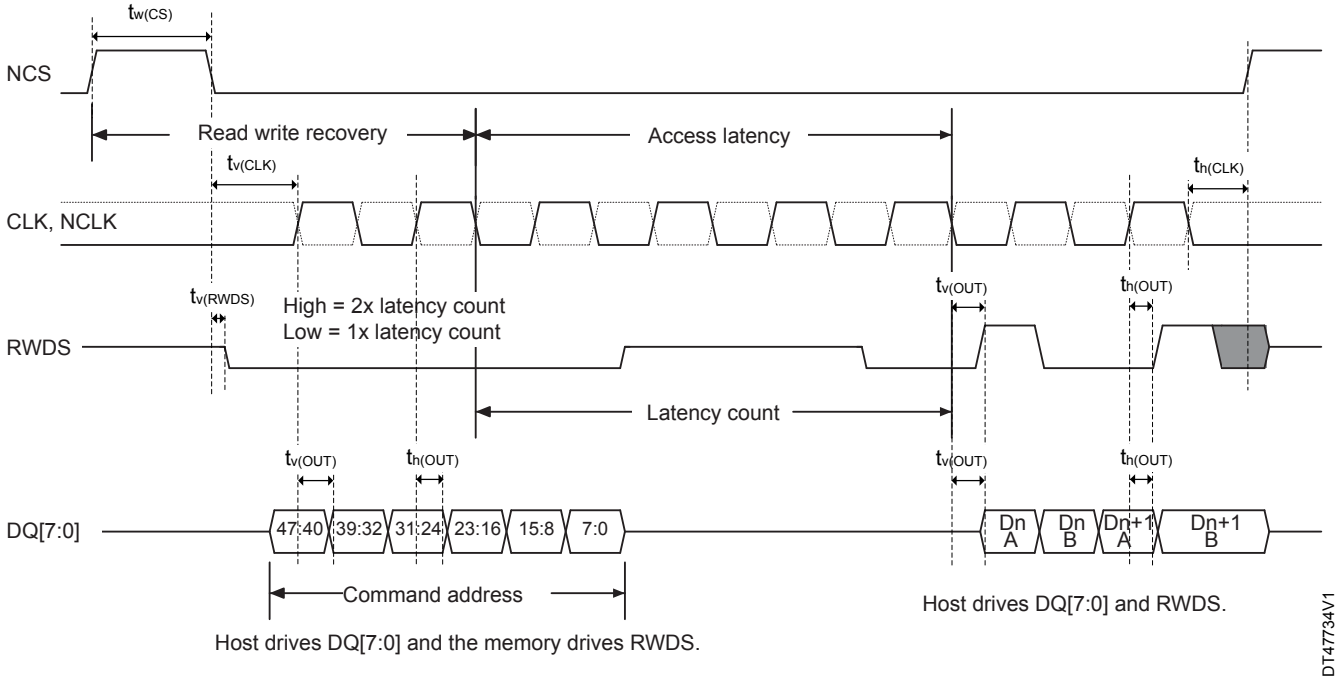


Figure 36. OCTOSPI HyperBus write



6.3.21 Delay block (DLYB) characteristics

Unless otherwise specified, the parameters given in Table 87 for the delay block are derived from tests performed under the ambient temperature and V_{DD} supply voltage summarized in Table 17. General operating conditions .

Table 87. DLYB characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{init}	Initial delay	Bypass mode	100	150	300	ps
t_{Δ}	Unit delay	Bypass mode	30	31	49	
		Lock mode	-	T / 32[(1)]	-	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{Δ}	Unit delay	Lock mode	-1	-	+15	%

1. *T is the period of the DLL clock.*

6.3.22 12-bit ADC characteristics

Unless otherwise specified, the parameters given in Table 88. ADC characteristics are derived from tests performed under the ambient temperature, frequency and V_{DDA} supply voltage conditions summarized in Table 17. General operating conditions.

Table 88. ADC characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency	-	0.7	-	70	MHz
f_s	Sampling rate	resolution = 12 bits	0.05	-	5	MSps
		resolution = 10 bits	0.058	-	5.83	
		resolution = 8 bits	0.07	-	7	
		resolution = 6 bits	0.0875	-	8.75	
tc(1)	Conversion cycle	resolution = 12 bits	-	14	-	1 / f_{ADC}
		resolution = 10 bits	-	12	-	
		resolution = 8 bits	-	10	-	
		resolution = 6 bits	-	8	-	
f_{TRIG}	External trigger frequency	f_{ADC} = 70 MHz, Resolution = 12 bits	-	-	TBD	MHz
			-	-	TBD	1 / f_{AD}C
V_{AIN}(1)	Conversion voltage range(2)	Single ended	0	-	V_{REF+}	V
		Differential	-V_{REF+}	-	V_{REF+}	
V_{CMIV}(1)	Common mode input voltage	Differential	-	V_{REF+} / 2	-	V
C_{ADC}	Internal sample and hold capacitor	-	-	2.56	-	pF
t_{STAB}	ADC Start-up time	-	-	**5**	-	µs
t_{LATR}(1)	Trigger conversion latency regular and injected channels without conversion abort	CKMODE = 0	-	TBD	-	1 / f_{ADC}
		CKMODE = 1	-	TBD	-	
$t_{LATRINJ}$(1)	Trigger conversion latency regular injected channels aborting a regular conversion	CKMODE = 0	-	TBD	-	1 / f_{ADC}
		CKMODE = 1	-	TBD	-	
t_S(1)	Sampling time	-	2.5	-	1501.5	1 / f_{ADC}
$I_{ADC(VDDA18ADC)}$	ADC supply current on $V_{DDA18ADC}$	f_s = 5 Msps, resolution = 12 bits	-	325	-	µA
		f_s = 5.8 Msps, resolution = 10 bits	-	340	-	
		Power down, ADEN = 0	-	10.5	-	
		Deep power down, ADEN = 0, DEEPPWD = 1	-	3.4	-	

1. *Specified by design, not tested in production.*
2. *All analog inputs must be between V_{SSA} and $V_{DDA18ADC}$.*

Table 89. ADC accuracy

Evaluated by characterization, not tested in production unless otherwise specified.

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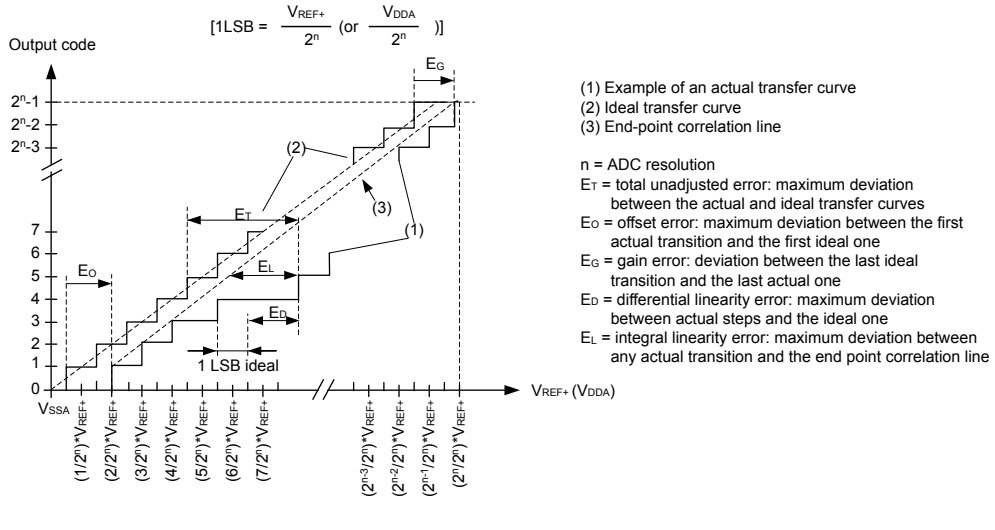
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error (TUE)	Single ended	-	12	33	±LSB
		Differential	-	7	18	
ED	Differential linearity error (DNL)	Single ended	-	1	4	±LSB
		Differential	-	1	3	
EL	Integral linearity error (INL)	Single ended	-	2	5	±LSB
		Differential	-	2	5	
ENOB	Effective number of bits	Single ended	-	9.75	-	Bits
		Differential	-	10.5	-	
SINAD	Signal-to-noise and distortion ratio(1)	Single ended	-	60.5	-	dB
		Differential	-	66.5	-	
SNR	Signal-to-noise ratio	Single ended	-	58.5	-	dB
		Differential	-	60.5	-	
THD	Total harmonic distortion	Single ended	-	-76	-	dB
		Differential	-	-79	-	
EG	Gain error	Vresus V_{REF+} value	-1	-	+1	%FullScale
EO	Offset error	Without calibration	-1	-	+1	
		After calibration	-2	-	2	LSB

1. *Value measured with a -0.5 dBFS input signal and then extrapolated to full scale.*

Figure 37. ADC accuracy characteristics



1. *Refer to Table 90 for the values of R_{AIN}, R_{ADC} and C_{ADC}.*
2. *$C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to Table 62. I/O static characteristics). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.*
3. *Refer to Table 62. I/O static characteristics for value of I_{lkg}.*
4. *Refer to Figure 11. Power supply scheme .*

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Table 90. Minimum sampling time versus RAIN

Specified by design, not tested in production.

Symbol	Parameter	Conditions (Resolution / R_{AIN} in ohms)		Min	Typ	Max	Unit
t_{s_min}	Minimum sampling time	12 bits	47	32	-	-	ns
			68	33	-	-	
			100	34	-	-	
			150	36	-	-	
			220	38	-	-	
			330	42	-	-	
			470	47	-	-	
			680	55	-	-	
			1000[(1)]	70	-	-	
t_{s_min}	Minimum sampling time	10 bits	47	23	-	-	ns
			68	24	-	-	
			100	25	-	-	
			150	26	-	-	
			220	28	-	-	
			330	30	-	-	
			470	33	-	-	
			680	38	-	-	
			1000	45	-	-	
			1500	55	-	-	
			2200	71	-	-	
			3300	97	-	-	
			4700	133	-	-	
			6800[(1)]	238	-	-	
t_{s_min}	Minimum sampling time	8 bits	47	17	-	-	ns
			68	17	-	-	
			100	18	-	-	
			150	19	-	-	
			220	20	-	-	
			330	22	-	-	
			470	25	-	-	
			680	28	-	-	
			1000	34	-	-	
			1500	42	-	-	
			2200	53	-	-	
			3300	70	-	-	
			4700	94	-	-	
			6800	128	-	-	
			10000	183	-	-	
			15000	277	-	-	

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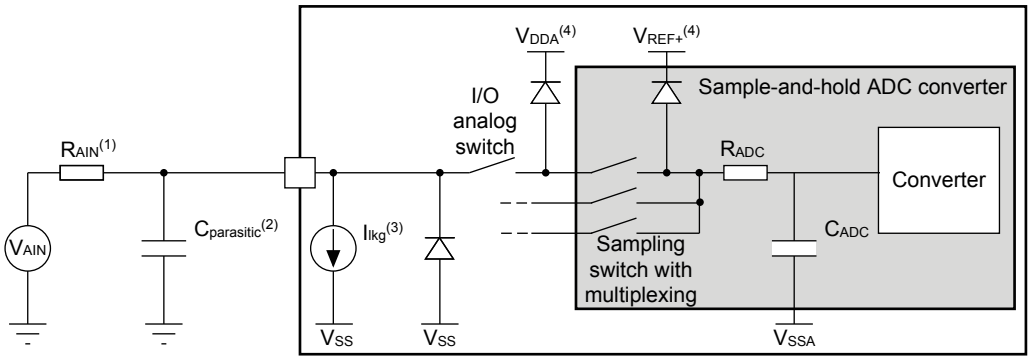
Symbol	Parameter	Conditions (Resolution / R_{AIN} in ohms)		Min	Typ	Max	Unit
t_{s_min}	Minimum sampling time	8 bits	22000[1]	435	-	-	ns

1. *Maximum external input impedance value authorized for the given Resolution.*

Figure 38. Typical connection diagram using the ADC with TT pins featuring analog switch function



6.3.22.1 *General PCB design guidelines*

PCB design guidelines are provided in AN5489 "Getting started with STM32MP25xx lines hardware development" available from the ST website www.st.com.

6.3.23 Voltage reference buffer (VREFBUF) characteristics

Table 91. VREFBUF characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DDA18ADC}$	Analog supply voltage		VRS = 000	1.62	1.8	1.98	V
			VRS = 001	1.75	1.8	1.98	
V_{REFBUF_OUT}	Voltage Reference Buffer Output	@30 °C, @I_{LOAD} = 10 µA, $V_{DDA18ADC}$ = 1.8 V	VRS = 000	1.203	1.21	1.2123	
			VRS = 001	1.491	1.5	1.5015	
TRIM	Trim step resolution	-		-	±0.05	±0.1	%
C_L	Load Capacitor	-		0.5	1.1	1.5	µF
esr	Equivalent Serial Resistor of C_L	-		-	-	1	Ω
I_{LOAD}	External DC load current	All ADCs ON		-	-	0.8	mA
		All ADCs OFF		-	-	2	
I_{LINE_REG}	Line regulation	1.62 V ≤ $V_{DDA18ADC}$ ≤ 1.98 V		-	5400	9800	ppm/V
I_{LOAD_REG}	Load regulation	100 µA ≤ I_{LOAD} ≤ 800 µA		-	5300	8600	ppm/mA
T_{coeff}	Temperature coefficient	-40 °C < T_J < +125 °C		-	TBD	-	ppm/°C
PSRR	Power supply rejection	DC		48	76	-	dB
		100 kHz		51	60	-	
t_{START}	Start-up time	-		-	260	388	µs

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{INRUSH}	Control of max. DC current drive on V_{REFBUF_OUT} during start-up phase (t_{START})			-	-	10	mA
$I_{VDDA18ADC(VREFBUF)}$	VREFBUF supply current $V_{DDA18ADC}$ (excluding internal and external load)	ENVR = 1	I_{LOAD} = 0.8 mA DC	-	9	21	µA
			Peak during 2 × ADC conversion	-	48	56	
		ENVR = 0		-	3	6.5	µA

6.3.24 Digital Temperature Sensor (DTS) characteristics

Table 92. DTS characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{DTS}	Operating frequency	-	4	-	8	MHz
Res	Resolution	-	8	10	12	Bits
Step	Step size	For respecively 8, 10 and 12 bits resolution	0.86	0.22	0.06	°C
t_{conv}	Conversion time	For respecively 8, 10 and 12 bits resolution	512	2048	8192	1 / f_{DTS}
t_{pwrup}	Power up time	-	-	-	256	
T_A	Accuracy	From -20 to +125 °C	-	-	3[(1)]	°C
		From -40° C to -20 °C	-	-	6	
G	G constant	Refer to reference manual for the formula	59.7			°C
H	H constant	Refer to reference manual for the formula	204.4			°C
J	J constant	Refer to reference manual for the formula	-0.16			°C / MHz
Cal5	Cal5 constant	Refer to reference manual for the formula	4094			-
TS_{loc}	Sensor location	TS0 sensor	Inside padring[(2)]			-
		TS1 sensor	Inside device logic[(2)]			-
$I_{DTS(VDDA18AON)}$	DTS supply current on $V_{DDA18AON}$	f_{DTS} = 8 MHz, continuous measurements, single sensor	-	120	160	µA
		At 1 measurement/s	-	-	1	
		f_{DTS} clock stopped	-	-	1	
$I_{DTS(VDDCORE)}$	DTS supply current on V_{DDCORE}	f_{DTS} = 8 MHz	-	-	15	µA

1. *Guaranteed by test in production.*
2. *Temperature in padring sensor (side of the silicon die) is usually slightly lower than device logic sensor as most heat is generated inside device logic.*

6.3.25 V_{BAT}, V_{DDCPU}, V_{DDCORE}, V_{DDGPU} ADC measurement characteristics

Table 93. V_{BAT}, V_{DDCPU}, V_{DDCORE}, V_{DDGPU} ADC measurement characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	-	130	-	kΩ
Q	Ratio on V_{BAT} measurement	-	-	4	-	-
E_r	Error on Q	-	-1	-	+1	%

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{S_VBAT}[1]	ADC sampling time when reading the V_{BAT}	-	34	-	-	ns
t_{S_VDDCPU}[1]	ADC sampling time when reading the V_{DDCPU}	-	34	-	-	ns
$t_{S_VDDCORE}$[1]	ADC sampling time when reading the V_{DDCORE}	-	34	-	-	ns
t_{S_VDDGPU}[1]	ADC sampling time when reading the V_{DDGPU}	-	34	-	-	ns

1. *Specified by design, not tested in production.*

6.3.26 Temperature and V_{BAT} monitoring characteristic for tamper detection

Table 94. TEMP and V_{BAT} Monitoring characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TEMPH	High T_J temperature monitoring	-	110	-	125	° C
TEMPL	Low T_J temperature monitoring	-	-40	-	-30	
V08CAPH	High V_{08CAP} supply monitoring[1]	-	0.88	-	1	V
V08CAPL	Low V_{08CAP} supply monitoring[1]	-	0.6	-	0.72	-
V08CAP_filter	V_{08CAP} supply monitoring glitch filter[1]	-	-	-	1	µs

1. *V08CAP is an internal regulator supplied by V_{SW}. V_{SW} is equal to V_{DD} when present or V_{BAT} otherwise.*

6.3.27 Voltage monitoring characteristics

Table 95. Voltage monitoring characteristics (V_{DDCORE}, V_{DDCPU}, V_{DDGPU}, PVD_IN, $V_{DDA18ADC}$, $V_{DDIO1/2/3/4}$, $V_{DD33USB}$, $V_{DD33UCPD}$)

Evaluated by characterization, not tested in production unless otherwise specified.

Parameter	Conditions		Min	Typ	Max	Unit
V_{DDCORE} monitoring						
Threshold on rising edge	To set VCOREH bit (overvoltage)		0.88[1]	-	-	V
Threshold on falling edge	To set VCOREL bit (undervoltage)		-	-	0.72[1]	
Hysteresis on monitoring	To clear VCOREL or VCOREH bit		-	45	-	mV
Supply current on $V_{DDA18AON}$	VCOREMONEN = 1		-	1.5	-	µA
V_{DDCPU} monitoring						
Threshold on rising edge	To set VCPUH bit (overvoltage)		0.99[1]	-	-	V
Threshold on falling edge	To set VCPUL bit (undervoltage)	VCPULLS = 0	-	-	0.72[1]	
		VCPULLS = 1	-	-	0.81	
Hysteresis on monitoring	To clear VCPUL or VCPUH bit		-	45	-	mV
Supply current on $V_{DDA18AON}$	VCPUMONEN = 1		-	1.5	-	µA
V_{DDGPU} monitoring						
Threshold on rising edge	To set VDDGPURDY bit	GPULVTEN = 0	0.61[1]	-	-	V
		GPULVTEN = 1	0.5	-	-	
Hysteresis on falling edge	To clear VDDGPURDY bit		-	45	-	mV
Delay after detection	To set VDDGPURDY bit		200	340	500	µs
	To clear VDDGPURDY bit		-	0	-	

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Parameter	Conditions		Min	Typ	Max	Unit
Supply current on $V_{DDA18AON}$	GPUVMEN = 1		-	1.19	-	µA
PVD_IN monitoring						
Threshold on rising edge	-		-	$V_{REFIN}T$	-	V
Hysteresis on monitoring	-		-	50	-	mV
Supply current on $V_{DDA18AON}$	PVDEN = 1		-	0.75	-	µA
$V_{DDA18ADC}$ monitoring						
Threshold on rising edge	-		-	-	1.55(1)	V
Hysteresis on monitoring	-		-	50	-	mV
Supply current on $V_{DDA18AON}$	AVMEN = 1		-	0.75	-	µA
Supply current on $V_{DDA18ADC}$	AVMEN = 1		-	1	-	µA
V_{DDIO1} monitoring						
Threshold on rising edge	-		-	-	1.55(1)	V
Hysteresis on monitoring	-		-	50	-	mV
Supply current on $V_{DDA18AON}$	VDDIO1VMEN = 1		-	0.75	-	µA
Supply current on V_{DDIO1}	Always ON	VDDIO1 = 1.8 V	-	0.5	-	µA
		VDDIO1 = 3.3 V	-	0.92	-	
V_{DDIO2} monitoring						
Threshold on rising edge	-		-	-	1.55(1)	V
Hysteresis on monitoring	-		-	50	-	mV
Supply current on $V_{DDA18AON}$	VDDIO2VMEN = 1		-	0.75	-	µA
Supply current on V_{DDIO2}	Always ON	VDDIO2 = 1.8 V	-	0.5	-	µA
		VDDIO2 = 3.3 V	-	0.92	-	
V_{DDIO3} monitoring						
Threshold on rising edge	-		-	-	1.55(1)	V
Hysteresis on monitoring	-		-	50	-	mV
Supply current on $V_{DDA18AON}$	VDDIO3VMEN = 1		-	0.75	-	µA
Supply current on V_{DDIO3}	Always ON	VDDIO3 = 1.8 V	-	0.5	-	µA
		VDDIO3 = 3.3 V	-	0.92	-	
V_{DDIO4} monitoring						
Threshold on rising edge	-		-	-	1.55(1)	V
Hysteresis on monitoring	-		-	50	-	mV
Supply current on $V_{DDA18AON}$	VDDIO4VMEN = 1		-	0.75	-	µA
Supply current on V_{DDIO4}	Always ON	VDDIO4 = 1.8 V	-	0.5	-	µA
		VDDIO4 = 3.3 V	-	0.92	-	
$V_{DD33USB}$ monitoring						
Threshold on rising edge	-		-	-	1.55(1)	V
Hysteresis on monitoring	-		-	50	-	mV
Supply current on $V_{DDA18AON}$	USB33VMEN = 1		-	0.75	-	µA
Supply current on $V_{DD33USB}$	Always ON		-	0.92	-	µA

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Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD33UCPD}$ monitoring					
Threshold on rising edge	-	-	-	1.55[1]	V
Hysteresis on monitoring	-	-	50	-	mV
Supply current on $V_{DDA18AON}$	UCPDVMEN = 1	-	0.75	-	µA
Supply current on $V_{DD33UCPD}$	Always ON	-	0.92	-	µA

1. *Guaranteed by test in production.*

6.3.28 Compensation cell characteristics

Table 96. Compensation cell characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{COMPCELL}$	$V_{DDA18AON}$ current consumption during code calculation	Using a 16 MHz clock (HSI / 8)	-	TBD	TBD	mA
Tready	Time needed to have the first code calculation after enabling		-	96	-	µs
Tmeasure	Time needed to update the code		-	832	-	

6.3.29 Multi-function digital filter (MDF) characteristics

Table 97. MDF characteristics (WARNING: DUMMY DATA TBD)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CKI}	Input clock frequency via MDF_CKIx pin, in SLAVE SPI mode	-	-	-	25	MHz
f_{CCKI}	Input clock frequency via MDF_CCK[1:0] pin, in SLAVE SPI mode	-	-	-	25	
f_{CCKO}	Output clock frequency in MASTER SPI mode	-	-	-	25	
f_{CCKOLF}	Output clock frequency in LF_MASTER SPI mode	-	-	-	5	
f_{SYMB}	Input symbol rate in Manchester mode	-	-	-	20	
t_{HCKI} t_{LCKI}	MDF_CKIx input clock high and low time	In SLAVE SPI mode	2 × $T_{mdf_proc_ck}$[1]	-	-	ns
t_{HCCKI} t_{LCCKI}	MDF_CCK[1:0] input clock high and low time	In SLAVE SPI mode	2 × $T_{mdf_proc_ck}$[1]	-	-	
t_{HCCKO} t_{LCCKO}	MDF_CCK[1:0] output clock high and low time	In MASTER SPI mode	2 × $T_{mdf_proc_ck}$[1]	-	-	
$t_{HCCKOLF}$ $t_{LCCKOLF}$	MDF_CCK[1:0] output clock high and low time	In LF_MASTER SPI mode	$T_{mdf_proc_ck}$[1]	-	-	
t_{SUCKI}	Data setup time with respect to MDF_CKIx input	In SLAVE SPI mode, measured on rising and falling edge	1.5	-	-	
t_{HDCKI}	Data hold time with respect to MDF_CKIx input		0	-	-	

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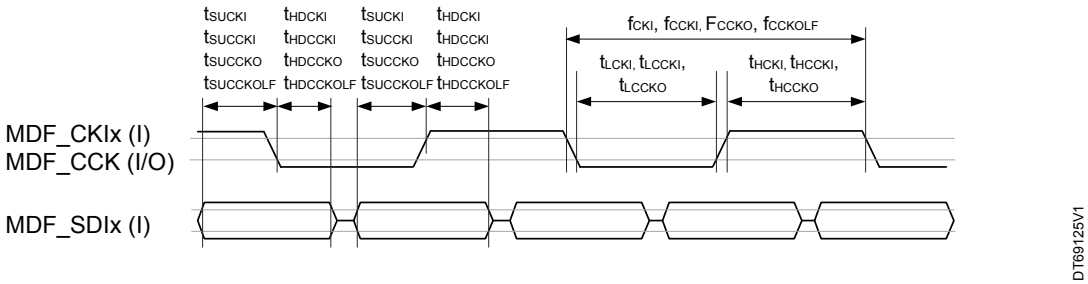
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SUCCKI}	Data setup time with respect to MDF_CCK[1:0] input	In SLAVE SPI mode: MDF_CCK[1:0] configured in input, measured on rising and falling edge	1.5	-	-	ns
t_{HDCCKI}	Data hold time with respect to MDF_CCK[1:0] input		0.5	-	-	
t_{SUCCKO}	Data setup time with respect to MDF_CCK[1:0] output	In MASTER SPI mode: MDF_CCK[1:0] configured in output, measured on rising and falling edge	3.5	-	-	
t_{HDCCKO}	Data hold time with respect to MDF_CCK[1:0] output		1.5	-	-	
$t_{SUCCKOLF}$	Data setup time with respect to MDF_CCK[1:0] output	In LF_MASTER SPI mode, MDF_CCK[1:0] configured in output, measured on rising and falling edge	19.5	-	-	
$t_{HDCCKOLF}$	Data hold time with respect to MDF_CCK[1:0] output		0	-	-	

1. *Tmdf_proc_ck is the period of the MDF processing clock.*

Figure 39. MDF timing diagram



6.3.30 Audio digital filter (ADF) characteristics

Table 98. ADF characteristics (WARNING: DUMMY DATA TBD)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CCKI}	Input clock frequency via ADF_CCK[1:0] pin, in SLAVE SPI mode	-	-	-	25	MHz
f_{CCKO}	Output clock frequency in MASTER SPI mode	-	-	-	25	
f_{CCKOLF}	Output clock frequency in LF_MASTER SPI mode	-	-	-	5	
f_{SYMB}	Input symbol rate in Manchester mode	-	-	-	20	
t_{HCCKI} t_{LCCKI}	ADF_CCK[1:0] input clock high and low time	In SLAVE SPI mode	$2 \times T_{adf_proc_ck}$(1)	-	-	ns
t_{HCCKO} t_{LCCKO}	ADF_CCK[1:0] output clock high and low time	In MASTER SPI mode	$2 \times T_{adf_proc_ck}$(1)	-	-	
$t_{HCCKOLF}$ $t_{LCCKOLF}$	ADF_CCK[1:0] output clock high and low time	In LF_MASTER SPI mode	$T_{adf_proc_ck}$(1)	-	-	

1. *Tadf_proc_ck is the period of the ADF processing clock.*

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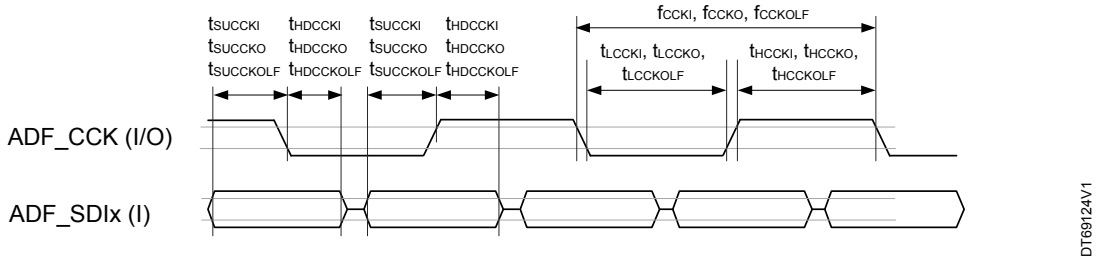
Figure 40. ADF timing diagram



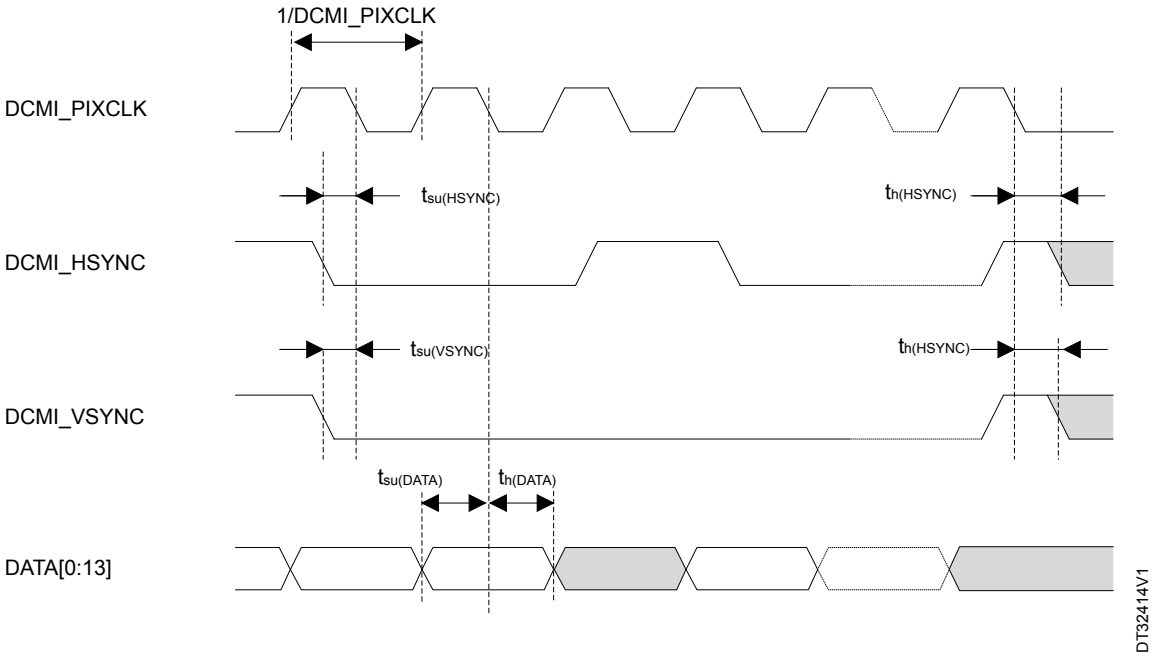
6.3.31 Camera interface (DCMI) characteristics

Table 99. DCMI characteristics (WARNING: DUMMY DATA TBD)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
clock_ratio	Frequency ratio DCMI_PIXCLK / f_{HCLK}	-	-	0.4	-
DCMI_PIXCLK	Pixel clock input	-	-	80	MHz
DPIXEL	Pixel clock input duty cycle	30	-	70	%
tsu(DATA)	Data input setup time	2	-	-	ns
th(DATA)	Data hold time	1	-	-	
tsu(HSYNC) tsu(VSYNC)	DCMI_HSYNC and DCMI_VSYNC input setup times	2	-	-	
th(HSYNC) th(VSYNC)	DCMI_HSYNC and DCMI_VSYNC input hold times	1	-	-	

Figure 41. DCMI timing diagram



6.3.32 Camera interface (DCMIPP) characteristics

Unless otherwise specified, the parameters given in Table 100 for DCMIPP are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

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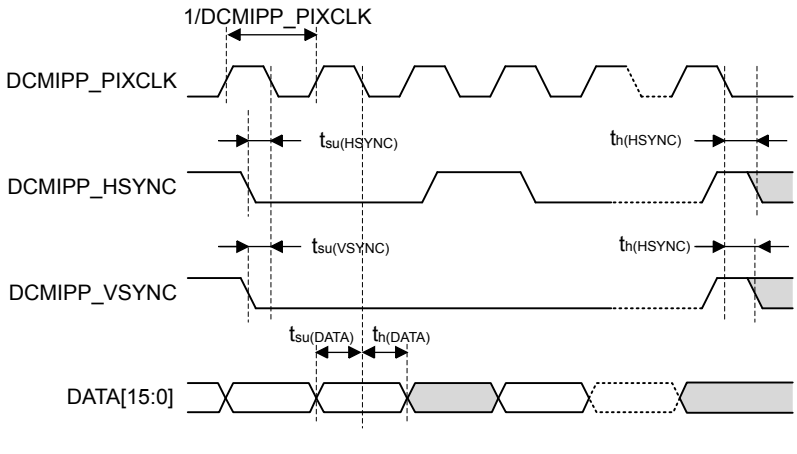
- DCMIPP_PIXCLK polarity: falling (refer to AN5489 "Getting started with STM32MP25xx lines hardware development") available from the ST website www.st.com.
- DCMIPP_VSYNC and DCMIPP_HSYNC polarity: high
- Data formats: 16 bits
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 × V_{DD}

Table 100. DCMIPP characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DCMIPP_PIXCLK	Pixel clock input	-	-	-	120	MHz
DPixel	Pixel clock input duty cycle	-	30	-	70	%
$t_{su(DATA)}$	Data input setup time	-	2	-	-	ns
$t_{h(DATA)}$	Data input hold time	-	3	-	-	
$t_{su(HSYNC)}$ $t_{su(VSYNC)}$	DCMIPP_HSYNC / DCMIPP_VSYNC input setup time	-	2	-	-	
$t_{h(HSYNC)}$ $t_{h(VSYNC)}$	DCMIPP_HSYNC / DCMIPP_VSYNC input hold time	-	3	-	-	

Figure 42. DCMIPP timing diagram



6.3.33 Parallel interface (PSSI) characteristics

Table 101. PSSI transmit characteristics (WARNING: DUMMY DATA TBD)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
clock_ratio	Frequency ratio DCMI_PDCK/f_{HCLK}	-	-	-	0.4	-
PSSI_PDCK	PSSI clock input	3.0 V ≤ V_{DD} ≤ 3.6 V	-	-	TBD(1)	MHz
		1.71 V ≤ V_{DD} ≤ 1.89 V	-	-	TBD(1)	
D_{PIXEL}	PSSI clock input duty cycle	-	30	-	70	%
$t_{OV(DATA)}$	Data output valid time	3.0 V ≤ V_{DD} ≤ 3.6 V	-	-	14	ns
		1.71 V ≤ V_{DD} ≤ 1.89 V	-	-	21	
$t_{OH(DATA)}$	Data output hold time	-	7	-	-	
$t_{OV(DE)}$	DE output valid time		-	-	12.5	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{OH(DE)}$	DE output hold time	-	6	-	-	ns
$t_{SU(RDY)}$	RDY input setup time	-	0	-	-	
$t_{H(RDY)}$	RDY input hold time		0	-	-	

1. *This maximal frequency does not consider receiver setup and hold timings.*

Figure 43. PSSI transmit timing diagram

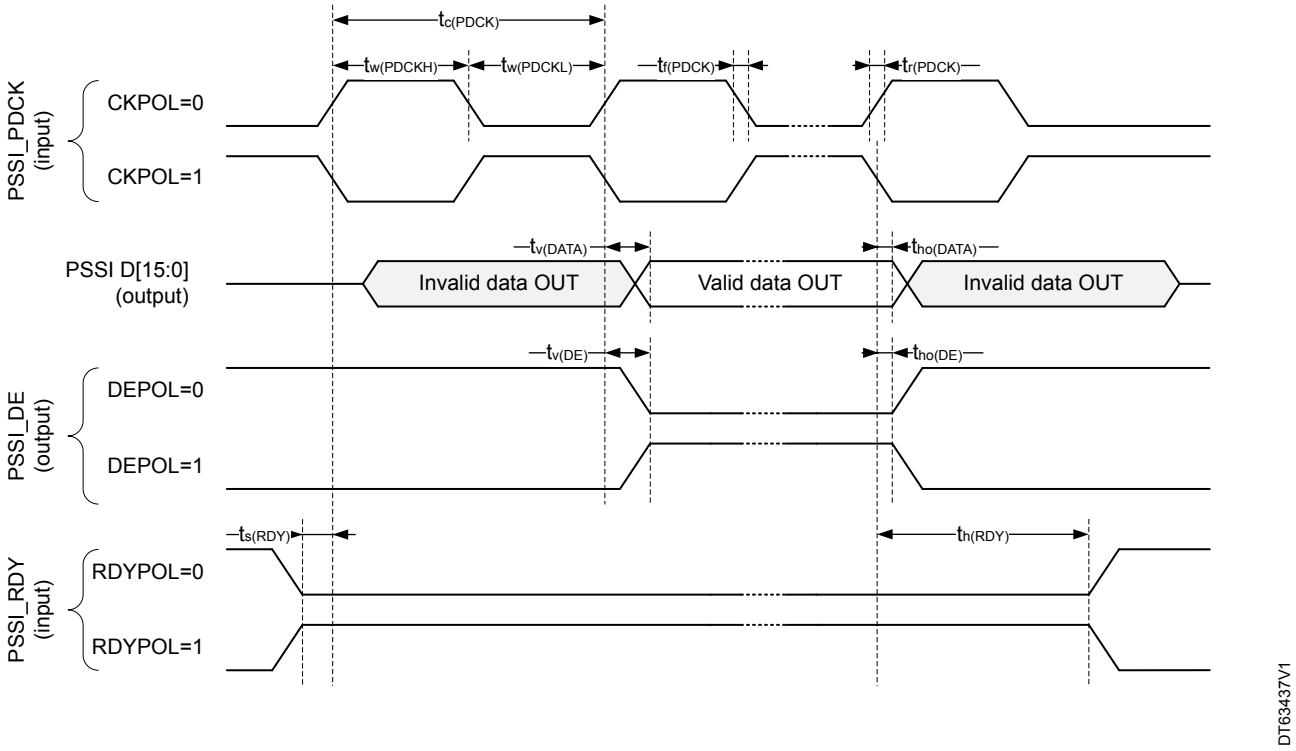

Table 102. PSSI receive characteristics (WARNING: DUMMY DATA TBD)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
clock_ratio	Frequency ratio DCMI_PDCK/f_{HCLK}	-	-	-	0.4	-
PSSI_PDCK	PSSI clock input	-	-	-	64	MHz
D_{PIXEL}	PSSI clock input duty cycle	-	30	-	70	%
$t_{SU(DATA)}$	Data input setup time	-	2	-	-	ns
$t_{H(DATA)}$	Data input hold time	-	1.5	-	-	
$t_{SU(DE)}$	DE input setup time	-	0.5	-	-	
$t_{H(DE)}$	DE input hold time	-	2	-	-	
$t_{OV(RDY)}$	RDY output valid time	-	-	-	12	
$t_{OH(RDY)}$	RDY output hold time	-	6	-	-	

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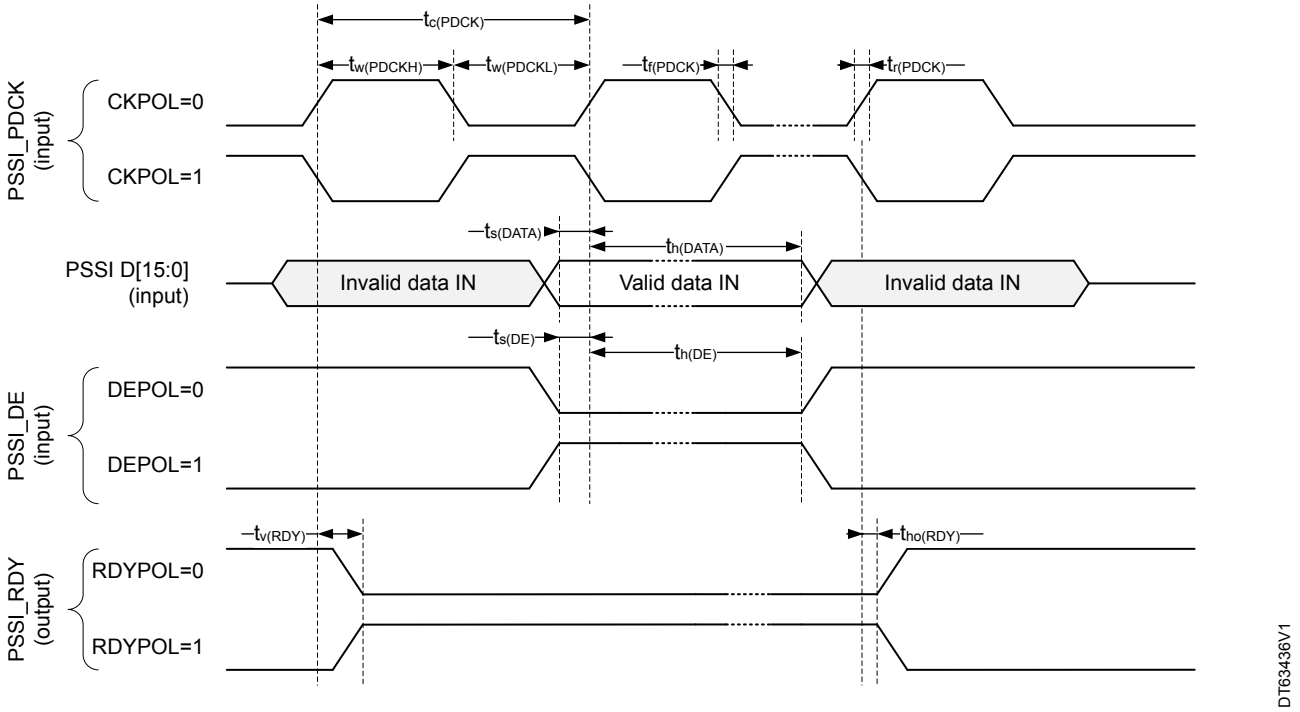
Figure 44. PSSI receive timing diagram



6.3.34 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in Table 103 for the LTDC interface are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- LCD_CLK polarity: low (signals change on CLK rising edge)
- LCD_DE polarity: low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits
- Output speed is set to:
  - LTDC Clock: OSPEEDRy[1:0] = 11
  - Other LTDC signals: OSPEEDRy[1:0] = 01
- Advanced I/O configurations:
  - LTDC Clock: RET = 0, INVCLK = 0, DE = 0, DLYPATH = 0
  - Other LTDC signals: RET = 1, INVCLK = 0, DE = 0, DLYPATH = 0
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 × V_{DD}
- I/O compensation cell enabled
- VDDxVRSEL activated when $V_{DDx} \leq 2.7$ V

Table 103. LTDC characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CLK}	LTDC clock output frequency	C = 20 pF	-	-	148.5	MHz
		C = 30 pF			120	
D_{CLK}	LTDC clock output duty cycle	-	45	-	55	%

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(CLKH)}$, $t_{w(CLKL)}$	Clock high time, low time	-	$t_{w(CLK)}$ / 2 - 0.5	-	$t_{w(CLK)}$ / 2 + 0.5	ns
$t_{v(DATA)}$	Data output valid time	-	-	-	4	
$t_{h(DATA)}$	Data output hold time	-	1	-	-	
$t_{v(HSYNC)}$, $t_{v(VSYNC)}$, $t_{v(DE)}$	HSYNC/VSYNC/DE output valid time	-	-	-	3.5	
$t_{h(HSYNC)}$, $t_{h(VSYNC)}$, $t_{h(DE)}$	HSYNC / VSYNC / DE output hold time	-	0.5	-	-	

Figure 45. LCD-TFT horizontal timing diagram

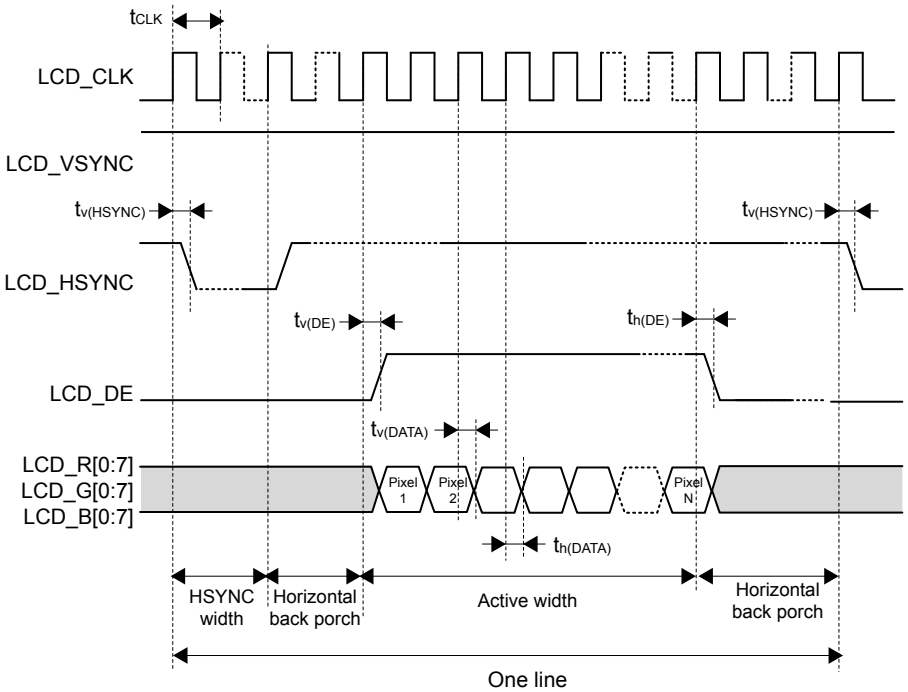

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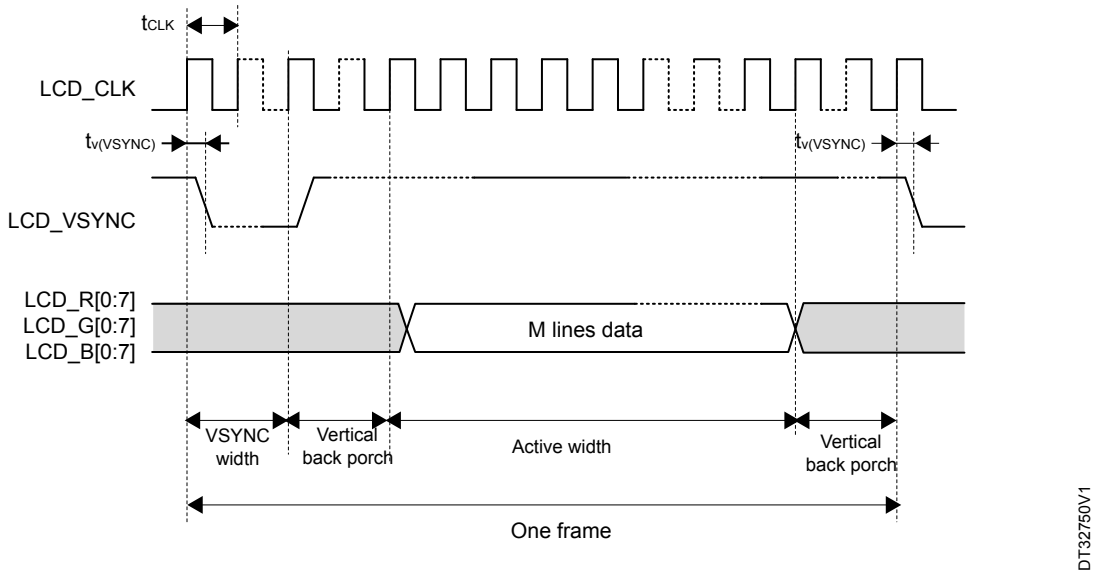
Figure 46. **LCD-TFT vertical timing diagram**



6.3.35 Timer characteristics

The parameters given in Table 104 are guaranteed by design.

Refer to Section 6.3.16: I/O port characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 104. **TIMx characteristics**

TIMx is used as a general term to refer to the TIM1 to TIM20 timers.
Specified by design, not tested in production.

Symbol	Parameter	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	1	-	$t_{TIMxCLK}$
$f_{TIMxCLK}$	Timer kernel clock	0	200	MHz
f_{EXT}	Timer external clock frequency on CH1 to CH4	0	$f_{TIMxCLK}$ / 2	
Res_{TIM}	Timer resolution	-	16	bit
	Timer resolution (TIM2 to TIM5)	-	32	
t_{MAX_COUNT}	Maximum possible count with 16-bit counters	-	65536	$t_{TIMxCLK}$
	Maximum possible count with 32-bit counter (TIM2 to TIM5)		65536 × 65536	

Table 105. **LPTIMx characteristics**

LPTIMx is used as a general term to refer to the LPTIM1 to LPTIM5 timers.
Specified by design, not tested in production.

Symbol	Parameter	Min	Max	Unit
$t_{res(LPTIM)}$	Timer resolution time	1	-	$t_{LPTIMxCLK}$
$f_{LPTIMxCLK}$	Timer kernel clock	0	100	MHz
	Timer kernel clock (autonomous mode)	0	32768	Hz
f_{EXT}	Timer external clock frequency on IN1 and IN2	0	$f_{LPTIMxCLK/2}$	MHz
Res_{LPTIM}	Timer resolution	-	16	bit
t_{MAX_COUNT}	Maximum possible count	-	65536	$t_{LPTIMxCLK}$

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6.3.36 Communications interfaces

6.3.36.1 *I2C interface characteristics*

The I2C interface meets the timings requirements of the I^2C-bus specification for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s.
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I^2C timings requirements are guaranteed by design when the I2C peripheral is properly configured and when the i2c_ker_ck frequency is greater than the minimum shown in the table below:

Table 106. Minimum i2c_ker_ck frequency in all I2C modes (WARNING: DUMMY DATA TBD)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Unit
$f_{(I2CCLK)}$	I2CCLK frequency	Standard-mode	-	2	MHz
		Fast-mode	Analog filter ON, DNF-=-0	8	
			Analog filter OFF, DNF-=-1	9	
		Fast-mode Plus	Analog filter ON, DNF-=-0	19	
			Analog filter OFF, DNF-=-1	16	

The SDA and SCL I/O requirements are met with the following restrictions:

- The SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.
- The 20 mA output drive requirement in Fast-mode Plus is not supported. This limits the maximum load C_{load} supported in Fm+, which is given by these formulas:

$t_{r(SDA/SCL)} = 0.8473 \times R_p \times C_{load}$

$R_{p(min)} = (V_{DD} - V_{OL(max)}) / I_{OL(max)}$

Where R_p is the I2C lines pull-up. Refer to Section 6.3.16: I/O port characteristics for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to Table 107. I2C analog filter characteristics for the analog filter characteristics:

Table 107. I2C analog filter characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbols	Parameters	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(1)	120(2)	ns

1. *Spikes with widths below t_{AF}(min) are filtered. At T_J = -40 °C, the guaranteed minimum is 40 ns.*
2. *Spikes with widths above t_{AF}(max) are not filtered.*

6.3.36.2 *I3C interface characteristics*

The I3C timings are in line with timings requirements of the MIPI® I3C specification v1.1, except for the ones given in Table 108. This can be mitigated by increasing the corresponding SCL low duration in the I3C_TIMINGR0 register.

The I3C peripheral supports:

- I3C SDR-only as controller
- I3C SDR-only as target
- I3C SCL bus clock frequency up to 12.5 MHz

Unless otherwise specified, the parameters given in Table 108 for the I3C interface are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11

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- Capacitive load C = 30 pF
- I/O compensation cell enabled
- VDDxVRSEL activated when $V_{DDx} \leq 2.7$ V

Table 108. I3C specific timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SU_OD}	SDA data setup time during Open-Drain mode	Controller	19.5	-	-	ns
t_{SU_PP}	SDA sata setup time in Push-Pull mode	Controller	15	-	-	ns

Table 109. I3C pin characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$R_{PU(I3C)}$	I3C pull-up	1600	2200	2800	Ω
$R_{HK(I3C)}$	I3C high keeper (weak pull-up)	125	160	195	kΩ

6.3.36.3 *SPI interface characteristics*

Unless otherwise specified, the parameters given in Table 110 for the SPI interface are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions , with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$
- I/O compensation cell enabled
- VDDxVRSEL activated when $V_{DDx} \leq 2.7$ V

Refer to Section 6.3.16: I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 110. SPI characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SPI clock frequency	Master mode 1.71 V < V_{DD} < 1.89 V	-	-	115	MHz
		Master mode 3.0 V < V_{DD} < 3.6 V	-	-	105	
		Slave receiver mode	-	-	100	
		Slave mode transmitter/full duplex	-	-	41.5[(1)]	
$t_{su(NSS)}$	NSS setup time	Slave mode	4	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	1	-	-	
$t_{w(SCKH)}$, $t_{w(SCKL)}$	SCK high and low time	Master mode	T_{pclk} - 1	T_{pclk}	T_{pclk} + 1	
$t_{su(MI)}$	Data input setup time	Master mode	4.5	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	1	-	-	
$t_{h(SI)}$		Slave mode	1	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	11	15	15	
$t_{dis(SO)}$	Data output disable time	Slave mode	12.5	14.5	17.5	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{v(MO)}$	Data output valid time	Master mode	-	3	3.5	ns
$t_{v(SO)}$		Slave mode	-	11.5	12	
$t_{h(MO)}$	Data output hold time	Master mode	2	-	-	
$t_{h(SO)}$		Slave mode	10	-	-	

1. *Maximum frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50%.*

Figure 47. SPI timing diagram - master mode

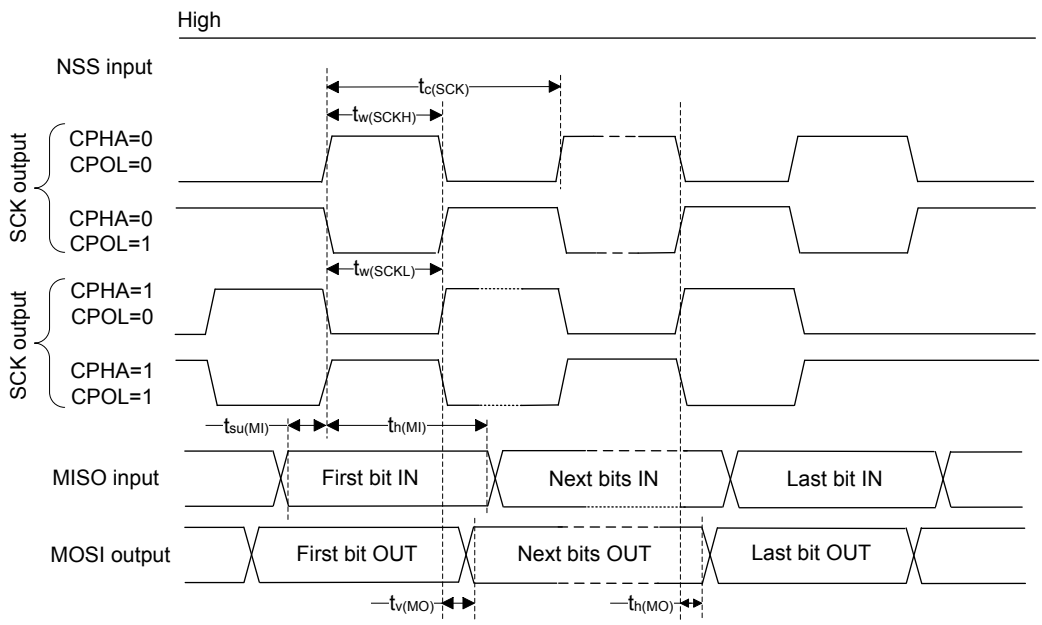

Figure 48. SPI timing diagram - slave mode and CPHA = 0

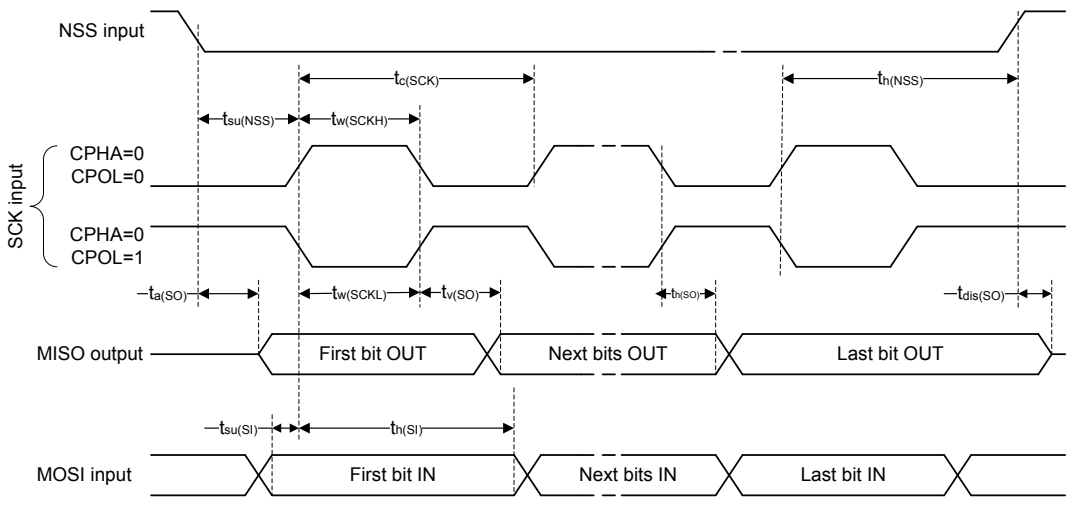

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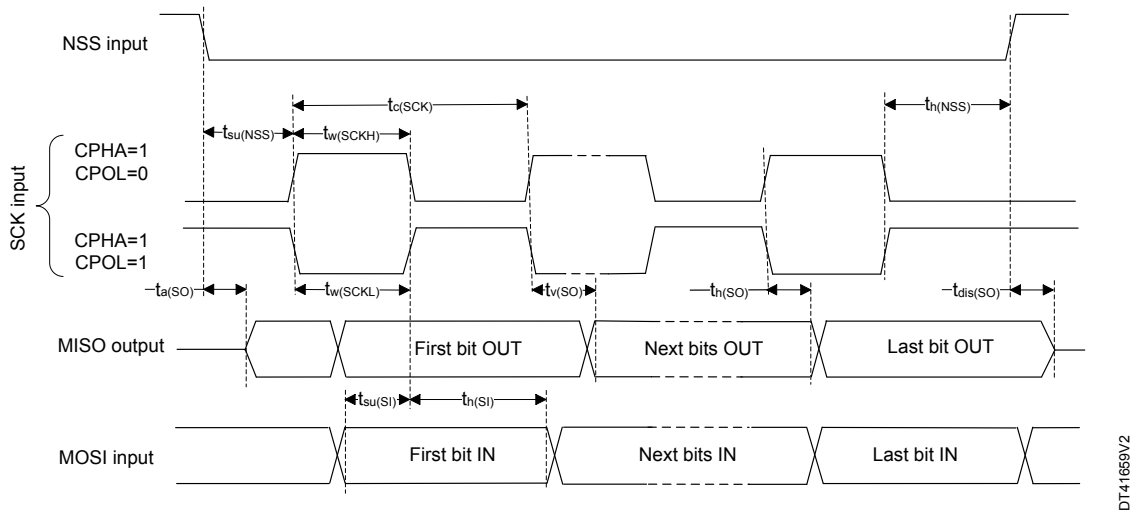
Figure 49. SPI timing diagram - slave mode and CPHA = 1



6.3.36.4 *I2S interface characteristics*

Unless otherwise specified, the parameters given in Table 111 for the I2S interface are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions , with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C= 30 pF
- Measurement points are done at CMOS levels: 0.5 × V_{DD}
- I/O compensation cell enabled

Refer to Section 6.3.16: I/O port characteristics for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 111. I2S characteristics (WARNING: DUMMY DATA TBD)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{MCK}	I2S main clock output	-	256 × 8K	-	256 × F_s	MHz
f_{CK}	I2S clock frequency	Master data	-	-	64 × F_s	MHz
		Slave data	-	-	64 × F_s	
$t_{v(WS)}$	WS valid time	Master mode	-	-	6.5	ns
$t_{h(WS)}$	WS hold time	Master mode	0.5	-	-	
$t_{su(WS)}$	WS setup time	Slave mode	1	-	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	-	
$t_{su(SD_MR)}$	Data input setup time	Master receiver	2	-	-	
$t_{su(SD_SR)}$		Slave receiver	1.5	-	-	
$t_{h(SD_MR)}$	Data input hold time	Master receiver	2	-	-	
$t_{h(SD_SR)}$		Slave receiver	0.5	-	-	
$t_{v(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	-	15	
$t_{v(SD_MT)}$		Master transmitter (after enable edge)	-	-	1	
$t_{h(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	8.5	-	-	
$t_{h(SD_MT)}$		Master transmitter (after enable edge)	0	-	-	

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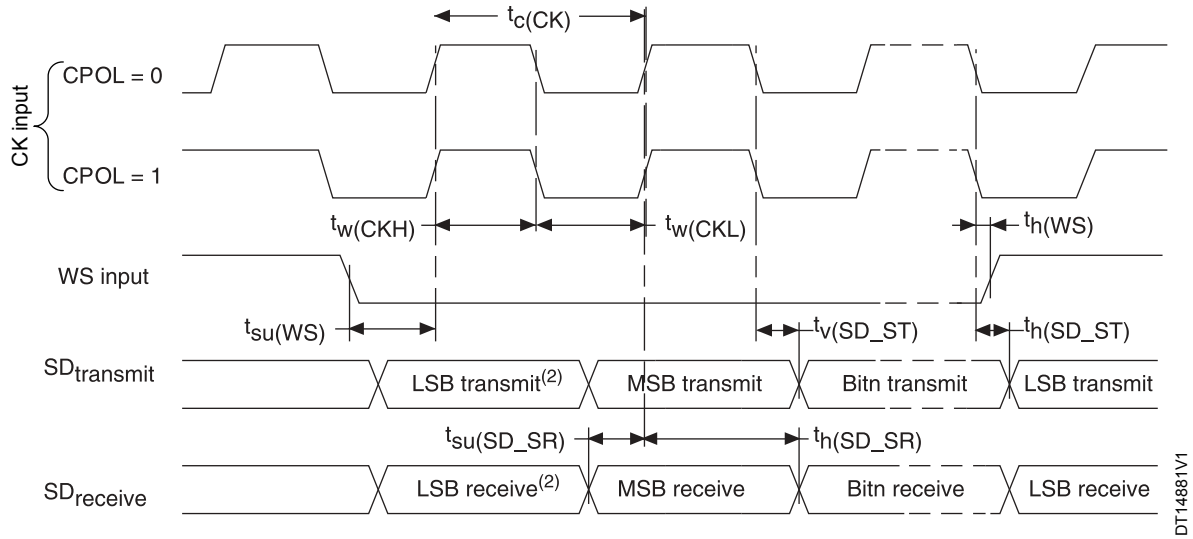
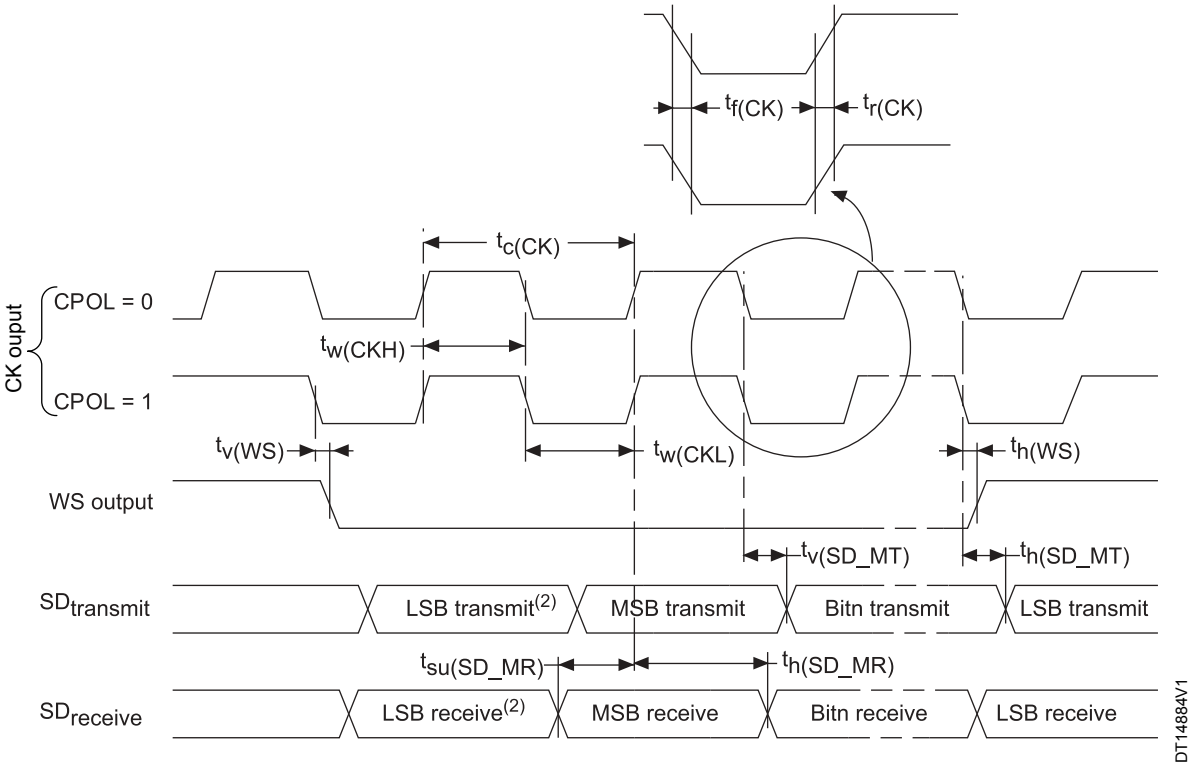
Figure 50. I2S slave timing diagram (Philips protocol)



1. *LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.*

Figure 51. I2S master timing diagram (Philips protocol)



1. *LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.*

6.3.36.5 *SAI interface characteristics*

Unless otherwise specified, the parameters given in Table 112 for SAI are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions , with the following configuration:

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- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are performed at CMOS levels: 0.5 × V_{DD}

Refer to Section 6.3.16: I/O port characteristics for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 112. SAI characteristics (WARNING: DUMMY DATA TBD)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{MCK}	SAI main clock output	-	-	-	TBD	MHz
f_{CK}	SAI bit clock frequency(1)	Master transmitter	-	-	TBD	MHz
		Master receiver	-	-	TBD	
		Slave transmitter	-	-	TBD	
		Slave receiver	-	-	TBD	
$t_{v(FS)}$	FS valid time	Master mode	-	-	11	ns
$t_{su(FS)}$	FS setup time	Slave mode	7	-	-	
$t_{h(FS)}$	FS hold time	Master mode	2	-	-	
		Slave mode	2.5	-	-	
$t_{su(SD_A_MR)}$	Data input setup time	Master receiver	2	-	-	
$t_{su(SD_B_SR)}$		Slave receiver	1.5	-	-	
$t_{h(SD_A_MR)}$	Data input hold time	Master receiver	3	-	-	
$t_{h(SD_B_SR)}$		Slave receiver	0.5	-	-	
$t_{v(SD_B_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	-	11	
$t_{h(SD_B_ST)}$	Data output hold time	Slave transmitter (after enable edge)	8.5	-	-	
$t_{v(SD_A_MT)}$	Data output valid time	Master transmitter (after enable edge)	-	-	10	
$t_{h(SD_A_MT)}$	Data output hold time	Master transmitter (after enable edge)	7	-	-	

1. *APB clock frequency must be at least twice SAI clock frequency.*

Figure 52. SAI master timing waveforms

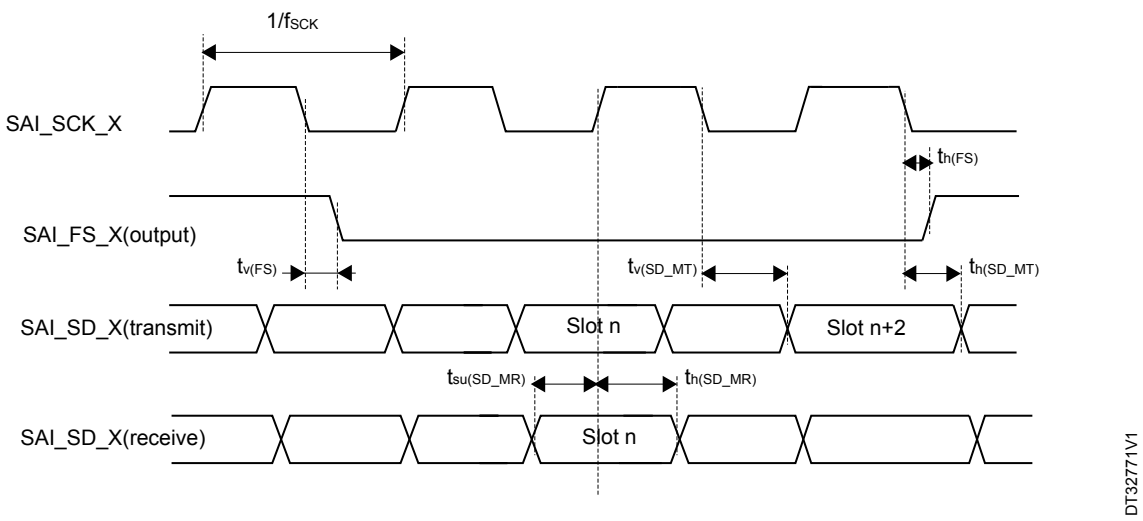

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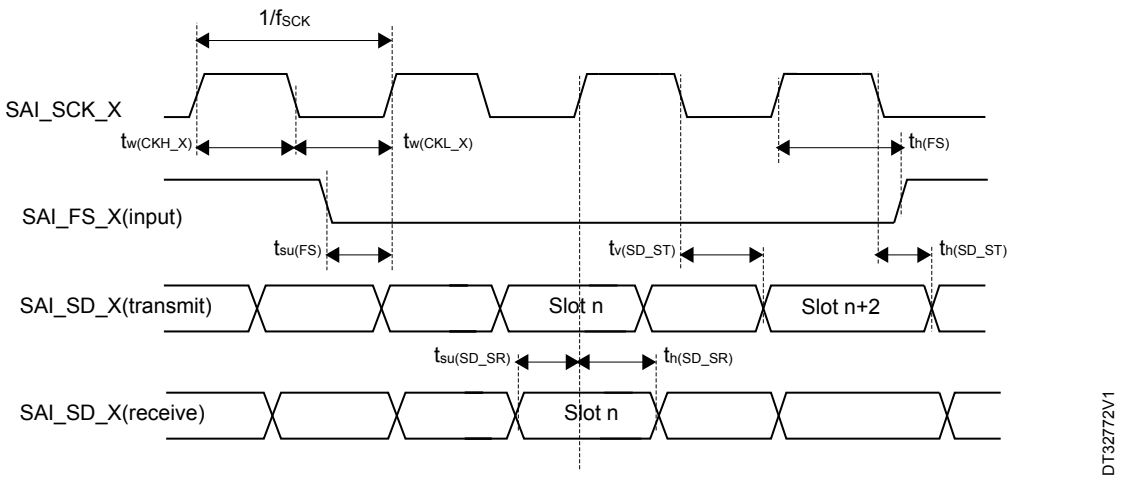
Figure 53. SAI slave timing waveforms



6.3.36.6 *SD/SDIO MMC card host interface (SDMMC) characteristics*

Unless otherwise specified, the parameters given in Table 113 for the SDIO/MMC interface are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions , with the following configuration:

- Output speed is set as table below
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 × V_{DD}
- I/O compensation cell enabled
- VDDxVRSEL activated when $V_{DDx} \leq 2.7$ V

Refer to Section 6.3.16: I/O port characteristics for more details on the input/output characteristics.

Table 113. SDMMC GPIO OSPEEDR settings for timing measurements

Voltage range (V)	Max clock frequency (MHz)	OSPEEDRy[1:0]	
		Clock	Data
1.71 - 1.89 and 2.7 - 3.6	26/25	00	00
	52/50	01	00
	DDR 52/50	01	01
	100	01	00
2.7 - 3.6	120	11	10
1.71 - 1.89	166	11	10

Table 114. SDMMC characteristics for SD-Card or SDIO usage

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	V_{DDIOx} = 2.7 V to 3.6 V	0	-	120	MHz
		V_{DDIOx} = 1.71 V to 1.89 V	0	-	166	
clock_ratio	SDMMC_CK / f_{pclk} frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} = 52 MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 52 MHz	8.5	9.5	-	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D inputs (referenced to CK) in High-Speed/SDR/DDR mode[1]						
t_{ISU}	Input setup time HS	-	2	-	-	ns
t_{IH}	Input hold time HS	-	2	-	-	
t_{IDW}[2]	Input valid window (variable window)	-	2.5	-	-	
CMD, D outputs (referenced to CK) in high-speed/SDR/DDR mode[1]						
t_{OV}	Output valid time HS	-	-	7.5	8	ns
t_{OH}	Output hold time HS	-	4.5	-	-	
CMD, D inputs (referenced to CK) in default mode						
t_{ISUD}	Input setup time SD	-	2.5	-	-	ns
t_{IHD}	Input hold time SD	-	2	-	-	
CMD, D outputs (referenced to CK) in default mode						
t_{OVD}	Output valid default time SD	-	-	1	2	ns
t_{OHD}	Output hold default time SD	-	0	-	-	

1. *SD-Card 3 V / 1.8 V support on SDMMC3 requires an external voltage translator for which timings should be taken into account.*
2. *The minimum window of time where the data needs to be stable for proper sampling in tuning mode.*

Table 115. SDMMC characteristics for e•MMC usage

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	V_{DDIOx} = 2.7 V to 3.6 V	0	-	120	MHz
		V_{DDIOx} = 1.71 V to 1.89 V	0	-	166	
clock_ratio	SDMMC_CK/f_{pclk} frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} = 52 MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time		8.5	9.5	-	
CMD, D inputs (referenced to CK)						
t_{ISU}	Input setup time HS	-	2	-	-	ns
t_{IH}	Input hold time HS	-	2	-	-	
t_{IDW}[1]	Input valid window (variable window)	-	2.5	-	-	
CMD, D outputs (referenced to CK)						
t_{OV}	Output valid time HS	-	-	7.5	8	ns
t_{OH}	Output hold time HS	-	4.5	-	-	

1. *The minimum window of time where the data needs to be stable for proper sampling in tuning mode.*

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Figure 54. **SD high-speed mode**

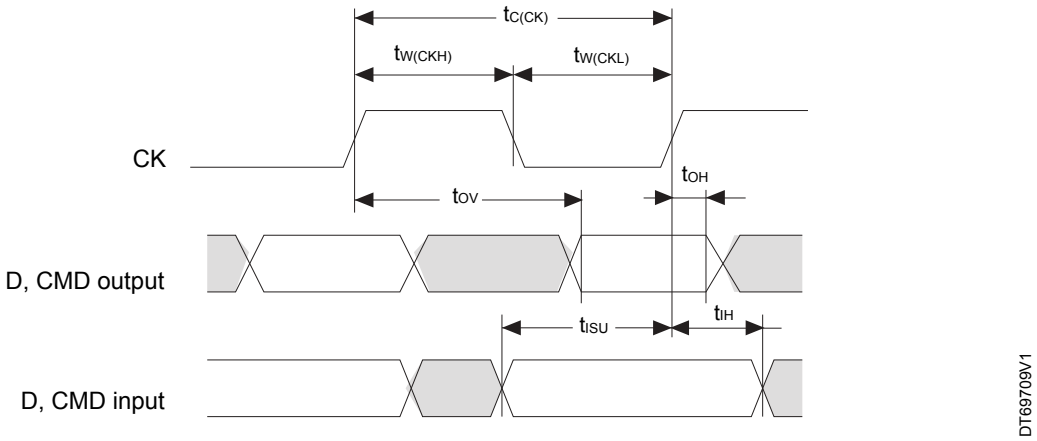


Figure 55. **SD default mode**

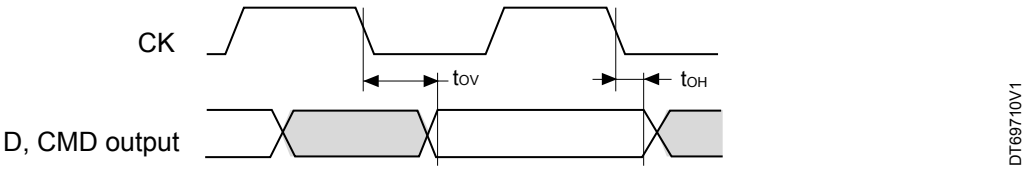
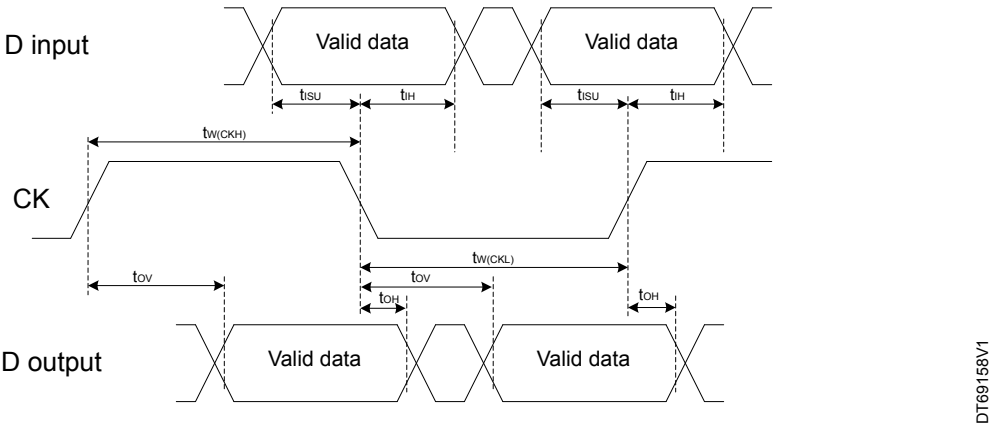


Figure 56. **SDMMC DDR mode**



6.3.36.7 *FDCAN (controller area network) interface*

Refer to Section 6.3.16: I/O port characteristics for more details on the input/output alternate function characteristics (FDCANx_TX and FDCANx_RX).

6.3.36.8 *Ethernet (ETH) characteristics*

Unless otherwise specified, the parameters given in Table 116, Table 117, Table 118 and Table 119. Ethernet MAC timings for RGMII (WARNING: DUMMY DATA TBD) for MDIO/SMA, RMII, GMII, RGMII and MII are derived from tests performed under the ambient temperature, F_{axiss_ck} frequency summarized in Table 17. General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 20 pF
- Measurement points are done at CMOS levels: 0.5 × V_{DD}.

Refer to I/O port characteristics for more details on the input/output characteristics.

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Table 116 gives the list of Ethernet MAC timings for the MDIO/SMA and Figure 57 shows the corresponding timing diagram.

Table 116. Ethernet MAC timings for MDIO/SMA (WARNING: DUMMY DATA TBD)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time (2.5 MHz)	-	-	400	-	ns
$t_{d(MDIO)}$	Write data valid time	-	0.5	1	3	
$t_{su(MDIO)}$	Read data setup time	-	13.5	-	-	
$t_{h(MDIO)}$	Read data hold time	-	0	-	-	

Figure 57. Ethernet MDIO/SMA timing diagram

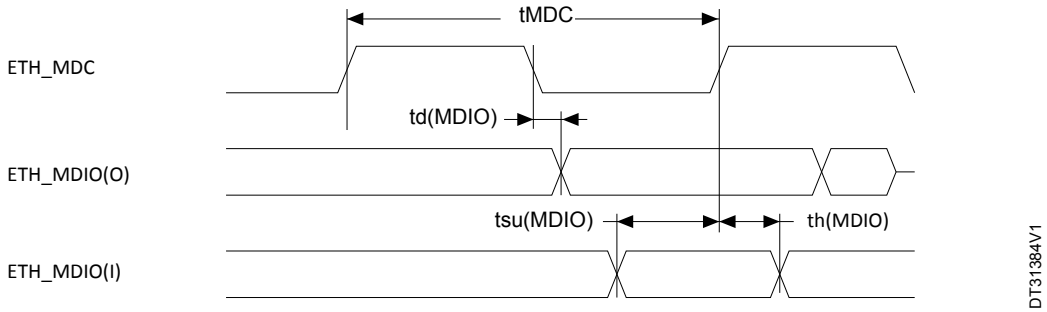

Table 117 gives the list of Ethernet MAC timings for the RMII and Figure 58 shows the corresponding timing diagram.

Table 117. Ethernet MAC timings for RMII (WARNING: DUMMY DATA TBD)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	-	2	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	-	1.5	-	-	
$t_{su(CRS)}$	Carrier sense setup time	-	1.5	-	-	
$t_{ih(CRS)}$	Carrier sense hold time	-	1.5	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	-	5.5	6.5	9.5	
$t_{d(TXD)}$	Transmit data valid delay time	-	6	6.5	10	

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Figure 58. Ethernet RMII timing diagram

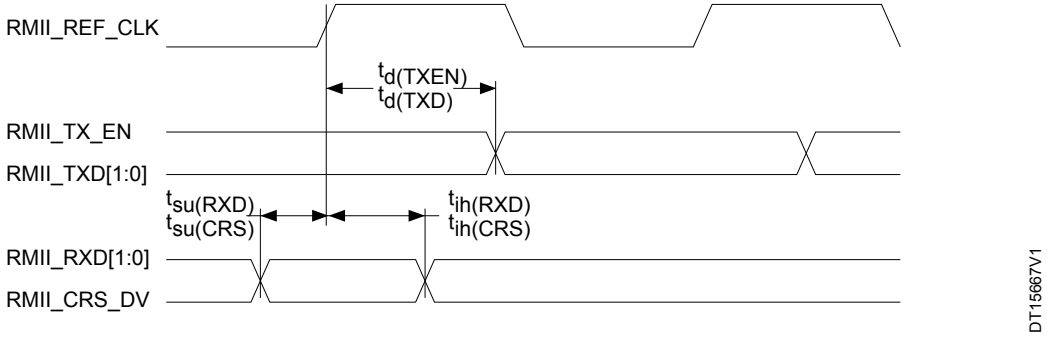

Table 118 gives the list of Ethernet MAC timings for MII and Figure 59 shows the corresponding timing diagram.

Table 118. Ethernet MAC timings for MII (WARNING: DUMMY DATA TBD)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	-	2	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	-	1	-	-	
$t_{su(DV)}$	Data valid setup time	-	1	-	-	
$t_{ih(DV)}$	Data valid hold time	-	0.5	-	-	
$t_{su(ER)}$	Error setup time	-	1	-	-	
$t_{ih(ER)}$	Error hold time	-	0.5	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	-	6	7.5	10.5	
$t_{d(TXD)}$	Transmit data valid delay time	-	7	8	11	

Figure 59. Ethernet MII timing diagram

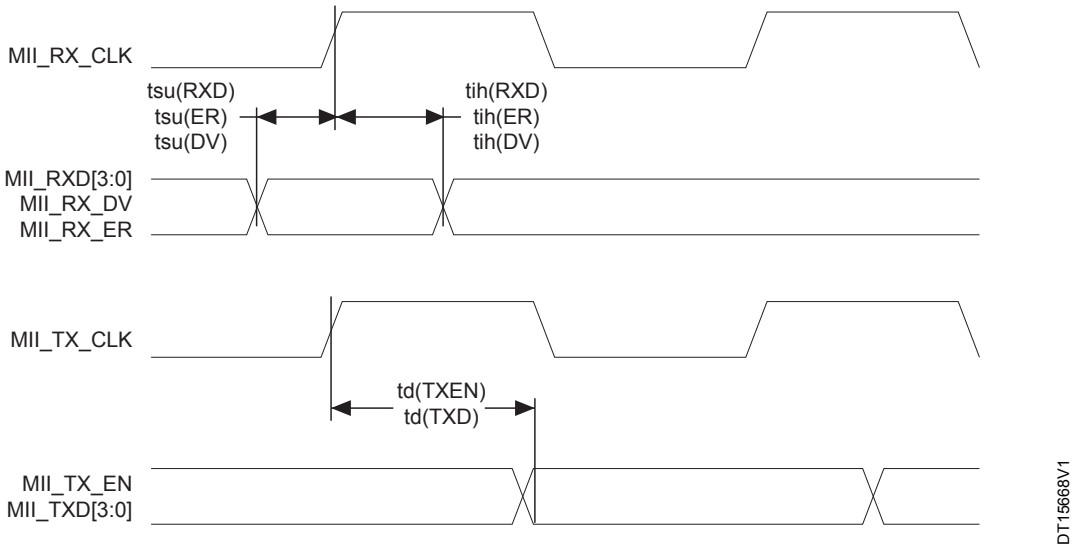

Table 119. Ethernet MAC timings for RGMII (WARNING: DUMMY DATA TBD)

Evaluated by characterization, not tested in production unless otherwise specified.

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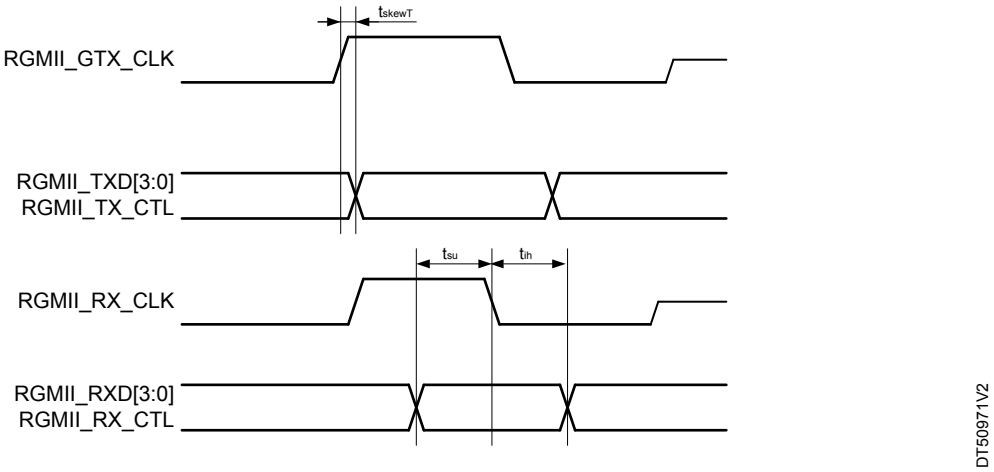
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	-	1.12[(1)]	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	-	0.83[(1)]	-	-	
$t_{su(RX_CTL)}$	Receive control valid setup time	-	1.12[(1)]	-	-	
$t_{ih(RX_CTL)}$	Receive control valid hold time	-	0.83[(1)]	-	-	
$t_{skew(TX_CTL)}$	Transmit control valid delay time	-	-0.25	0.25	0.5	
$t_{skew(TXD)}$	Transmit data valid delay time	-	-0.25	0.25	0.5	

1. *Specified by design, not tested in production.*

Figure 60. Ethernet RGMII timing diagram



6.3.36.9 *USART interface characteristics*

Unless otherwise specified, the parameters given in Table 120 for USART are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 120 , with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 × V_{DD}

Refer to Section 6.3.16: I/O port characteristics for more details on the input/output alternate function characteristics (NSS, CK, TX, RX for USART).

Table 120. USART characteristics (WARNING: DUMMY DATA TBD)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	Master mode	-	-	TBD	MHz
		Slave mode	-	-	TBD	
$t_{su(NSS)}$	NSS setup time	Slave mode	t_{ker} + 2[(1)]	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2	-	-	ns
$t_{w(CKH)}$, $t_{w(CKL)}$	CK high and low time	Master mode	1 / f_{CK} / 2 - 1	1 / f_{CK} / 2	1 / f_{CK} / 2 + 1	ns
$t_{su(RX)}$	Data input setup time	Master mode	t_{ker} + 3[(1)]	-	-	ns
		Slave mode	2	-	-	
$t_{h(RX)}$	Data input hold time	Master mode	1	-	-	ns

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{h(RX)}$	Data input hold time	Slave mode	1	-	-	ns
$t_{v(TX)}$	Data output valid time	Slave mode	-	10	18	ns
		Master mode	-	0.5	1	
$t_{h(TX)}$	Data output hold time	Slave mode	8	-	-	ns
		Master mode	0	-	-	

1. t_{ker} *is the usart_ker_ck_pres clock period defined in the product reference manual.*

Figure 61. USART timing diagram in master mode

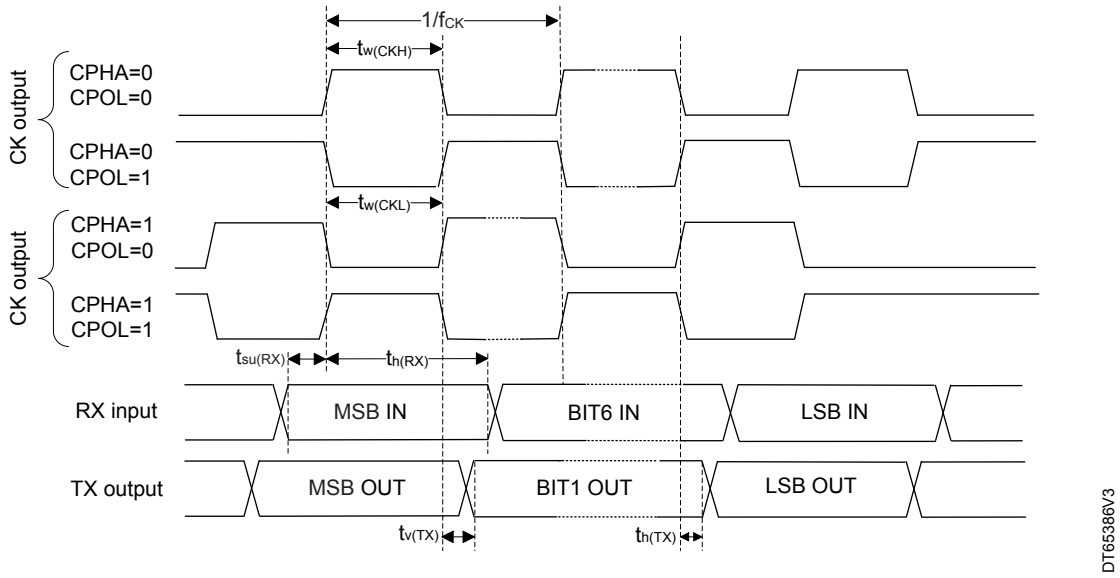
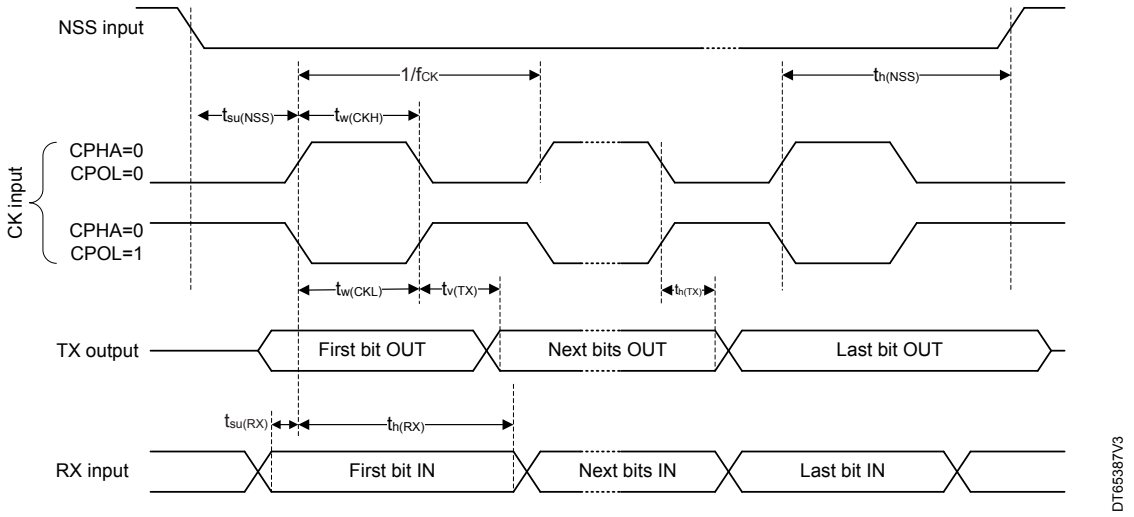


Figure 62. USART timing diagram in slave mode



6.3.37 Embedded PHYs characteristics

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6.3.37.1 DDR PHY characteristics

Table 121. DDR PHY characteristics

Specified by design, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{ZQ}	External resistor on DDR_ZQ	-	237.6	240	242.4	Ω
DDR4, 2400 Mbps, 32-bit, 10 ACx4, 1 Rank, DBI off						
$I_{VDDCORE(DDRPHY)}$[1]	Supply current on V_{DDCORE}	Read	-	135	235	mA
		Write	-	175	290	
		Idle	-	80.5	165	
		DFI_LP	-	26	97.5	
		Inactive	-	3.65	70	
		Retention[2]		OFF		
$I_{VDDA18DDR}$[1]	Supply current on $V_{DDA18DDR}$	Read	-	4.3	-	mA
		Write	-	4.3	-	
		Idle	-	4.3	-	
		DFI_LP	-	4.3	-	
		Inactive	-	0.12	0.16	
		Retention[2]		OFF		
$I_{VDDQDDR}$[1]	Supply current on V_{DDQDDR}	Read	-	415	490	mA
		Write	-	310	360	
		Idle	-	72	84.5	
		DFI_LP	-	2.85	5.5	
		Inactive	-	0.12	1.9	
		Retention[2]	-	0.017	1.7	
DDR4, 2400 Mbps, 16-bit, 10 ACx4, 1 Rank, DBI off						
$I_{VDDCORE(DDRPHY)}$[1]	Supply current on V_{DDCORE}	Read	-	93.5	160	mA
		Write	-	115	190	
		Idle	-	65	125	
		DFI_LP	-	22	70	
		Inactive	-	3.65	70	
		Retention[2]		OFF		
$I_{VDDA18DDR}$[1]	Supply current on $V_{DDA18DDR}$	Read	-	4.3	-	mA
		Write	-	4.3	-	
		Idle	-	4.3	-	
		DFI_LP	-	4.3	-	
		Inactive	-	0.12	0.16	
		Retention[2]		OFF		
$I_{VDDQDDR}$[1]	Supply current on V_{DDQDDR}	Read	-	235	275	mA
		Write	-	180	215	
		Idle	-	37	43	
		DFI_LP	-	1.9	3.6	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{VDDQDDR}$[1]	Supply current on V_{DDQDDR}	Inactive	-	0.12	1.35	mA
		Retention[2]	-	0.017	1.2	
DDR3L, 2133 Mbps, 32-bit, 10 ACx4, 1 Rank						
$I_{VDDCORE(DDRPHY)}$[1]	Supply current on V_{DDCORE}	Read	-	130	210	mA
		Write	-	170	275	
		Idle	-	76.5	150	
		DFI_LP	-	25	86.5	
		Inactive	-	3.6	60	
		Retention[2]	OFF			
$I_{VDDA18DDR}$[1]	Supply current on $V_{DDA18DDR}$	Read	-	4.3	-	mA
		Write	-	4.3	-	
		Idle	-	4.3	-	
		DFI_LP	-	4.3	-	
		Inactive	-	0.12	0.16	
		Retention[2]	OFF			
$I_{VDDQDDR}$[1]	Supply current on V_{DDQDDR}	Read	-	420	475	mA
		Write	-	475	530	
		Idle	-	71.5	79.5	
		DFI_LP	-	3.25	5.85	
		Inactive	-	0.135	2	
		Retention[2]	-	0.0225	1.75	
DDR3L, 2133 Mbps, 16-bit, 10 ACx4, 1 Rank						
$I_{VDDCORE(DDRPHY)}$[1]	Supply current on V_{DDCORE}	Read	-	88.5	145	mA
		Write	-	110	175	
		Idle	-	62.5	115	
		DFI_LP	-	21	62.5	
		Inactive	-	3.6	60	
		Retention[2]	OFF			
$I_{VDDA18DDR}$[1]	Supply current on $V_{DDA18DDR}$	Read	-	4.3	-	mA
		Write	-	4.3	-	
		Idle	-	4.3	-	
		DFI_LP	-	4.3	-	
		Inactive	-	0.12	0.16	
		Retention[2]	OFF			
$I_{VDDQDDR}$[1]	Supply current on V_{DDQDDR}	Read	-	245	275	mA
		Write	-	270	305	
		Idle	-	39.5	44.5	
		DFI_LP	-	2.15	3.85	
		Inactive	-	0.135	1.4	
		Retention[2]	-	0.0225	1.2	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LPDDR4, 2400 Mbps, 32-bit, 10 ACx4, 1 Rank, DBI off						
$I_{VDDCORE(DDRPHY)}$[1]	Supply current on V_{DDCORE}	Read	-	140	245	mA
		Write	-	165	285	
		Idle	-	73	160	
		DFI_LP	-	25	99	
		Inactive	-	3.65	70.5	
		Retention[2]	OFF			
$I_{VDDA18DDR}$[1]	Supply current on $V_{DDA18DDR}$	Read	-	4.3	-	mA
		Write	-	4.3	-	
		Idle	-	4.3	-	
		DFI_LP	-	4.3	-	
		Inactive	-	0.12	0.16	
		Retention[2]	OFF			
$I_{VDDQDDR}$[1]	Supply current on V_{DDQDDR}	Read	-	125	150	mA
		Write	-	480	545	
		Idle	-	49.5	57.5	
		DFI_LP	-	2.6	4.85	
		Inactive	-	0.11	1.75	
		Retention[2]	-	0.0185	1.55	
LPDDR4, 2400 Mbps, 16-bit, 10 ACx4, 1 Rank, DBI off						
$I_{VDDCORE(DDRPHY)}$[1]	Supply current on V_{DDCORE}	Read	-	91	160	mA
		Write	-	110	185	
		Idle	-	59.5	120	
		DFI_LP	-	22	70	
		Inactive	-	3.65	70.5	
		Retention[2]	OFF			
$I_{VDDA18DDR}$[1]	Supply current on $V_{DDA18DDR}$	Read	-	4.3	-	mA
		Write	-	4.3	-	
		Idle	-	4.3	-	
		DFI_LP	-	4.3	-	
		Inactive	-	0.12	0.16	
		Retention[2]	OFF			
$I_{VDDQDDR}$[1]	Supply current on V_{DDQDDR}	Read	-	110	125	mA
		Write	-	285	325	
		Idle	-	48.5	56	
		DFI_LP	-	1.7	3.2	
		Inactive	-	0.11	1.25	
		Retention[2]	-	0.0185	1.1	
Low power exit latency						
t_{EXIT}	Exit latency from DFI_LP state	-	-	2	-	DFI_CLK

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{EXIT}	Exit latency from inactive state	DDR3L, DDR4	-	3	-	µs
		LPDDR4	-	3 + 2560 DDR_CLK	-	
	Exit latency from retention state after supplies restored	DDR3L, DDR4	-	3	-	
		LPDDR4	-	3 + 2560 DDR_CLK	-	

1. *Evaluated by characterization, not tested in production.*
2. *V_{DDCORE} OFF, $V_{DDA18DDR}$ OFF.*

6.3.37.2 DSI PHY Characteristics

Table 122. DSI PHY characteristics

Specified by design, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{CK}	DSI link clock frequency	High-Speed mode (HS)		40	-	1250	MHz
rate	Data rate per lane	High-Speed mode (HS)		80	-	2500	Mbps
UI	Unit interval	equal to 0.5 / f_{CK} (HS)		0.4	-	12.5	ns
$t_{clkhs2lp}$	Time to switch DSI_CK from High-Speed to LP	fixed part		-	-	TBD	ns
		variable part UI = 0.5 / f_{CK} (HS)		-	-	TBD	UI
$t_{clklp2hs}$	Time to switch DSI_CK from LP to High-Speed	fixed part		-	-	TBD	ns
		variable part UI = 0.5 / f_{CK} (HS)		-	-	TBD	UI
t_{hs2lp}	Time to switch DSI_Dx from High-Speed to LP	fixed part		-	-	TBD	ns
		variable part UI = 0.5 / f_{CK} (HS)		-	-	TBD	UI
t_{lp2hs}	Time to switch DSI_Dx from LP to High-Speed	fixed part		-	-	TBD	ns
		variable part UI = 0.5 / f_{CK} (HS)		-	-	TBD	UI
R_{EXT}	External resistor on REXT	Connected to ground		198	200	202	Ω
$I_{VDDCORE(DSIPHY)}$[1]	Supply current on V_{DDCORE}[2]	High-Speed Transmit[3]	4 lanes @1 Gbps	-	1.55	9.6	mA
			4 lanes @1.5 Gbps	-	2.05	11	
			4 lanes @2 Gbps	-	2.55	11.5	
			4 lanes @2.5 Gbps	-	3.05	12.5	
		LP Transmit	Lane 0 @10 Mbps, PLL @2.5 Gbps	-	2.05	10.5	
		ULPS Transmit	PLL disabled	-	0.155	8.05	
$I_{VDDA18DSI}$	Supply current on $V_{DDA18DSI}$[2]	High-Speed Transmit[3]	4 lanes	-	5.35	9.55	mA
		LP Transmit	Lane 0 @10 Mbps, PLL @2.5 Gbps	-	3.85	5.05	
		ULPS Transmit	PLL disabled	-	0.0155	0.0385	
I_{VDDDSI}	Supply current on V_{DDDSI}	High-Speed Transmit[3]	4 lanes @1Gbps	-	14.5	19	mA
			4 lanes @1.5 Gbps	-	17	23	

Prerelease product(s)

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{VDDDSI}	Supply current on V_{DDDSI}	High-Speed Transmit(3)	4 lanes @2 Gbps	-	19.5	26.5	mA
			4 lanes @2.5 Gbps	-	22.5	30	
		LP Transmit	Lane 0 @10 Mbps, PLL @2.5 Gbps	-	7.45	10.5	
		ULPS Transmit	PLL disabled	-	0.0505	0.805	

1. *Evaluated by characterization, not tested in production.*
2. *values includes PLL power consumption.*
3. *HS mode: assume PRBS9 pattern on data lanes and 100% occupation; that is, continuous HS.*

6.3.37.3 CSI PHY Characteristics

Table 123. CSI PHY characteristics

Specified by design, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{EXT}	External resistor on REXT	Connected to ground		198	200	202	Ω
$I_{VDDCORE(CSIPHY)}$(1)	Supply current on V_{DDCORE}	High-speed receive(2)	2 lanes @1 Gbps	-	2.8	12	mA
			2 lanes @1.5 Gbps	-	3.7	13	
			2 lanes @2 Gbps	-	4.7	14.5	
			2 lanes @2.5 Gbps	-	5.7	15.5	
		LP receive	Lane 0 @10 Mbps	-	0.71	8	
		ULPS receive	ck_ker_csi2phy stopped	-	0.35	8.4	
$I_{VDDA18CSI}$(1)	Supply current on $V_{DDA18CSI}$	High-speed receive(2)	2 lanes @1 Gbps	-	2.2	2.85	mA
			2 lanes @1.5 Gbps	-	2.3	3	
			2 lanes @2 Gbps	-	2.6	3.35	
			2 lanes @2.5 Gbps	-	2.6	3.35	
		LP receive	Lane 0 @10Mbps	-	1.7	2.3	
		ULPS receive	ck_ker_csi2phy stopped	-	0.015	0.1	
I_{VDDCSI}(1)	Supply current on V_{DDCSI}	High-speed receive(2)	2 lanes @1 Gbps	-	3.95	5.1	mA
			2 lanes @1.5 Gbps	-	4.5	5.8	
			2 lanes @2 Gbps	-	3.8	5.5	
			2 lanes @2.5 Gbps	-	4.3	6	
		LP receive	Lane 0 @10 Mbps	-	0.9	1.5	
		ULPS receive	ck_ker_csi2phy stopped	-	0.04	0.6	

1. *Evaluated by characterization, not tested in production.*
2. *HS mode: assume PRBS9 pattern on data lanes and 100% occupation; that is, continuous HS.*

6.3.37.4 LVDS PHY Characteristics

Table 124. LVDS PHY characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LVDS lane characteristics						
V_{OH}	Output voltage high	-	1350	1400	1450	mV
V_{OL}	Output voltage low	-	995	1000	1050	mV

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\|V_{OD}\|$	Output differential voltage	-	340	370	420	mV
V_{OS}	Output offset voltage	-	1150	1200	1250	mV
R_O	Output impedance, single ended	-	44	60.5	76.5	Ω
ΔR_O	Ro mismatch between P and N output	-	-	-	8	%
$\|\Delta V_{OD}\|$	Change in $\|V_{OD}\|$ between 0 and 1	-	0.01	1.15	2.6	mV
ΔV_{OS}	Change in V_{OS} between 0 and 1	-	0.4	1.2	11	mV
Is	Output current (drawn from $V_{DDA18LVDS}$)	Static current on 100Ω differential load	2.55	3.2	3.9	mA
		Outputs shorted to ground	10	14	25.5	mA
		Outputs shorted together	2.55	3.15	8.05	mA
t_f	V_{OD} fall time, 20 – 80%(1)(2)	-	195	270	340	ps
t_r	V_{OD} rise time, 20 – 80%(1)(2)	-	175	245	400	ps
ppV_{OD}	Dynamic output signal balance(1)(2)	-	46	87.5	140	mV
LVDS bandgap characteristics						
$I_{VDDA18LVDS}$	Bandgap supply current on $V_{DDA18LVDS}$	- -	-	0.805	1.25	mA
$I_{VDDLVDS}$	Bandgap supply current on V_{DDLVDS}	- -	-	3.25	3.95	mA

1. *Loading conditions are: two 50Ω resistors, two 2.5 pF caps at each output, one 2.5 pF cap at middle point.*
2. *Specification for default configuration (no pre-emphasis).*

6.3.37.5 *USB2PHY Characteristics*

Table 125. USB high-speed PHY characteristics

Specified by design, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{TXRTUNE}$	External resistor on TXRTUNE	Connected to ground		198	200	202	Ω
$I_{VDDCORE(USB2PHY)}$(1)	Supply current on V_{DDCORE}	HS transmit, maximum transition density(2)		-	5.05	11.5	mA
		HS transmit, minimum transition density(3)		-	4.35	11.5	
		HS Idle(4)		-	6.55	12	
		FS transmit, maximum transition density(5)		-	6.05	12	
		LS transmit, maximum transition density(6)		-	3.35	12.5	
		Suspend(7)		-	2.6	6.05	
		Sleep(8)		-	2.15	6.45	
		Battery charging	VDATDETENB = 0, VDATSRCENB = 1(9)	-	1.5	8.2	
			VDATDETENB = 1, VDATSRCENB = 1	-	2.8	10.5	
$I_{VDDA18USB}$(1)	Supply current on $V_{DDA1V8USB}$	HS transmit, maximum transition density(2)		-	17	19.5	mA
		HS transmit, minimum transition density(3)		-	14.5	15.5	
		HS idle(4)		-	5.05	5.85	
		FS Transmit, maximum transition density(5)		-	5	5.9	
		LS Transmit, maximum transition density(6)		-	5.1	6.15	
		Suspend(7)		-	0.027	0.115	

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{VDDA18USB}$[1]	Supply current on $V_{DDA1V8USB}$	Sleep[8]		-	0.032	1.8	mA
		Battery charging	VDATDETENB = 0, VDATSRCENB = 1[9]	-	3.55	5.4	
			VDATDETENB = 1, VDATSRCENB = 1	-	4.3	5.4	
$I_{VDD33USB}$[1]	Supply current on $V_{DD33USB}$	HS transmit, maximum transition density[2]		-	3.45	3.6	mA
		HS transmit, minimum transition density[3]		-	2.4	2.55	
		HS idle[4]		-	2.2	3.2	
		FS transmit, maximum transition density[5]		-	12	13.5	
		LS transmit, maximum transition density[6]		-	12	13	
		Suspend[7]		-	0.059	0.21	
		Sleep[8]		-	0.086	0.2	
		Battery charging	VDATDETENB = 0, VDATSRCENB = 1[9]	-	2.1	2.4	
			VDATDETENB = 1, VDATSRCENB = 1	-	2.2	2.4	

1. *Evaluated by characterization, not tested in production.*
2. *Packet transmission by one transceiver operating in device mode while driving all 0's data (constant JKJK on DP/DM). Loading of 10 pF. Transfers do not include any interpacket delay.*
3. *Packet transmission by one transceiver operating in device mode while driving all 1's data (alternating 7-bit strings of J, then K on DP/DM). Loading of 10 pF. Transfers do not include any interpacket delay.*
4. *HS receive mode with no traffic on the line.*
5. *Packet transmission by one transceiver operating in device mode while driving all 0's data (constant JKJK on DP/DM). Loading of 50 pF. Transfers do not include any interpacket delay.*
6. *Packet transmission by one transceiver operating in host mode while driving all 0's data (constant JKJK on DP/DM). Loading of 600 pF. Transfers do not include any interpacket delay.*
7. *Suspend when operating in device mode with no far-side host termination on DP/DM during measurements. Measurements taken when COMMONONN (SYSCFG_USB2PHYxCR.USB2PHYxCMN) is deasserted.*
8. *Sleep mode when operating in Device mode with no far-side host termination on DP/DM during measurements.*
9. *PHY is in suspend (with clocks turned OFF), non-driving mode and operating as a portable device in the 'dead battery' condition.*

6.3.37.6 COMBOPHY Characteristics

Table 126. COMBOPHY characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{EXT}[1]	External resistor on REXT	Connected to ground		198	200	202	Ω
$I_{VDDCOMBOPHY}$	Supply current on $V_{DDCOMBOPHY}$	P0 mode	5 Gbps	-	22	38	mA
			2.5 Gbps	-	14	37.5	
		P0s mode	5 Gbps	-	16.5	33	
			2.5 Gbps	-	13	28	
		P1 mode	5 Gbps	-	9.7	24.5	
			2.5 Gbps	-	9.7	24.5	
		P1.CPM	-	-	1.45	14.5	
		P1.1	-	-	0.215	12.5	
		P1.2	-	-	0	12	

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{VDDCOMBOPHY}$	Supply current on $V_{DDCOMBOPHY}$	P2	-	-	1.35	14.5	mA
		P2.CPM	-	-	1.2	14	
		Power down	-	-	0.19	13	
$I_{VDDCOMBOPHYTX}$	Supply current on $V_{DDCOMBOPHYTX}$	P0 mode	5 Gbps	-	12	15	mA
			2.5 Gbps	-	6.4	8.9	
		P0s mode	5 Gbps	-	1.4	2.4	
			2.5 Gbps	-	1.4	2.4	
		P1 mode	5 Gbps	-	1.4	2.4	
			2.5 Gbps	-	1.4	2.4	
		P1.CPM	-	-	1.45	2.4	
		P1.1	-	-	1.45	2.4	
		P1.2	-	-	0.005	0.405	
		P2	-	-	0.005	0.41	
		P2.CPM	-	-	0.005	0.41	
		Power down	-	-	0.008	0.425	
$I_{VDDA18COMBOPHY}$	Supply current on $V_{DDA18COMBOPHY}$	P0 mode	5 Gbps	-	24.5	29.5	mA
			2.5 Gbps	-	17.5	24	
		P0s mode	5 Gbps	-	14.5	20.5	
			2.5 Gbps	-	14	19.5	
		P1 mode	5 Gbps	-	8.4	11.5	
			2.5 Gbps	-	8.4	11.5	
		P1.CPM	-	-	2.35	2.75	
		P1.1	-	-	2.2	2.55	
		P1.2	-	-	0.375	0.785	
		P2	-	-	1.2	2.05	
		P2.CPM	-	-	0.54	0.985	
		Power down	-	-	0.049	0.105	
N_{FTS}[(1)]	Minimum number of FTS ordered sets that must be sent for retraining when transitioning from P0s to P0			48	-	-	FTS
$t_{P0s_to_P0}$	Time from pipe powerdown change to P0		5 Gbps	-	-	48	ns
			2.5 Gbps	-	-	96	
$t_{P1_to_P0}$	Time from pipe powerdown change to P0		5 Gbps	-	-	0.9	µs
			2.5 Gbps	-	-	1.8	
$t_{P2_to_P0}$	Time from pipe powerdown change to P0		100 MHz reference clock	-	-	260	µs
$t_{P0_to_P2}$	Time from pipe powerdown change to P2		-	-	-	250	ns
$t_{P2_to_P1}$	Time from pipe powerdown change to P1		100 MHz reference clock	-	-	255	µs
$t_{Reset_to_ready}$	Time from pipe reset de-assertion to PHY acknowledgment		100 MHz reference clock	-	-	255	-
t_{MPLL_lock}	Time from phy_mpll_en assertion to when phy_mpll_state is high		100 MHz reference clock	-	-	15	µs
$t_{Resistor_tuning}$	Time to complete a resistor tune		-	-	-	8	-

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{Common_mode}	Time to establish Common mode when exiting reset or P2 state		-	-	240	µs
$t_{P1.1_to_P1}$	Time from macN_pclkreq_n assertion to pipeN_clkreq_n assertion		-	-	15	-
$t_{P1.2_to_P1}$	Time from macN_pclkreq_n assertion to pipeN_clkreq_n assertion		-	-	15	µs
$t_{P1.2_to_P1_to_P0}$	Time from macN_pclkreq_n assertion to pipeN_clkreq_n assertion and pipeN_powerdown request to P0 until PHY acknowledgment		-	-	16.8	-
$t_{P1.CPM_to_P1}$	Time from macN_pclkreq_n assertion to pipeN_clkreq_n assertion		-	-	15	µs
$t_{COMMON_MODE_REC}$	Time for the Common mode voltage to be reached on pins while transmitting in Recovery mode. This parameter applies to an exit from P1.2 through P1 to P0 (Recovery) and represents the extra time in which the MAC is required to send TS1 ordered sets.		-	-	55	µs

1. *Specified by design, not tested in production.*

Table 127. PCIE REFCLKGEN characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol[1]	Parameter	Conditions	Min	Typ	Max	Unit
$I_{VDDPCIECLK}$	Power consumption on $V_{DDPCIECLK}$	100 MHz clock	-	-	3	mA
Z_O	Single ended output impedance	IMP_CTRL = 0b11000	52	61	70	Ω
		IMP_CTRL = 0b11001	48	56.5	65	
		IIMP_CTRL = 0b11010	45	53	64	
		IMP_CTRL = 0b11011 (default)	42	49.5	57.5	
		IMP_CTRL = 0b11100	40	47	54	
		IMP_CTRL = 0b11101	37.5	44.5	51	
		IMP_CTRL = 0b11110	35.5	42	48.5	
		IMP_CTRL = 0b11111	34	40	46	
V_{SWING}	Singled ended swing in % of $V_{DDPCIECLK}$	IMP_CTRL[4:3] = 0b00000	-	55	-	%
		IMP_CTRL[4:3] = 0b01000	-	70	-	
		IMP_CTRL[4:3] = 0b10000	-	85	-	
		IMP_CTRL[4:3] = 0b11000	-	100	-	
		IMP_CTRL[4:3] = 0b00001	-	66	-	
		IMP_CTRL[4:3] = 0b01001	-	77	-	
		IMP_CTRL[4:3] = 0b10001	-	89	-	
		IMP_CTRL[4:3] = 0b11001	-	100	-	
		IMP_CTRL[4:3] = 0b00010	-	61	-	
		IMP_CTRL[4:3] = 0b01010	-	74	-	
		IMP_CTRL[4:3] = 0b10010	-	87	-	
		IMP_CTRL[4:3] = 0b11010	-	100	-	
		IMP_CTRL[4:3] = 0b00011	-	70	-	
		IMP_CTRL[4:3] = 0b01011	-	90	-	
		IMP_CTRL[4:3] = 0b10011	-	80	-	
		IMP_CTRL[4:3] = 0b11011 (default)	-	100	-	
		IMP_CTRL[4:3] = 0b00100	-	58	-	
		IMP_CTRL[4:3] = 0b01100	-	70	-	
		IMP_CTRL[4:3] = 0b10100	-	85	-	

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Symbol[1]	Parameter	Conditions	Min	Typ	Max	Unit
V_{SWING}	Singled ended swing in % of $V_{DDPCIECLK}$	IMP_CTRL[4:3] = 0b11100	-	100	-	%
		IMP_CTRL[4:3] = 0b00101	-	68	-	
		IMP_CTRL[4:3] = 0b01101	-	79	-	%
		IMP_CTRL[4:3] = 0b10101	-	90	-	
		IMP_CTRL[4:3] = 0b11101	-	100	-	
		IMP_CTRL[4:3] = 0b00110	-	64	-	
		IMP_CTRL[4:3] = 0b01110	-	76	-	
		IMP_CTRL[4:3] = 0b10110	-	88	-	
		IMP_CTRL[4:3] = 0b11110	-	100	-	
		IMP_CTRL[4:3] = 0b00111	-	71	-	
		IMP_CTRL[4:3] = 0b01111	-	80	-	
		IMP_CTRL[4:3] = 0b10111	-	90	-	
		IMP_CTRL[4:3] = 0b11111	-	100	-	
t_r/t_f	Rise and Fall time[2] [3] [4]		0.6	-	4	V/ns
V_{CROSS}	Absolute crossing point voltage[5][6][7]		250	400	550	mV
ΔV_{CROSS}	Variation of V_{CROSS} over all rising clock edges[5][6][8]		-	-	140	mV
Duty_Cycle	Duty cycle[2]		40	50	60	%
Matching	Rising edge rate to falling edge rate matching[5][9]		-	-	20	%

1.
2. *PCIE_CLKOUTP and PCIE_CLKOUTN are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load CL = 2 pF.*
3. *Measured from -150 mV to +150 mV on the differential waveform (derived from PCIE_CLKOUTP minus PCIE_CLKOUTN). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.*
4. *Measurement taken from differential waveform.*
5. *Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.*
6. *Measured at crossing point where the instantaneous voltage value of the rising edge of PCIE_CLKOUTP equals the falling edge of PCIE_CLKOUTN.*
7. *Measurement taken from single ended waveform.*
8. *Defined as the total variation of all crossing voltages of rising PCIE_CLKOUTP and falling PCIE_CLKOUTN. This is the maximum allowed variance in V_{CROSS} for any particular system.*
9. *Matching applies to rising edge rate for PCIE_CLKOUTP and falling edge rate for PCIE_CLKOUTN. It is measured using a ± 75 mV window centered on the median cross point where PCIE_CLKOUTP rising meets PCIE_CLKOUTN falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of PCIE_CLKOUTP should be compared to the fall edge rate of PCIE_CLKOUTN, the maximum allowed difference should not exceed 20% of the slowest edge rate.*

6.3.37.7 UCPDPHY Characteristics

Table 128. UCPDPHY characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{BITRATE}$	Bit rate (ensured by adequate RCC and UCPD settings)		270	300	330	Kbps
$C_{RECEIVER}$	Local capacitance added on PCB on each CC line		200	470	600	pF

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TRANSMITTER						
V_{SWING}	Voltage swing applies on CC pin to both no load condition and under the load condition.		1.05	1.125	1.2	V
Z_{DRIVER}	TX output impedance. Source output impedance at the Nyquist frequency of USB2.0 low speed (750 kHz) while the source is driving the CC line.		33	-	75	Ω
T_r / T_f	Rise / Fall Time. 10% to 90% / 90% to 10% amplitude points, minimum is under an unloaded condition. Maximum set by TX mask.		300	-	735	ns
DCYCLE	TX duty cycle at 0.5625 V (see Y5Tx , BMC Tx 'ONE' mask and BMC Tx 'ZERO' mask in the PD Specification)[1]		47	-	53	%
RECEIVER						
V_{IL}	Rx receive input thresholds. The position of the center line of the inner mask is dependent on whether the receiver is sourcing or sinking power or is power neutral[1]	sourcing power	-	-	0.4825	V
V_{IH}			0.8925	-	-	
V_{IL}		sinking power	-	-	0.2325	V
V_{IH}			0.6425	-	-	
Hysteresis	Rx receive input hysteresis		0.15	-	-	
N_{COUNT}[2]	Number of transitions for signal detection (number to count to detect non-idle bus).		3	-	-	-
$t_{TRANWIN}$[2]	Time window for detecting non-idle bus.		12	-	20	µs
Z_{BMCRX}[3]	Receiver input impedance		1	-	-	MΩ

1. *Refer to the "USB Power Delivery (PD) Specification" Revision 3.1, Version 1.8.*
2. *BMC packet collision is avoided by the detection of signal transitions at the receiver. Detection is active when a minimum of NCOUNT transitions occur at the receiver within a time window of $t_{TRANWIN}$. After waiting $t_{TRANWIN}$ without detecting NCOUNT transitions, the bus is declared idle. This times are informative for UCPDPHY as it is done digitally inside UCPD Peripheral.*
3. *Does not include pull-up or pull-down resistance from cable detect. Transmitter is Hi-Z.*

6.3.38 JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in Table 129 and Table 130 for JTAG/SWD are derived from tests performed under the ambient temperature, frequency and V_{DD} supply voltage summarized in Table 17. General operating conditions , with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 0x10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 × V_{DD}

Refer to Section 6.3.16: I/O port characteristics for more details on the input/output characteristics.

Table 129. JTAG dynamic characteristics (WARNING: DUMMY DATA TBD)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp}	TCK clock frequency	3.0 V < V_{DD} < 3.6 V	-	-	TBD	MHz
$1/t_{c(TCK)}$		1.71 V < V_{DD} < 1.89 V	-	-	TBD	
$t_{isu(TMS)}$	TMS input setup time	-	2.5	-	-	ns
$t_{ih(TMS)}$	TMS input hold time	-	1	-	-	
$t_{isu(TDI)}$	TDI input setup time	-	2	-	-	
$t_{ih(TDI)}$	TDI input hold time	-	1	-	-	
$t_{ov\ (TDO)}$	TDO output valid time	3.0 V < V_{DD} < 3.6 V	-	8	14	

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{ov\ (TDO)}$	TDO output valid time	1.71 V < V_{DD} < 1.89 V	-	8	18	ns
$t_{oh(TDO)}$	TDO output hold time	-	7	-	-	

Figure 63. JTAG timing diagram

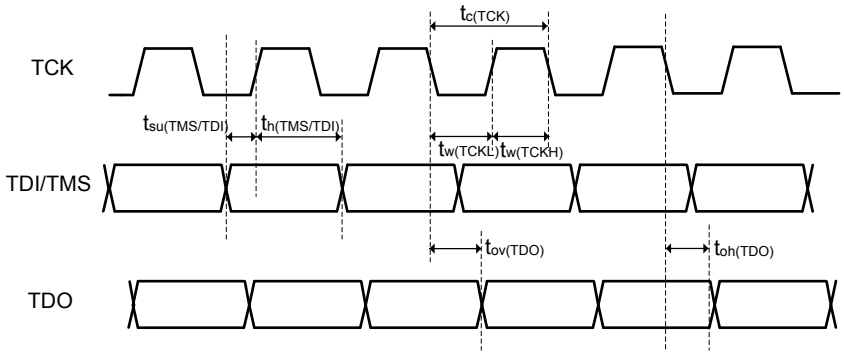
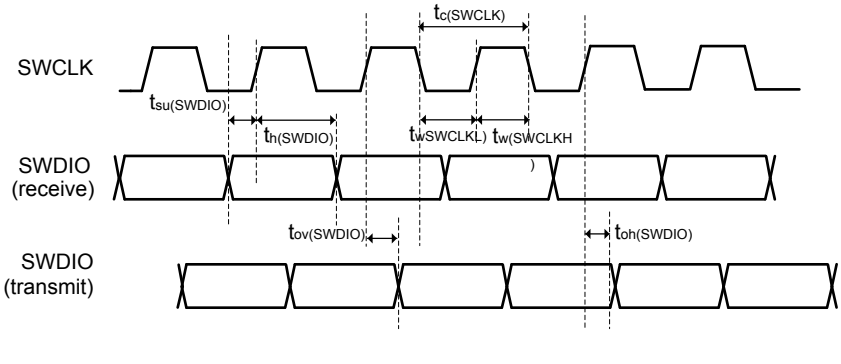


Table 130. SWD dynamic characteristics (WARNING: DUMMY DATA TBD)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp}	SWCLK clock frequency	3.0 V < V_{DD} < 3.6 V	-	-	TBD	MHz
$1/t_{c(SWCLK)}$		1.71 V < V_{DD} < 1.89 V	-	-	TBD	
$t_{isu(SWDIO)}$	SWDIO input setup time	-	2.5	-	-	ns
$t_{ih(SWDIO)}$	SWDIO input hold time	-	1	-	-	
$t_{ov\ (SWDIO)}$	SWDIO output valid time	3.0 V < V_{DD} < 3.6 V	-	8.5	14	
		1.71 V < V_{DD} < 1.89 V	-	8.5	18	
$t_{oh(SWDIO)}$	SWDIO output hold time	-	8	-	-	

Figure 64. SWD timing diagram



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7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 VFBGA361 package information (B09U)

This VFBGA is a 361-ball, 10 x 10 mm, very thin fine pitch ball grid array package.

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Figure 65. VFBGA361 - Outline

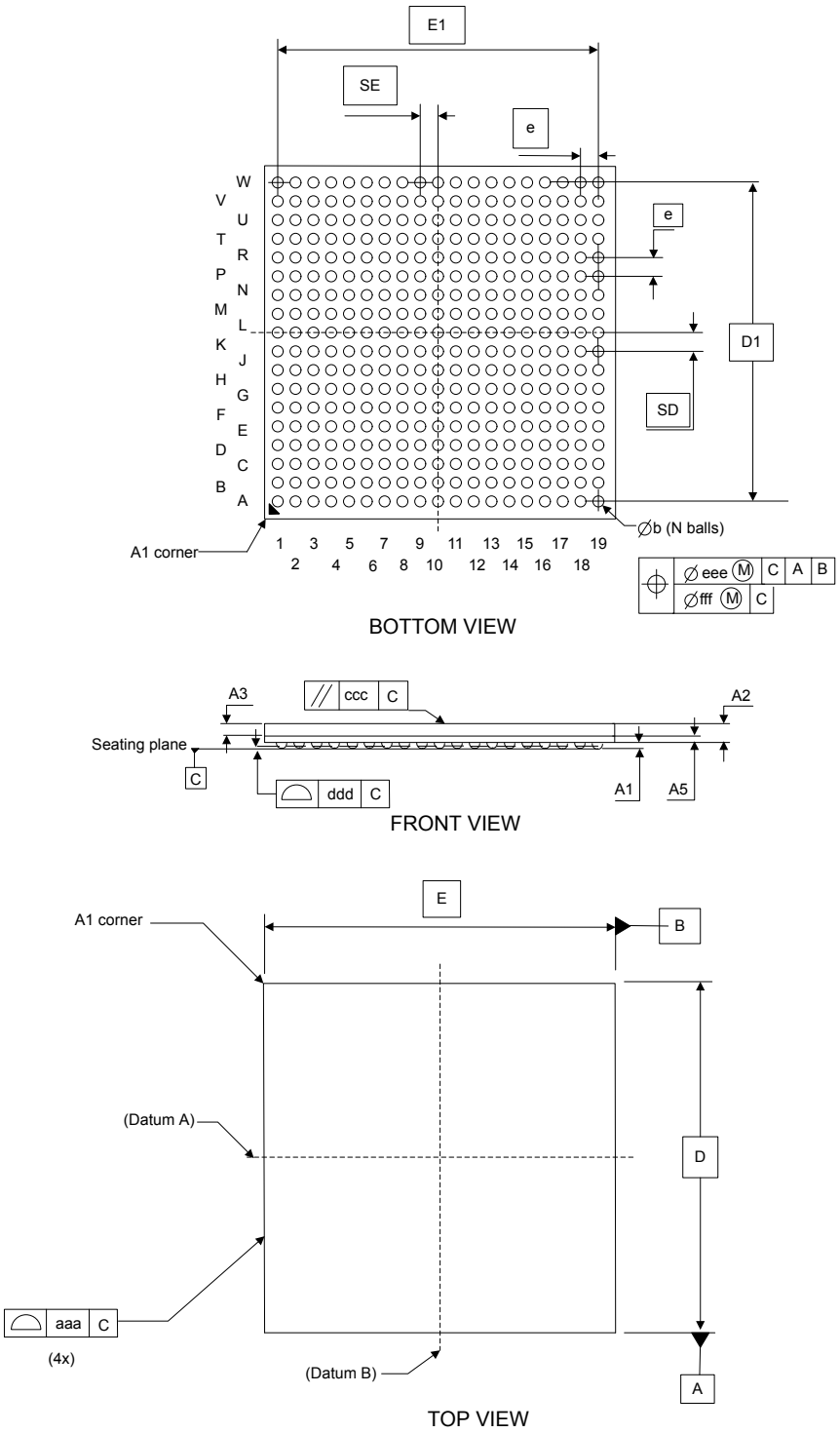

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Table 131. **VFBGA361 - Mechanical data**

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	1.00	-	-	0.0394
A1[3]	0.155	-	-	0.0061	-	-
b[4]	0.260	0.310	0.360	0.0102	0.0122	0.0142
D[5]	10.00 BSC			0.3937 BSC		
D1	9.000 BSC			0.3543 BSC		
E	10.00 BSC			0.3937 BSC		
E1	9.000 BSC			0.3543 BSC		
e[6]	0.500 BSC			0.0197 BSC		
N[7]	361					
SD[8]	0.500			0.0197		
SE[8]	0.500			0.0197		
aaa[9]	0.150			0.0059		
ccc[9]	0.200			0.0079		
ddd[9]	0.080			0.0031		
eee[9]	0.150			0.0059		
fff[9]	0.050			0.0020		

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*
2. *The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane*
3. *A1 is defined as the distance from the seating plane to the lowest point on the package body.*
4. *Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.*
5. *BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table*
6. *e(x) represents the solder ball grid pitch(es).*
7. *N represents the total number of balls on the BGA.*
8. *Basic dimensions SD(x) & SE(y) are defined with respect to datums A and B. They define the position of the centre ball(s) of the ball matrix.*
9. *Tolerance of form and position drawing.*

7.2 VFBGA424 package information (B0MP)

This VFBGA is a 424-ball, 14 x 14 mm, very thin fine pitch ball grid array package.

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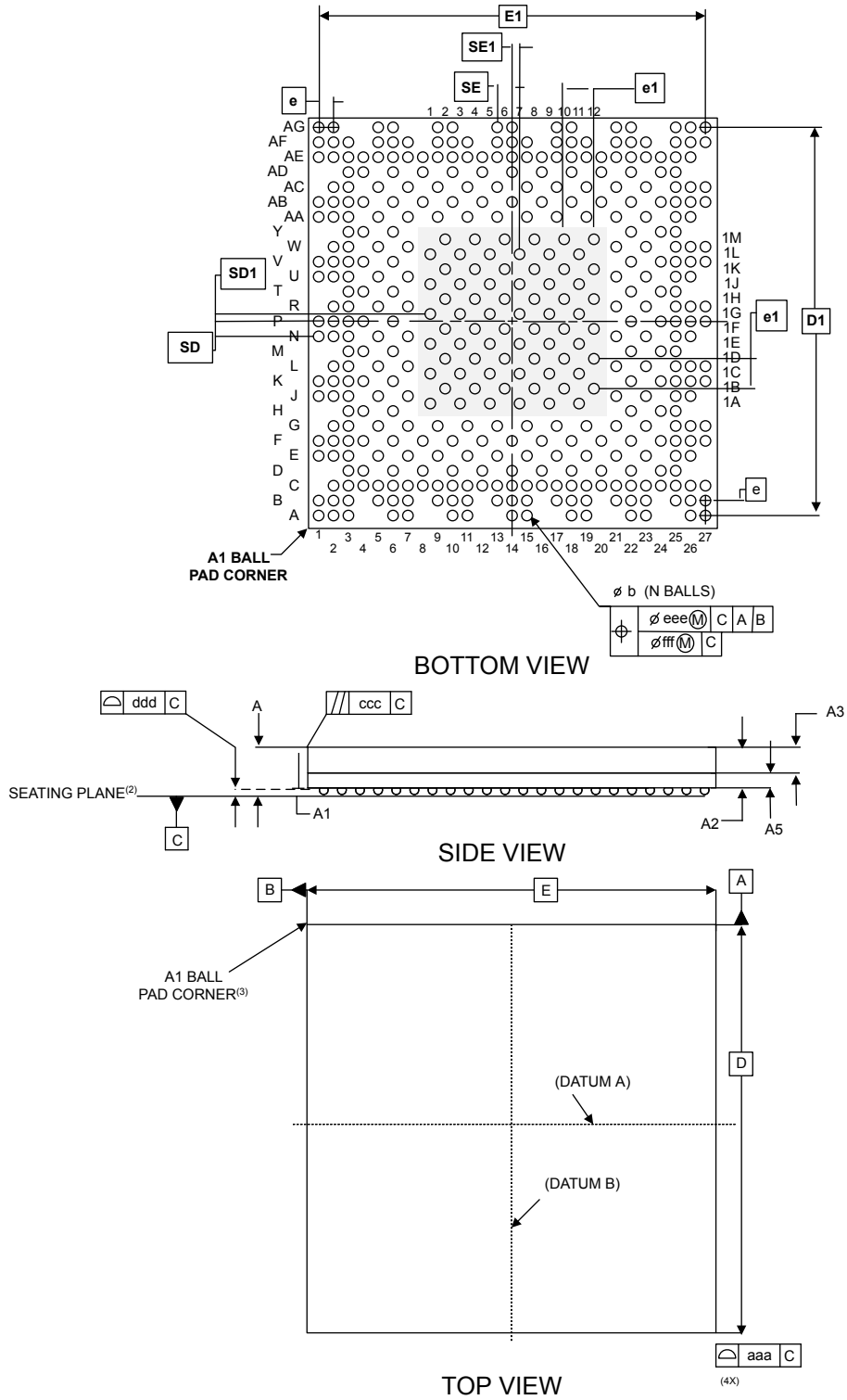
Figure 66. **VFBGA424 - Outline**



1. *Drawing is not to scale.*
2. *Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.*

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3. *The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.*

Table 132. VFBGA424 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	1.000	-	-	0.0394
A1[3]	0.155	-	-	0.0061	-	-
b[4]	0.260	0.310	0.360	0.0102	0.0122	0.0142
D[5]	14.000 BSC			0.5512 BSC		
D1[5]	13.000 BSC			0.5118 BSC		
E[5]	14.000 BSC			0.5512 BSC		
E1[5]	13.000 BSC			0.5118 BSC		
e[5][6]	0.500 BSC			0.0197 BSC		
e1[5][6]	1.000 BSC			0.0394 BSC		
N[7]	424					
SD[5][8]	0.500 BSC			0.0197 BSC		
SE[5][8]	0.500 BSC			0.0197 BSC		
SD1[5][8]	0.250 BSC			0.0098 BSC		
SE1[5][8]	0.250 BSC			0.0098 BSC		
aaa[9]	0.150			0.0059		
ccc[9]	0.200			0.0079		
ddd[9]	0.100			0.0031		
eee[9]	0.150			0.0059		
fff[9]	0.050			0.0020		

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*
2. *The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane*
3. *A1 is defined as the distance from the seating plane to the lowest point on the package body.*
4. *Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.*
5. *BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table*
6. *e(x) represents the solder ball grid pitch(es).*
7. *N represents the total number of balls on the BGA.*
8. *Basic dimensions SD(x) & SE(y) are defined with respect to datums A and B. They define the position of the centre ball(s) of the ball matrix.*
9. *Tolerance of form and position drawing.*

7.3 TFBGA436 package information (B0MS)

This TFBGA is a 436-ball, 18 x 18 mm, thin fine pitch ball grid array package.

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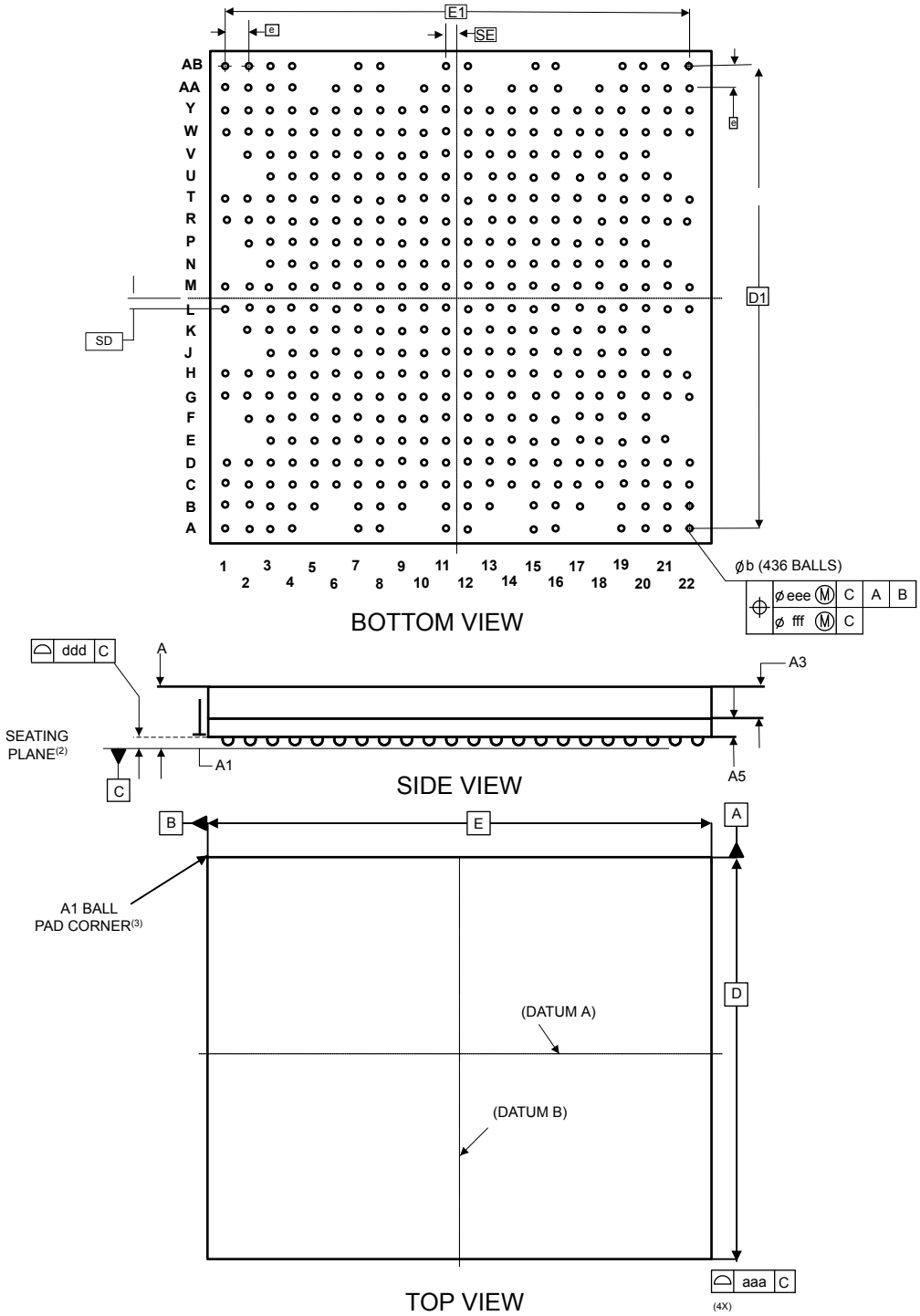
Figure 67. TFBGA436 - Outline



1. *Drawing is not to scale.*
2. *Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.*
3. *The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.*

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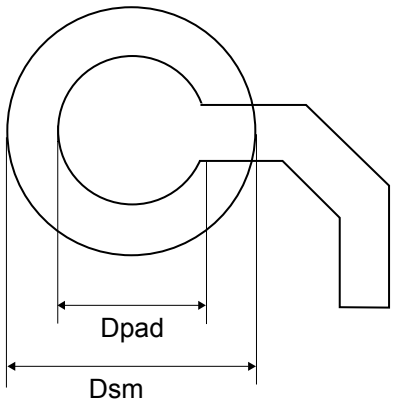
Table 133. TFBGA436 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	1.20	-	-	0.0472
A1[3]	0.240	-	-	0.0094	-	-
b[4]	0.380	0.430	0.480	0.0150	0.0169	0.0189
D[5]	18.000 BSC			0.7087 BSC		
D1[5]	16.800 BSC			0.6614 BSC		
E[5]	18.000 BSC			0.7087 BSC		
E1[5]	16.800 BSC			0.6614 BSC		
e[5][6]	0.800 BSC			0.0315 BSC		
N[7]	436					
SD[5][8]	0.400 BSC			0.0157 BSC		
SE[5][8]	0.400 BSC			0.0157 BSC		
aaa[9]	0.150			0.0059		
ccc[9]	0.200			0.0079		
ddd[9]	0.150			0.0059		
eee[9]	0.150			0.0059		
fff[9]	0.080			0.0031		

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*
2. *The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane*
3. *A1 is defined as the distance from the seating plane to the lowest point on the package body.*
4. *Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.*
5. *BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table*
6. *e(x) represents the solder ball grid pitch(es).*
7. *N represents the total number of balls on the BGA.*
8. *Basic dimensions SD(x) & SE(y) are defined with respect to datums A and B. They define the position of the centre ball(s) of the ball matrix.*
9. *Tolerance of form and position drawing.*

Figure 68. TFBGA436 - Footprint example



DT_BGA_WLCSP_FT_V1

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Table 134. **TFBGA436 - Example of PCB design rules**

Dimension	Values
Pitch	0.8 mm
Dpad	0.320 mm
Dsm	0.420 mm typ. (depends on soldermask registration tolerance)
Stencil opening	0.320 mm
Stencil thickness	0.125 to 0.100 mm

7.4 Device marking

Refer to technical note "Reference device marking schematics for STM32 microcontrollers and microprocessors" (TN1433) available on www.st.com, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as "ES", "E" or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use.

In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

7.5 Package thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, can be calculated using the following equation:

$$T_J \max = T_A \max + \left(P_D \max \times \Theta_{JA}\right)$$

where:

- T_A max is the maximum ambient temperature in °C.
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W.
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max:

$$P_D \max = P_{INT} \max + P_{I/O} \max)$$

- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins:

$$P_{I/O} \max = \sum\left(V_{OL} \times I_{OL}\right) + \sum\left(\left(V_{DDIOx} - V_{OH}\right)\right) \times I_{OH}$$

taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 135. **Package thermal characteristics**

Symbol	Parameter	Package	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient	VFBGA361 10×10 mm	TBD	°C/W
		VFBGA424 14×14 mm	TBD	
		TFBGA436 18×18 mm	TBD	
Θ_{JB}	Thermal resistance junction-board	VFBGA361 10×10 mm	TBD	
		VFBGA424 14×14 mm	TBD	
		TFBGA436 18×18 mm	TBD	
Θ_{JC}	Thermal resistance junction-top case	VFBGA361 10×10 mm	TBD	
		VFBGA424 14×14 mm	TBD	
		TFBGA436 18×18 mm	TBD	

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7.5.1 Reference documents

- JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air) available on www.jedec.org.
- For information on thermal management, refer to application note *"Guidelines for thermal management on STM32 applications" (AN5036)* available on www.st.com.

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8 Ordering information

Example: STM32 MP 257 F AI 3 ␣ T

Device family

STM32 = Arm® -based 32- or 64-bit processor

Product type

MP = MPU product

Device subfamily

251 = STM32MP251 line

253 = STM32MP253 line

255 = STM32MP255 line

257 = STM32MP257 line

Security option

C = Secure boot, cryptography hardware, 1.2 GHz CPU1, 800 MHz GPU[1]

F = Secure boot, cryptography hardware, 1.5 GHz CPU1, 900 MHz GPU[1]

Package and ball count

AL = VFBGA361 10x10, 361 balls pitch 0.5 mm

AK = VFBGA424 14x14, 424 balls pitch 0.5 mm

AI = TFBGA436 18x18, 436 balls pitch 0.8 mm

Junction temperature range

3 = -40 °C < T_J < +125 °C

Options

␣ (absent) = no options

Packing

T = Tape and reel

No character = tray or tube

1. *GPU is absent in some devices (see Section 2 for details).*

Note: For a list of available options (such as speed and package) or for further information on any aspect of this device, contact your nearest ST sales office.

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Revision history

Table 136. **Document revision history**

Date	Revision	Changes
19-Mar-2024	1	Initial release.

Prerelease product(s)

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Contents

1 Introduction 5
2 Description 6
3 Functional overview 13
3.1 Dual-core Arm Cortex-A35 subsystem (CA35SS) 13
3.1.1 Features 13
3.1.2 Overview 13
3.2 Arm Cortex-M33 core with TrustZone and FPU (CM33) 14
3.3 Arm Cortex-M0+ core (CM0P) 14
3.4 Graphic processing unit (GPU) 15
3.5 Neural processor unit (NPU) 15
3.6 Memories 15
3.6.1 External SDRAM 15
3.6.2 Embedded SRAM 16
3.7 DDR3L/DDR4/LPDDR4 controller (DDRCTRL) 16
3.8 Boot modes 16
3.9 Power supply management (PWR) 19
3.9.1 Power supply scheme 19
3.9.2 Power-supply supervisor 20
3.10 Low-power strategy 21
3.11 Resource isolation framework (RIF) 21
3.12 Reset and clock controller (RCC) 21
3.12.1 Features 22
3.12.2 Clock management 22
3.12.3 Reset sources 22
3.13 Hardware semaphore (HSEM) 23
3.14 Inter-processor communication controller (IPCC1/2) 23
3.14.1 Main features 23
3.15 General-purpose input/outputs (GPIO) 24
3.16 Bus-interconnect matrix 24
3.17 High-performance DMA controllers (HPDMA1/2/3) 27
3.18 Low-power DMA controller (LPDMA1) 28
3.19 Cortex-M33 nested vectored interrupt controller (NVIC) 28
3.20 Cortex-M0+ nested vectored interrupt controller (NVIC) 28
3.21 Extended interrupt and event controller (EXTI1/2) 28
3.22 Cyclic redundancy check calculation unit (CRC) 29

Prerelease product(s)

Downloaded from Arrow.com.

3.23 Flexible memory controller (FMC) . . . 29
3.24 Octo-SPI memory interface (OCTOSPI1/2) . . . 29
3.25 On-the-fly decoder (OTFDEC1/2) . . . 29
3.26 Octo-SPI I/O manager (OCTOSPIM) . . . 29
3.27 Analog-to-digital converters (ADC1/2/3) . . . 30
3.28 Digital temperature sensor (DTS) . . . 30
3.29 V_{BAT} operation . . . 30
3.30 Voltage reference buffer (VREFBUF) . . . 30
3.31 Multifunction digital filter (MDF1) . . . 30
3.31.1 Features . . . 31
3.32 Audio digital filter (ADF1) . . . 31
3.32.1 Features . . . 31
3.33 Digital camera interface (DCMI) . . . 32
3.34 Parallel synchronous slave interface (PSSI) . . . 32
3.35 Digital camera interface with pixel processing (DCMIPP) . . . 32
3.36 Camera serial interface (CSI) . . . 33
3.37 LCD-TFT display controller (LTDC) . . . 33
3.38 Display serial interface (DSI) . . . 34
3.39 LVDS display interface (LVDS) . . . 34
3.40 Video encoder (VENC) . . . 35
3.41 Video decoder (VDEC) . . . 35
3.42 True random number generator (RNG) . . . 35
3.43 Hash processor (HASH) . . . 35
3.44 Cryptographic processor (CRYP1/2) . . . 36
3.45 Secure AES (SAES) . . . 36
3.46 Public key accelerator (PKA) . . . 36
3.47 Boot and security and OTP control (BSEC) . . . 36
3.48 Timers and watchdogs . . . 36
3.48.1 Advanced-control timers (TIM1/8/20) . . . 37
3.48.2 General-purpose timers (TIM2/3/4/5/10/11/12/13/14/15/16/17) . . . 38
3.48.3 Basic timers (TIM6/TIM7) . . . 38
3.48.4 Low-power timer (LPTIM1/2/3/4/5) . . . 38
3.48.5 Independent watchdog (IWDG1/2/3/4/5) . . . 38
3.48.6 System window watchdog (WWDG1/2) . . . 38
3.48.7 SysTick timer . . . 38
3.48.8 Cortex-A35 generic timers (CNT) . . . 39

Prerelease product(s)

Downloaded from Arrow.com.

3.49 System timer generation (STGEN) . . . 39
3.50 Real-time clock (RTC) . . . 39
3.51 Tamper and backup registers (TAMP) . . . 40
3.52 Inter-integrated circuit interface (I2C1/2/3/4/5/6/7/8) . . . 40
3.53 Improved inter-integrated circuit (I3C1/2/3/4) . . . 40
3.54 Universal synchronous asynchronous receiver transmitter (USART1/2/3/6, UART4/5/7/8/9) . . . 42
3.55 Low-power universal asynchronous receiver transmitter (LPUART1) . . . 42
3.56 Serial peripheral interface (SPI1/2/3/4/5/6/7/8) inter-integrated sound interfaces (I2S1/2/3) . . . 43
3.57 Serial audio interfaces (SAI1/2/3/4) . . . 43
3.58 SPDIF receiver interface (SPDIFRX) . . . 43
3.59 Secure digital input/output MultiMediaCard interface (SDMMC1/2/3) . . . 44
3.60 Controller area network (FDCAN1/2/3). . . . 44
3.61 Universal serial bus Hi-Speed host (USBH). . . . 44
3.62 USB Type-C Power Delivery controller (UCPD1) . . . 44
3.63 Universal serial bus 3.0 dual role data (USB3DR) . . . 45
3.64 PCI Express interface (PCIE) . . . 45
3.65 5-Gbit/s PHY controller (COMBOPHY). . . . 46
3.66 Gigabit Ethernet MAC interface (ETH1/2) . . . 46
3.67 Gigabit Ethernet switch (ETHSW). . . . 47
3.68 Debug infrastructure . . . 47
4 Pinouts/ballouts, pin description, and alternate functions . . . 48
4.1 Ballout schematics . . . 48
4.2 Ball description . . . 52
4.3 Alternate functions . . . 79
5 Memory mapping . . . 96
6 Electrical characteristics . . . 97
6.1 Parameter conditions . . . 97
6.1.1 Minimum and maximum values . . . 97
6.1.2 Typical values . . . 97
6.1.3 Typical curves . . . 97
6.1.4 Loading capacitor . . . 97
6.1.5 Pin input voltage . . . 97
6.1.6 Power supply scheme . . . 98
6.1.7 Current consumption measurement . . . 99
6.2 Absolute maximum ratings . . . 99

Prerelease product(s)

Downloaded from Arrow.com.

6.3 Operating conditions . . . 101
6.3.1 General operating conditions . . . 101
6.3.2 Operating conditions at power-up / power-down . . . 103
6.3.3 Embedded reset and power control block characteristics . . . 103
6.3.4 Embedded reference voltage . . . 104
6.3.5 Supply current characteristics . . . 105
6.3.6 Wakeup time from low-power modes . . . 133
6.3.7 External clock source characteristics . . . 136
6.3.8 External clock source security characteristics . . . 141
6.3.9 Internal clock source characteristics . . . 141
6.3.10 PLL characteristics . . . 142
6.3.11 PLL spread spectrum clock generation (SSCG) characteristics . . . 144
6.3.12 Memory characteristics . . . 144
6.3.13 EMC characteristics . . . 144
6.3.14 Absolute maximum ratings (electrical sensitivity) . . . 146
6.3.15 I/O current injection characteristics . . . 146
6.3.16 I/O port characteristics . . . 147
6.3.17 NRST pin characteristics . . . 153
6.3.18 DDR IOs characteristics . . . 154
6.3.19 FMC characteristics . . . 154
6.3.20 OCTOSPI interface characteristics . . . 166
6.3.21 Delay block (DLYB) characteristics . . . 170
6.3.22 12-bit ADC characteristics . . . 171
6.3.23 Voltage reference buffer (VREFBUF) characteristics . . . 174
6.3.24 Digital Temperature Sensor (DTS) characteristics . . . 175
6.3.25 V_{BAT}, V_{DDCPU}, V_{DDCORE}, V_{DDGPU} ADC measurement characteristics . . . 175
6.3.26 Temperature and V_{BAT} monitoring characteristic for tamper detection . . . 176
6.3.27 Voltage monitoring characteristics . . . 176
6.3.28 Compensation cell characteristics . . . 178
6.3.29 Multi-function digital filter (MDF) characteristics . . . 178
6.3.30 Audio digital filter (ADF) characteristics . . . 179
6.3.31 Camera interface (DCMI) characteristics . . . 180
6.3.32 Camera interface (DCMIPP) characteristics . . . 180
6.3.33 Parallel interface (PSSI) characteristics . . . 181
6.3.34 LCD-TFT controller (LTDC) characteristics . . . 183
6.3.35 Timer characteristics . . . 185
6.3.36 Communications interfaces . . . 186
6.3.37 Embedded PHYs characteristics . . . 198

Prerelease product(s)

Downloaded from Arrow.com.

6.3.38 JTAG/SWD interface characteristics 209
7 Package information 211
7.1 VFBGA361 package information (B09U) 211
7.2 VFBGA424 package information (B0MP) 213
7.3 TFBGA436 package information (B0MS) 215
7.4 Device marking 218
7.5 Package thermal characteristics 218
7.5.1 Reference documents 219
8 Ordering information 220
Important security notice 221
Revision history 222
List of tables 228
List of figures 231

Prerelease product(s)

Downloaded from Arrow.com.

List of tables

Table 1. STM32MP25xC/F features and peripheral counts . . . 7
Table 2. STM32MP25xC/F differences per product lines . . . 9
Table 3. STM32MP25xC/F differences per packages . . . 10
Table 4. Default interfaces . . . 16
Table 5. Boot sources . . . 17
Table 6. Minimum set of default pins used during boot ROM phase . . . 17
Table 7. Timer feature comparison . . . 37
Table 8. USART/UART features . . . 42
Table 9. I/O power domains . . . 51
Table 10. Legend/abbreviations used in the ballout table . . . 52
Table 11. STM32MP25xC/F ball definitions . . . 53
Table 12. Alternate functions AF0 to AF7 . . . 79
Table 13. Alternate functions AF8 to AF15 . . . 88
Table 14. Voltage characteristics . . . 100
Table 15. Current characteristics . . . 100
Table 16. Thermal characteristics . . . 100
Table 17. General operating conditions . . . 101
Table 18. Operating conditions at power-up / power-down . . . 103
Table 19. Embedded reset and power control block characteristics . . . 104
Table 20. Embedded reference voltage characteristics . . . 105
Table 21. Embedded reference voltage calibration value . . . 105
Table 22. Current consumption (I_{DDCORE}) in Run modes . . . 107
Table 23. Current consumption (I_{DDCPU}) in Run modes . . . 112
Table 24. Current consumption (I_{DDGPU}) in Run modes . . . 116
Table 25. Current consumption (I_{DD}) in Run modes . . . 117
Table 26. Current consumption (I_{DDA18}) in Run modes . . . 119
Table 27. Current consumption ($I_{DDA18AON}$) in Run modes . . . 120
Table 28. Current consumption (I_{BAT}) in Run modes . . . 121
Table 29. Current consumption in Stop modes . . . 122
Table 30. Current consumption in LPLV-Stop modes . . . 125
Table 31. Current consumption in Standby1 mode . . . 128
Table 32. Current consumption in Standby2 mode . . . 130
Table 33. Current consumption in VBAT1 mode . . . 131
Table 34. Current consumption in VBAT2 mode . . . 132
Table 35. D1 (CPU1) low-power mode wakeup timings . . . 134
Table 36. D2 (CPU2) low-power mode wakeup timings . . . 134
Table 37. D3 (CPU3) low-power mode wakeup timings . . . 135
Table 38. Wakeup time using USART/LPUART . . . 136
Table 39. High-speed external (HSE) user clock characteristics (digital bypass) . . . 136
Table 40. High-speed external (HSE) user clock characteristics (analog bypass) . . . 137
Table 41. Low-speed external (LSE) user clock characteristics (digital bypass) . . . 138
Table 42. Low-speed external (LSE) user clock characteristics (analog bypass) . . . 139
Table 43. High-speed external (HSE) oscillator characteristics . . . 139
Table 44. Low-speed external (LSE) oscillator characteristics . . . 140
Table 45. High-speed external user clock security system (HSE CSS) . . . 141
Table 46. Low-speed external user clock security system (LSE CSS) . . . 141
Table 47. HSI oscillator characteristics . . . 141
Table 48. MSI oscillator characteristics . . . 142
Table 49. LSI oscillator characteristics . . . 142
Table 50. PLL1 to PLL8 characteristics . . . 142
Table 51. PLL_USB characteristics . . . 143
Table 52. PLL_DSI characteristics . . . 143

Prerelease product(s)

Downloaded from Arrow.com.

Table 53. PLL_LVDS characteristics . . . 143
Table 54. PLL2 to PLL8 SSCG parameters constraints . . . 144
Table 55. OTP characteristics . . . 144
Table 56. EMS characteristics . . . 145
Table 57. EMI characteristics for f_{HSE} = 40 MHz and F_{PLL1} = 1200 MHz . . . 145
Table 58. EMI characteristics for f_{HSE} = 40 MHz and F_{PLL1} = 1500 MHz . . . 146
Table 59. ESD absolute maximum ratings . . . 146
Table 60. Electrical sensitivities . . . 146
Table 61. I/O current injection susceptibility . . . 147
Table 62. I/O static characteristics . . . 147
Table 63. Output voltage characteristics for all I/Os except those on V_{SW} . . . 149
Table 64. Output voltage characteristics for I/Os supplied by V_{SW} . . . 149
Table 65. Output timing characteristics (V_{DD} = 3.0 - 3.6 V or V_{DDIOx} = 2.7 - 3.6 V, VDDIOxVRSEL = 0) . . . 149
Table 66. Output timing characteristics (V_{DD}/V_{DDIOx} = 1.71 - 1.89 V, VDDIOxVRSEL = 1) . . . 150
Table 67. Output timing characteristics (V_{DD}/V_{DDIOx} = 1.71 - 1.89 V, VDDIOxVRSEL = 0 degraded mode) . . . 152
Table 68. GPIO advance config delay characteristics (WARNING: DUMMY DATA TBD) . . . 153
Table 69. NRST pin characteristics . . . 153
Table 70. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings . . . 154
Table 71. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings . . . 154
Table 72. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings . . . 155
Table 73. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings . . . 156
Table 74. Asynchronous multiplexed PSRAM/NOR read timings . . . 157
Table 75. Asynchronous multiplexed PSRAM/NOR read - NWAIT timings . . . 157
Table 76. Asynchronous multiplexed PSRAM/NOR write timings . . . 158
Table 77. Asynchronous multiplexed PSRAM/NOR write - NWAIT timings . . . 159
Table 78. Synchronous non-multiplexed NOR/PSRAM read timings . . . 160
Table 79. Synchronous non-multiplexed PSRAM write timings . . . 161
Table 80. Synchronous multiplexed NOR/PSRAM read timings . . . 162
Table 81. Synchronous multiplexed PSRAM write timings . . . 163
Table 82. NAND flash read timings . . . 165
Table 83. NAND flash write timings . . . 165
Table 84. OCTOSPI characteristics in SDR mode (WARNING: DUMMY DATA TBD) . . . 166
Table 85. OCTOSPI characteristics in DTR mode (without DQS) (WARNING: DUMMY DATA TBD) . . . 167
Table 86. OCTOSPI characteristics in DTR mode (with DQS or HyperBus) (WARNING: DUMMY DATA TBD) . . . 168
Table 87. DLYB characteristics . . . 170
Table 88. ADC characteristics . . . 171
Table 89. ADC accuracy . . . 171
Table 90. Minimum sampling time versus RAIN . . . 173
Table 91. VREFBUF characteristics . . . 174
Table 92. DTS characteristics . . . 175
Table 93. V_{BAT}, V_{DDCPU}, V_{DDCORE}, V_{DDGPU} ADC measurement characteristics . . . 175
Table 94. TEMP and V_{BAT} Monitoring characteristics . . . 176
Table 95. Voltage monitoring characteristics (V_{DDCORE}, V_{DDCPU}, V_{DDGPU}, PVD_IN, $V_{DDA18ADC}$, $V_{DDIO1/2/3/4}$, $V_{DD33USB}$, $V_{DD33UCPD}$) . . . 176
Table 96. Compensation cell characteristics . . . 178
Table 97. MDF characteristics (WARNING: DUMMY DATA TBD) . . . 178
Table 98. ADF characteristics (WARNING: DUMMY DATA TBD) . . . 179
Table 99. DCMI characteristics (WARNING: DUMMY DATA TBD) . . . 180
Table 100. DCMIPP characteristics . . . 181
Table 101. PSSI transmit characteristics (WARNING: DUMMY DATA TBD) . . . 181
Table 102. PSSI receive characteristics (WARNING: DUMMY DATA TBD) . . . 182
Table 103. LTDC characteristics . . . 183
Table 104. TIMx characteristics . . . 185
Table 105. LPTIMx characteristics . . . 185

Prerelease product(s)

Downloaded from Arrow.com.

Table 106. Minimum i2c_ker_ck frequency in all I2C modes (WARNING: DUMMY DATA TBD) . . . 186
Table 107. I2C analog filter characteristics . . . 186
Table 108. I3C specific timings . . . 187
Table 109. I3C pin characteristics . . . 187
Table 110. SPI characteristics . . . 187
Table 111. I2S characteristics (WARNING: DUMMY DATA TBD) . . . 189
Table 112. SAI characteristics (WARNING: DUMMY DATA TBD) . . . 191
Table 113. SDMMC GPIO OSPEEDR settings for timing measurements . . . 192
Table 114. SDMMC characteristics for SD-Card or SDIO usage . . . 192
Table 115. SDMMC characteristics for *e*•MMC usage . . . 193
Table 116. Ethernet MAC timings for MDIO/SMA (WARNING: DUMMY DATA TBD) . . . 195
Table 117. Ethernet MAC timings for RMII (WARNING: DUMMY DATA TBD) . . . 195
Table 118. Ethernet MAC timings for MII (WARNING: DUMMY DATA TBD) . . . 196
Table 119. Ethernet MAC timings for RGMII (WARNING: DUMMY DATA TBD) . . . 196
Table 120. USART characteristics (WARNING: DUMMY DATA TBD) . . . 197
Table 121. DDR PHY characteristics . . . 199
Table 122. DSI PHY characteristics . . . 202
Table 123. CSI PHY characteristics . . . 203
Table 124. LVDS PHY characteristics . . . 203
Table 125. USB high-speed PHY characteristics . . . 204
Table 126. COMBOPHY characteristics . . . 205
Table 127. PCIE REFCLKGEN characteristics . . . 207
Table 128. UCPDPHY characteristics . . . 208
Table 129. JTAG dynamic characteristics (WARNING: DUMMY DATA TBD) . . . 209
Table 130. SWD dynamic characteristics (WARNING: DUMMY DATA TBD) . . . 210
Table 131. VFBGA361 - Mechanical data . . . 213
Table 132. VFBGA424 - Mechanical data . . . 215
Table 133. TFBGA436 - Mechanical data . . . 217
Table 134. TFBGA436 - Example of PCB design rules . . . 218
Table 135. Package thermal characteristics . . . 218
Table 136. Document revision history . . . 222

Prerelease product(s)

Downloaded from Arrow.com.

List of figures

Figure 1. STM32MP25xC/F block diagram . . . 12
Figure 2. AXI STNoC multi-frequency network . . . 25
Figure 3. MCU multi-Layer AHB 400 MHz . . . 25
Figure 4. MCU multi-Layer AHB 200 MHz . . . 26
Figure 5. SmartRun multi-Layer AHB matrix . . . 27
Figure 6. STM32MP25xC/F VFBGA361 pinout . . . 48
Figure 7. STM32MP25xC/F VFBGA424 pinout . . . 49
Figure 8. STM32MP25xC/F TFBGA436 pinout . . . 50
Figure 9. Pin loading conditions . . . 97
Figure 10. Pin input voltage . . . 97
Figure 11. Power supply scheme . . . 98
Figure 12. Current consumption measurement scheme . . . 99
Figure 13. High-speed external clock source AC timing diagram (digital bypass) . . . 137
Figure 14. High-speed external clock source AC timing diagram (analog bypass) . . . 138
Figure 15. Low-speed external clock source AC timing diagram (digital bypass) . . . 138
Figure 16. Low-speed external clock source AC timing diagram (analog bypass) . . . 139
Figure 17. Typical application with a 40 MHz crystal . . . 140
Figure 18. Typical application with a 32.768 kHz crystal . . . 141
Figure 19. V_{IL}/V_{IH} for TT I/Os . . . 148
Figure 20. Recommended NRST pin protection . . . 153
Figure 21. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms . . . 155
Figure 22. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms . . . 156
Figure 23. Asynchronous multiplexed PSRAM/NOR read waveforms . . . 158
Figure 24. Asynchronous multiplexed PSRAM/NOR write waveforms . . . 159
Figure 25. Synchronous non-multiplexed NOR/PSRAM read timings . . . 161
Figure 26. Synchronous non-multiplexed PSRAM write timings . . . 162
Figure 27. Synchronous multiplexed NOR/PSRAM read timings . . . 163
Figure 28. Synchronous multiplexed PSRAM write timings . . . 164
Figure 29. NAND controller waveforms for read access . . . 165
Figure 30. NAND controller waveforms for write access . . . 166
Figure 31. OCTOSPI timing diagram - SDR mode . . . 167
Figure 32. OCTOSPI timing diagram - DTR mode . . . 168
Figure 33. OCTOSPI HyperBus clock . . . 169
Figure 34. OCTOSPI HyperBus read . . . 169
Figure 35. OCTOSPI HyperBus read with double latency . . . 170
Figure 36. OCTOSPI HyperBus write . . . 170
Figure 37. ADC accuracy characteristics . . . 172
Figure 38. Typical connection diagram using the ADC with TT pins featuring analog switch function . . . 174
Figure 39. MDF timing diagram . . . 179
Figure 40. ADF timing diagram . . . 180
Figure 41. DCMI timing diagram . . . 180
Figure 42. DCMIPP timing diagram . . . 181
Figure 43. PSSI transmit timing diagram . . . 182
Figure 44. PSSI receive timing diagram . . . 183
Figure 45. LCD-TFT horizontal timing diagram . . . 184
Figure 46. LCD-TFT vertical timing diagram . . . 185
Figure 47. SPI timing diagram - master mode . . . 188
Figure 48. SPI timing diagram - slave mode and CPHA = 0 . . . 188
Figure 49. SPI timing diagram - slave mode and CPHA = 1 . . . 189
Figure 50. I2S slave timing diagram (Philips protocol) . . . 190
Figure 51. I2S master timing diagram (Philips protocol) . . . 190
Figure 52. SAI master timing waveforms . . . 191
Figure 53. SAI slave timing waveforms . . . 192

Prerelease product(s)

Downloaded from Arrow.com.

Figure 54. SD high-speed mode . . . 194
Figure 55. SD default mode . . . 194
Figure 56. SDMMC DDR mode . . . 194
Figure 57. Ethernet MDIO/SMA timing diagram . . . 195
Figure 58. Ethernet RMII timing diagram . . . 196
Figure 59. Ethernet MII timing diagram . . . 196
Figure 60. Ethernet RGMII timing diagram . . . 197
Figure 61. USART timing diagram in master mode . . . 198
Figure 62. USART timing diagram in slave mode . . . 198
Figure 63. JTAG timing diagram . . . 210
Figure 64. SWD timing diagram . . . 210
Figure 65. VFBGA361 - Outline . . . 212
Figure 66. VFBGA424 - Outline . . . 214
Figure 67. TFBGA436 - Outline . . . 216
Figure 68. TFBGA436 - Footprint example . . . 217

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