Embedded Multi-Media Card

EMMC08G-W100-A06U

KINGSTON TECHNOLOGY COMPANY, INC.

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Embedded Multi-Media Card Specification (*e*•MMC™5.0)

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Embedded Multi-Media Card Specification (*e*•MMC™5.0)

1 Product Features

- Packaged managed NAND flash memory
- 153-ball JEDEC VFBGA
- Nominal operating voltage range:
  - VCCQ = 1.8 V/3.3 V
  - VCC = 3.3 V
- RoHS Compliant
- Compliant with e•MMC™ 5.0 JEDEC Standard Number JESD84-B50
- e•MMC™ Feature Support:
  - High-speed *e*•MMC™ protocol
  - Variable clock frequencies of 0-200MHz.
  - Eleven-wire interface (clock, 1 bit command, 8 bit data bus) and a hardware reset.
  - Supports three different data bus widths: 1 bit(default), 4 bits, 8 bits
  - Bus Modes:
    - Single data transfer rate: up to 52Mbyte/s (using 8 parallel data lines at 52 MHz)
    - Dual data rate mode (DDR-104) : up to 104Mbyte/s @ 52MHz
    - High speed, single data rate mode (HS-200) : up to 200MB/s @ 200MHz
  - Supports alternate boot operation mode to provide a simple boot sequence method
  - Supports SLEEP/AWAKE (CMD5).
  - Host initiated explicit sleep mode for power saving
  - Enhanced write protection with permanent and partial protection options
  - Multiple user data partition with enhanced attribute for increased reliability
  - Background operation & High Priority Interrupt (HPI)
  - Error free memory access
    - Cyclic Redundancy Code (CRC) for reliable command and data communication
    - Internal error correction code (ECC) for improved data storage integrity
    - Internal enhanced data management algorithm
    - Data protection for sudden power failure during program operations
  - Secure bad block erase commands
  - Enhanced write protection with permanent and partial protection options
  - Field firmware update(FFU)
  - Pre EOL information
  - Optimal Size
  - Production State Awareness
  - Power Off Notification for Sleep

2 Product Description

Kingston e•MMC™ products conforms to the JEDEC e•MMC™ 5.0 standard. These devices are an ideal universal storage solution for many commercial and industrial embedded applications, including smart phones, tablet PCs, PDAs, eBook readers, digital cameras, recorders, media players, electronic learning products, digital TVs and set-top boxes. In a single integrated packaged device, e•MMC™ combines MLC NAND flash memory with an onboard e•MMC™ controller, providing an industry standard interface to the host. The onboard e•MMC™ controller directly manages NAND flash media which relieves the host processor of tasks, including flash media error control, wear-leveling, page and block management and performance optimization. The industry standard interface to the host processor ensures compatibility across all future NAND flash generations throughout the product life cycle.

2.1 e•MMC™ Standard Specification

Kingston e•MMC™ devices are fully compliant with the JEDEC Standard Specification No. JESD84-B50. This datasheet provides technical specifications for Kingston's family of e•MMC™ devices. A brief description of some of the major features of this product family is also provided. Refer to the JEDEC e•MMC™ standard for specific information related to e•MMC™ device function and operation.

3 Product Specification

3.1 System Performance

Refer to Specifications.

3.2 Power Consumption

Refer to Specifications.

3.3 Device and Partition Capacity

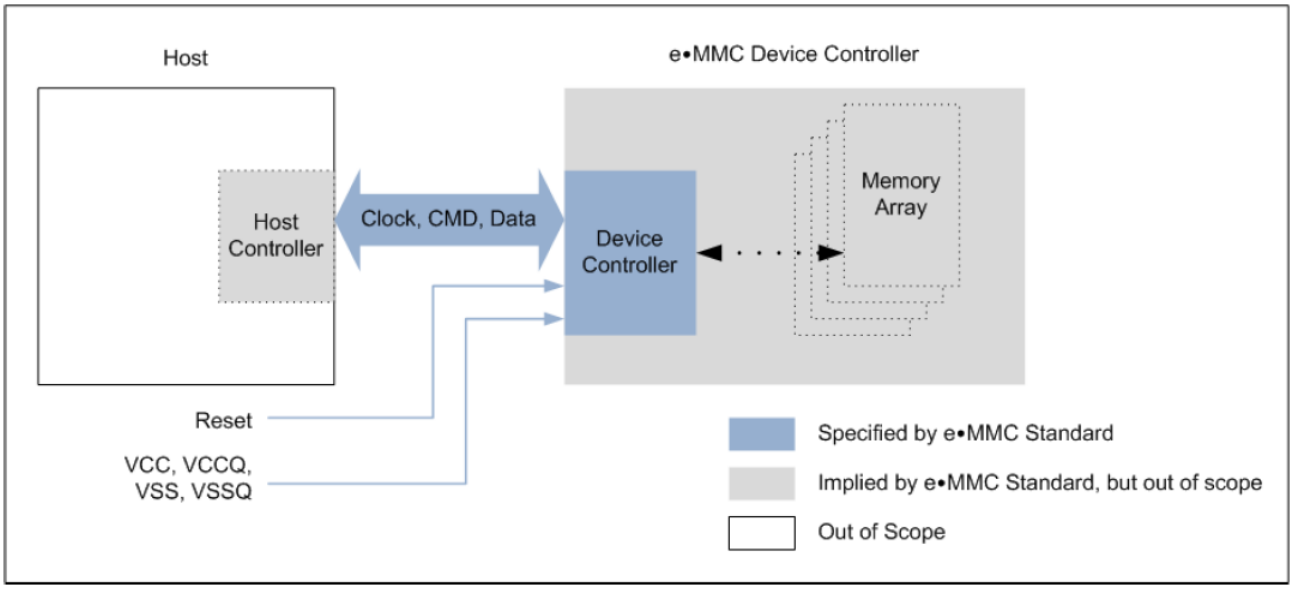
Total NAND flash capacity is divided across the 2 boot partitions, RPMB partition and the general purpose storage partition. A small portion of the NAND storage capacity is used for the storage of the onboard controller firmware and address mapping tables. Additionally, several NAND blocks are held in reserve to support replacement of failed blocks over the life of the e•MMC™ device. For actual device capacity, refer to Specifications.

4 e•MMC™ Device and System

4.1 e•MMC™ System Overview

The e•MMC™ specification covers the behavior of the interface and the Device controller. As part of this specification the existence of a host controller and a memory storage array are implied but the operation of these pieces is not fully specified.
The Kingston e•MMC™ device contains a single chip MMC controller and NAND flash memory module. The micro-controller interfaces with a host system allowing data to be written to and read from the NAND flash memory module. The controller relieves the host from the details of managing the NAND flash memory.

Figure 1: System Overview



4.2 Memory Addressing

Previous implementations of the e•MMC™ specification (versions up to v4.1) are following byte addressing with 32 bit field. This addressing mechanism permitted e•MMC™ densities up to and including 2 GB.

To support larger densities the addressing mechanism was updated to support sector addresses (512 B sectors). The sector addresses will be used for all devices with capacity larger than 2 GB.

To determine the addressing mode used, the host should read bit [30:29] in the OCR register.

4.3 e•MMC™ Signal Description

The e•MMC™ device transfers data via a configurable number of data bus signals. The communication signals are:

4.3.1 Clock (CLK)

Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.

4.3.2 Command (CMD)

This signal is a bidirectional command channel used for device initialization and transfer of commands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the e•MMC™ host controller to the e•MMC™ device and responses are sent from the device to the host.

4.3.3 Data Bus (DAT0-DAT7)

These are bidirectional data channels. The DAT signals operate in push-pull mode. These bidirectional signals are driven by either the e•MMC™ device or the host controller. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the e•MMC™ host controller. The e•MMC™ device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode, the device disconnects the internal pull-ups of lines DAT1–DAT7.

Table 1: Inputs/Outputs

Name	Type	Description
CLK	I	Clock
DAT0	I/O/PP	Data
DAT1	I/O/PP	Data
DAT2	I/O/PP	Data
DAT3	I/O/PP	Data
DAT4	I/O/PP	Data
DAT5	I/O/PP	Data
DAT6	I/O/PP	Data
DAT7	I/O/PP	Data
CMD	I/O/PP/OD	Command/Response
RST_n	I	Hardware Reset
Vcc	S	Supply voltage for core
Vccq	S	Supply voltage for I/O
Vss	S	Supply ground for core
Vssq	S	Supply ground for I/O
Note: I=Input; O=Ouput; PP=Push-Pull; OD=Open_Drain; NC=Not Connected(or logical high); S=Power Supply		

4.4 Bus Protocol

After a power-on reset, the host must initialize the device by a special message-based e•MMC™ bus protocol. For more details, refer to section 5.3.1 of the JEDEC Standard Specification No.JESD84-B50.

4.5 Bus Speed Modes

e•MMC™ defines several bus speed modes.

Table 2: Bus Speeds

Mode Name	Data Rate	I/O Voltage	Bus Width	Frequency	Max Data Transfer
Legacy	Single	3.3/1.8V	1, 4, 8	0-26MHz	26 MB/s
High Speed SDR	Single	3.3/1.8V	4, 8	0-52MHz	52 MB/s
High Speed DDR	Dual	3.3/1.8V	4, 8	0-52MHz	104 MB/s
HS200	Single	1.8V	4, 8	0-200MHz	200 MB/s

4.5.1 HS200 Bus Speed Mode

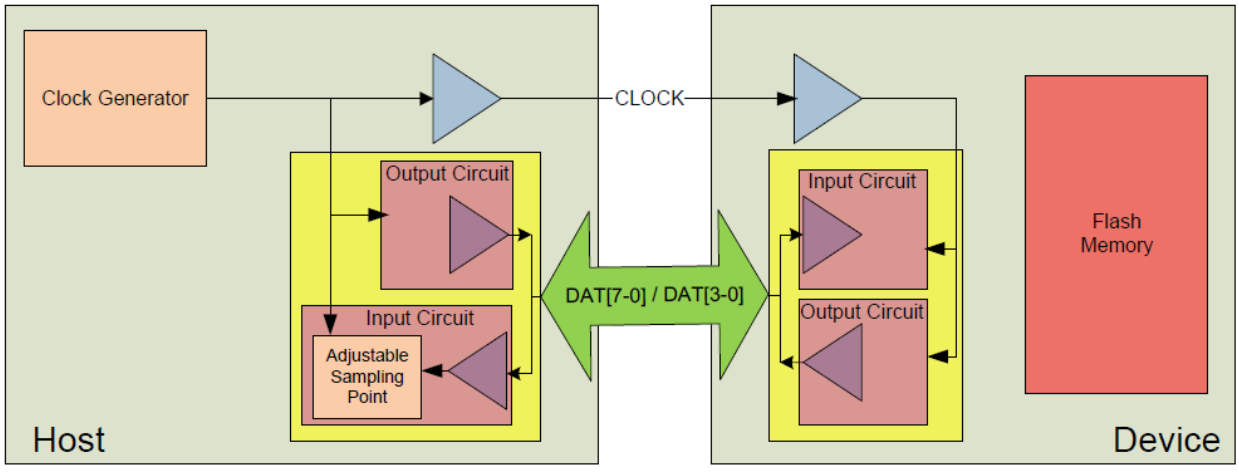
The HS200 mode offers the following features:

- SDR Data sampling method
- CLK frequency up to 200MHz Data rate – up to 200MB/s
- 8-bits bus width supported
- Single ended signaling with 4 selectable Drive Strength
- Signaling levels of 1.8V
- Tuning concept for Read Operations

4.5.2 HS200 System Block Diagram

Figure 2 shows a typical HS200 host and device system. The host has a clock generator, which supplies CLK to the device. For write operations, clock and data direction are the same, write data can be transferred synchronous with CLK, regardless of transmission line delay. For read operations, clock and data direction are opposite; the read data received by Host is delayed by round-trip delay, output delay and latency of host and device. For reads, the host needs to have an adjustable sampling point to reliably receive the incoming data. Refer to section 5.3.5 of the JEDEC Standard Specification No.JESD84-B50 for host read tuning.

Figure 2: HS200 Block Diagram



5 e•MMC™ Functional Description

5.1 e•MMC™ Overview

All communication between host and device are controlled by the host (master). The host sends a command, which results in a device response. For more details, refer to section 6.1 of the JEDEC Standard Specification No.JESD84-B50.

Five operation modes are defined for the e•MMC™ system (hosts and devices):

· Boot operation mode

· Device identification mode

· Interrupt mode

· Data transfer mode

· Inactive mode

5.2 Boot Operation Mode

In boot operation mode, the master (e•MMC™ host) can read boot data from the slave (e•MMC™ device) by keeping CMD line low or sending CMD0 with argument + 0xFFFFFFFA, before issuing CMD1. The data can be read from either boot area or user area depending on register setting. For more details, refer to section 6.3 of the JEDEC Standard Specification No.JESD84-B50.

5.3 Device Identification Mode

While in device identification mode the host resets the device , validates operation voltage range and access mode, identifies the device and assigns a Relative device Address (RCA) to the device on the bus. All data communication in the Device Identification Mode uses the command line (CMD) only. For more details, refer to section 6.4 of the JEDEC Standard Specification No.JESD84-B50.

5.4 Interrupt Mode

The interrupt mode on the e•MMC™ system enables the master (e•MMC™ host) to grant the transmission allowance to the slaves (device) simultaneously. This mode reduces the polling load for the host and hence, the power consumption of the system, while maintaining adequate responsiveness of the host to a device request for service. Supporting e•MMC™ interrupt mode is an option, both for the host and the device. For more details, refer to section 6.5 of the JEDEC Standard Specification No.JESD84-B50.

5.5 Data Transfer Mode

When the device is in Stand-by State, communication over the CMD and DAT lines will be performed in push-pull mode. For more details, refer to section 6.6 of the JEDEC Standard Specification No.JESD84-B50.

5.5.1 Data Read

The DAT0-DAT7 bus line levels are high when no data is transmitted. For more details, refer to section 6.6.10 of the JEDEC Standard Specification No.JESD84-B50.

5.5.2 Data Write

The data transfer format of write operation is similar to the data read. For more details, refer to section 6.6.11 of the JEDEC Standard Specification No.JESD84-B50.

5.5.3 Erase

In addition to the implicit erase executed by the device as part of the write operation, the e•MMC™ standard provides a host explicit erase function. For more details, refer to section 6.6.12 of the JEDEC Standard Specification No.JESD84-B50.

5.5.4 TRIM

The TRIM operation is similar to the default erase operation described (See section 6.6.12 of JESD84-B50). The TRIM function applies the erase operation to write blocks instead of erase groups. The TRIM function allows the host to identify data that is no longer required so that the device can erase the data if necessary during background erase events. For more details, refer to section 6.6.13 of the JEDEC Standard Specification No.JESD84-B50.

5.5.5 Sanitize

The Sanitize operation is a feature, in addition to TRIM and Erase that is used to remove data from the device. The use of the Sanitize operation requires the device to physically remove data from the unmapped user address space. For more details, refer to section 6.6.14 of the JEDEC Standard Specification No.JESD84-B50.

5.5.6 Discard

The Discard is similar in operation to TRIM. The Discard function allows the host to identify data that is no longer required so that the device can erase the data if necessary during background erase events. For more details, refer to section 6.6.15 of the JEDEC Standard Specification No.JESD84-B50.

5.5.7 Write Protect Management

In order to allow the host to protect data against erase or write, the e•MMC™ will support two levels of write protect commands. For more details, refer to section 6.6.18 of the JEDEC Standard Specification No.JESD84-B50.

5.5.8 Application-Specific Commands

The e•MMC™ system is designed to provide a standard interface for a variety of applications types. In this environment, it is anticipated that there will be a need for specific customers/applications features. For more details, refer to section 6.6.23 of the JEDEC Standard Specification No.JESD84-B50.

5.5.9 Sleep (CMD5)

A device may be switched between a Sleep state and a Standby state by SLEEP/AWAKE (CMD5). In the Sleep state the power consumption of the memory device is minimized. For more details, refer to section 6.6.24 of the JEDEC Standard Specification No.JESD84-B50.

5.5.10 Replay Protected Memory Block

A signed access to a Replay Protected Memory Block is provided. This function provides means for the system to store data to the specific memory area in an authenticated and replay protected manner. For more details, refer to section 6.6.25 of the JEDEC Standard Specification No.JESD84-B50.

5.5.11 Dual Data Rate Mode Selection

After the host verifies that the device complies with version 4.4, or higher, of this standard, and supports dual data rate mode, it may enable the dual data rate data transfer mode in the device. For more details, refer to section 6.6.26 of the JEDEC Standard Specification No.JESD84-B50.

5.5.12 Dual Data Rate Mode Operation

After the device has been enabled for dual data rate operating mode, the block length parameter of CMD17, CMD18, CMD24, CMD25 and CMD56 automatically default to 512 bytes and cannot be changed by CMD16 (SET_BLOCKLEN) command which becomes illegal in this mode. For more details, refer to section 6.6.27 of the JEDEC Standard Specification No.JESD84-B50.

5.5.13 Background Operations

Devices have various maintenance operations that need to be perform internally. In order to reduce latencies during time critical operations like read and write, it is better to execute maintenance operations at other times – when the host is not being serviced. For more details, refer to section 6.6.28 of the JEDEC Standard Specification No.JESD84-B50.

5.5.14 High Priority Interrupt (HPI)

In some scenarios, different types of data on the device may have different priorities for the host. For example, writing operation may be time consuming, so there might be a need to suppress the writing to allow demand paging requests in order to launch a process when requested by the user. For more details, refer to section 6.6.29 of the JEDEC Standard Specification No.JESD84-B50.

5.5.15 Context Management

To better differentiate between large sequential operations and small random operations, and to improve multitasking support, contexts can be associated with groups of read or write commands. Associating a group of commands with a single context allows the device to optimize handling of the data. For more details, refer to section 6.6.30 of the JEDEC Standard Specification No.JESD84-B50.

5.5.16 Data Tag Mechanism

The mechanism permits the device to receive from the host information about specific data types (for instance file system metadata, time-stamps, configuration parameters, etc.). The information is conveyed before a write multiple blocks operation at well-defined addresses. By receiving this information the device can improve the access rate during the following read and update operations and offer a more reliable and robust storage. For more details, refer to section 6.6.31 of the JEDEC Standard Specification No.JESD84-B50.

5.5.17 Packed Commands

Read and write commands can be packed in groups of commands (either all read or all write) that transfer the data for all commands in the group in one transfer on the bus, to reduce overheads. For more details, refer to section 6.6.32 of the JEDEC Standard Specification No.JESD84-B50.

5.5.18 Real Time Clock Information

Providing real time clock information to the device may be useful for internal maintenance operations. Host may provide either absolute time (based on UTC) if available, or relative time.

This feature provides a mechanism for the host to update both real time clock and relative time updates (see CMD49). For more details, refer to section 6.6.38 of the JEDEC Standard Specification No.JESD84-B50.

5.5.19 Power Off Notification

The host should notify the device before it powers the device off. This allows the device to better prepare itself for being powered off. For more details, refer to section 6.6.39 of the JEDEC Standard Specification No.JESD84-B50.

5.6 Inactive Mode

The device will enter inactive mode if either the device operating voltage range or access mode is not valid. The device can also enter inactive mode with GO_INACTIVE_STATE command (CMD15). The device will reset to Pre-idle state with power cycle. For more details, refer to section 6.1 of the JEDEC Standard Specification No.JESD84-B50.

5.7 Clock Control

The e•MMC™ bus clock signal can be used by the host to put the device into energy saving mode, or to control the data flow (to avoid under-run or over-run conditions) on the bus. The host is allowed to lower the clock frequency or shut it down. For more details, refer to section 6.7 of the JEDEC Standard Specification No.JESD84-B50.

5.8 Error Conditions

Refer to section 6.8 of the JEDEC Standard Specification No.JESD84-B50.

5.9 Minimum Performance

Refer to section 6.9 of the JEDEC Standard Specification No.JESD84-B50.

5.10 Commands

Refer to section 6.10 of the JEDEC Standard Specification No.JESD84-B50.

5.11 Device State Transition Table

Refer to section 6.11 of the JEDEC Standard Specification No.JESD84-B50.

5.12 Responses

Refer to section 6.12 of the JEDEC Standard Specification No.JESD84-B50.

5.13 Timings

Refer to section 6.15 of the JEDEC Standard Specification No.JESD84-B50.

5.14 H/W Reset Operation

Figure 3: Hardware Reset Operation

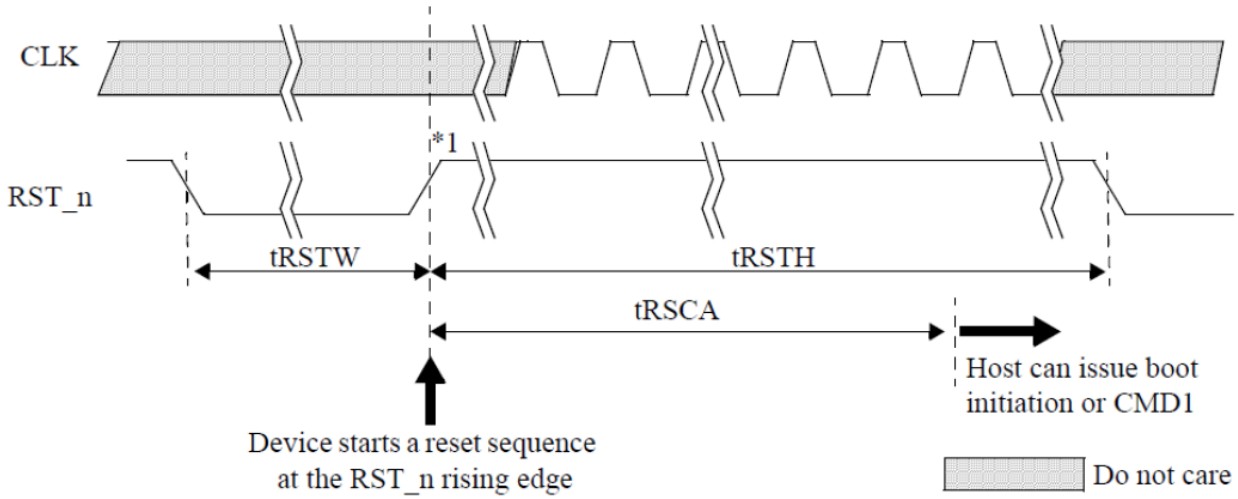


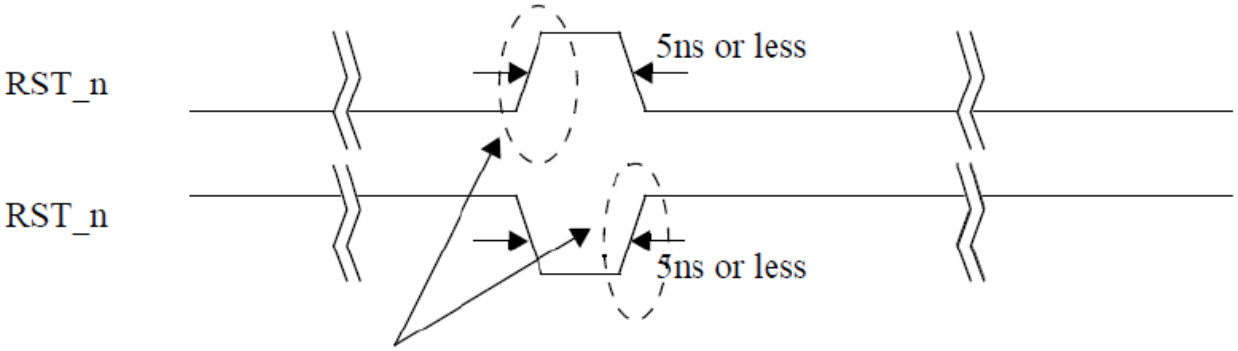
Table 3: Hardware Reset Timing

Symbol	Comment	Min	Max	Unit
tRSTW	RST_n pulse width	1		µs
tRSCA	RST_n to cmd time	200[1]		µs
tRSTH	RST_n high period	1		µs
Note[1]: 74 cycles of clock signal required before issuing CMD1 or CMD0 with argument 0xFFFFFFFA				

5.15 Noise Filtering Timing for H/W Reset

Device must filter out 5ns or less pulse width for noise immunity

Figure 4: Noise Filtering Timing



Device must not detect 5ns or less of positive or negative RST_n pulse. Device must detect more than or equal to 1us of positive or negative RST_n pulse width.

5.16 Field Firmware Update (FFU)

Field Firmware Update (FFU) enables feature enhancements in the field. Using this mechanism the host downloads a new version of the firmware to the e•MMC™ device and, following a successful download, instructs the e•MMC™ device to install the new downloaded firmware into the device.

In order to start the FFU process the host first checks if the e•MMC™ device supports FFU capabilities by reading SUPPPORTED_MODES and FW_CONFIG fields in the EXT_CSD. If the e•MMC™ device supports the FFU feature the host may start the FFU process. The FFU process starts by switching to FFU Mode in MODE_CONFIG field in the EXT_CSD. In FFU Mode, the host should use closed-ended or open ended commands for downloading the new firmware and reading vendor proprietary data. In this mode, the host should set the argument of these commands to be as defined in FFU_ARG field.

If these commands have a different argument the device behavior is not defined and the FFU process may fail. The host should set Block Length to be DATA_SECTOR_SIZE. Downloaded firmware bundle must be DATA_SECTOR_SIZE size aligned (internal padding of the bundle might be required). Once in FFU Mode, the host may send the new firmware bundle to the device using one or more write commands.

The host could regain regular functionality of write and read commands by setting MODE_CONFIG field in the EXT_CSD back to Normal state. Switching out of FFU Mode may abort the firmware download operation. When the host is switched back to FFU Mode, the host should check the FFU Status to get an indication about the number of sectors which were downloaded successfully by reading the NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED in the extended CSD. If the number of sectors which were downloaded successfully is zero the host should re-start downloading the new firmware bundle from its first sector. If the number of sectors which were downloaded successfully is positive the host should continue the download from the next sector, which would resume the firmware download operation.

If the MODE_OPERATION_CODES field is not supported by the device the host sets to NORMAL state and initiates a CMD0/HW_Reset/Power cycle to install the new firmware. In this case the device doesn't need to use NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED.
In both cases, if a CMD0/HW_Reset/Power Cycle occurred before the host successfully downloaded the new firmware bundle to the device, the firmware download process will be aborted.

5.17 Device Life time

5.17.1 DEVICE LIFE TIME SET TYPE B

This field provides an estimated indication of the device life time which is reflected by the average wear out of memory of Type B relative to its maximum estimated device life time

Table 4: Device Life Time Set TYPE B

Value	Description
0x00	Not Defined
0x01	0% - 10% Device Life Time Used
0x02	10% - 20% Device Life Time Used
0x03	20% - 30% Device Life Time Used
0x04	30% - 40% Device Life Time Used
0x05	40% - 50% Device Life Time Used
0x06	50% - 60% Device Life Time Used
0x07	60% - 70% Device Life Time Used
0x08	70% - 80% Device Life Time Used
0x09	80% - 90% Device Life Time Used
0x0A	90% - 100% Device Life Time Used
0x0B	Exceeded Maximum Device Life Time
Others	Reserved

5.17.2 DEVICE LIFE TIME SET TYPE A

This field provides an estimated indication of the device life time which is reflected by the average wear out of memory of Type A relative to its maximum estimated device life time

Table 5: Device Life Time Set TYPE A

Value	Description
0x00	Not Defined
0x01	0% - 10% Device Life Time Used
0x02	10% - 20% Device Life Time Used
0x03	20% - 30% Device Life Time Used
0x04	30% - 40% Device Life Time Used
0x05	40% - 50% Device Life Time Used
0x06	50% - 60% Device Life Time Used
0x07	60% - 70% Device Life Time Used
0x08	70% - 80% Device Life Time Used
0x09	80% - 90% Device Life Time Used
0x0A	90% - 100% Device Life Time Used
0x0B	Exceeded Maximum Device Life Time
Others	Reserved

5.18 Pre EOL Information

This field provides information about device life time reflected by average reserved blocks.

Table 6: Pre-EOL Information

Value	Pre-EOL Info.	Description
0x00	Not Defined	Not Defined
0x01	Normal	Normal
0x02	Warning	Consumed 80% of Reserved Blocks
0x03	Urgent	
0x04 – 0xFF	Reserved	

5.19 Optimal Size

5.19.1 OPTIMAL READ SIZE

This field provides the minimum optimal (for the device) read unit size for the different partitions.

Table 7: Optimal Read Size

Value	Optimal Read Size
0x00	Not Defined
0x01	4KB x 1 = 4KB
0x02	4KB x 2 = 8KB
…	
0xFF	4KB x 255 = 1020KB

5.19.2 OPTIMAL WRITE SIZE

This field provides the minimum optimal (for the device) write unit size for the different partitions. “Optimal” relates to the minimum wear out done by the device.

Table 8: Optimal Write Size

Value	Optimal Write Size
0x00	Not Defined
0x01	4KB x 1 = 4KB
0x02	4KB x 2 = 8KB
…	
0xFF	4KB x 255 = 1020KB

5.19.3 OPTIMAL TRIM UNIT SIZE

This field provides the minimum optimal (for the device) trim unit size for the different partitions. “Optimal” relates to the minimum wear out done by the device.

Table 9: Optimal Trim Unit Size

Value	Optimal Trim Unit Size
0x00	Not Defined
0x01	4KB x 1 = 4KB
0x02	4KB x 2 = 8KB
0x03	4KB x 4 = 16KB
0x15	4KB x 2^20 = 4GB

5.20 Production State Awareness

The e•MMC™ device can utilize this information to determine whether or not it is in a production environment, causing it to operate differently than it operates in the field.

For example, content loaded into the storage device prior to soldering has a higher probability for data corruption during device soldering. The e•MMC™ device could use “special” internal operations for loading content prior to device soldering which would reduce production failures and use “regular” operations post-soldering.

The PRODUCTION_STATE_AWARENESS [133] field in extended CSD is used as a mechanism for the host to notify the device whether it is in a pre or post soldering state.
This specification defines two methods: Manual Mode and Auto Mode, to manage the device production state.

Before loading any data, the PRE_LOADING_DATA_SIZE field must be set. The host is expected to make sure that the device is clean prior to setting this field. Any data previously written to the device is expected to be erased using CMD35, CMD36 and CMD38.

If the host erases data, over writes existing data or preformed re-partition while the device is in a pre-production state, the host should restart the production state awareness process by re-setting PRE_LOADING_DATA_SIZE.

5.20.1 Manual Mode

When using Manual Mode, the host explicitly sets the production state by changing the PRODUCTION_STATE_AWARENESS field to the PRE_SOLDERING_WRITES state prior to soldering and before the host loads content to the device. Once all content loading has been completed, the host should set the PRODUCTION_STATE_AWARENESS field to the PRE_SOLDERING_POST_WRITES state. In this state the host should not write content to the device until soldering is performed. Once soldered, the host should set the PRODUCTION_STATE_AWARENESS field to the Normal state. If the host writes to a device not in PRE_SOLDERING_WRITES state, the device may response with an error. PRODUCTION_STATE_AWARENESS state change may exceed the switch command timeout. The maximum timeout for PRODUCTION_STATE_AWARENESS state change is defined by the device manufacturer in INI_ PRODUCTION_STATE_AWARENESS_TIMEOUT [218].

5.21 Power off Notification for Sleep

The host should notify the device before it powers the device off. This allows the device to better prepare itself for being powered off. Power the device off means to turn off all its power supplies. In particular, the host should issue a power off notification (POWER_OFF_LONG, POWER_OFF_SHORT) if it intends to turn off both VCC and VCCQ. It may use a power off notification (SLEEP_NOTIFICATION) if it intends to turn-off VCC after moving the device to the Sleep state.

To indicate to the device that power off notification is supported by the host, the host shall first set the POWER_OFF_NOTIFICATION byte in EXT_CSD [34] to POWERED_ON (0x01). To execute a power off notification, before removing power to the device, the host will set either POWER_OFF_SHORT

(0x02) or POWER_OFF_LONG (0x03). The host should waits for the busy line to be de-asserted before removing power. Once the setting has changed to either 0x02 or 0x03, the host may safely power off the device.

The host may issue the SLEEP_AWAKE (CMD5) command to enter or to exit from the Sleep state if POWER_OFF_NOTIFICATION byte is set to POWERED_ON. Before moving to the Standby state and then to the Sleep state, the host will set POWER_OFF_NOTIFICATION to SLEEP_NOTIFICATION and waits for the DAT0 line to de-assert. While in the Sleep state, VCC (Memory supply) may be turned off as defined in section 4.1.6 of the JEDEC specification. Removing power supplies other than VCC while the device is in the Sleep state may result in undefined device behavior. Before removing all power supplies, the host should transition the device out of the Sleep state back to the Transfer state using CMD5 and CMD7 and then execute a power off notification by setting the POWER_OFF_NOTIFICATION byte to either POWER_OFF_SHORT or POWER_OFF_LONG.

If the host continues to send commands to the device after switching to the power off setting (POWER_OFF_LONG, POWER_OFF_SHORT or SLEEP_NOTIFICATION) or performs HPI during its busy condition, the device will restore the POWER_OFF_NOTIFICATION byte to POWERED_ON.
If the host tries to change POWER_OFF_NOTIFICATION to 0x00 after writing another value, a SWITCH_ERROR is generated.

The difference between the two power-off modes is how urgently the host wants to turn power off. The device should respond to POWER_OFF_SHORT quickly under the generic CMD6 timeout. If more time is acceptable, POWER_OFF_LONG may be used and the device will respond to it within the POWER_OFF_LONG_TIME timeout.

While POWER_OFF_NOTIFICATION is set to POWERED_ON, the host will:

- Keep the device power supplies alive (both Vcc and Vccq) and in their active mode
- Not power off the device intentionally before changing POWER_OFF_NOTIFICATION to either POWER_OFF_LONG or POWER_OFF_SHORT
- Not power off VCC intentionally before changing POWER_OFF_NOTIFICATION to SLEEP_NOTIFICATION and before moving the device to the Sleep state. Before moving to the Sleep state, the host may set the POWER_OFF_NOTIFICATION byte to SLEEP_NOTIFICATION (0x04) if aware that the device is capable of autonomously initiating background operations for possible performance improvements. The host should wait for the busy line (DAT0) to be de-asserted. The busy line may be asserted up to the time period defined in SLEEP_NOTIFICATION_TIME in EXT_CSD [216]. Once the setting has changed to 0x04, the host may set the device into the Sleep mode (CMD7+CMD5). After exiting from the Sleep mode the POWER_OFF_NOTIFICATION byte will restore its value to POWERED_ON. HPI may interrupt the SLEEP_NOTIFICATION operation. In that case the POWER_OFF_NOTIFICATION byte will restore to POWERED_ON.

6 Device Registers

The JEDEC e•MMC™ standard defines six device registers that contain specific device information and provide a means for e•MMC™ device configuration. These registers are: OCR, CID, CSD, EXT_CSD, RCA and DSR. Register access is performed using specific commands (see section 6.10 of JESD84-B50). The OCR, CID and CSD registers carry the device/content specific information, while the RCA and DSR registers are configuration registers storing actual configuration parameters. The EXT_CSD register carries both, device specific information and actual configuration parameters.

6.1 CID Register

The Card IDentification (CID) register is 128 bits wide. It contains the device identification information used during the identification phase (e•MMC™ protocol). For detailed register content, please refer to CID Registers.

6.2 CSD Register

The Card-Specific Data (CSD) register provides information on how to access the device contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed and whether the DSR register can be used. For detailed register content, please refer to CSD Registers.

6.3 Extended CSD Register

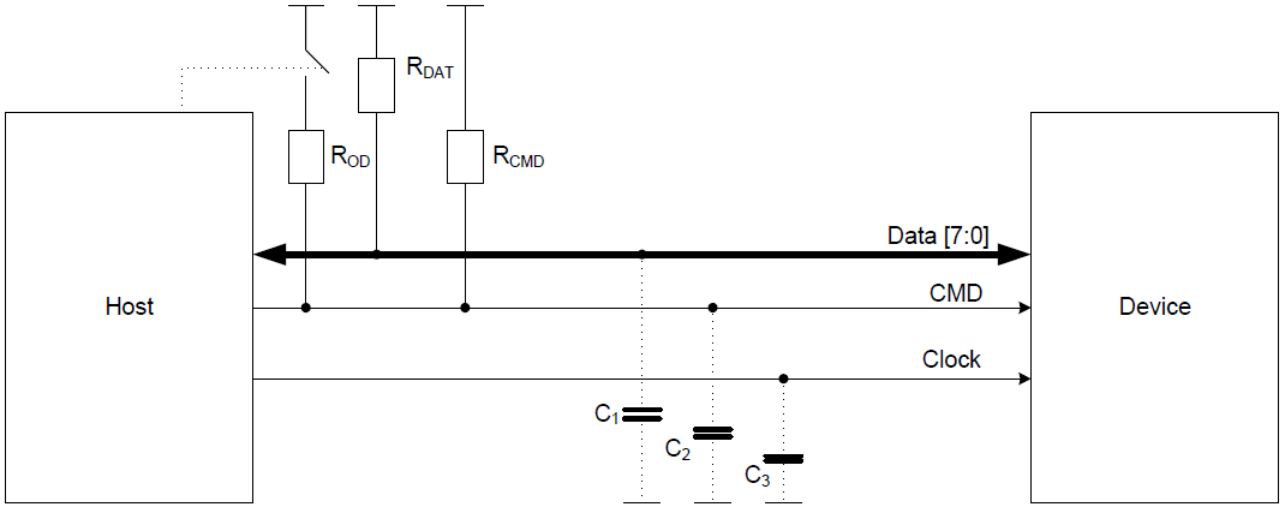
The 512 byte long Extended CSD register defines the device properties and selected modes. The most significant 320 bytes are refered to as the properties segment. This segment defines the device capabilities and cannot be modified by the host. The lower 192 bytes are the modes segment. This segment defines the current working configuration for the device. These modes can be changed by the host by means of the SWITCH command. For detailed register setting value, please refer to Extended CSD Registers.

7 The e•MMC™ Bus

The e•MMC™ bus has ten communication lines and three supply lines:

- CMD： Command is a bidirectional signal. The host and device drivers are operating in one of two modes, open drain and push/pull.
- DAT0-7： Data lines are bidirectional signals. The host and device drivers are operating in push-pull mode
- CLK： Clock is a host to device signal. CLK operates in push-pull mode

Figure 5: e•MMC™ Bus Lines



The R_{OD} is switched on and off by the host synchronously to the open-drain or push-pull mode transitions. The host is not required to have open drain drivers, but must recognize this mode to switch on the R_{OD}. R_{DAT} and R_{CMD} are pull-up resistors protecting the CMD and the DAT lines against bus floating when all device drivers are in a high-impedance mode.

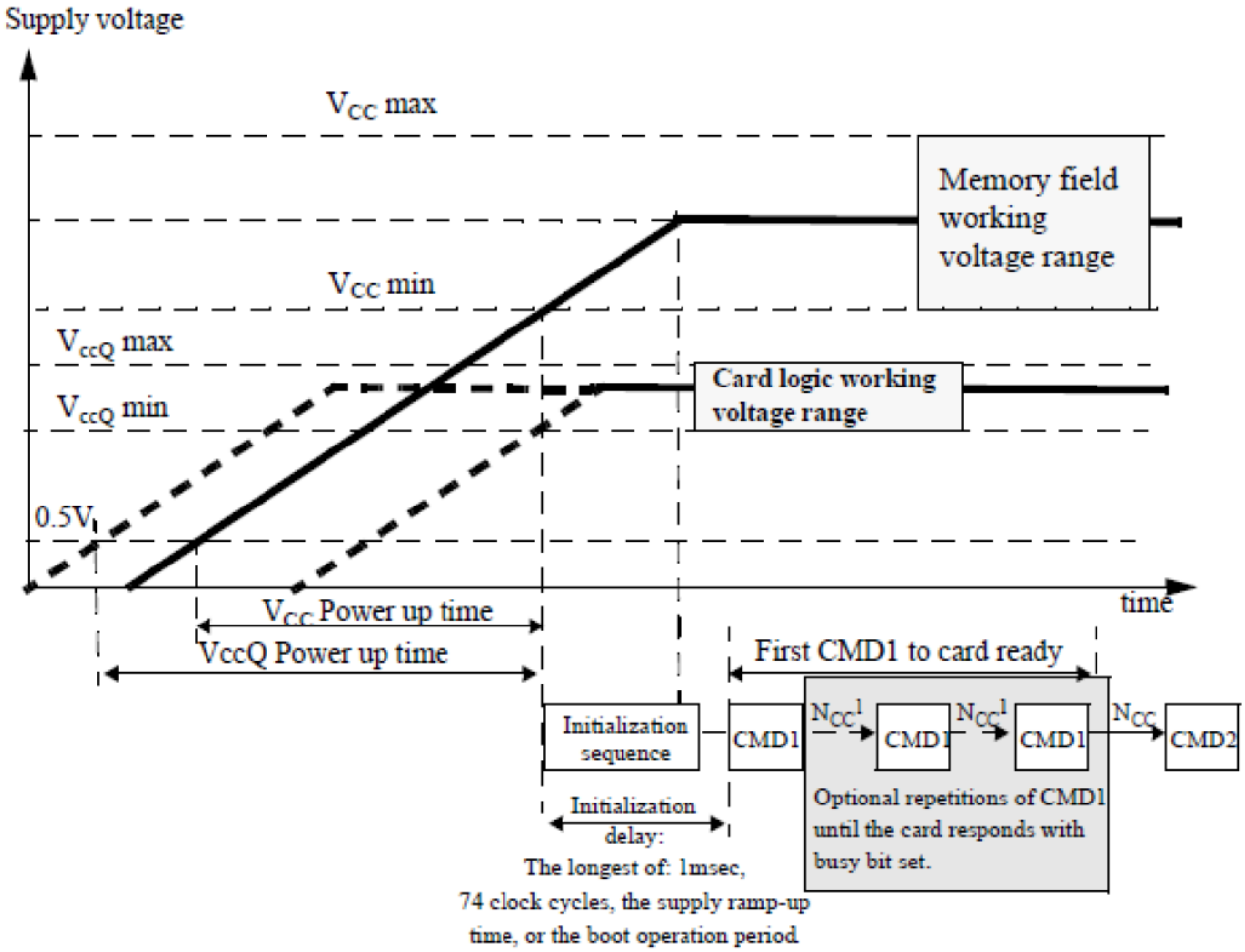
A constant current source can replace the R_{OD} by achieving a better performance (constant slopes for the signal rising and falling edges). If the host does not allow the switchable R_{OD} implementation, a fixed R_{CMD} can be used).

7.1 Power-up

7.1.1 e•MMC™ Power-up

An e•MMC™ bus power-up is handled locally in each device and in the bus master. Figure 6 shows the power-up sequence and is followed by specific instructions regarding the power-up sequence. Refer to section 10.1 of the JEDEC Standard Specification No.JESD84-B50 for specific instructions regarding the power-up sequence.

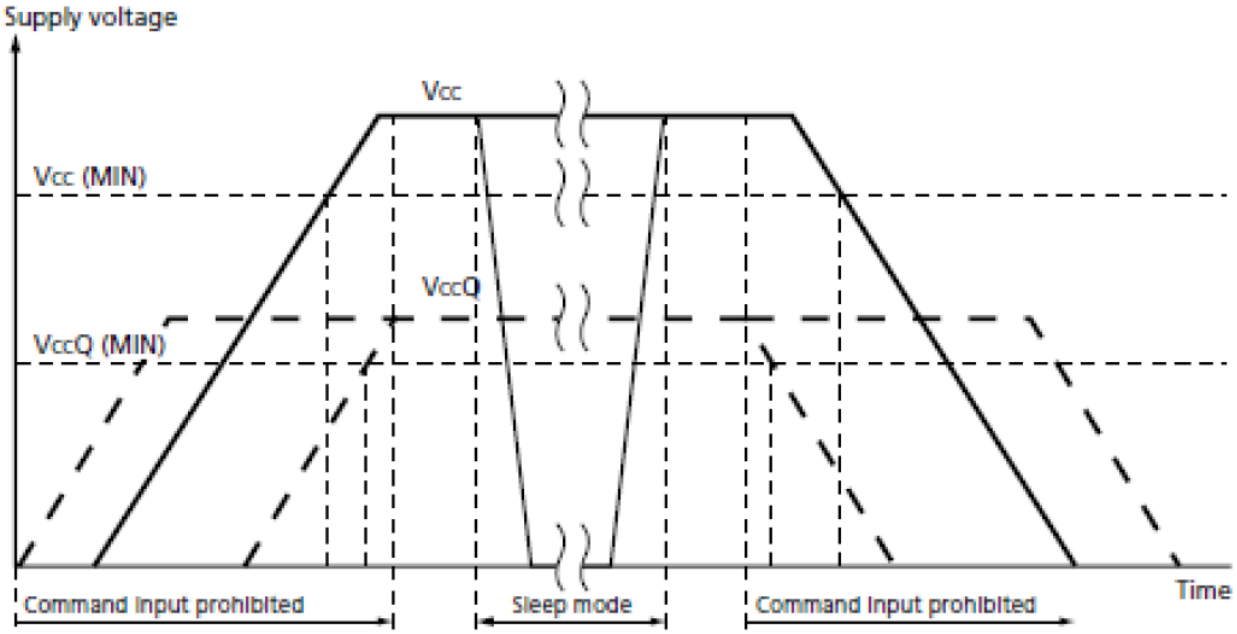
Figure 6: Power-Up



7.1.2 e•MMC™ Power Cycling

The host can execute any sequence of VCC and VCCQ power-up/power-down. However, the host must not issue any commands until VCC and VCCQ are stable within each operating voltage range. After the slave enters sleep mode, the host can power-down VCC to reduce power consumption. It is necessary for the slave to be ramped up to VCC before the host issues CMD5 (SLEEP_AWAKE) to wake the slave unit. For more information about power cycling see section 10.1.3 of the JEDEC Standard Specification No.JESD84-B50.

Figure 7: Power Cycling



7.2 Bus Operating Conditions

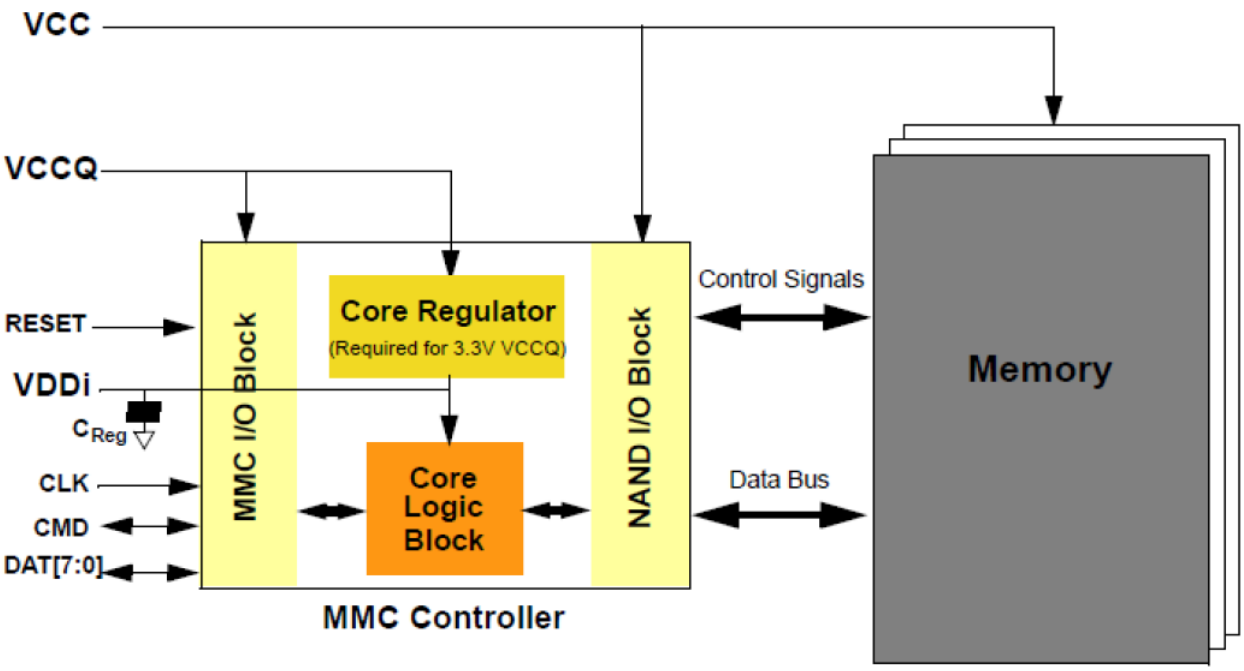
Table 10: Bus Operation Conditions

Parameter	Min	Max	Unit
Peak Voltage All Lines	-0.5	Vccq + 0.5	V
All Inputs **Input Leakage Current (before initialization and/or internal pull-up resistors)**	-100	100	µA
All Inputs **Input Leakage Current (after initialization and/or internal pull-up resistors)**	-2	2	µA
All Outputs **Output Leakage Current (before initialization)**	-100	100	µA
All Outputs **Output Leakage Current (after initialization)**	-2	2	µA

7.2.1 Power supply: e•MMC™

In the e•MMC™, VCC is used for the NAND flash device and its interface voltage; VCCQ is for the controller and the MMC interface voltage shown in Figure 8. The core regulator is optional and only required when internal core logic voltage is regulated from VCCQ. A C_{Reg} capacitor must be connected to the VDDi terminal to stabilize regulator output on the system.

Figure 8: Power Supply



7.2.2 e•MMC™ Power Supply Voltage

The e•MMC™ supports one or more combinations of VCC and VCCQ as shown in Table 15. The VCCQ must be defined at equal to or less than VCC. The available voltage configuration is shown.

Table 11: Power Supply Voltage

Parameter	Symbol	MIN	MAX	Unit
Supply Voltage (NAND)	Vcc	2.7	3.6	V
Supply Voltage (I/O)	Vccq	2.7	3.6	V
		1.65	1.95	V
Supply Power-Up for 3.3V	t_{PRUH}		35	ms
Supply Power-Up for 1.8V	t_{PRUL}		25	ms

The e•MMC™ must support at least one of the valid voltage configurations, and can optionally support all valid voltage configurations.

Table 12: Valid Voltages

Vcc	Vccq	
	1.65-1.95V	2.7-3.6V
2.7 – 3.6	Valid	Valid
Note 1: Vccq (I/O) 3.3V range is not supported in HS200 devices		

7.2.3 Bus Signal Line Load

The total capacitance C_L of each line of the e•MMC™ bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself, and the capacitance C_{DEVICE} of the device connected to this line, $C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$ and requiring the sum of the host and bus capacitances not to exceed 20 pF (see Table 17).

Table 13: Bus Signal Line Load

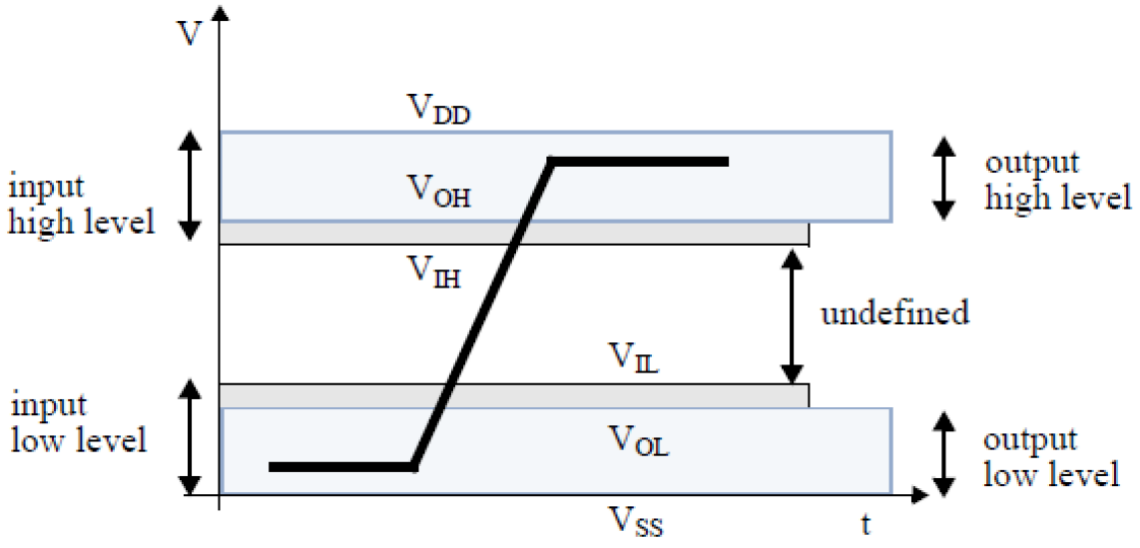
Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7	50	Kohm	to prevent bus floating
Pull-up resistance for DAT0–7	R_{DAT}	10	50	Kohm	to prevent bus floating
Pull-up resistance for RST_n	R_{RST_n}	4.7	50	Kohm	It is not necessary to put pull-up resistance on RST_n (H/W rest) line. If host does not use H/W reset. (Extended CSD register [162] = 0 b).
Bus signal line capacitance	CL		30	pF	Single Device
Single Device capacitance	C_{BGA}		12	pF	
Maximum signal line inductance			16	nH	
Impedance on CLK / CMD / DAT0~7		45	55	ohm	Impedance match
Serial's resistance on CLK line	SR_{CLK}	0	47	ohm	
Serial's resistance on	SR_{CMD}	0	47	ohm	

CMD / DAT0~7 line	$SR_{DAT0\sim7}$				
VccQ decoupling capacitor		2.2+0.1	4.7+0.22	µF	Capacitors should be located as close as possible to the balls defined in order to minimize connection parasitic
	CH1	1	2.2		CH1 should be placed adjacent to VccQ-VssQ balls (#K6 and #K4 accordingly, next to DAT [7..0] balls), It should be located as close as possible to the balls defined in order to minimize connection parasitic.
VCC capacitor value		1+0.1	4.7+0.22	µF	Capacitors should be located as close as possible to the balls defined in order to minimize connection parasitic
V_{Ddi} capacitor value	C_{REG}	1	4.7+0.1	µF	To stabilize regulator output to controller core logics. It should be located as close as possible to the balls defined in order to minimize connection parasitic

7.3 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

Figure 9: Bus Signal Levels



7.3.1 Open-Drain Mode Bus Signal Level

Table 14: Open-Drain Modes Bus Signal Level

Parameter	Symbol	Min	Max	Unit	Conditions
Output High Voltage	V_{OH}	V_{DD} – 0.2		V	IOH = -100µA
Output Low Voltage	V_{OL}		0.3	V	IOL = 2 mA

The input levels are identical to the push-pull mode bus signal levels.

7.3.2 Push-Pull Mode Bus Signal Level— e•MMC™

The device input and output voltages must be within the following specified ranges for any VDD of the allowed voltage range. For 2.7V-3.6V VCCQ range (compatible with JESD8C.01)

Table 15: Push-Pull Mode Bus Signal Level

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	VOH	0.75 * VCCQ		V	IOH = -100 µA @ VCCQ min
Output LOW voltage	VOL		0.125 * VCCQ	V	IOL = 100 µA @ VCCQ min
Input HIGH voltage	VIH	0.625 * VCCQ	VCCQ + 0.3	V	
Input LOW voltage	VIL	VSS – 0.3	0.25 * VCCQ	V	

For 1.65V – 1.95, V_{CCQ} range compatible with EIA/JEDEC Standard “EIA/JESD8-7 Normal Range

Table 16: EIA/JEDEC Voltage

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	VOH	V V_{CCQ} – 0.45V		V	IOH = -2mA
Output LOW voltage	VOL		0.45V	V	IOL = 2mA
Input HIGH voltage	VIH	0.65 * V_{CCQ} [1]	V_{CCQ} + 0.3	V	
Input LOW voltage	VIL	V_{SS} – 0.3	0.35 * V_{DD} [2]	V	
Note1：0.7 * V_{DD} for MMC™4.3 and older revisions. Note2：0.3 * V_{DD} for MMC™4.3 and older revisions.					

7.3.3 Bus Operating Conditions for HS200

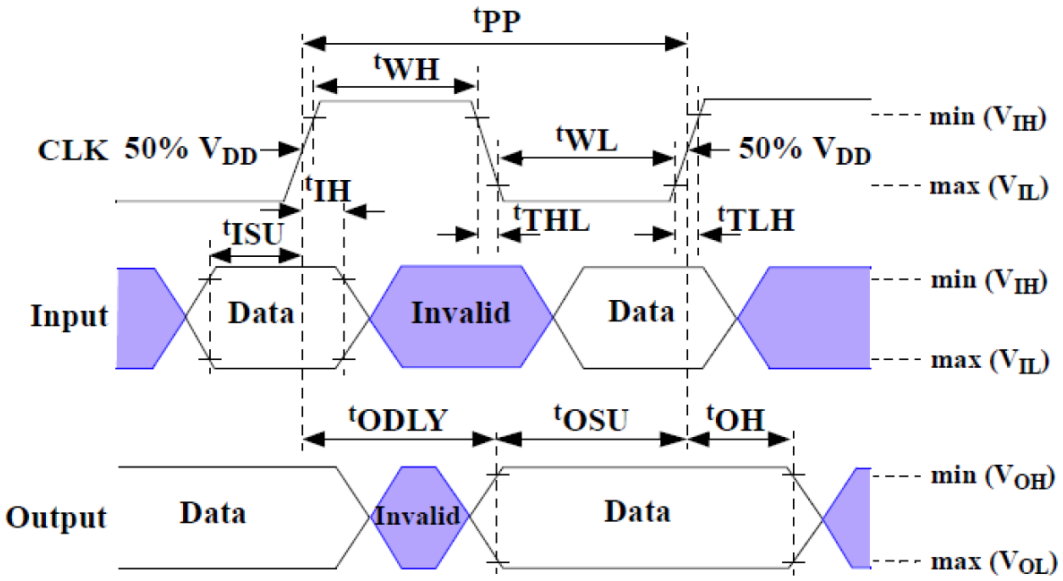
The bus operating conditions for HS200 devices is the same as specified in sections 10.5.1 of JESD84-B50through 10.5.2 of JESD84-B50. The only exception is that VCCQ=3.3v is not supported.

7.3.4 Device Output Driver Requirements for HS200

Refer to section 10.5.4 of the JEDEC Standard Specification No.JESD84-B50.

7.4 Bus Timing

Figure 10: Bus Timing



Data must always be sampled on the rising edge of the clock.

7.4.1 Device Interface Timings

Table 17: High-Speed Device Interface Timing

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK[1]					
Clock frequency Data Transfer Mode (PP)[2]	fPP	0	52[3]	MHz	CL ≤ 30 pF Tolerance:+100KHz
Clock frequency Identification Mode (OD)	fOD	0	400	kHz	Tolerance: +20KHz
Clock high time	tWH	6.5		ns	CL ≤ 30 pF
Clock low time	tWL	6.5		ns	CL ≤ 30 pF
Clock rise time[4]	tTLH		3	ns	CL ≤ 30 pF
Clock fall time	tTHL		3	ns	CL ≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	tISU	3		ns	CL ≤ 30 pF
Input hold time	tIH	3		ns	CL ≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	tODLY		13.7	ns	CL ≤ 30 pF
Output hold time	tOH	2.5		ns	CL ≤ 30 pF
Signal rise time[5]	tRISE		3	ns	CL ≤ 30 pF
Signal fall time	tFALL		3	ns	CL ≤ 30 pF

Note1：CLK timing is measured at 50% of VDD.
Note2：A *e*•MMC™ shall support the full frequency range from 0-26Mhz or 0-52MHz
Note3：Device can operate as high-speed Device interface timing at 26 MHz clock frequency.
Note4：CLK rise and fall times are measured by min (VIH) and max (VIL).
Note5：Inputs CMD DAT rise and fall times are measured by min (VIH) and max (VIL) and outputs CMD DAT rise and fall times are measured by min (VOH) and max (VOL).

Table 18: Backward-Compatible Device Interface Timing

Parameter	Symbol	Min	Max.	Unit	Remark[1]
Clock CLK[2]					
Clock frequency Data Transfer Mode (PP)[3]	fPP	0	26	MHz	CL ≤ 30 pF
Clock frequency Identification Mode (OD)	fOD	0	400	kHz	
Clock high time	tWH	10			CL ≤ 30 pF
Clock low time	tWL	10		ns	CL ≤ 30 pF
Clock rise time[4]	tTLH		10	ns	CL ≤ 30 pF
Clock fall time	tTHL		10	ns	CL ≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	tISU	3		ns	CL ≤ 30 pF
Input hold time	tIH	3		ns	CL ≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output set-up time[5]	tOSU	11.7		ns	CL ≤ 30 pF
Output hold time[5]	tOH	8.3		ns	CL ≤ 30 pF

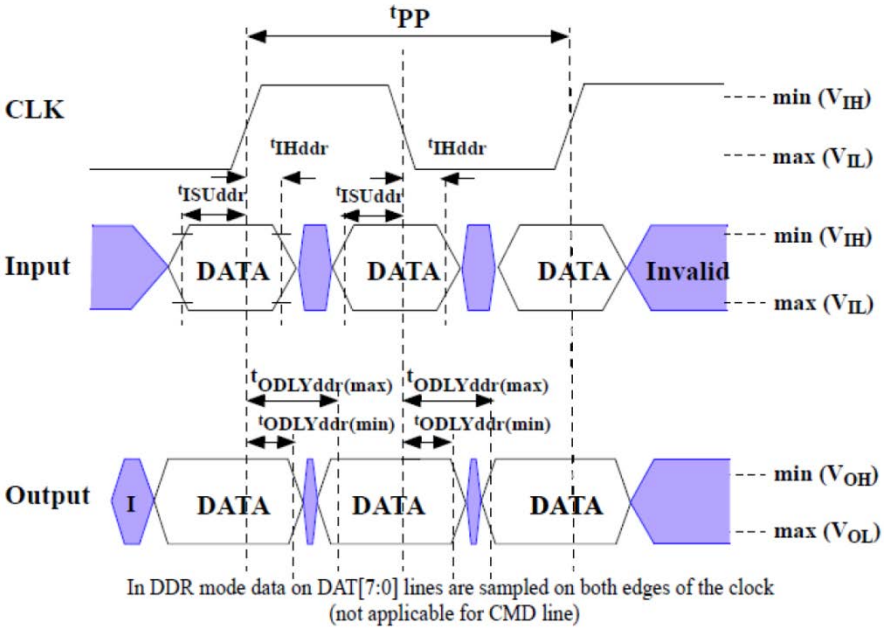
Note1：The Device must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.
Note2：CLK timing is measured at 50% of VDD.
Note3：For compatibility with Devices that support the v4.2 standard or earlier, host should not use > 26 MHz before switching to high-speed interface timing.
Note4：CLK rise and fall times are measured by min (VIH) and max (VIL).
Note5：tOSU and tOH are defined as values from clock rising edge. However, there may be Devices or devices which utilize

clock falling edge to output data in backward compatibility mode. Therefore, it is recommended for hosts either to settWL value as long as possible within the range which will not go over tCK-tOH(min) in the system or to use slow clock frequency, so that host could have data set up margin for those devices. In this case, each devicewhich utilizes clock falling edge might show the correlation either between tWL and tOSU or between tCK and tOSU for the device in its own datasheet as a note or its application notes.

7.5 Bus Timing for DAT Signals During Dual Data Rate Operation

These timing parameters apply to the DAT[7:0] signals only when the device is configured for dual data mode operation. In this dual data mode, the DAT signals operates synchronously of both the rising and the falling edges of CLK. The CMD signal still operates synchronously of the rising edge of CLK and complies with the bus timing specified in section 10.5, so there is no timing change for the CMD signal.

Figure 11: Data I/O In Dual Data Rate Mode



7.5.1 Dual Data Rate Interface Timings

Table 19: High-Speed Dual Data Rate Interface Timing

Parameter	Symbol	Min	Max.	Unit	Remark
Input CLK[1]					
Clock duty cycle		45	55	%	Includes jitter, phase noise
Input DAT (referenced to CLK-DDR mode)					
Input set-up time	tISUddr	2.5		ns	CL ≤ 20 pF
Input hold time	tIHddr	2.5		ns	CL ≤ 20 pF
Output DAT (referenced to CLK-DDR mode)					
Output delay time during data transfer	tODLYddr	1.5	7	ns	CL ≤ 20 pF
Signal rise time (all signals)[2]	tRISE		2	ns	CL ≤ 20 pF
Signal fall time (all signals)	tFALL		2	ns	CL ≤ 20 pF

Note1：CLK timing is measured at 50% of VDD.

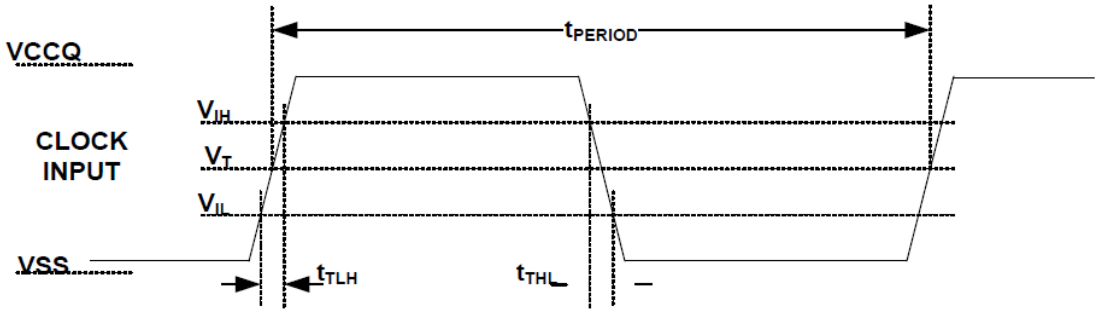
Note2：Inputs CMD, DAT rise and fall times are measured by min (V_{IH}) and max (V_{IL}), and outputs CMD, DAT rise and fall times are measured by min (V_{OH}) and max (V_{OL})

7.6 Bus Timing Specification in HS200 Mode

7.6.1 HS200 Clock Timing

Host CLK Timing in HS200 mode will conform to the timing specified in Figure 12 and Table 22. CLK input will satisfy the clock timing over all possible operation and environment conditions. CLK input parameters should be measured while CMD and DAT lines are stable high or low, as close as possible to the device. The maximum frequency of HS200 is 200MHz. Hosts can use any frequency up to the maximum that HS200 mode allows.

Figure 12: HS200 Clock Timing



Note1：V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

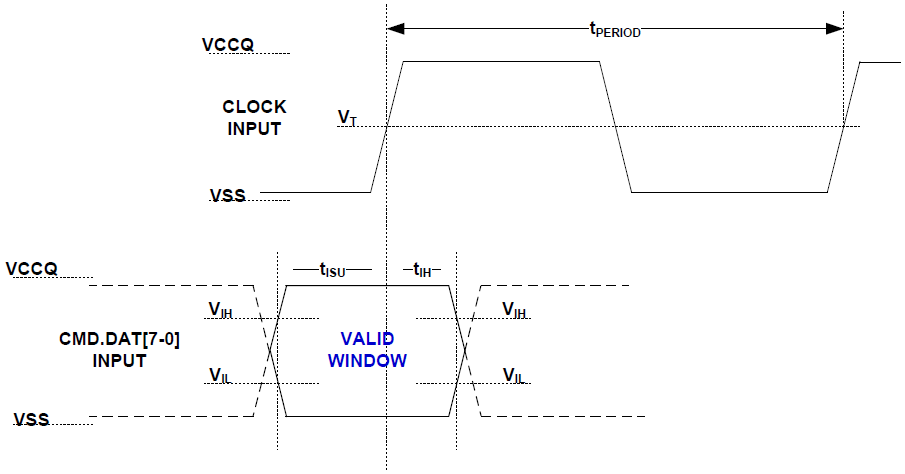
Note2：V_T=0.975V – Clock Threshold, indicates clock reference point for timing measurements.

Table 20: HS200 Clock Signal Timing

Symbol	Min.	Max.	Unit	Remark
t_{PERIOD}	5	-	ns	200MHz (Max.), between rising edges
t_{TLH}, t_{THL}	-	0.2* t_{PERIOD}	ns	t_{TLH}, t_{THL} < 1ns (max.) at 200MHz, C_{BGA}=12pF, The absolute maximum value of t_{TLH}, t_{THL} is 10ns regardless of clock frequency.
Duty Cycle	30	70	%	

7.6.2 HS200 Device Input Timing

Figure 13: HS200 Device Input Timing



Note1: t_{ISU} and t_{IH} are measured at V_{IL}(max.) and V_{IH}(min.).
Note2: V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

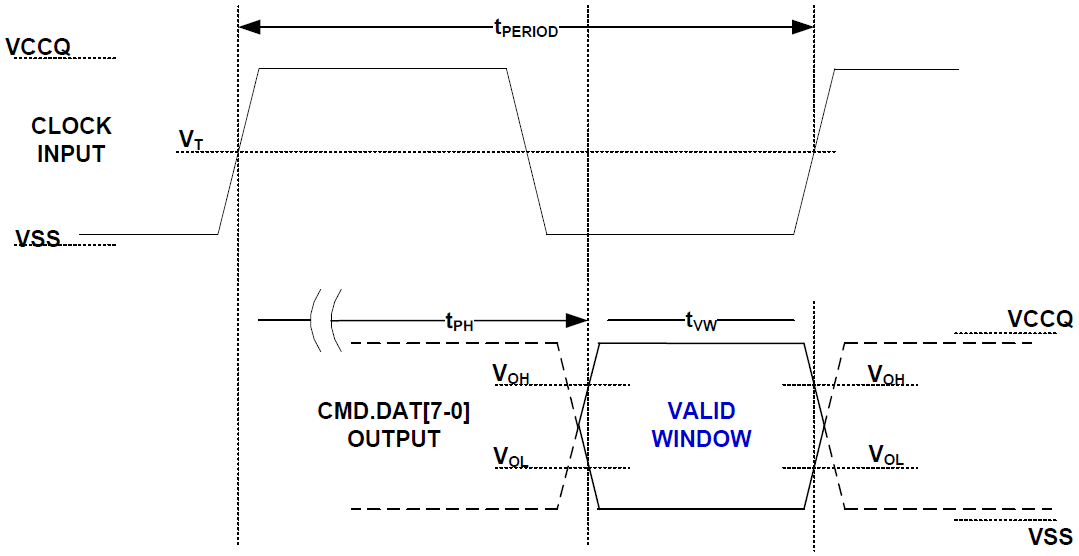
Table 21: HS200 Device Input Timing

Symbol	Min.	Max.	Unit	Remark
t_{ISU}	1.4	-	ns	$5pF \leq C_{BGA} \leq 12pF$
t_{IH}	0.8		ns	$5pF \leq C_{BGA} \leq 12pF$

7.6.3 HS200 Device Output Timing

t_{PH} parameter is defined to allow device output delay to be longer than t_{PERIOD}. After initialization, the t_{PH} may have random phase relation to the clock. The host is responsible for finding the optimal sampling point for the device outputs while switching to the HS200 mode. While setting the sampling point of data, a long term drift, which mainly depends on temperature drift, should be considered. The temperature drift is expressed by ΔT_{PH}. Output valid data window (t_{VW}) is available regardless of the drift (ΔT_{PH}) but position of data window varies by the drift.

Figure 14: HS200 Device Output Timing

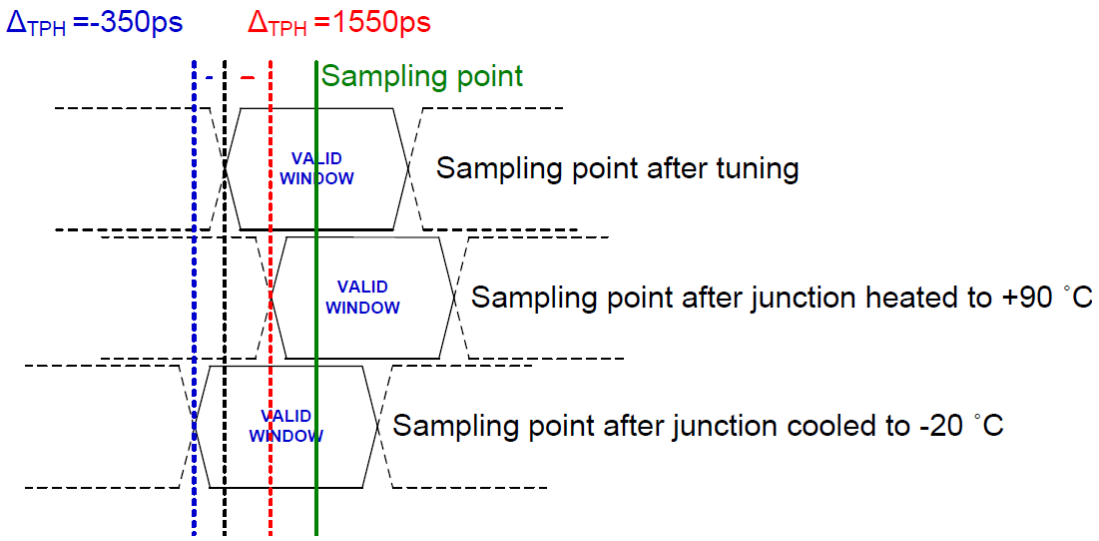


Note: V_{OH} denotes V_{OH}(min.) and V_{OL} denotes V_{OL}(max.).

Table 22: HS200 Output Timing

Symbol	Min.	Max.	Unit	Remark
t_{PH}	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
ΔT_{PH}	-350 (ΔT=-20°C)	+1550 (ΔT=90°C)	ps	Delay variation due to temperature change after tuning. Total allowable shift of output valid window (T_{VW}) from last system Tuning procedure ΔT_{PH} is 2600ps for ΔT from -25°C to 125°C during operation.
T_{VW}	0.575	-	UI	t_{VW}=2.88ns at 200MHz Using test circuit in Figure 15 including skew among CMD and DAT lines created by the Device. Host path may add Signal Integrity induced noise, skews, etc. Expected T_{VW} at Host input is larger than 0.475UI.
Note1: Unit Interval (UI) is one bit nominal time. For example, UI=5ns at 200MHz.				

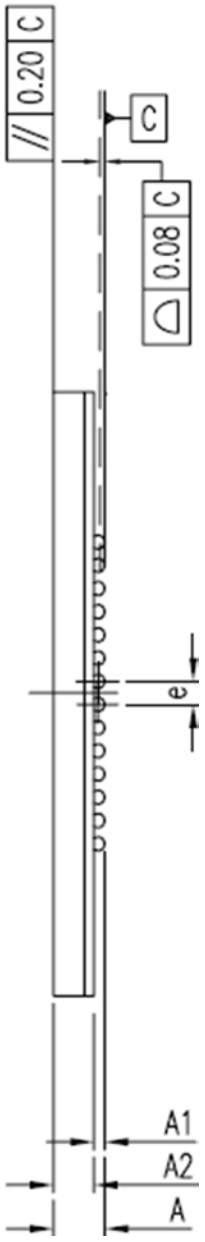
Figure 15: ΔTPH Consideration



Implementation Guide: Host system should be designed in a manner that avoids sampling errors that may be caused by the ΔT_{PH} drift. The tuning procedure should be performed after device wakes up, and after sleep. The ΔT_{PH} drift can be mitigated by reduction of operating frequency.

8 Package Dimensions

FIGURE 16: PACKAGE MECHANICAL 2



Min 0.15mm
Max 0.92mm
Max 1.0mm

FIGURE 17: PACKAGE MECHANICAL 1

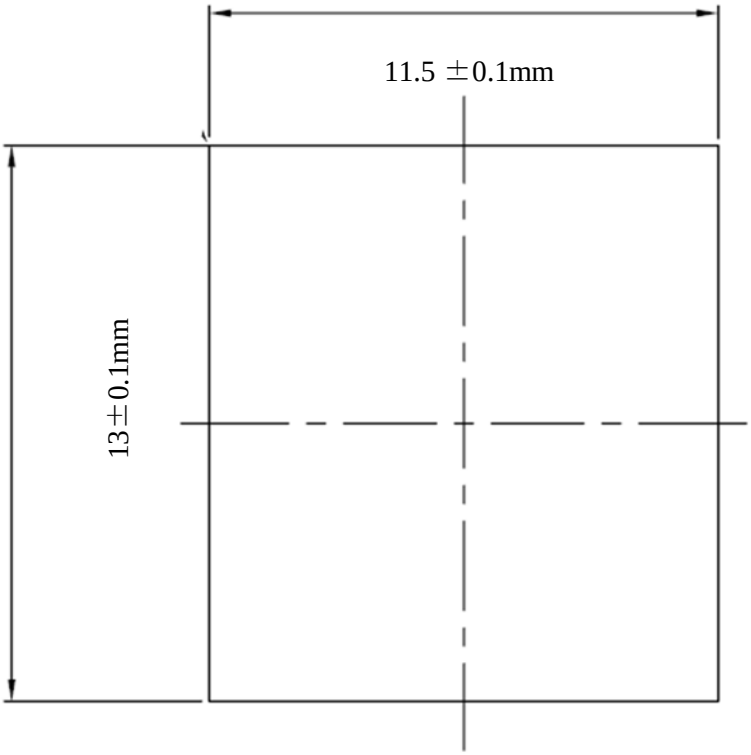
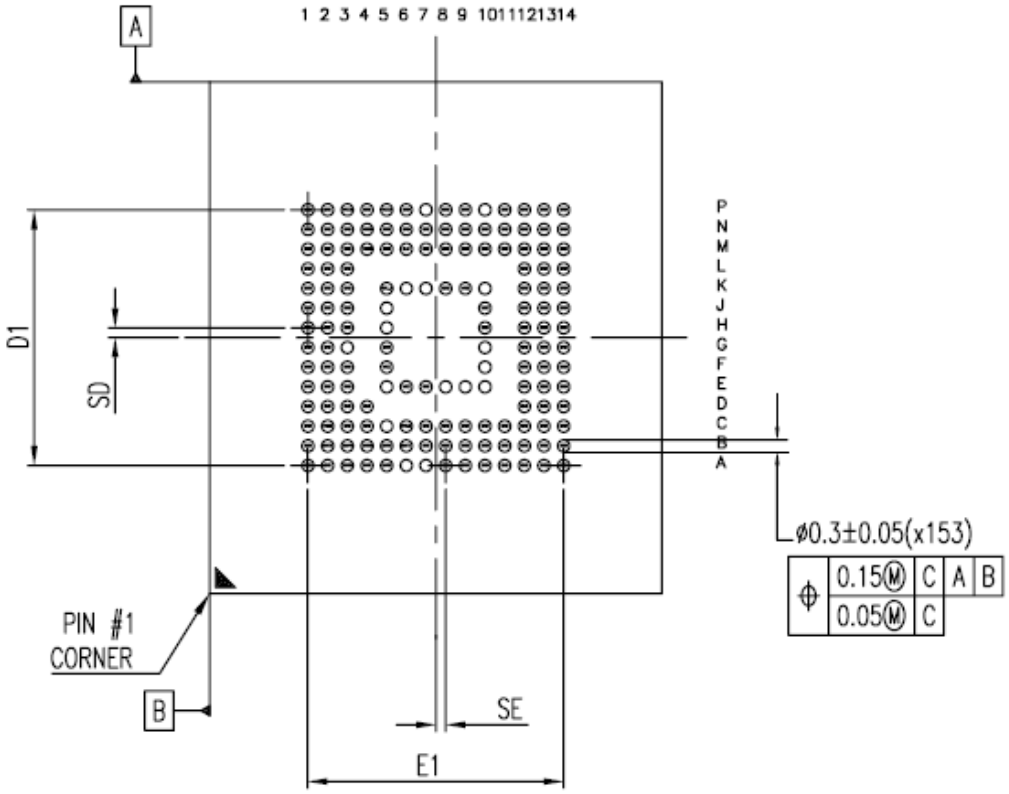


Figure 18: Ball View



BOTTOM VIEW

N	SE (MM)	SD (MM)	E1(MM)	D1(MM)	JEDEC(REF)
153	0.25 BSC.	0.25 BSC.	6.50 BSC.	6.50 BSC.	MO-276 BA

9 Ball Assignment (153 ball)

9.1 HS200

TABLE 23: BALL ASSIGNMENT TOP VIEW (HS200)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NC	NC	DAT0	DAT1	DAT2	RFU	RFU	NC	NC	NC	NC	NC	NC	NC	A
B	NC	DAT3	DAT4	DAT5	DAT6	DAT7	NC	NC	NC	NC	NC	NC	NC	NC	B
C	NC	Vddi	NC	Vssq	NC	Vccq	NC	NC	NC	NC	NC	NC	NC	NC	C
D	NC	NC	NC	NC								NC	NC	NC	D
E	NC	NC	NC		RFU	Vcc	Vss	RFU	RFU	RFU		NC	NC	NC	E
F	NC	NC	NC		Vcc					RFU		NC	NC	NC	F
G	NC	NC	RFU		Vss					RFU		NC	NC	NC	G
H	NC	NC	NC		RFU					Vss		NC	NC	NC	H
J	NC	NC	NC		RFU					Vcc		NC	NC	NC	J
K	NC	NC	NC		RST_n	RFU	RFU	Vss	Vcc	RFU		NC	NC	NC	K
L	NC	NC	NC									NC	NC	NC	L
M	NC	NC	NC	Vccq	CMD	CLK	NC	NC	NC	NC	NC	NC	NC	NC	M
N	NC	Vssq	NC	Vccq	Vssq	NC	NC	NC	NC	NC	NC	NC	NC	NC	N
P	NC	NC	Vccq	Vssq	Vccq	Vssq	RFU	NC	NC	RFU	NC	NC	NC	NC	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Note1: Both RFU and NC balls are not electrically connected. RFU balls may be defined with functionality by the Joint Electron Device Engineering Council (JEDEC) in future revisions of the eMMC standard. Kingston's eMMC 5.0 (HS200) product line will maintain these RFU balls as not connected. Please refer to Kingston's design guidelines for more info.

9.2 HS400

TABLE 24: BALL ASSIGNMENT TOP VIEW (HS400)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NC	NC	DAT0	DAT1	DAT2	Vss	RFU	NC	NC	NC	NC	NC	NC	NC	A
B	NC	DAT3	DAT4	DAT5	DAT6	DAT7	NC	NC	NC	NC	NC	NC	NC	NC	B
C	NC	Vddi	NC	Vssq	NC	Vccq	NC	NC	NC	NC	NC	NC	NC	NC	C
D	NC	NC	NC	NC								NC	NC	NC	D
E	NC	NC	NC		RFU	Vcc	Vss	Vsf	Vsf	Vsf		NC	NC	NC	E
F	NC	NC	NC		Vcc					Vsf		NC	NC	NC	F
G	NC	NC	RFU		Vss					Vsf		NC	NC	NC	G
H	NC	NC	NC		DS					Vss		NC	NC	NC	H
J	NC	NC	NC		Vss					Vcc		NC	NC	NC	J
K	NC	NC	NC		RST_n	RFU	RFU	Vss	Vcc	Vsf		NC	NC	NC	K
L	NC	NC	NC									NC	NC	NC	L
M	NC	NC	NC	Vccq	CMD	CLK	NC	NC	NC	NC	NC	NC	NC	NC	M
N	NC	Vssq	NC	Vccq	Vssq	NC	NC	NC	NC	NC	NC	NC	NC	NC	N
P	NC	NC	Vccq	Vssq	Vccq	Vssq	RFU	NC	NC	RFU	NC	NC	NC	NC	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Note1: Changes from HS200 to HS400 are as follows:
DS: H5
Vss: A6, J5
Vsf: E8, E9, E10, F10, G10, K10

10 Marking

Figure 19: EMMC Marking

Kingston Logo
240xxxx-xxx.xxxx：Internal control number
YYWW：Date code (YY– Last 2 digital of year, WW- Work week)
PPPPPPPP： Internal control number
xxxxxxx-xxxx Sales P/N
2xxxxxx : Internal control number
Country：TAIWAN

11 Part Decoder

TABLE 25: PART DECODER

EMMC	08G	-	W	1	00	-	WXYZ
A	B	C	D	E	F	G	H

Description	
A: Product Type	B: eMMC Capacity
C: N/A	D: Product Segment
E: NAND Type	F: Generation

A: Product Type		**B: eMMC Capacity**	
Symbol	Description	Symbol	Description
EMMC	Embedded Multi Media Chip	04G	4 GB
		08G	8GB
		16G	16 GB
		32G	32 GB
		64G	64 GB
C: N/A		**D: Product Segment**	
Symbol	Description	Symbol	Description
-	-	S	Standard
		E	Elite
		W	Industrial Temperature
E: NAND		**F: MODEL**	
Symbol	Description	Symbol	Description
1	A19	00	Model 00
		10	Model 10
G: N/A		**H: FIRMWARE**	
Symbol	Description	Symbol	Description
-	-	WXYZ	Firmware and Configuration

12 Specifications

Part #	Capacity (GB)	Pacakge (FBGA)	L x W x H (mm)	Temp. Range	Sequential (MB/s)		Power Consumption (mA)			Boot 1 & 2, RPMB (KB)	User Capacity (Bytes)	Settings
					Read	Write	Read	Write	Standby			
EMMC08G-W100-A06U	8	153	11.5x13x1.0	Industrial	135	12	130	85	0.159	4096	7818182656	HS200, MLC

TABLE 26: TEMPERATURE

Temperature	Operating (C)	Storage (C)
Standard	-25 to +85	-40 to +85
Industrial	-40 to +85	-55 to +85

13 Register Values

13.1 Extended CSD Registers

TABLE 27: EXTENDED CSD REGISTERS

Field Name	[Byte Addr]	Value
Reserved	[511:506]	0
EXT_SECURITY_ERR	[505:505]	0x00
S_CMD_SET	[504:504]	0x01
HPI_FEATURES	[503:503]	0x03
BKOPS_SUPPORT	[502:502]	0x01
MAX_PACKED_READS	[501:501]	0x3C
MAX_PACKED_WRITES	[500:500]	0x3C
DATA_TAG_SUPPORT	[499:499]	0x01
TAG_UNIT_SIZE	[498:498]	0x03
TAG_RES_SIZE	[497:497]	0x00
CONTEXT_CAPABILITIES	[496:496]	0x05
LARGE_UNIT_SIZE_M1	[495:495]	0x03
EXT_SUPPORT	[494:494]	0x03
SUPPORTED_MODES	[493:493]	0x01
FFU_FEATURES	[492:492]	0x00
OPERATION_CODE_TIMEOUT	[491:491]	0x00
FFU_ARG	[490:487]	0
Reserved	[486:306]	0
NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	[305:302]	0
VENDOR_PROPRIETARY_HEALTH_REPORT	[301:270]	0
DEVICE_LIFE_TIME_EST_TYP_B	[269:269]	0x01
DEVICE_LIFE_TIME_EST_TYP_A	[268:268]	0x01
PRE_EOL_INFO	[267:267]	0x01
OPTIMAL_READ_SIZE	[266:266]	0x01
OPTIMAL_WRITE_SIZE	[265:265]	0x04
OPTIMAL_TRIM_UNIT_SIZE	[264:264]	0x01
DEVICE_VERSION	[263:262]	0
FIRMWARE_VERSION	[261:254]	6
PWR_CL_DDR_200_360	[253:253]	0x00
CACHE_SIZE	[252:249]	32
GENERIC_CMD6_TIME	[248:248]	0x19
POWER_OFF_LONG_TIME	[247:247]	0xFF
BKOPS_STATUS	[246:246]	0x00
CORRECTLY_PRG_SECTORS_NUM	[245:242]	0
INI_TIMEOUT_AP	[241:241]	0x32
Reserved	[240:240]	0x00
PWR_CL_DDR_52_360	[239:239]	0x00

PWR_CL_DDR_52_195	[238:238]	0x00
PWR_CL_200_195	[237:237]	0x00
PWR_CL_200_130	[236:236]	0x00
MIN_PERF_DDR_W_8_52	[235:235]	0x00
MIN_PERF_DDR_R_8_52	[234:234]	0x00
Reserved	[233:233]	0x00
TRIM_MULT	[232:232]	0x0F
SEC_FEATURE_SUPPORT	[231:231]	0x55
SEC_ERASE_MULT	[230:230]	0x06
SEC_TRIM_MULT	[229:229]	0x09
BOOT_INFO	[228:228]	0x07
Reserved	[227:227]	0x00
BOOT_SIZE_MULT	[226:226]	0x20
ACC_SIZE	[225:225]	0x06
HC_ERASE_GRP_SIZE	[224:224]	0x08
ERASE_TIMEOUT_MULT	[223:223]	0x01
REL_WR_SEC_C	[222:222]	0x01
HC_WP_GRP_SIZE	[221:221]	0x02
S_C_VCC	[220:220]	0x08
S_C_VCCQ	[219:219]	0x08
PRODUCTION_STATE_AWARENESS_TIMEOUT	[218:218]	0x00
S_A_TIMEOUT	[217:217]	0x10
SLEEP_NOTIFICATION_TIME	[216:216]	0x0F
SEC_COUNT	[215:212]	15269888
Reserved	[211:211]	0x00
MIN_PERF_W_8_52	[210:210]	0x08
MIN_PERF_R_8_52	[209:209]	0x08
MIN_PERF_W_8_26_4_52	[208:208]	0x08
MIN_PERF_R_8_26_4_52	[207:207]	0x08
MIN_PERF_W_4_26	[206:206]	0x08
MIN_PERF_R_4_26	[205:205]	0x08
Reserved	[204:204]	0x00
PWR_CL_26_360	[203:203]	0x00
PWR_CL_52_360	[202:202]	0x00
PWR_CL_26_195	[201:201]	0x00
PWR_CL_52_195	[200:200]	0x00
PARTITION_SWITCH_TIME	[199:199]	0x03
OUT_OF_INTERRUPT_TIME	[198:198]	0x04
DRIVER_STRENGTH	[197:197]	0x0F
DEVICE_TYPE	[196:196]	0x17
Reserved	[195:195]	0x00
CSD_STRUCTURE	[194:194]	0x02

Reserved	[193:193]	0x00
EXT_CSD_REV	[192:192]	0x07
CMD_SET	[191:191]	0x00
Reserved	[190:190]	0x00
CMD_SET_REV	[189:189]	0x00
Reserved	[188:188]	0x00
POWER_CLASS	[187:187]	0x00
Reserved	[186:186]	0x00
HS_TIMING	[185:185]	0x01
Reserved	[184:184]	0x00
BUS_WIDTH	[183:183]	0x02
Reserved	[182:182]	0x00
ERASED_MEM_CONT	[181:181]	0x00
Reserved	[180:180]	0x00
PARTITION_CONFIG	[179:179]	0x00
BOOT_CONFIG_PROT	[178:178]	0x00
BOOT_BUS_CONDITIONS	[177:177]	0x00
Reserved	[176:176]	0x00
ERASE_GROUP_DEF	[175:175]	0x00
BOOT_WP_STATUS	[174:174]	0x00
BOOT_WP	[173:173]	0x00
Reserved	[172:172]	0x00
USER_WP	[171:171]	0x00
Reserved	[170:170]	0x00
FW_CONFIG	[169:169]	0x00
RPMB_SIZE_MULT	[168:168]	0x20
WR_REL_SET	[167:167]	0x00
WR_REL_PARAM	[166:166]	0x05
SANITIZE_START	[165:165]	0x00
BKOPS_START	[164:164]	0x00
BKOPS_EN	[163:163]	0x00
RST_n_FUNCTION	[162:162]	0x00
HPI_MGMT	[161:161]	0x00
PARTITIONING_SUPPORT	[160:160]	0x07
MAX_ENH_SIZE_MULT	[159:157]	466
PARTITIONS_ATTRIBUTE	[156:156]	0x00
PARTITION_SETTING_COMPLETED	[155:155]	0x00
GP_SIZE_MULT_4	[154:152]	0
GP_SIZE_MULT_3	[151:149]	0
GP_SIZE_MULT_2	[148:146]	0
GP_SIZE_MULT_1	[145:143]	0
ENH_SIZE_MULT	[142:140]	0

ENH_START_ADDR	[139:136]	0
Reserved	[135:135]	0x00
SEC_BAD_BLK_MGMNT	[134:134]	0x00
PRODUCTION_STATE_AWARENESS	[133:133]	0x00
TCASE_SUPPORT	[132:132]	0x00
PERIODIC_WAKEUP	[131:131]	0x00
PROGRAM _CID_CSD_DDR_SUPPORT	[130:130]	0x01
Reserved	[129:128]	0
VENDOR_SPECIFIC_FIELD	[127:64]	0
NATIVE_SECTOR_SIZE	[63:63]	0x00
USE_NATIVE_SECTOR	[62:62]	0x00
DATA_SECTOR_SIZE	[61:61]	0x00
INI_TIMEOUT_EMU	[60:60]	0x0A
CLASS_6_CTRL	[59:59]	0x00
DYNCAP_NEEDED	[58:58]	0x00
EXCEPTION_EVENTS_CTRL	[57:56]	0
EXCEPTION_EVENTS_STATUS	[55:54]	0
EXT_PARTITIONS_ATTRIBUTE	[53:52]	0
CONTEXT_CONF	[51:37]	0
PACKED_COMMAND_STATUS	[36:36]	0x00
PACKED_FAILURE_INDEX	[35:35]	0x00
POWER_OFF_NOTIFICATION	[34:34]	0x00
CACHE_CTRL	[33:33]	0x00
FLUSH_CACHE	[32:32]	0x00
Reserved	[31:31]	0x00
MODE_CONFIG	[30:30]	0x00
MODE_OPERATION_CODES	[29:29]	0x00
Reserved	[28:27]	0
FFU_STATUS	[26:26]	0x00
PRE_LOADING_DATA_SIZE	[25:22]	0
MAX_PRE_LOADING_DATA_SIZE	[21:18]	7634944
PRODUCT_STATE_AWARENESS_ENABLEMENT	[17:17]	0x01
SECURE_REMOVAL_TYPE	[16:16]	0x00
Reserved	[15:0]	0

13.2 CSD Registers

TABLE 28:CSD REGISTERS

Field Name	[Byte Addr]	Value
CSD_Structure	[127:126]	0x03 (V2.0)
SPEC_VER	[125:122]	0x04 (V4.0~4.2)
reserved	[121:120]	0x00
TAAC	[119:112]	0x4F (40ms)
NSAC	[111:104]	0x01
TRAN_SPEED	[103:96]	0x32 (25Mbit/s)
CCC	[95:84]	0x0F5
READ_BL_LEN	[83:80]	0x09 (512 Bytes)
READ_BL_PARTIAL	[79:79]	0x00
WRITE_BLK_MISALIGN	[78:78]	0x00
READ_BLK_MISALIGN	[77:77]	0x00
DSR_IMP	[76:76]	0x00
reserved	[75:74]	0x00
C_SIZE	[73:62]	0xfff
VDD_R_CURR_MIN	[61:59]	0x07 (100mA)
VDD_R_CURR_MAX	[58:56]	0x07 (200mA)
VDD_W_CURR_MIN	[55:53]	0x07 (100mA)
VDD_W_CURR_MAX	[52:50]	0x07 (200mA)
C_SIZE_MULT	[49:47]	0x07 (512 Bytes)
ERASE_GRP_SIZE	[46:42]	0x1F
ERASE_GRP_MULT	[41:37]	0x1F
WP_GRP_SIZE	[36:32]	0x0F
WP_GRP_ENABLE	[31:31]	0x01
DEFAULT_ECC	[30:29]	0x00
R2W_FACTOR	[28:26]	0x02
WRITE_BL_LEN	[25:22]	0x09 (512 Bytes)
WRITE_BL_PARTIAL	[21:21]	0x00
reserved	[20:17]	0x00
CONTENT_PROT_APP	[16:16]	0x00
FILE_FORMAT_GRP	[15:15]	0x00
COPY	[14:14]	0x00
PERM_WRITE_PROTECT	[13:13]	0x00
TMP_WRITE_PROTECT	[12:12]	0x00
FILE_FORMAT	[11:10]	0x00
ECC	[9:8]	0x00
CRC	[7:1]	0x30
reserved	[0:0]	0x01

13.3 CID Registers

TABLE 29:CID REGISTERS

Field Name	[Byte Addr]	Value
MID	[127:120]	0x70
reserved	[119:114]	0x00
CBX	[113:112]	0x01
OID	[111:104]	0x00
PNM	[103:56]	W10008
PRV	[55:48]	0x06
PSN[1]	[47:16]	0x01 0x64 0x09 0x6D
MDT[1]	[15:8]	0xC1 (December, 2014)
CRC[1]	[7:1]	0x71
reserved	[0:0]	0x01
1: Values will vary.		

14 History Revision

TABLE 30: HISTORY REVISION

Revision	Date	Description
v0.0.1	01/22/2015	Document Release