

MOSFET – Power, Dual N-Channel

40 V, 17.0 mΩ, 27 A

NVMFD5C478N

Features

- Small Footprint (5 x 6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVMFD5C478NWF – Wettable Flanks Product
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	40	V
Gate-to-Source Voltage	V _{GS}	±20	V
Continuous Drain Current R _{θJC} (Notes 1, 2, 3, 4)	T _C = 25°C	I _D	27
	T _C = 100°C		19
Power Dissipation R _{θJC} (Notes 1, 2, 3)	T _C = 25°C	P _D	23
	T _C = 100°C		12
Continuous Drain Current R _{θJA} (Notes 1 & 3, 4)	T _A = 25°C	I _D	9.8
	T _A = 100°C		6.9
Power Dissipation R _{θJA} (Notes 1, 3)	T _A = 25°C	P _D	3.1
	T _A = 100°C		1.5
Pulsed Drain Current	T _A = 25°C, t _p = 10 µs	I _{DM}	90
Operating Junction and Storage Temperature	T _J , T _{stg}	-55 to +175	°C
Source Current (Body Diode)	I _S	19	A
Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 1.4 A)	E _{AS}	48	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T _L	260	°C

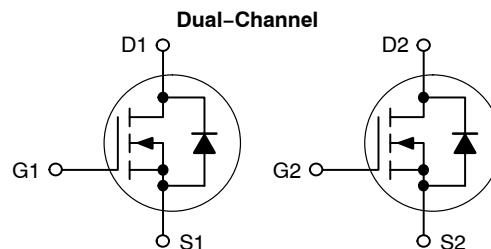
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

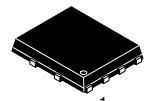
Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 3)	R _{θJC}	6.5	°C/W
Junction-to-Ambient – Steady State (Note 3)	R _{θJA}	48.8	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

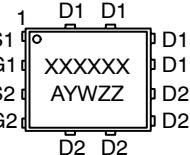
V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX
40 V	17.0 mΩ @ 10 V	27 A



PIN CONNECTION & MARKING DIAGRAM



**DFN8, 5x6
(S08FL)**
CASE 506BT



XXXXXX = 5C478N (NVMFD5C478N) or
478NWF (NVMFD5C478NWF)

A = Assembly Location

Y = Year

ZZ = Lot Traceability

WW = Work Week

▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

NVMFD5C478N

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0 \text{ V}, I_D = 250 \mu\text{A}$	40			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{GS}} = 0 \text{ V}, V_{\text{DS}} = 40 \text{ V}$	$T_J = 25^\circ\text{C}$		10	μA
			$T_J = 125^\circ\text{C}$		250	
Gate-to-Source Leakage Current	I_{GSS}	$V_{\text{DS}} = 0 \text{ V}, V_{\text{GS}} = 20 \text{ V}$			100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{\text{GS}(\text{TH})}$	$V_{\text{GS}} = V_{\text{DS}}, I_D = 20 \mu\text{A}$	2.5		3.5	V
Drain-to-Source On Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10 \text{ V}, I_D = 7.5 \text{ A}$		14	17	$\text{m}\Omega$
Forward Transconductance	g_{FS}	$V_{\text{DS}} = 3 \text{ V}, I_D = 7.5 \text{ A}$		2		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{iss}	$V_{\text{GS}} = 0 \text{ V}, f = 1.0 \text{ MHz}, V_{\text{DS}} = 25 \text{ V}$		325		pF
Output Capacitance	C_{oss}			165		
Reverse Transfer Capacitance	C_{rss}			10		
Total Gate Charge	$Q_{\text{G}(\text{TOT})}$	$V_{\text{GS}} = 10 \text{ V}, V_{\text{DS}} = 32 \text{ V}, I_D = 7.5 \text{ A}$		6.3		nC
Threshold Gate Charge	$Q_{\text{G}(\text{TH})}$			1.3		
Gate-to-Source Charge	Q_{GS}			2.0		
Gate-to-Drain Charge	Q_{GD}			1.2		

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{GS}} = 10 \text{ V}, V_{\text{DS}} = 32 \text{ V}, I_D = 7.5 \text{ A}, R_{\text{G}} = 1 \Omega$		7		ns
Rise Time	t_r			13		
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$			14		
Fall Time	t_f			4.5		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{\text{GS}} = 0 \text{ V}, I_S = 7.5 \text{ A}$	$T_J = 25^\circ\text{C}$		0.84	1.2	V
			$T_J = 125^\circ\text{C}$		0.72		
Reverse Recovery Time	t_{RR}	$V_{\text{GS}} = 0 \text{ V}, dI_S/dt = 100 \text{ A}/\mu\text{s}, I_S = 7.5 \text{ A}$			18		ns
Charge Time	t_a				7.0		
Discharge Time	t_b				11		
Reverse Recovery Charge	Q_{RR}				6		

5. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

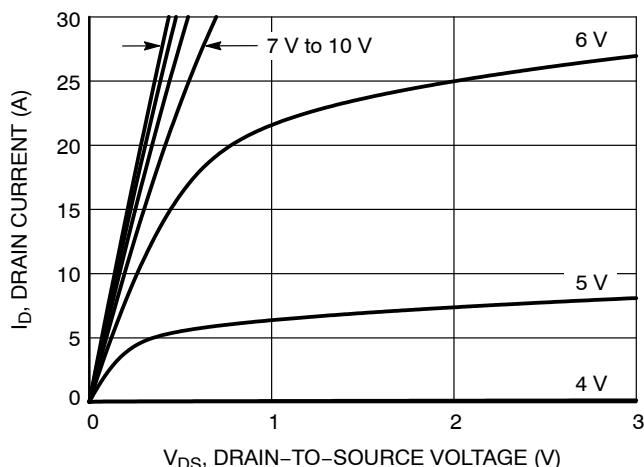


Figure 1. On-Region Characteristics

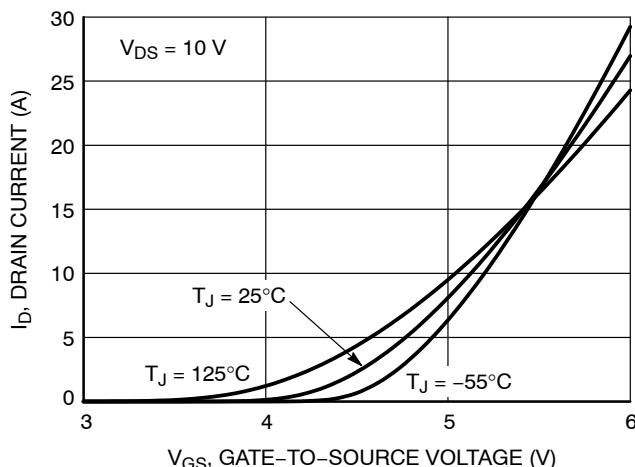


Figure 2. Transfer Characteristics

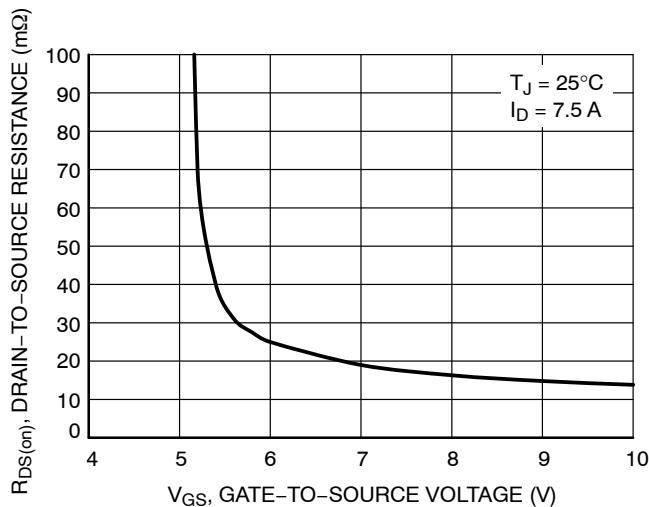


Figure 3. On-Resistance vs. Gate-to-Source Voltage

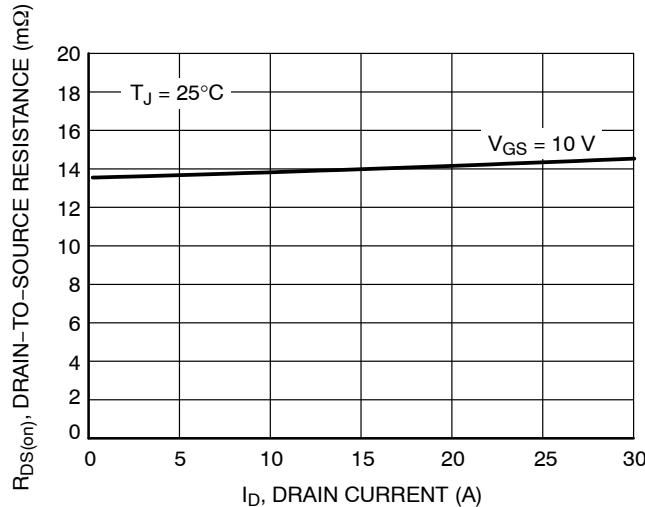


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

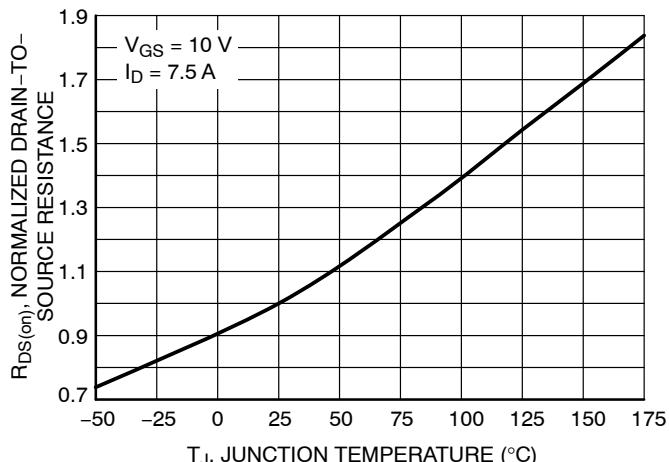


Figure 5. On-Resistance Variation with Temperature

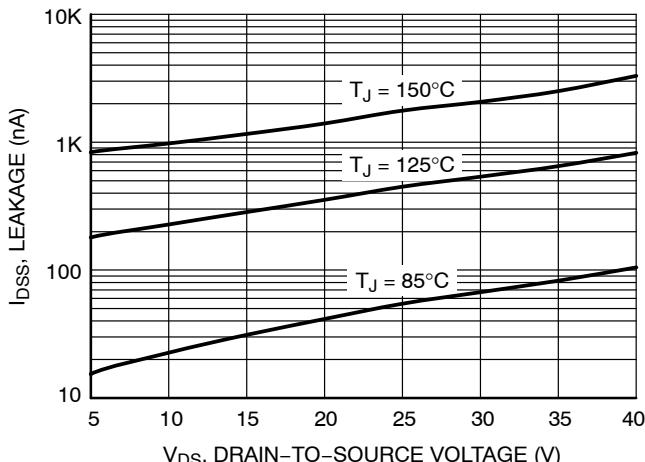


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

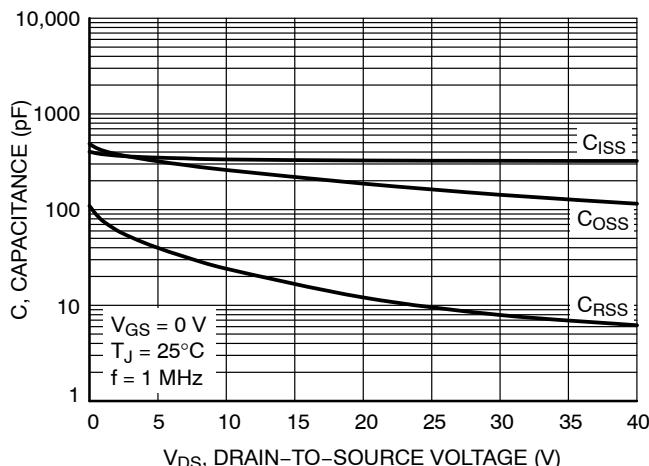


Figure 7. Capacitance Variation

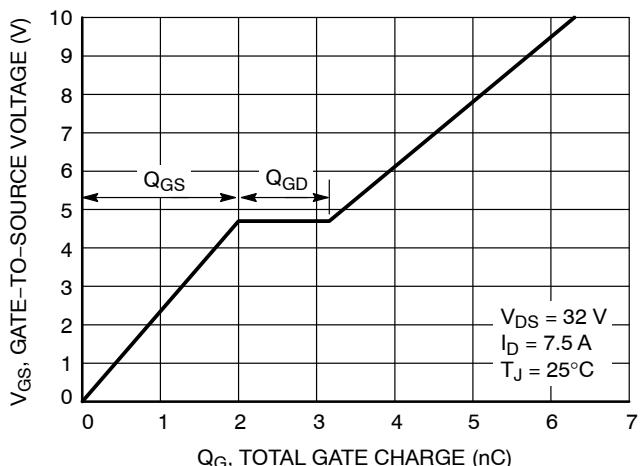


Figure 8. Gate-to-Source Voltage vs. Total Charge

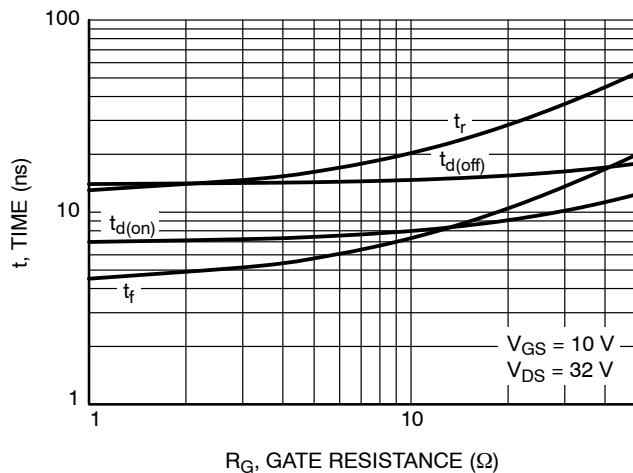


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

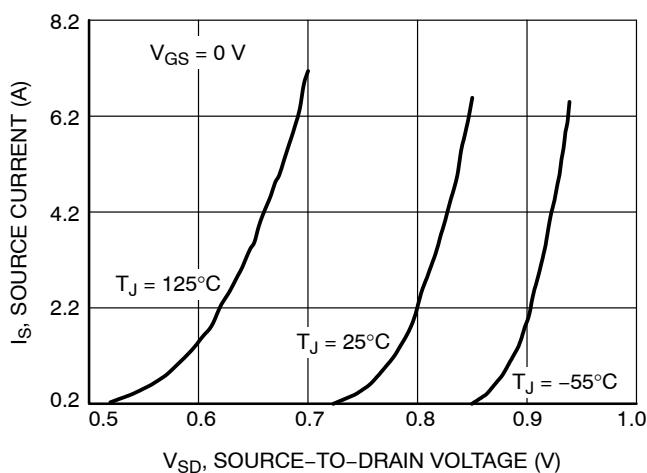


Figure 10. Diode Forward Voltage vs. Current

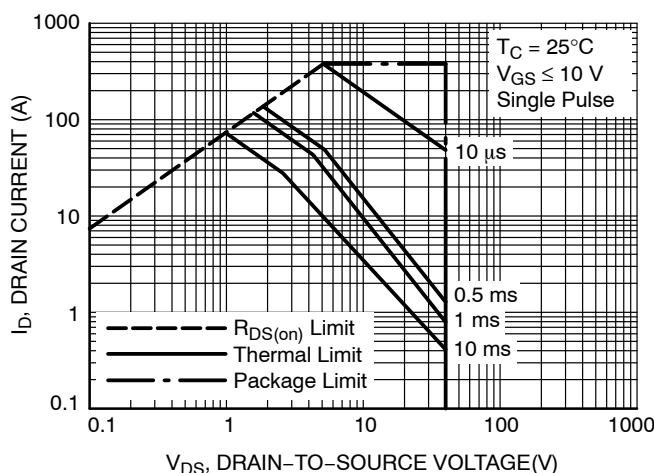


Figure 11. Maximum Rated Forward Biased Safe Operating Area

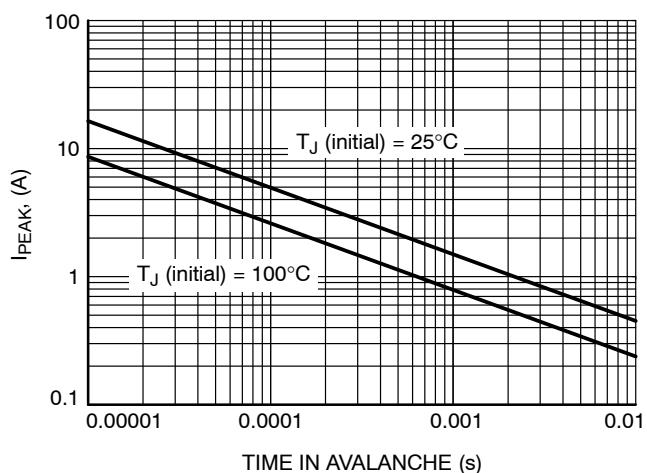
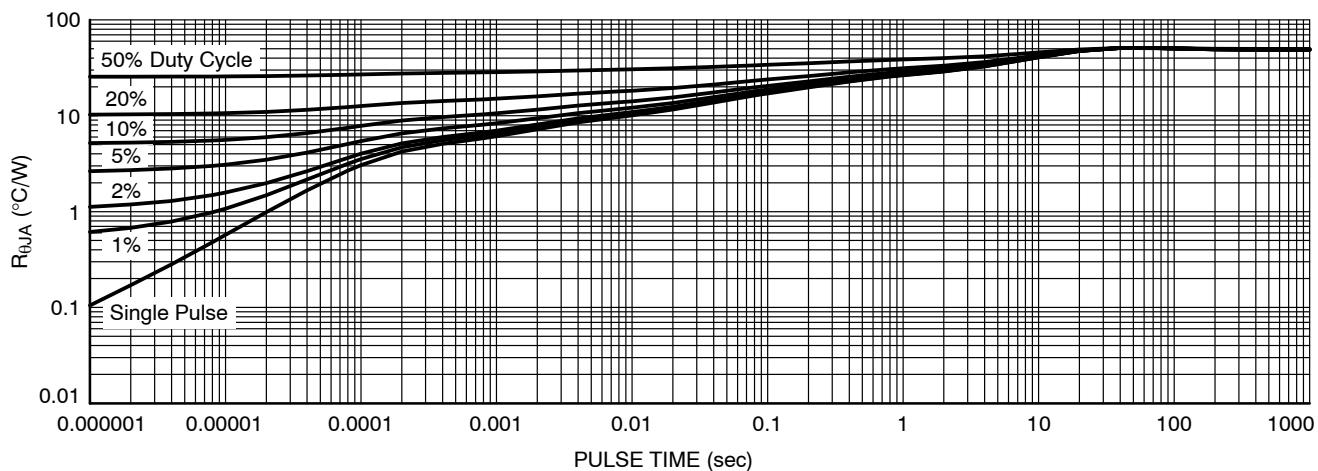


Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS**Figure 13. Thermal Characteristics****DEVICE ORDERING INFORMATION**

Device	Marking	Package	Shipping [†]
NVMFD5C478NT1G	5C478N	DFN8 (Pb-Free)	1500 / Tape & Reel
NVMFD5C478NWFT1G	478NWF	DFN8 (Pb-Free)	1500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



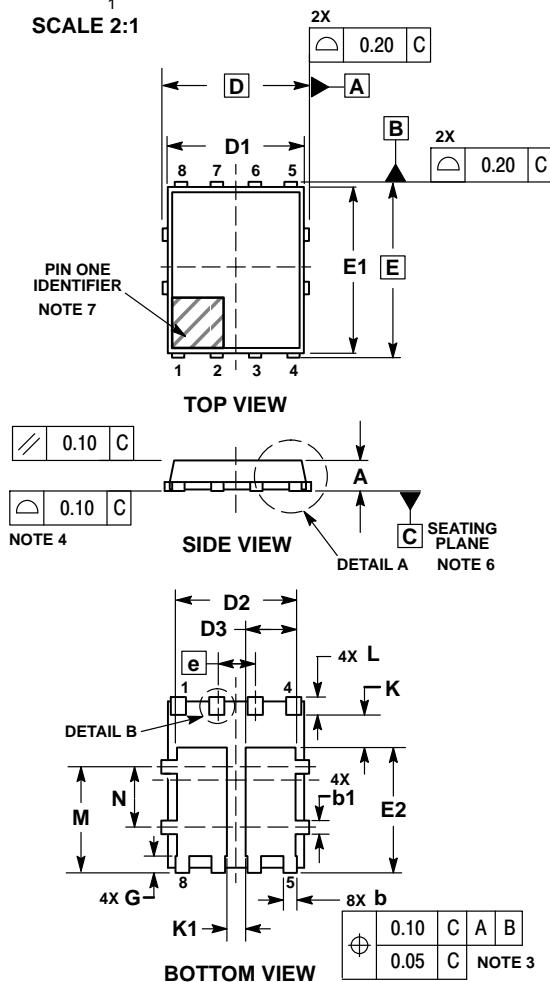
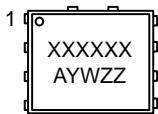
SCALE 2:1

DFN8 5x6, 1.27P Dual Flag (SO8FL-Dual)

CASE 506BT

ISSUE F

DATE 23 NOV 2021

GENERIC
MARKING DIAGRAM*

XXXXXX = Specific Device Code

A = Assembly Location

Y = Year

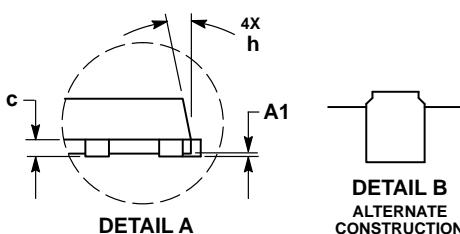
W = Work Week

ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

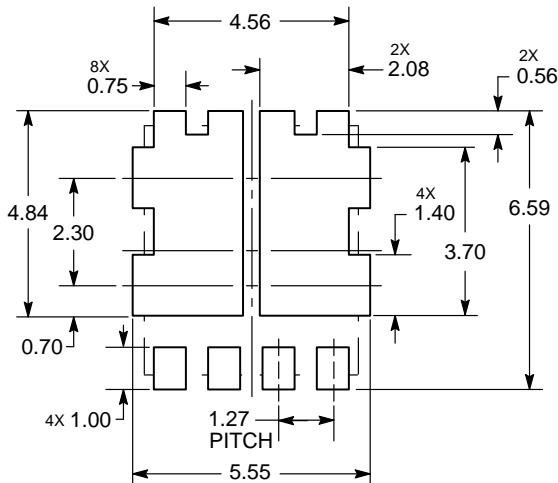
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. PROFILE TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. A VISUAL INDICATOR FOR PIN 1 MUST BE LOCATED IN THIS AREA.



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	—	1.10
A1	—	—	0.05
b	0.33	0.42	0.51
b1	0.33	0.42	0.51
c	0.20	—	0.33
D	5.15 BSC	—	—
D1	4.70	4.90	5.10
D2	3.90	4.10	4.30
D3	1.50	1.70	1.90
E	6.15 BSC	—	—
E1	5.70	5.90	6.10
E2	3.90	4.15	4.40
e	1.27 BSC	—	—
G	0.45	0.55	0.65
h	—	—	12°
K	0.51	—	—
K1	0.56	—	—
L	0.48	0.61	0.71
M	3.25	3.50	3.75
N	1.80	2.00	2.20

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN8 5X6, 1.27P DUAL FLAG (SO8FL-DUAL)	PAGE 1 OF 1

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