

Thyristor/Thyristor, 160 A (INT-A-PAK Power Modules)


INT-A-PAK

**RoHS
COMPLIANT**

FEATURES

- High voltage
- Electrically isolated by DBC ceramic (Al_2O_3)
- 3500 V_{RMS} isolating voltage
- Industrial standard package
- High surge capability
- Glass passivated chips
- Modules uses high voltage power thyristor/diodes in three basic configurations
- Simple mounting
- UL approved file E78996 
- Designed and qualified for multiple level
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- DC motor control and drives
- Battery charges
- Welders
- Power converters
- Lighting control
- Heat and temperature control

PRIMARY CHARACTERISTICS	
$I_{\text{T(AV)}}$	160 A
Type	Modules - thyristor, standard
Package	INT-A-PAK

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{\text{T(AV)}}$	85 °C	160	A
$I_{\text{T(RMS)}}$		355	
I_{TSM}	50 Hz	4870	
	60 Hz	5100	
I^2t	50 Hz	119	kA ² s
	60 Hz	108	
$I^2\sqrt{t}$		1190	kA ² √s
V_{RRM}	Range	1200, 1600	V
T_{J}	Range	-40 to +125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	$V_{\text{RRM}}/V_{\text{DRM}}$, MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	$V_{\text{RSM}}/V_{\text{DSM}}$, MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	$I_{\text{RRM}}/I_{\text{DRM}}$ AT 125 °C mA
VS-VSK.162	12	1200	1300	50
	16	1600	1700	



ON-STATE CONDUCTION				
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° conduction, half sine wave		160
				85
Maximum RMS on-state current	$I_{T(RMS)}$	As AC switch		355
Maximum peak, one-cycle on-state, non-repetitive surge current	I_{TSM}	t = 10 ms	No voltage reappplied	4870
		t = 8.3 ms	No voltage reappplied	5100
		t = 10 ms	100 % V_{RRM} reappplied	4100
		t = 8.3 ms	100 % V_{RRM} reappplied	4300
Maximum I^2t for fusing	I^2t	t = 10 ms	No voltage reappplied	119
		t = 8.3 ms	No voltage reappplied	108
		t = 10 ms	100 % V_{RRM} reappplied	84
		t = 8.3 ms	100 % V_{RRM} reappplied	76.7
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 ms to 10 ms, no voltage reappplied		1190
Low level value of threshold voltage	$V_{T(TO)1}$	$(16.7 \% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, T_J maximum		0.8
High level value of threshold voltage	$V_{T(TO)2}$	$(I > \pi \times I_{T(AV)})$, T_J maximum		0.98
Low level value on-state slope resistance	r_{t1}	$(16.7 \% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, T_J maximum		1.67
High level value on-state slope resistance	r_{t2}	$(I > \pi \times I_{T(AV)})$, T_J maximum		1.38
Maximum on-state voltage drop	V_{TM}	$I_{TM} = \pi \times I_{T(AV)}$, $T_J = 25^\circ\text{C}$, 180° conduction		1.54
Maximum forward voltage drop	V_{FM}	$I_{TM} = \pi \times I_{T(AV)}$, $T_J = 25^\circ\text{C}$, 180° conduction		1.54
Maximum holding current	I_H	Anode supply = 6 V initial $I_T = 30$ A, $T_J = 25^\circ\text{C}$		200
Maximum latching current	I_L	Anode supply = 6 V resistive load = 1 Ω Gate pulse: 10 V, 100 μs , $T_J = 25^\circ\text{C}$		400

SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Typical delay time	t_{gd}	$T_J = 25\text{ }^{\circ}\text{C}$	Gate current = 1 A, $dI_g/dt = 1\text{ A}/\mu\text{s}$ $V_d = 0.67\text{ \% }V_{\text{DRM}}$	1	μs
Typical rise time	t_{gr}			2	
Typical turn-off time	t_q	$I_{\text{TM}} = 300\text{ A}$, $-dI/dt = 15\text{ A}/\mu\text{s}$; $T_J = T_J$ maximum $V_R = 50\text{ V}$; $dV/dt = 20\text{ V}/\mu\text{s}$; gate 0 V, $100\text{ }\Omega$		50 to 200	

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES
Maximum peak reverse and off-state leakage current	I_{RRM} , I_{DRM}	$T_J = 125^\circ\text{C}$		50
RMS insulation voltage	V_{INS}	50 Hz, circuit to base, all terminals shorted, t = 1 s		3500
Critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, exponential to 67 % rated V_{DRM}		1000



TRIGGERING						
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS	
Maximum peak gate power	P _{GM}	t _p ≤ 5 ms, T _J = T _J maximum		12	W	
Maximum average gate power	P _{G(AV)}	f = 50 Hz, T _J = T _J maximum		3		
Maximum peak gate current	I _{GM}	t _p ≤ 5 ms, T _J = T _J maximum		3	A	
Maximum peak negative gate voltage	- V _{GT}			10	V	
Maximum required DC gate voltage to trigger	V _{GT}	T _J = - 40 °C	Anode supply = 6 V, resistive load; R _a = 1 Ω	4		
		T _J = 25 °C		2.5		
		T _J = T _J maximum		1.7		
Maximum required DC gate current to trigger	I _{GT}	T _J = - 40 °C		270	mA	
		T _J = 25 °C		150		
		T _J = T _J maximum		80		
Maximum gate voltage that will not trigger	V _{GD}	T _J = T _J maximum, rated V _{DRM} applied		0.3	V	
Maximum gate current that will not trigger	I _{GD}			10	mA	
Maximum rate of rise of turned-on current	dI/dt	T _J = T _J maximum, I _{TM} = 400 A rated V _{DRM} applied		300	A/μs	

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction operating temperature range	T_J		-40 to +125	$^\circ\text{C}$
Maximum storage temperature range	T_{Stg}		-40 to +150	
Maximum thermal resistance, junction to case per junction	R_{thJC}	DC operation	0.16	K/W
Maximum thermal resistance, case to heat sink per module	R_{thCS}	Mounting surface, smooth, flat and greased	0.05	
Mounting torque $\pm 10\%$	IAP to heat sink busbar to IAP	A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound. Lubricated threads.	4 to 6	Nm
Approximate weight			200	g
			7.1	oz.
Case style			INT-A-PAK	

ΔR CONDUCTION PER JUNCTION											
DEVICES	SINUSOIDAL CONDUCTION AT T _J MAXIMUM					RECTANGULAR CONDUCTION AT T _J MAXIMUM					UNITS
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
VS-VSK.162	0.0030	0.0031	0.0032	0.0033	0.0034	0.0029	0.0036	0.0039	0.0041	0.0040	K/W

Note

- Table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

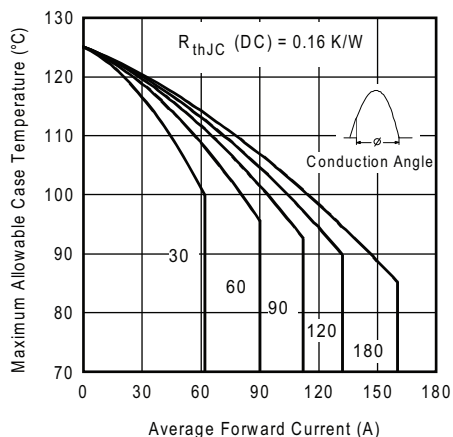


Fig. 1 - Current Ratings Characteristics

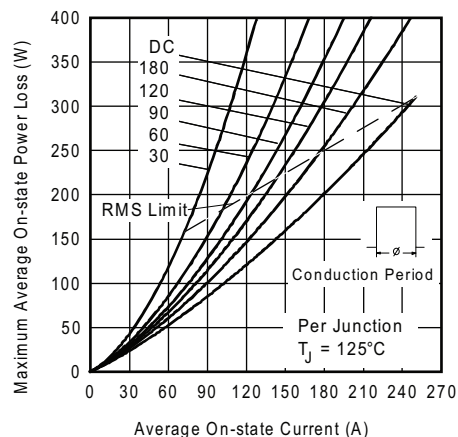


Fig. 4 - On-State Power Loss Characteristics

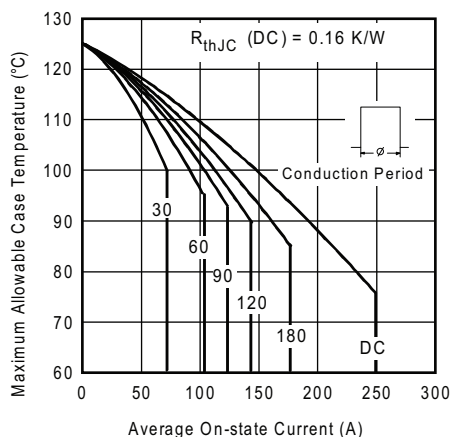


Fig. 2 - Current Ratings Characteristics

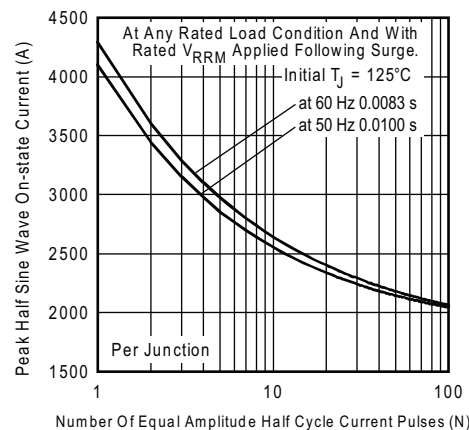


Fig. 5 - Maximum Non-Repetitive Surge Current

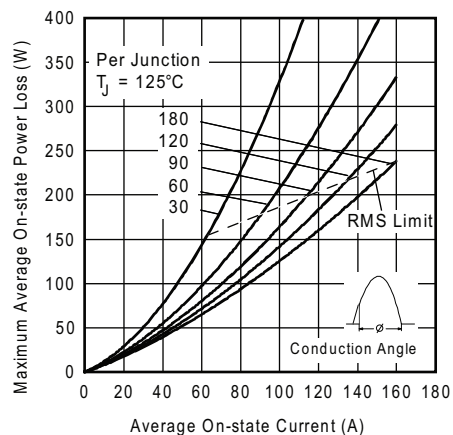


Fig. 3 - On-State Power Loss Characteristics

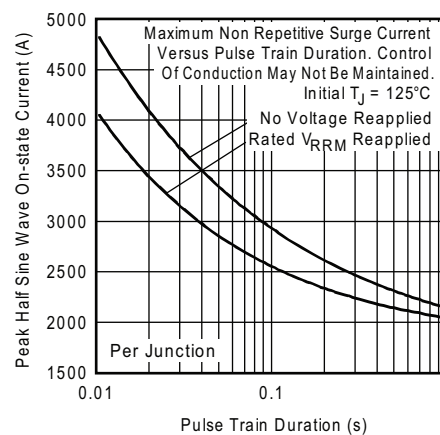


Fig. 6 - Maximum Non-Repetitive Surge Current

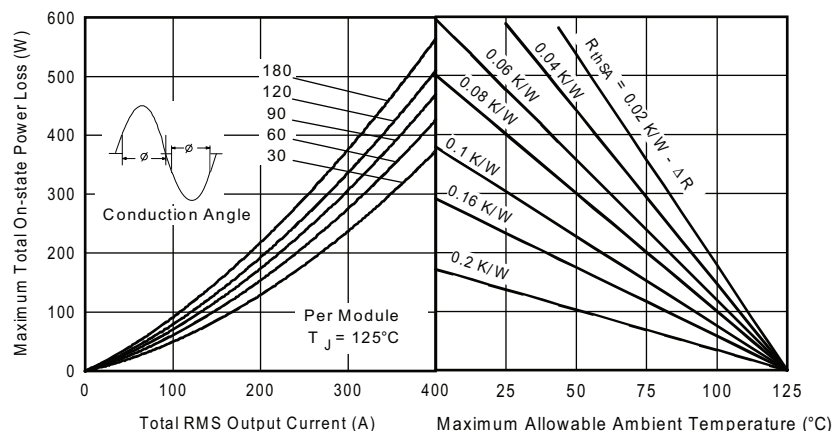


Fig. 7 - On-State Power Loss Characteristics

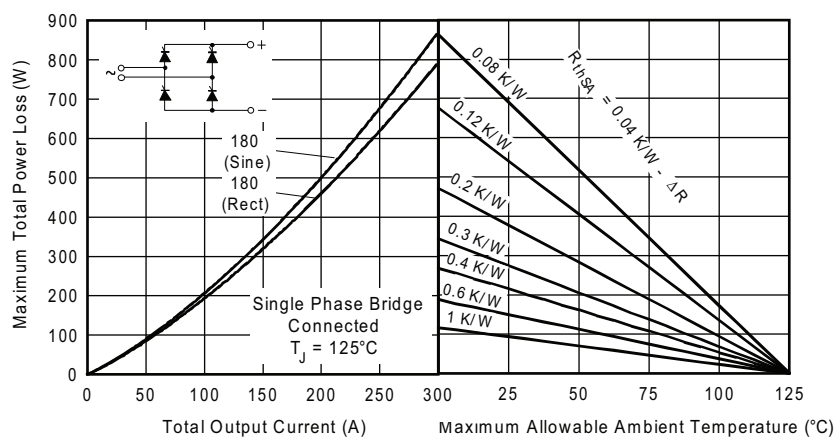


Fig. 8 - On-State Power Loss Characteristics

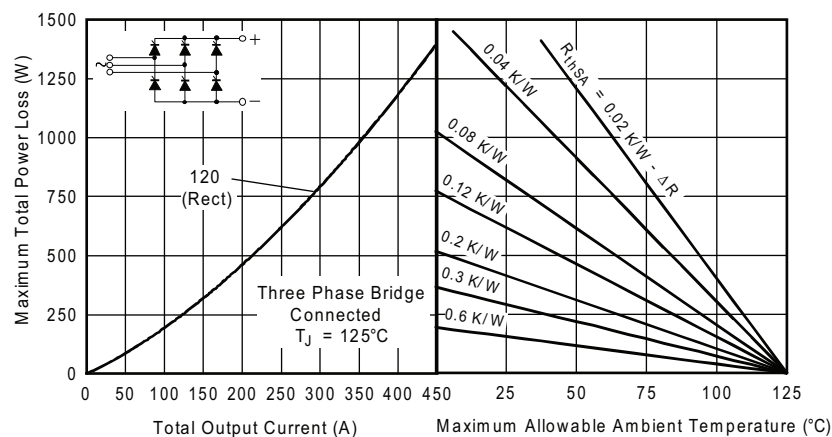


Fig. 9 - On-State Power Loss Characteristics

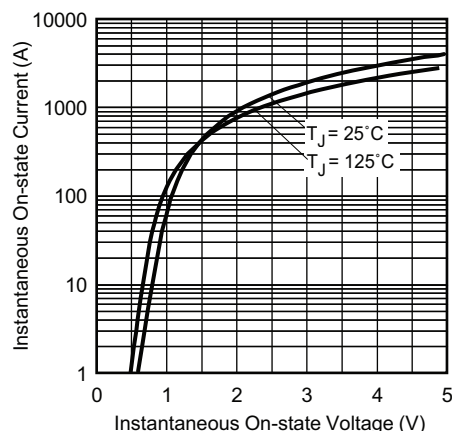


Fig. 10 - On-State Voltage Drop Characteristics

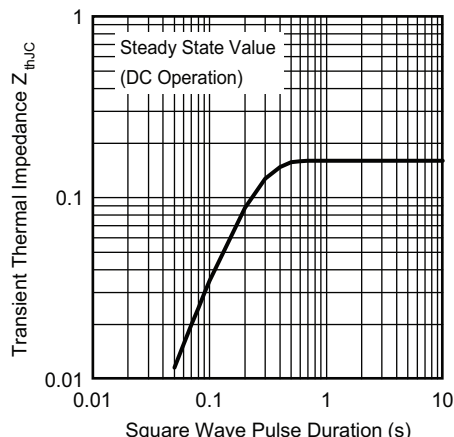


Fig. 11 - Thermal Impedance Z_{thJC} Characteristics

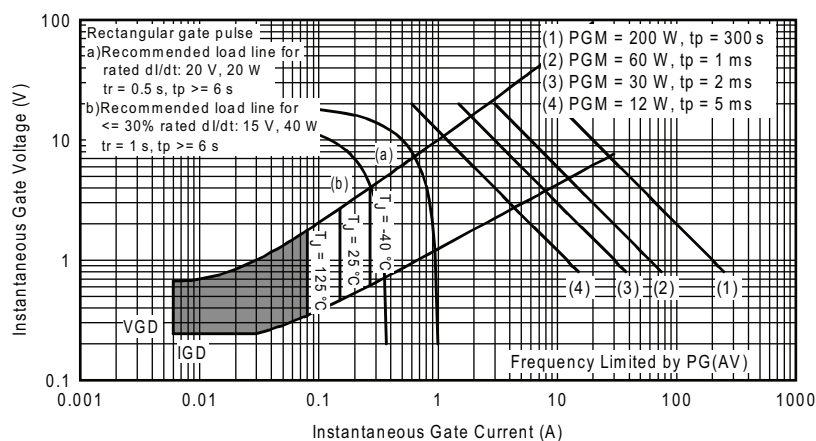


Fig. 12 - Gate Characteristics

ORDERING INFORMATION TABLE

Device code	VS-VS	KU	162	16	PbF
	1	2	3	4	5
1	Vishay Semiconductors product				
2	Circuit configuration				
3	Current rating: $I_{T(AV)}$				
4	Voltage code x 100 = V_{RRM}				
5	PbF = Lead (Pb)-free				

Note

- To order the optional hardware go to www.vishay.com/doc?95172



CIRCUIT CONFIGURATION		
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
Two SCRs common cathodes	U	VSKU 1 2 3 K1 G1 K2 G2 (1) (2) (3) G1 K1 K2 G2
Two SCRs common anodes	V	VSKV 1 2 3 K1 G1 K2 G2 (1) (2) (3) G1 K1 K2 G2

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95067

DIMENSIONS in millimeters (inches)





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