

MOSFET

OptiMOS™ Power-Transistor, 60 V

Features

- Dual-side cooled package with lowest Junction-top thermal resistance
- 175°C rated
- Optimized for high performance SMPS, e.g. sync. rec.
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

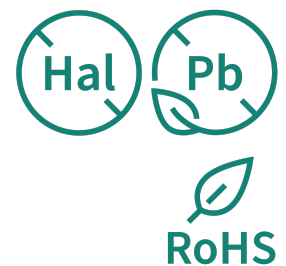
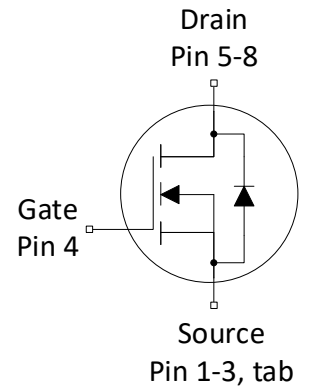
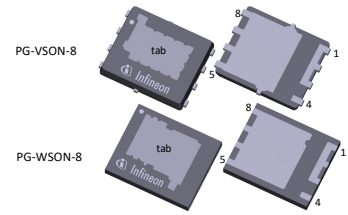
Product validation

Qualified according to relevant JEDEC tests.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	2.8	mΩ
I_D	137	A
Q_{oss}	43	nC
$Q_G(0..10V)$	37	nC

PG-VSON-8 / PG-WSON-8



Part number	Package	Marking	Related links
BSC028N06NSSC	PG-VSON-8 / PG-WSON-8	028N06SC	-



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1 Maximum ratings

at $T_j=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	137	A	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$
				97		$V_{GS}=10\text{ V}, T_C=100\text{ °C}$
				24		$V_{GS}=10\text{ V}, T_C=25\text{ °C}, R_{thJA}=50\text{ K/W}^2)$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	548	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	100	mJ	$I_D=50\text{ A}, R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	100	W	$T_C=25\text{ °C}$
				3.0		$T_A=25\text{ °C}, R_{thJA}=50\text{ K/W}^2)$
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}		0.9	1.5	K/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	0.7	1.4		
Device on PCB, 6 cm ² cooling area ⁵⁾	R_{thJA}		-	50		

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.1	2.8	3.3	V	$V_{DS}=V_{GS}$, $I_D=50\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.5	1	μA	$V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$
			10	100		$V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.3	2.8	m Ω	$V_{GS}=10\text{ V}$, $I_D=50\text{ A}$
			3.3	4.2		$V_{GS}=6\text{ V}$, $I_D=12.5\text{ A}$
Gate resistance	R_G	-	1.3	1.95	Ω	-
Transconductance	g_{fs}	50	100	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=50\text{ A}$

Table 5 Dynamic characteristics ⁶⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	2025	2700	3375	pF	$V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	495	660	825		
Reverse transfer capacitance	C_{rss}	8.5	28	56		
Turn-on delay time	$t_{d(on)}$	-	11	22	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=3\text{ }\Omega$
Rise time	t_r		38	57		
Turn-off delay time	$t_{d(off)}$		19	38		
Fall time	t_f		8	16		

⁶⁾ Defined by design. Not subject to production test

Table 6 Gate charge characteristics ⁷⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	9	12	16.5	nC	$V_{DD}=30\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	6	8	11	nC	
Gate to drain charge	Q_{gd}	5	7	10.3	nC	
Switching charge	Q_{sw}	8	12	17	nC	
Gate charge total	Q_g	31	37	49	nC	
Gate plateau voltage	$V_{plateau}$	4.0	4.6	5.2	V	
Gate charge total, sync. FET	$Q_{g(sync)}$	27	33	43	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge	Q_{oss}	32	43	54	nC	$V_{DD}=30\text{ V}$, $V_{GS}=0\text{ V}$

⁷⁾ See "Gate charge waveforms" for parameter definition. Defined by design, not subject to production test

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	77	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$			548		
Diode forward voltage	V_{SD}	-	0.88	1.2	V	$V_{GS}=0\text{ V}$, $I_F=50\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery time ⁸⁾	t_{rr}	14	35	56	ns	$V_R=30\text{ V}$, $I_F=50\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ⁸⁾	Q_{rr}		29	58	nC	

⁸⁾ Defined by design. Not subject to production test

4 Electrical characteristics diagrams

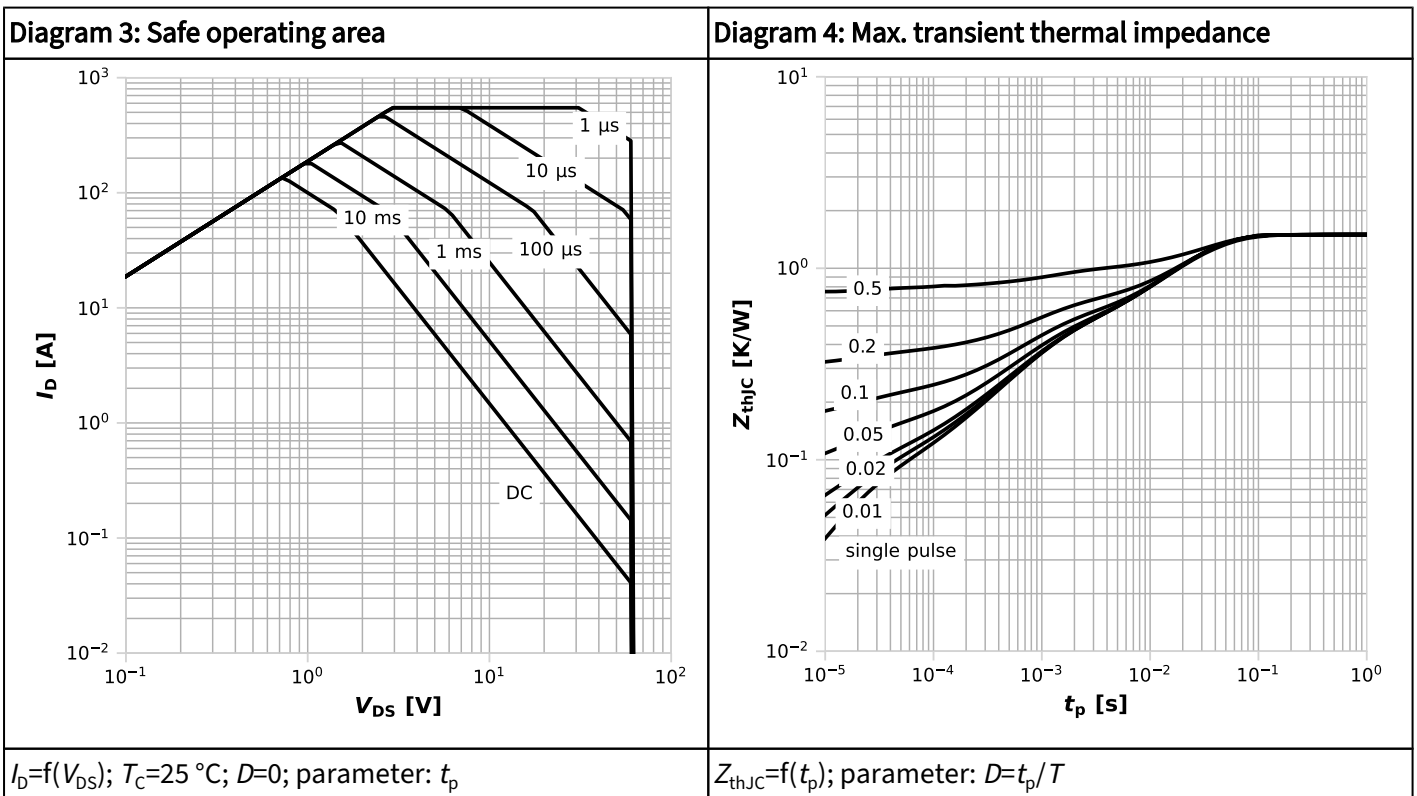
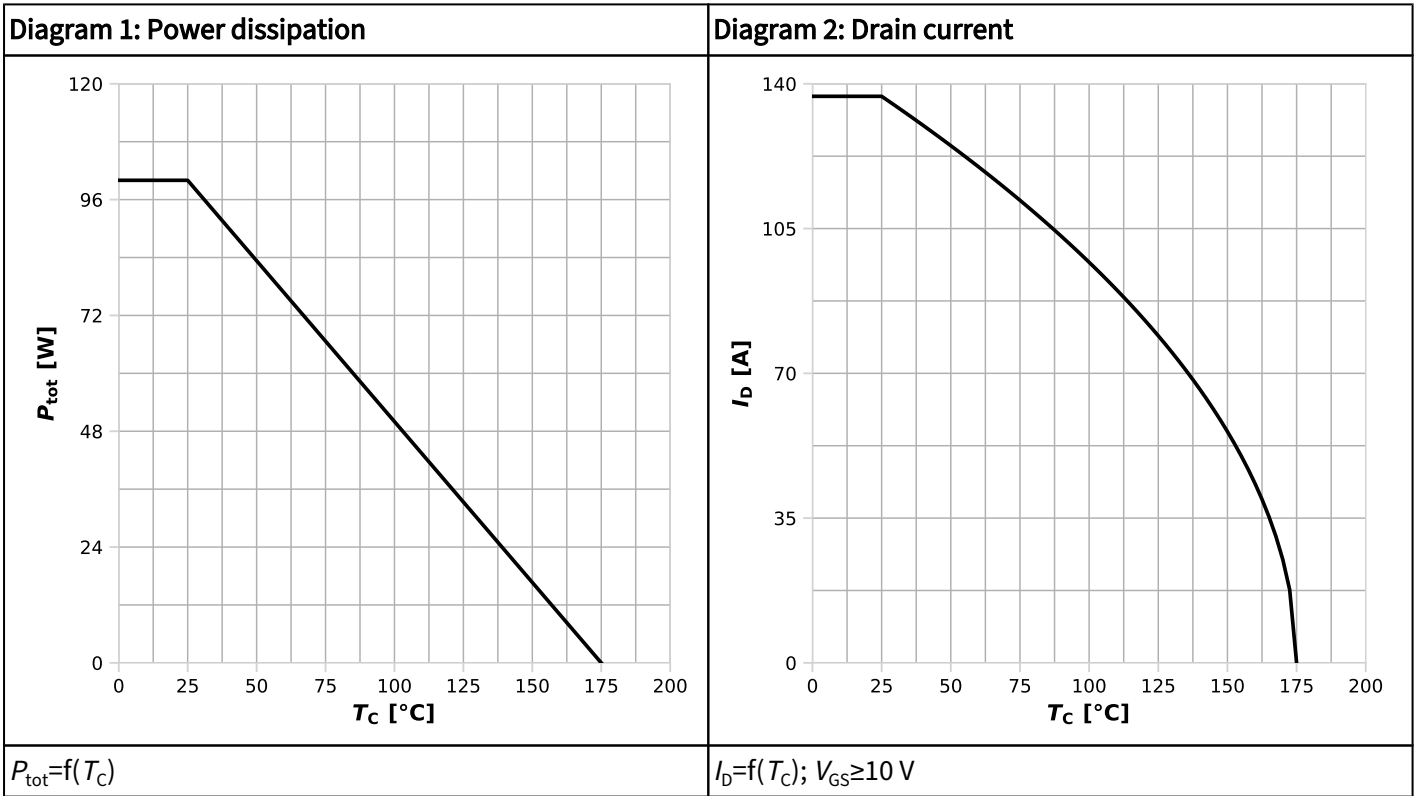
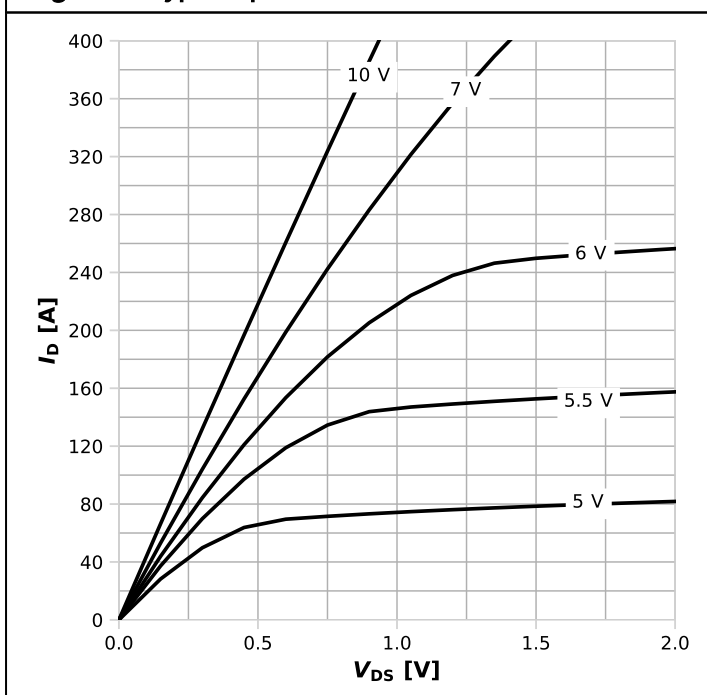
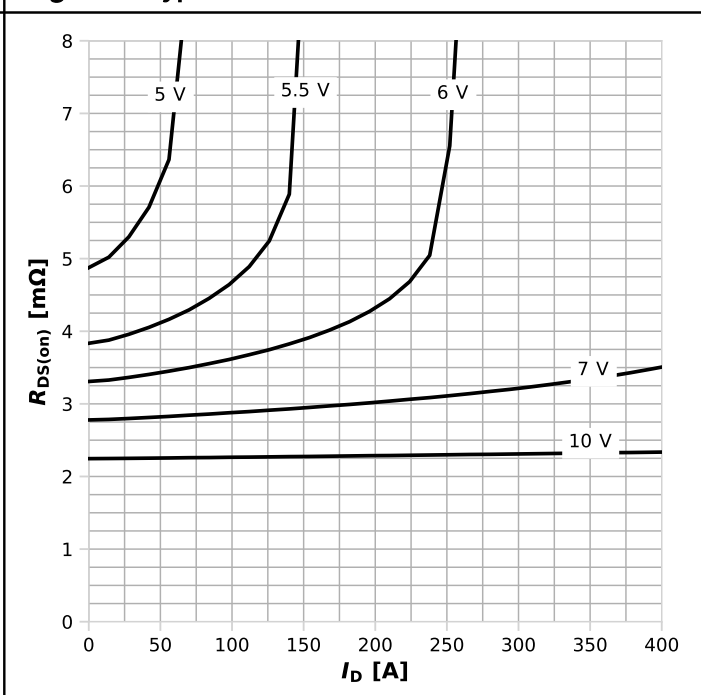


Diagram 5: Typ. output characteristics



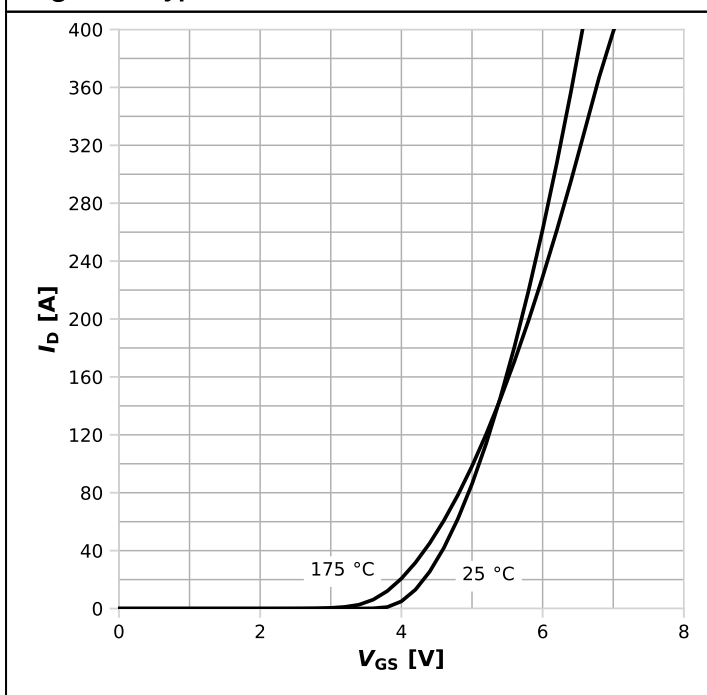
$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. drain-source on resistance



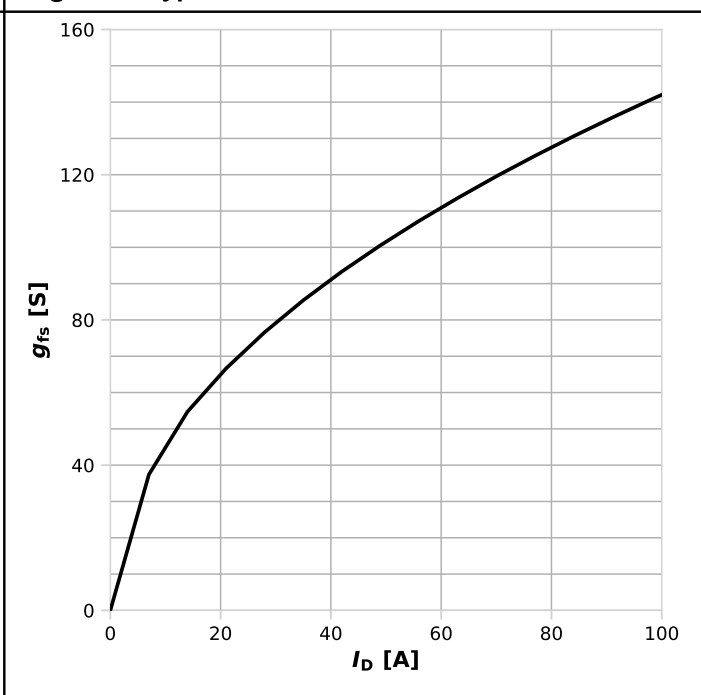
$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 7: Typ. transfer characteristics



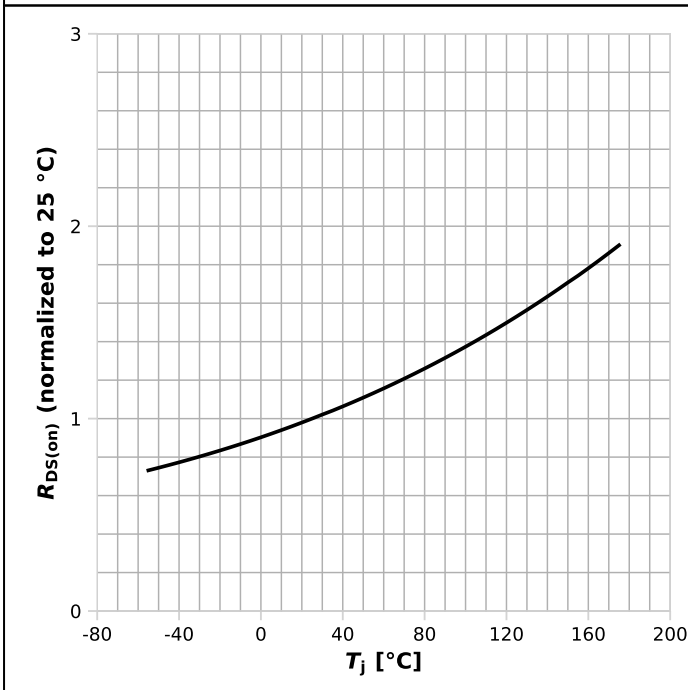
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}; \text{parameter: } T_j$

Diagram 8: Typ. forward transconductance



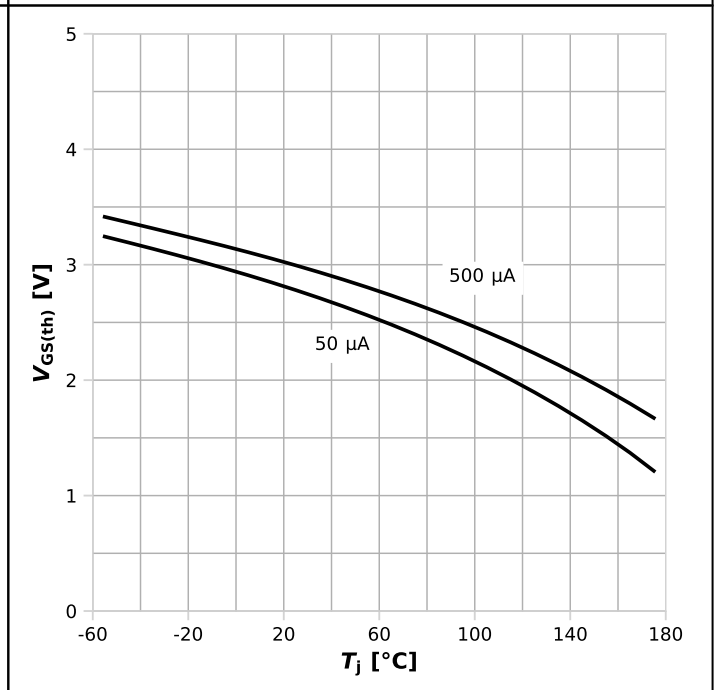
$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

Diagram 9: Drain-source on-state resistance



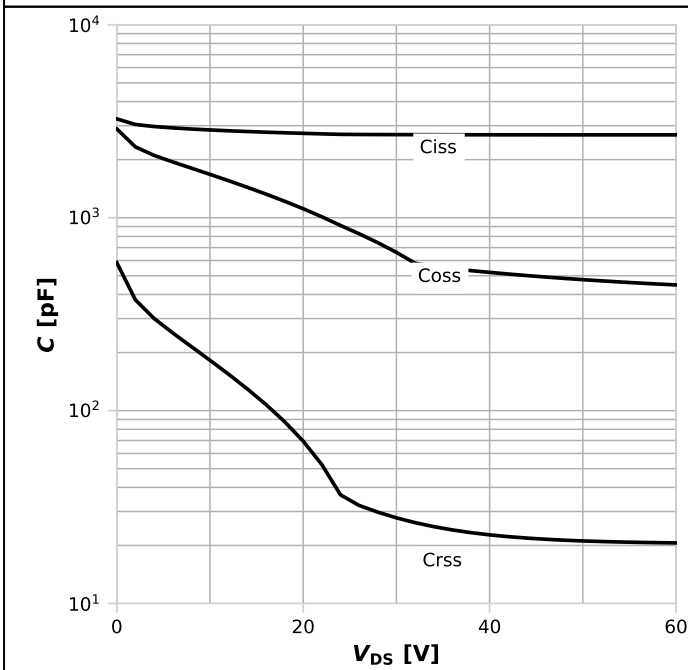
$R_{DS(on)}=f(T_j), I_D=50\text{ A}, V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



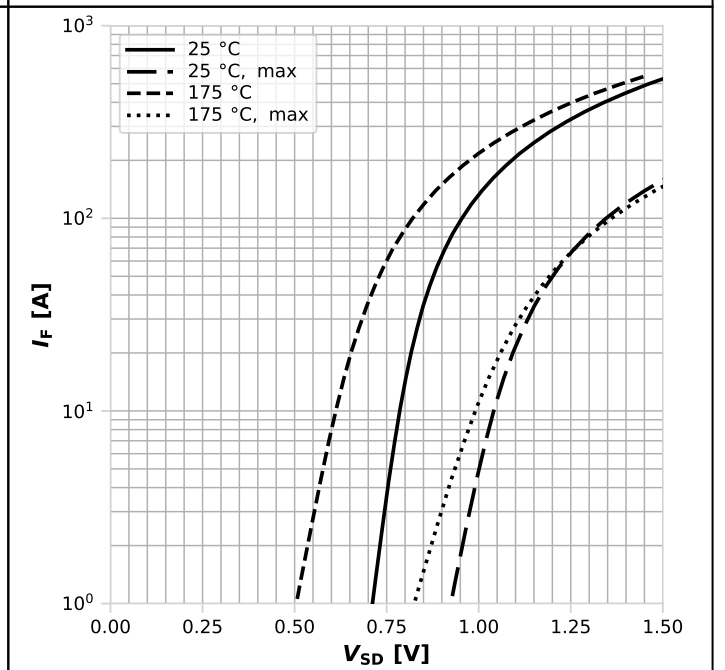
$V_{GS(th)}=f(T_j); V_{GS}=V_{DS}$

Diagram 11: Typ. capacitances



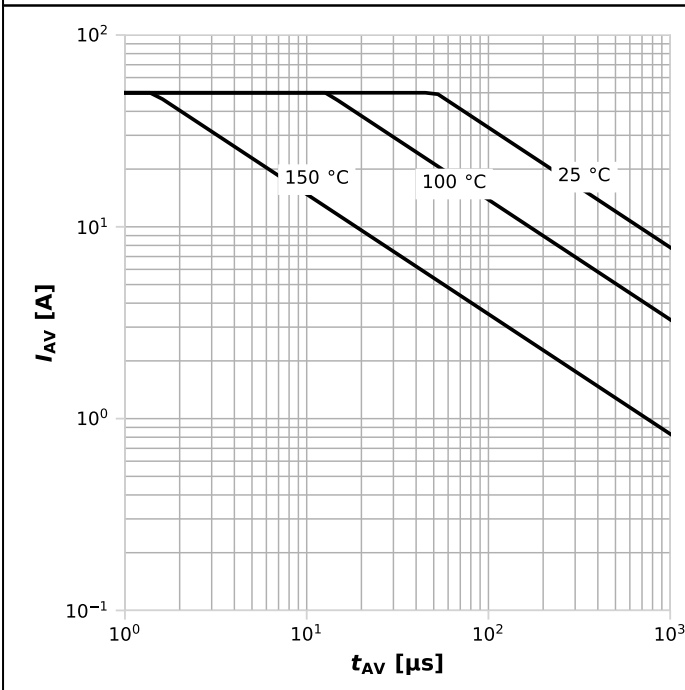
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

Diagram 12: Forward characteristics of reverse diode



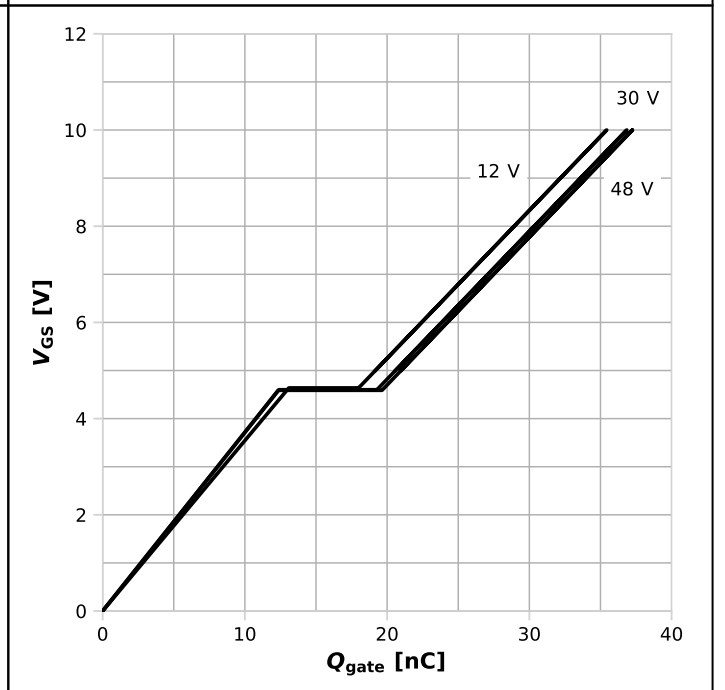
$I_F=f(V_{SD}); \text{parameter: } T_j$

Diagram 13: Avalanche characteristics



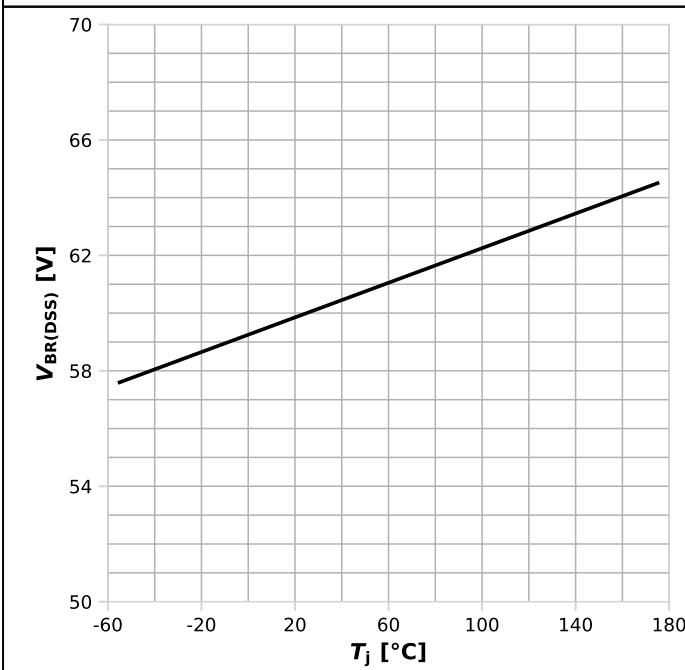
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



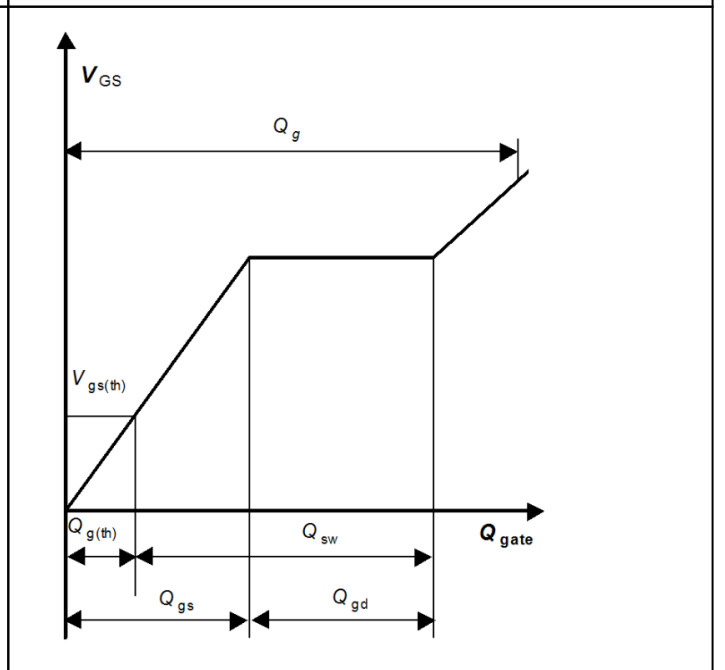
$V_{GS}=f(Q_{gate}); I_D=50 \text{ A pulsed}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



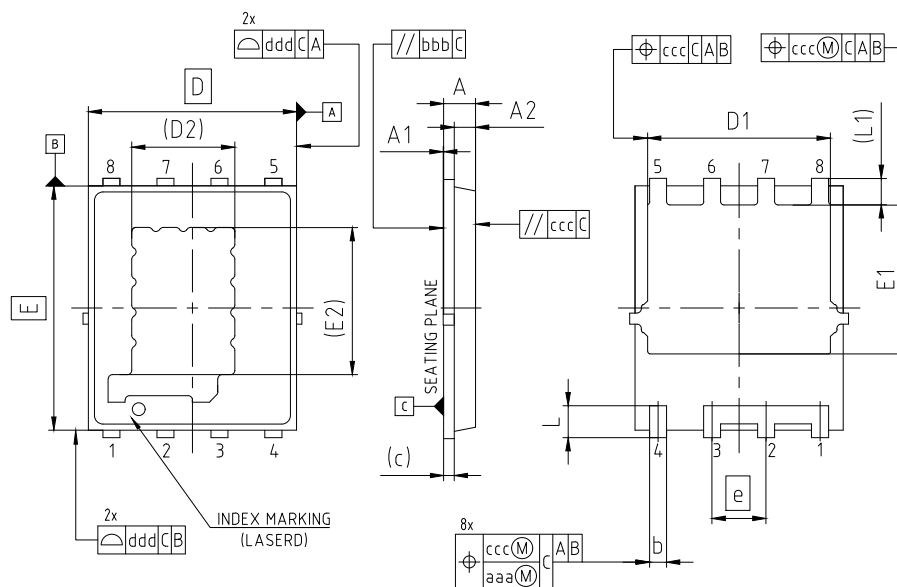
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Gate charge waveforms



-

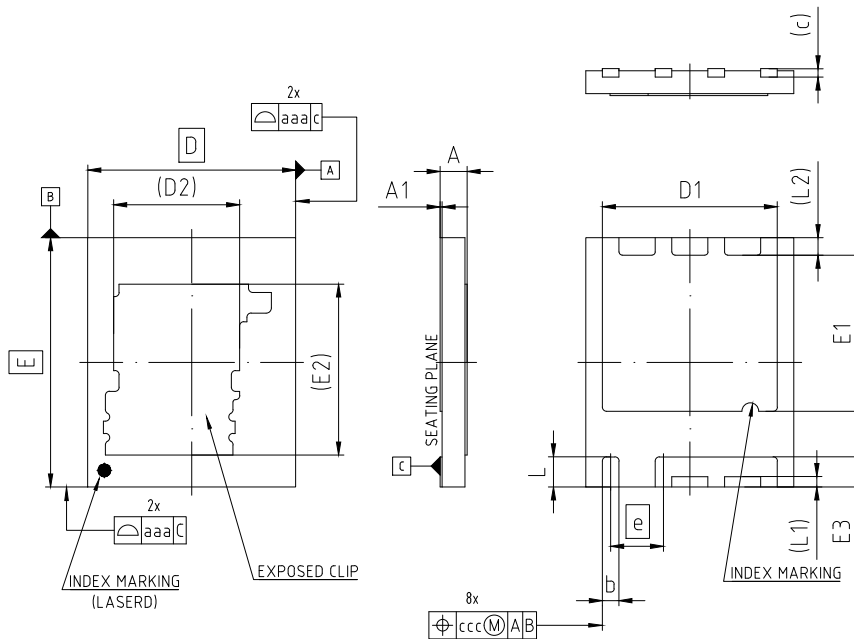
5 Package outlines



PACKAGE - GROUP NUMBER: PG-VSON-8-U01					
DIMENSIONS	MILLIMETERS		DIMENSIONS	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.65	0.85	e	1.27	
A1	0.00	0.05	L	0.70	0.90
A2	0.45	0.55	L1	0.52	0.72
b	0.35	0.55	aaa	0.05	
c		0.25	bbb	0.08	
D		4.90	ccc	0.10	
D1	4.20	4.40	ddd	0.15	
D2		2.43			
E		5.75			
E1	3.40	3.60			
E2		3.46			

NOTE: DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-VSON-8 / PG-WSON-8, dimensions in mm



PACKAGE - GROUP NUMBER: PG-WSN-8-U01					
DIMENSIONS	MILLIMETERS		DIMENSIONS	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.55	0.75	e	1.27	
A1	0.00	0.05	L	0.68	0.78
b	0.35	0.45	L1	0.25	
c	0.20		L2	0.42	
D	5.00		aaa	0.05	
D1	4.11	4.31	ccc	0.10	
D2	3.03				
E	6.00				
E1	3.66	3.86			
E2	4.11				
E3	0.63	0.83			

NOTE: DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 2 PG-VSON-8 / PG-WSN-8, dimensions in mm

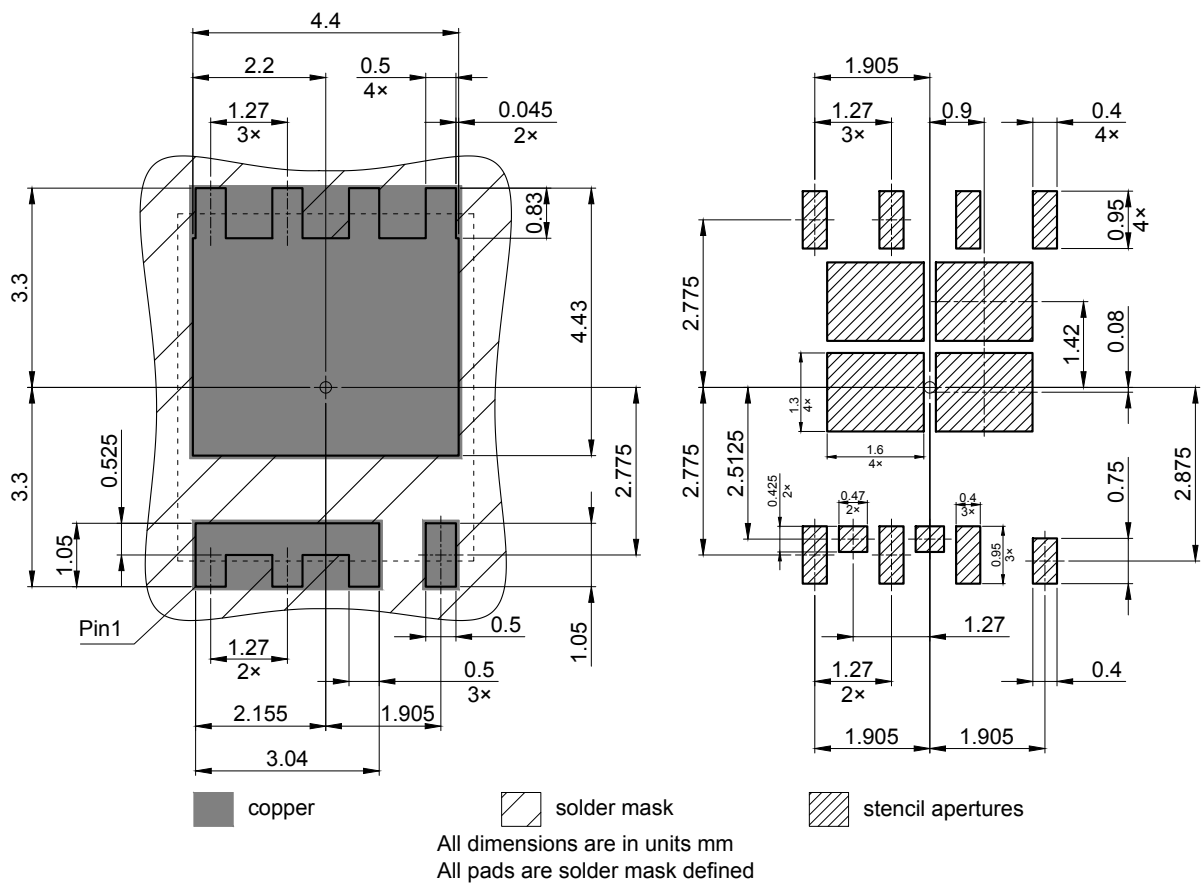
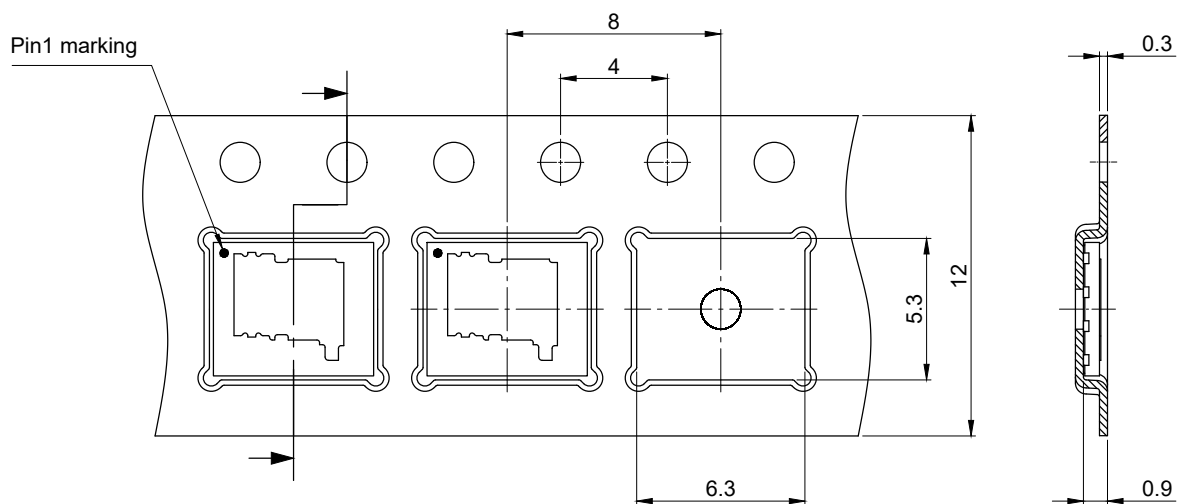


Figure 3 Footprint drawing PG-VSON-8 / PG-WSON-8, dimensions in mm



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 4 Packaging variant PG-VSON-8 / PG-WSON-8, dimensions in mm

Revision history

BSC028N06NSSC

Revision 2026-04-02, Rev. 2.4

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2019-11-19	Release of final version
2.1	2022-10-06	Update "Features
2.2	2025-05-27	Update package drawings
2.3	2025-12-17	Update switching symbol
2.4	2026-04-02	Update 3D image and schematics

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