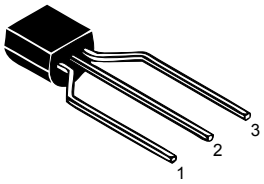
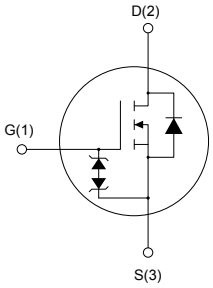
STQ1NK80ZR-AP

Datasheet

N-channel 800 V, 13 Ω typ., 0.3 A SuperMESH Power MOSFET in a TO-92 package



TO-92 ammopack



AM01476v1_noTAB

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STQ1NK80ZR-AP	800 V	16 Ω	0.3 A

- Extremely high dv/dt capability
- Gate charge minimized
- Improved ESD capability
- Zener-protected
- 100% avalanche tested

Applications

- Switching applications

Description

This high-voltage device is a Zener-protected N-channel Power MOSFET developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status link
STQ1NK80ZR-AP

Product summary	
Order code	STQ1NK80ZR-AP
Marking	Q1NK80ZR
Package	TO-92
Packing	Ammopack

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	800	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_L = 25 °C	0.3	A
	Drain current (continuous) at T_L = 100 °C	0.19	
I_{DM}(1)	Drain current (pulsed)	5	A
P_{TOT}	Total power dissipation at T_L = 25 °C	3	W
ESD	Gate-source human body model (R = 1.5 kΩ, C = 100 pF)	1	kV
dv/dt(2)	Peak diode recovery voltage slope	4.5	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 0.25 A, di/dt ≤ 200 A/µs, V_{DS} (peak) ≤ $V_{(BR)DSS}$, V_{DD} = 640 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance, junction-to-ambient	120	°C/W
R_{thJL}	Thermal resistance, junction-to-lead	40	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	1	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	50	mJ

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2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	800	-	-	V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 800 V	-	-	1	µA
		V_{GS} = 0 V, V_{DS} = 800 V, T_C = 125 °C(1)	-	-	50	
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V	-	-	±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3.0	3.8	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 0.5 A	-	13	16	Ω

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	160	-	pF
C_{oss}	Output capacitance		-	26	-	pF
C_{rss}	Reverse transfer capacitance		-	6.7	-	pF
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 to 640 V	-	9.5	-	pF
Q_g	Total gate charge	V_{DD} = 640, I_D = 1.1 A, V_{GS} = 0 to 10 V (see the Figure 14. Test circuit for gate charge behavior)	-	7.7	-	nC
Q_{gs}	Gate-source charge		-	1.4	-	nC
Qgd	Gate-drain charge		-	4.5	-	nC

1. *$C_{oss\ eq.}$ is defined as the constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 400 V, I_D = 0.55 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	7	-	ns
t_r	Rise time		-	23	-	ns
$t_{d(off)}$	Turn-off delay time		-	18	-	ns
t_f	Fall time		-	28	-	ns

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Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	0.3	A
I_{SDM}(1)	Source-drain current (pulsed)		-	-	5	A
V_{SD}(2)	Forward on voltage	I_{SD} = 1 A, V_{GS} = 0 V	-	-	1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 1.1 A, di/dt = 100 A/µs,	-	365	-	ns
Q_{rr}	Reverse recovery charge	V_{DD} = 50 V	-	802	-	nC
I_{RRM}	Reverse recovery current	(see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	4.4	-	A
t_{rr}	Reverse recovery time	I_{SD} = 1.1 A, di/dt = 100 A/µs,	-	389	-	ns
Q_{rr}	Reverse recovery charge	V_{DD} = 50 V, T_J = 150 °C	-	891	-	nC
I_{RRM}	Reverse recovery current	(see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	4.6	-	A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

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2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

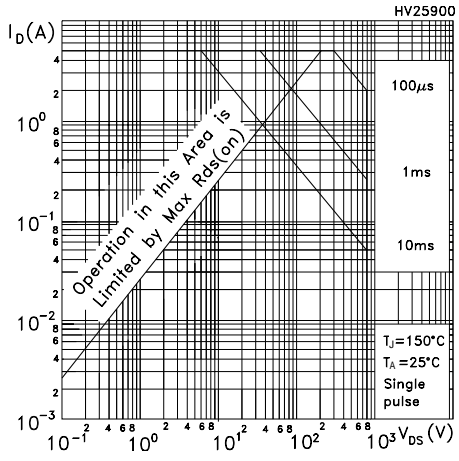


Figure 2. Normalized transient thermal impedance

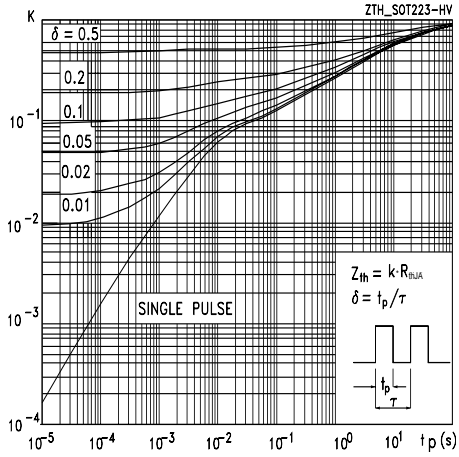


Figure 3. Typical output characteristics

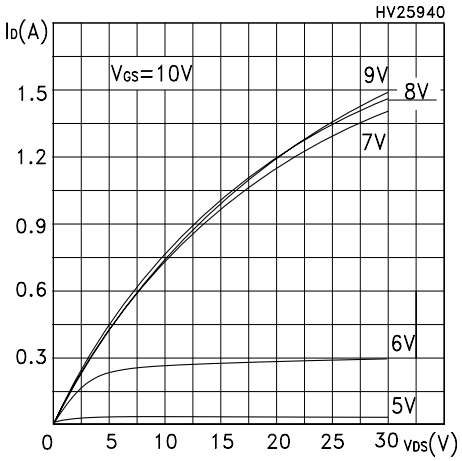


Figure 4. Typical transfer characteristics

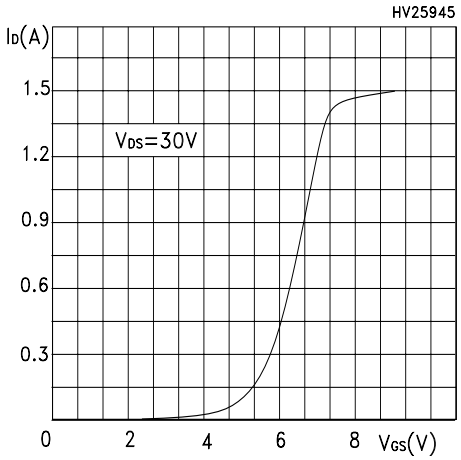


Figure 5. Typical gate charge characteristics

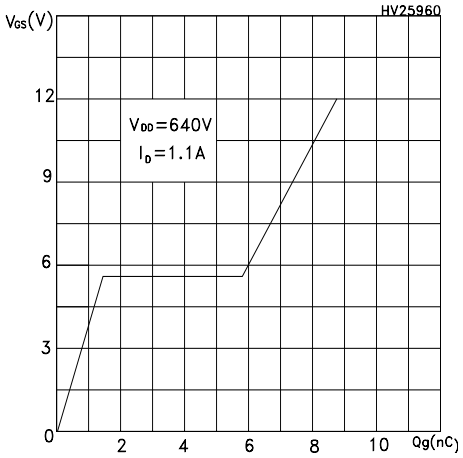
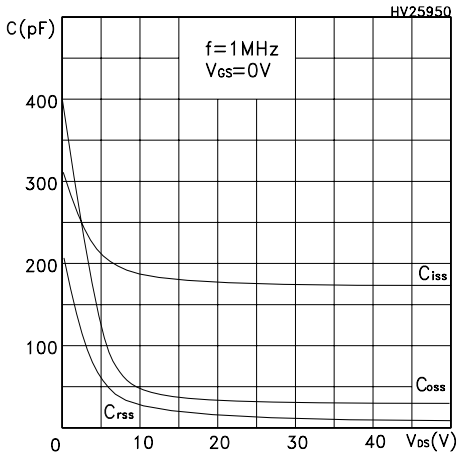


Figure 6. Typical capacitance characteristics



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Figure 7. Typical drain-source on-resistance

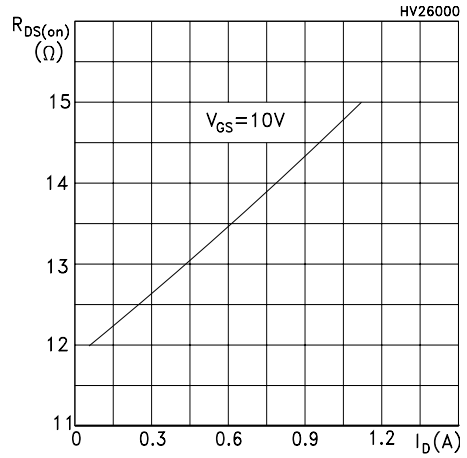


Figure 8. Normalized gate threshold vs temperature

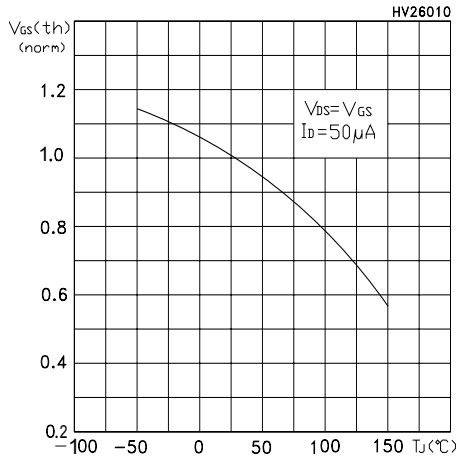


Figure 9. Normalized on-resistance vs temperature

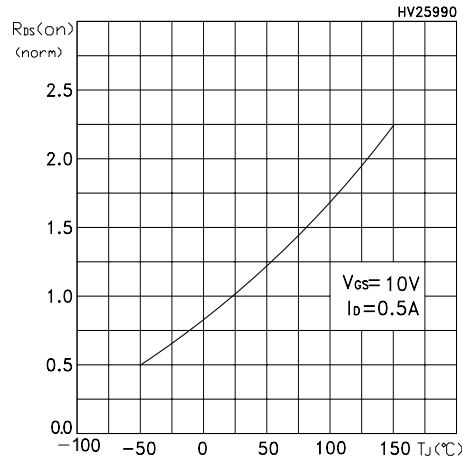


Figure 10. Typical reverse diode forward characteristics

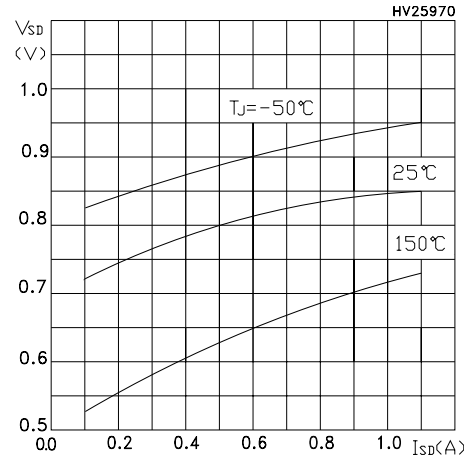


Figure 11. Normalized breakdown voltage vs temperature

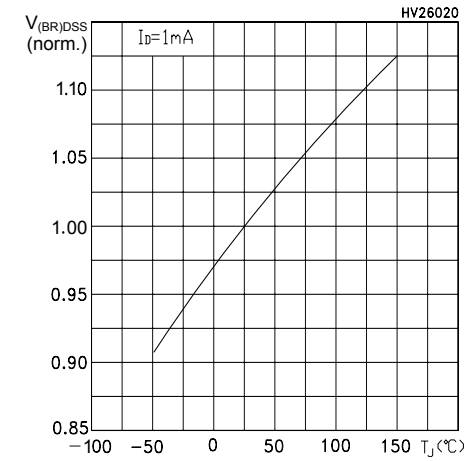
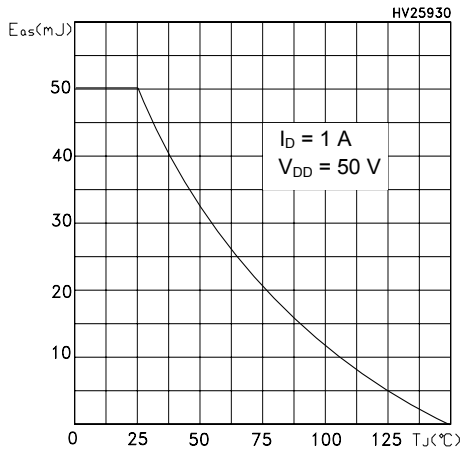


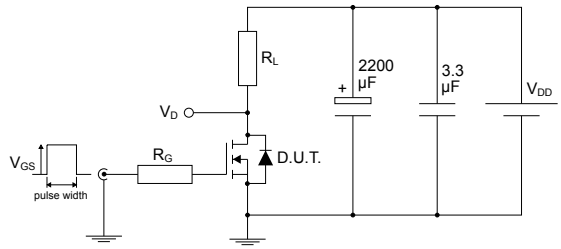
Figure 12. Maximum avalanche energy vs temperature



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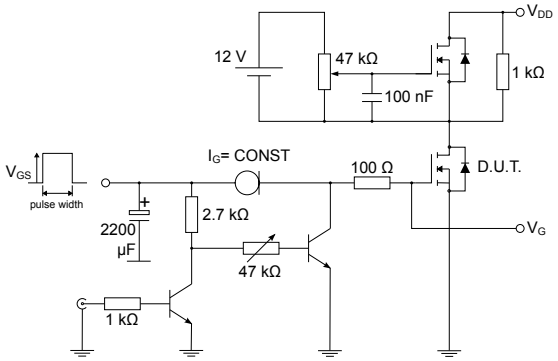
3 Test circuits

Figure 13. Test circuit for resistive load switching times



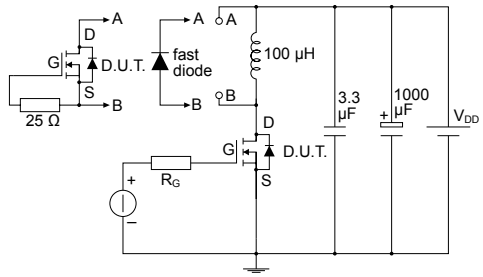
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Figure 14. Test circuit for gate charge behavior



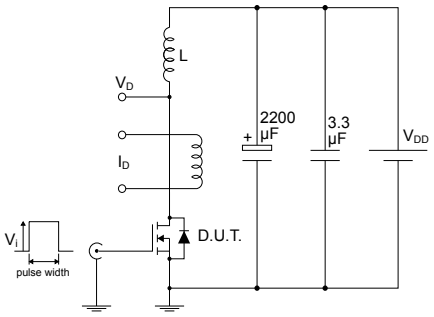
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Figure 15. Test circuit for inductive load switching and diode recovery times



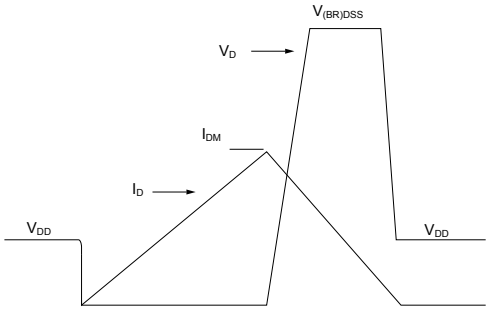
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Figure 16. Unclamped inductive load test circuit



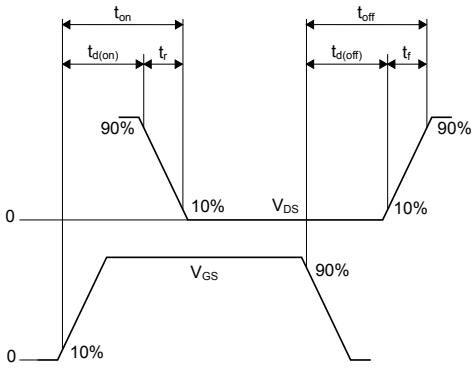
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Figure 17. Unclamped inductive waveform



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Figure 18. Switching time waveform



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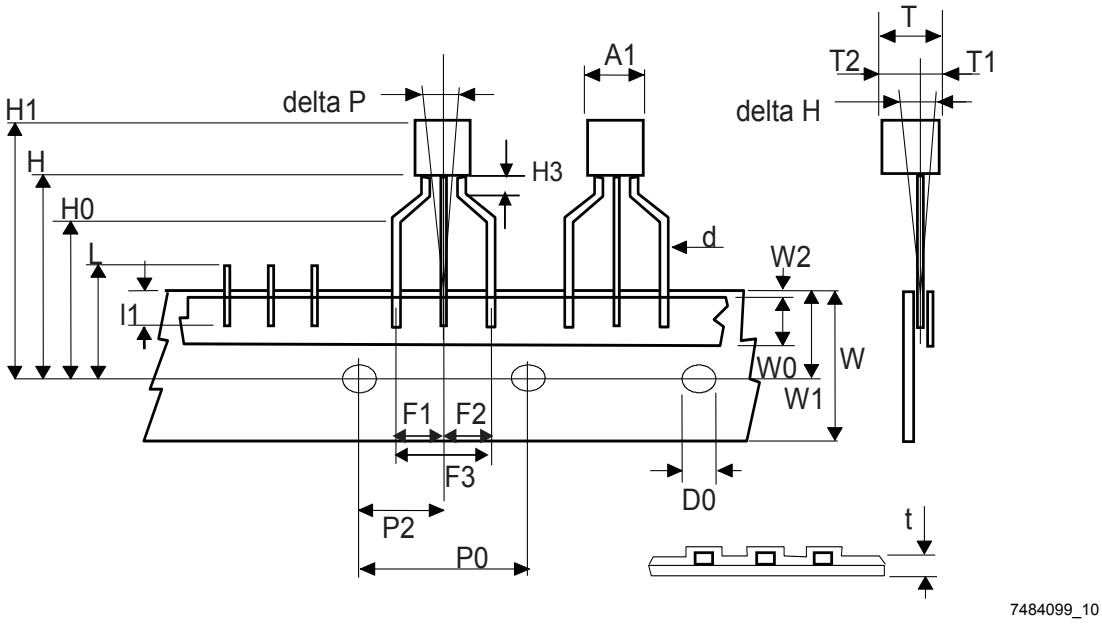
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-92 ammopack package information

Figure 19. TO-92 ammopack package outline



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Table 8. **TO-92 ammopack mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A1			4.80
T			3.80
T1			1.60
T2			2.30
d			0.48
P0	12.50	12.70	12.90
P2	5.65	6.35	7.05
F1, F2	2.40	2.54	2.94
F3	4.98	5.08	5.48
delta H	-2.00		2.00
W	17.50	18.00	19.00
W0	5.70	6.00	6.30
W1	8.50	9.00	9.25
W2			0.50
H	18.50		20.50
H0	15.50	16.00	16.50
H1			25.00
H3	0.50	1.00	2.00
D0	3.80	4.00	4.20
t			0.90
L			11.00
I1	3.00		
delta P	-1.00		1.00

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Revision history

Table 9. **Document revision history**

Date	Revision	Changes
24-Jul-2026	1	First release. Part number STQ1NK80ZR-AP previously included in datasheet DS14259.

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