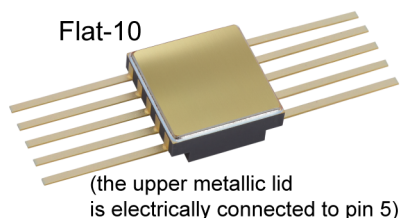


Rad-hard, 12-bit D/A converter



Product status link

[RHRDAC121](#)

Features

- 12-bit architecture
- Ensured monotonicity
- Rail-to-rail voltage output
- Power-on-reset to zero volt output
- Internal voltage reference
- SYNC interrupt facility
- 2.3 V to 3.6 V power supply range
- Power-down function
- Guaranteed over -55 °C to +125 °C ambient temperature
- Hermetic package
- 100 krad(Si) TID
- SEL-free up to 125 MeV.cm²/mg
- SMD: 5962R21208
- Mass: 0.42 g

Application

- Satellite equipment
- Telemetry
- Housekeeping

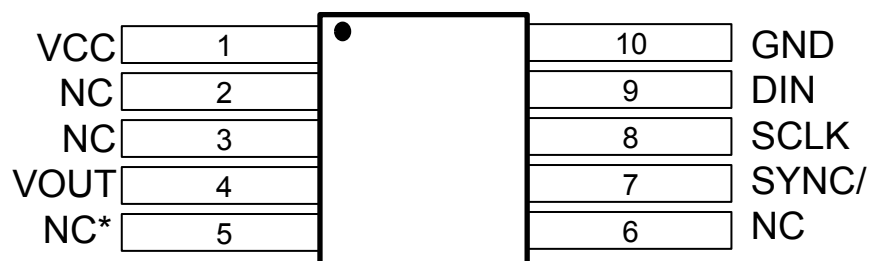
Description

The **RHRDAC121** is a 12-bit voltage-output digital-to-analog converter that can operate from 2.3 V to 3.6 V power supply drawing a very low current consumption, with an internal voltage referencing. The output features rail-to-rail swing and the three-wire serial interface operates at clock rates up to 20 MHz compatible with standard SPI.

The **RHRDAC121** comes in a hermetic ceramic Flat10-lead, and it can operate from -55 °C to +125 °C ambient temperature.

1 Functional description

Figure 1. Pin localization



*pin 5 is internally connected to the metallic upper lid,
 pin5 can be NC or it can be connected to ground to sink
 electronic charges

Figure 2. Block diagram

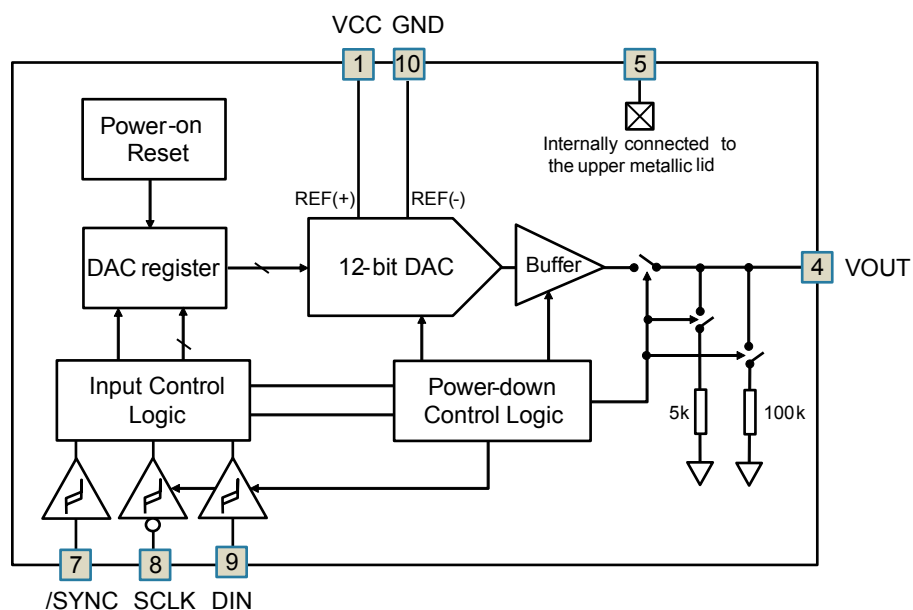


Table 1. Pin description

#	Name	Type	Description
1	Vcc	Supply	Power supply and reference input; must be decoupled to GND
2	NC	-	No connected, not internally connected to die
3	NC	-	No connected, not internally connected to die
4	VOUT	Output	Analog output voltage
5	NC	-	No connected, not internally connected to die, internally connected to the upper lid
6	NC	-	No connected, not internally connected to die
7	SYNC/	Input	Frame synchronization input for the data input. When this pin goes low, it enables the input shift register and data it is transferred on the falling edges of SCLK. The DAC is updated on the 16 th clock cycle unless SYNC/ is brought high before the 16 th clock, in which case the rising edge of SYNC acts as an interrupt and the write sequence is ignored by the DAC
8	SCLK	Input	Serial clock input; data is clocked into the input shift register on the falling edges of this pin
9	DIN	Input	Serial data input; data is clocked into the 16-bit shift register on the falling edges of SCLK after the fall of SYNC/
10	GND	-	Ground reference for the whole circuitry

2 Maximum ratings and operating conditions

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 2. Absolute maximum ratings

Symbol	Parameters	Value	Units
V _{CC} ⁽¹⁾	Maximum power supply between VCC and GND	-0.3 V to 4.8 V	V
V _I ⁽²⁾	Max. voltage on any pin vs. GND	-0.3 V to V _{CC} +0.3 V (and 4.8 V max.)	V
I _{in}	Max input current at any pin	±10	mA
T _{stg}	Maximum temperature storage	-65 to +150	°C
T _J	Maximum junction temperature	+150	°C
R _{thja}	Junction to ambient thermal resistance (Flat-10 package) ⁽³⁾	125	°C/W
R _{thjc}	Junction to case thermal resistance (Flat-10 package) ⁽³⁾	22	°C/W
ESD	HBM on all pins (human body model)	4 k	V
	CDM on all pins (charged device model)	1 k	V

1. All voltages, except differential I/O bus voltage, are with respect to the network ground terminal.
2. When the input voltage at any pin exceeds the power supplies (that is V_{IN} < GND or V_{IN} > V_{CC}), the current at that pin should be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.
3. Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on the amplifiers.

Table 3. Operating conditions

Symbol	Parameters	Min.	Max.	Units
V _{CC}	Supply voltage	2.3	3.6	V
V _I	Input voltage on any pin vs. GND	0	V _{CC}	V
SCLK	Clock frequency	1	20	MHz
I _{sink}	Output short circuit current at V _{out} low, V _{CC} = 2.3 V		-9	mA
	Output short circuit current at V _{out} low, V _{CC} = 3.6 V		-22	
I _{source}	Output short circuit current at V _{out} high, V _{CC} = 2.3 V		28	
	Output short circuit current at V _{out} high, V _{CC} = 3.6 V		65	
T _a	Ambient temperature range	-55	+125	°C

3 Radiations

Total dose (MIL-STD-883 TM 1019):

The products guaranteed in radiation within the RHA QML-V system fully comply with the MIL-STD-883 TM 1019 specification.

The RHRDAC121 is RHA QML-V, tested and characterized in full compliance with the MIL-STD-883 specification, between 50 and 300 rad/s only (full CMOS technology).

All parameters provided in [Table 5. Electrical characteristics in single-ended input](#) apply to both pre- and post-irradiation, as follows:

- All tests are performed in accordance with MIL-PRF-38535 and test method 1019 of MIL-STD-883 for total ionizing dose (TID).
- The initial characterization is performed in qualification only on both biased and unbiased parts.
- Each wafer lot is tested at high dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification.

Heavy ions:

The behavior of the product when submitted to heavy ions is not tested in production. Heavy-ion trials are performed on qualification lots only.

Table 4. Radiations

Type	Characteristics	Value	Unit
TID ⁽¹⁾	High-dose rate (50 - 300 rad/s) up to:	100	krad
Heavy-ions	SEL ⁽²⁾ immune up to : (with a particle angle of 60° at 125 °C and a fluence of 1 x 10 ⁷ ions/cm ² (10 Million of particles per cm ²))	125	MeV.cm ² /mg
	SEL immune up to: (with a particle angle of 0° at 125 °C and a fluence of 1 x 10 ⁷ ions/cm ² (10 million of particles per cm ²))	62.5	

1. A total ionizing dose (TID) of 100 krad(Si) is equivalent to 1000 Gy(Si), (1 gray = 100 rad).

2. SEL: single event latch-up.

4 Electrical characteristics

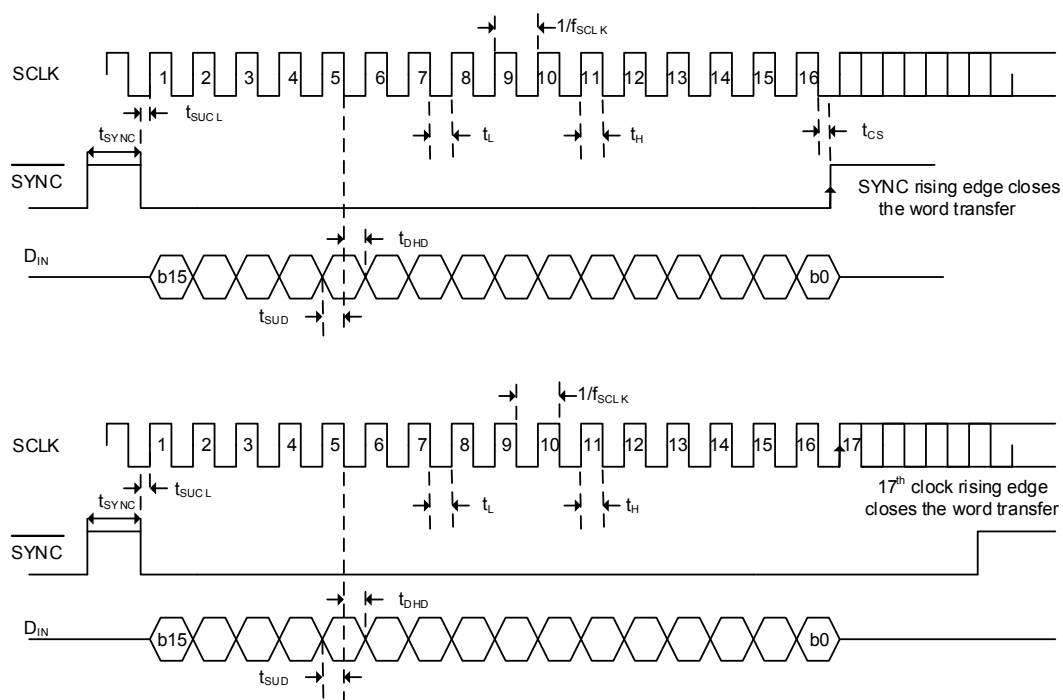
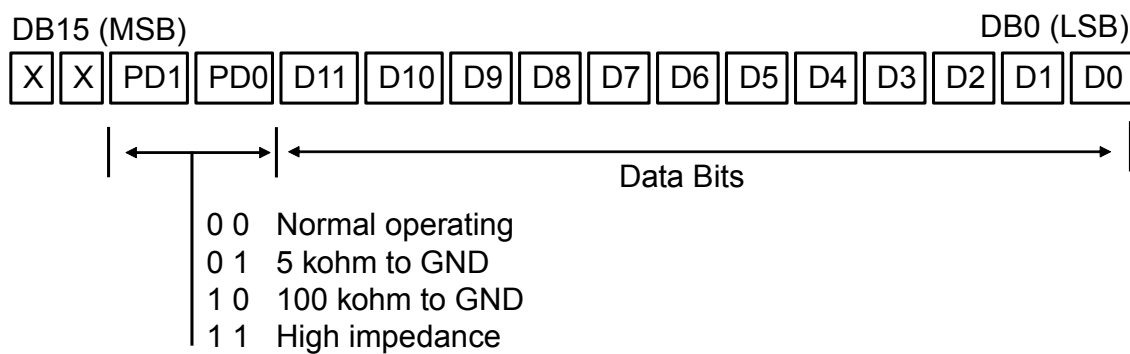
$V_{CC} = +3.3\text{ V}$, $GND = 0\text{ V}$, $f_{SCLK} = 20\text{ MHz}$, $C_L = 200\text{ pF}$, typ. values at $+25\text{ }^{\circ}\text{C}$, min./max. values at $-55\text{ }^{\circ}\text{C}/125\text{ }^{\circ}\text{C}$, unless otherwise specified.

Table 5. Electrical characteristics in single-ended input

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
Static characteristics						
	Resolution with no missing codes	From $-55\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$		12		Bits
INL	Integral non-linearity (end point method)	Over codes 48 to 4047	-4		4	LSB
DNL	Differential non-linearity	DNL max., V_{CC} from 2.3 V to 3.6 V			0.7	
		DNL min., V_{CC} from 2.3 V to 3.6 V	-0.7			
VOFF	Offset error	$I_{out}=0$			10	mV
FSE	Full scale error	$I_{out}=0$			-1	%FSR
GE	Gain error	All ones loaded to DAC register	-1		+1	%FSR
ZCED	Zero code error drift			-20		$\mu\text{V}/^{\circ}\text{C}$
TGE	Gain error tempCo			-0.7		ppm/ $^{\circ}\text{C}$
Output characteristics						
IPD_{sink}	I_{sink} on V_{out} pin in power-down mode	All PD mode			1	mA
ZCO	Zero code output	$I_{out} = 10\text{ }\mu\text{A}$		1	5	mV
		$I_{out} = 100\text{ }\mu\text{A}$		4.5	9	
FSO	Full scale output	$I_{out} = 10\text{ }\mu\text{A}$	3.290	3.298		V
		$I_{out} = 100\text{ }\mu\text{A}$	3.285	3.288		
	DC output impedance			0.1	16	Ohm
Logic input						
I_{in}	Input current		-200		+200	nA
V_{IL}	Input low voltage	From $-55\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ $V_{CC} = 3.6\text{ V}$			0.7	V
		From $-55\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ $V_{CC} = 2.3\text{ V}$			0.7	
V_{IH}	Input high voltage	From $-55\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ $V_{CC} = 3.6\text{ V}$	2			
		From $-55\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ $V_{CC} = 2.3\text{ V}$	1.7			
$C_{in}^{(1)}$	Input capacitance				3	pF

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
Consumption						
I_{CC}	Supply current (output unloaded)	Normal mode, $V_{CC}=3.6$ V, $f_{SCLK}=20$ MHz		165	180	μA
		Normal mode, $V_{CC}=3.6$ V, $f_{SCLK}=10$ MHz		145	160	
		Normal mode, $V_{CC}=3.6$ V, $f_{SCLK}=0$		110	140	
		All PD modes, $V_{CC}=3.6$ V, $f_{SCLK}=20$ MHz		60	80	
		All PD modes, $V_{CC}=3.6$ V, $f_{SCLK}=10$ MHz		38	50	
		All PD modes, $V_{CC}=3.6$ V, $f_{SCLK}=0$		0.5	1	
t_s	Output voltage settling time	FF0 to 00F code, no load CL = 200 pF		3.8	13	μs
		FF0 to 00F code, CL = 500 pF		4	13	
		00Fh to FF0h code, CL = 200 pF		3.2	13	
		00Fh to FF0h code, CL = 500 pF		4	13	
SR	Output slew rate		0.4		2	V/ μs
	Glitch impulse	Code change from 800h to 7FFh		12		nV/s
	Digital feedthrough			0.5		
T_{WU}	Wake-up time	$V_{CC} = 3.6$ V		3.5	6	μs
		$V_{CC} = 2.3$ V		4	7	
$1/f_{SCLK}$	Clock cycle time		50			ns
t_H	Clock high time		20			ns
t_L	Clock low time		20			ns
t_{SUCL}	Set-up time SYNC/ to SCLK rising edge		0			ns
t_{SUD}	Data set-up time		6			ns
t_{DHD}	Data hold time		4.5			ns
t_{CS}	Clock fall to rise of SYNC/	$V_{CC}=3.6$ V	13			ns
		$V_{CC}=2.3$ V	17			ns
t_{SYNC}	SYNC/ high time	$V_{CC}=3.6$ V	36			ns
		$V_{CC}=2.3$ V	35			ns

1. Guaranteed by design.

Figure 3. Serial interface

Figure 4. Input register


4.1 Typical characteristics

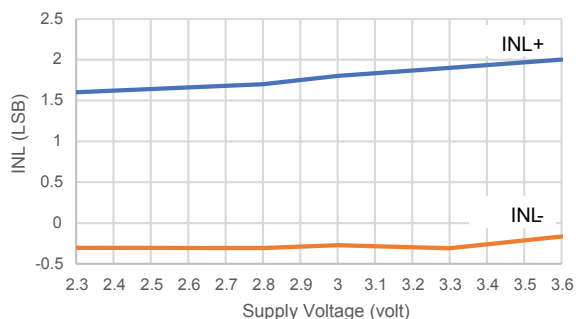
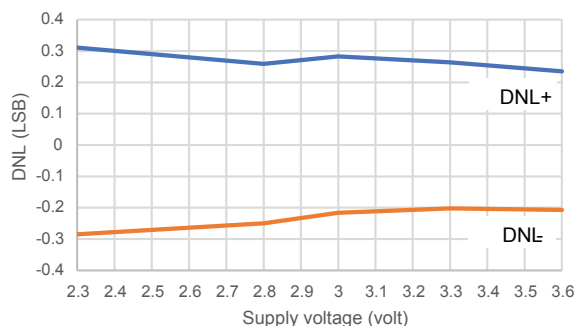
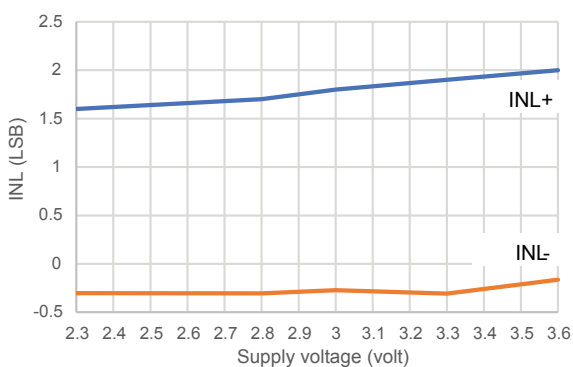
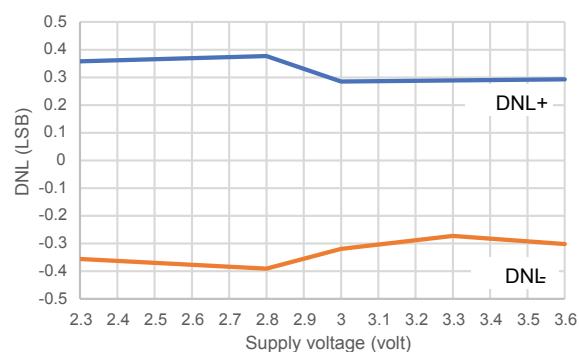
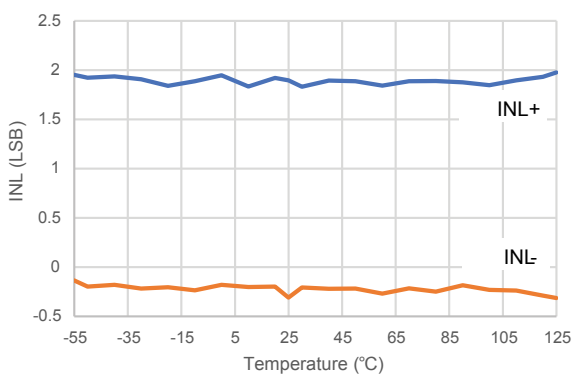
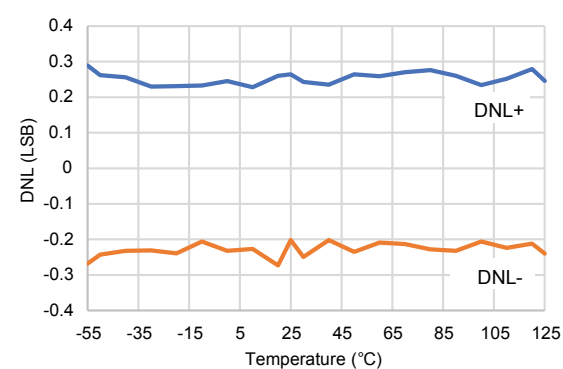
Figure 5. INL vs. Vcc (temp.=25 °C)

Figure 6. DNL vs. Vcc (temp.=25 °C)

Figure 7. INL vs. Vcc on full temp. range

Figure 8. DNL vs. Vcc on full temp. range

Figure 9. INL vs. temp. (Vcc=3.3V)

Figure 10. DNL vs. temp. (Vcc=3.3V)


Figure 11. INL vs. clock frequency (temp.=25 °C)

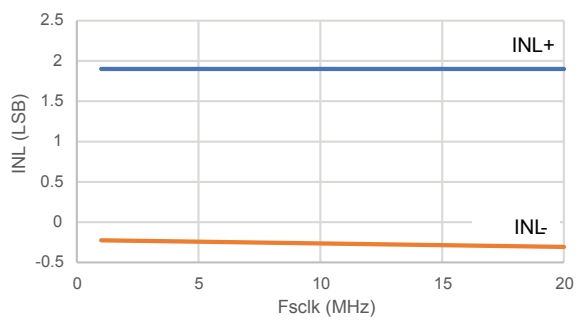
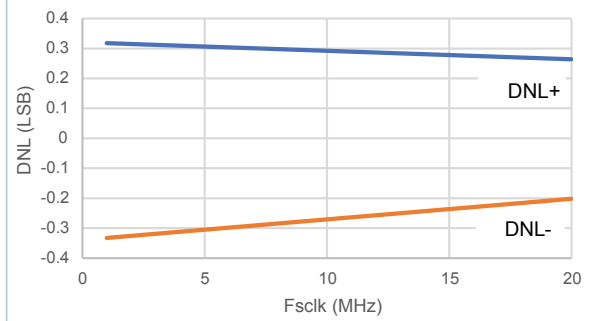


Figure 12. DNL vs. clock frequency (temp.=25 °C)

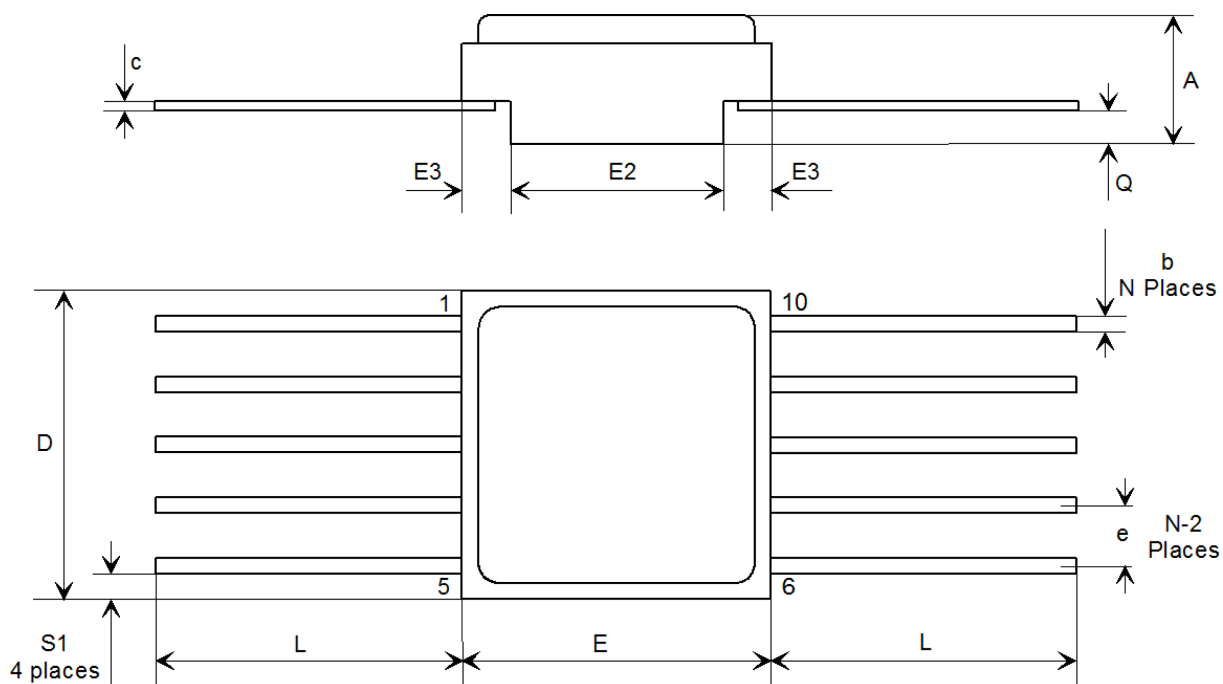


5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 Flat-10 package information

Figure 13. Flat-10 package outline



Note: The upper metallic lid is electrically connected to pin 5.

Table 6. Flat-10 mechanical data

Symbol	mm			Inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.26	2.44	2.62	.089	.096	.103
b	0.38	0.43	0.48	.015	.017	.019
c	0.102	0.127	0.152	.004	.005	.006
D	6.35	6.48	6.60	.250	.255	.260
E	6.35	6.48	6.60	.250	.255	.260
E2	4.32	4.45	4.58	.170	.175	.180
E3	0.88	1.01	1.14	.035	.040	.045
e		1.27			.050	
L	6.35		9.40	.250		.370
Q	0.66	0.79	0.92	.026	.031	.036
S1	0.16	0.485	0.81	.006	.019	.032
N		10			10	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

6 Ordering information

Order code	Description	Package	Lead finishing	Marking ⁽¹⁾	Packing
RH-DAC121K1	Engineering model	Flat-10	Gold	RH-DAC121K1	Strip pack
RHRDAC121K01V	Flight model		Gold	5962R2120801VXC	
RHRDAC121K02V	Flight model		Solder dip	5962R2120801VXA	

1. Specific marking only. Complete marking includes the following:

- ST logo
- Date code (date of the package was sealed) in YYWWA (year, week, and lot of index of the week)
- Country of origin (FR= France).

Note: Contact your ST sales office for information about the specific conditions for products in die form.

7 Other information

7.1 Date code

The date code (date the package was sealed) is structured as follows:

- Engineering model: 3yywwz
- Flight model: yywwz

Where:

yy = last two digits of the year, ww = week digits, z = lot index of the week

7.2 Product documentation

Each product shipment includes a set of associated documentation within the shipment box. This documentation depends on the quality level of the products, as detailed in the table below.

The certificate of conformance is provided on paper whatever the quality level. For QML parts, complete documentation, including the certificate of conformance, is provided on a CDROM.

Table 7. Product documentation

Quality level	Item
Engineering model	Certificate of conformance including: • Customer name • Customer purchase order number • ST sales order number and item • ST part number • Quantity delivered • Date code • Reference to ST datasheet • Reference to TN1181 on engineering models • ST Rennes assembly lot ID
	Certificate of Conformance including: • Customer name • Customer purchase order number • ST sales order number and item • ST part number • Quantity delivered • Date code • Serial numbers • Group C reference • Group D reference • Reference to applicable SMD • ST Rennes assembly lot ID
QML-V Flight	Quality control inspection (groups A, B, C, D, E)
	Screening electrical data in/out summary
	Precap report
	PIND (particle impact noise detection) test
	SEM (scanning electronic microscope) inspection report
	X-ray plates

Revision history

Table 8. Document revision history

Date	Version	Changes
22-Jan-2021	1	Initial release.
10-Jan-2021	2	Added SMD features on the cover page. Updated Rthja and Iin values in Table 2 , Heavy-ions value in Table 4 and SR values in Table 5 . Added Isink and Isource parameters in Table 3 .

Contents

1	Functional description	2
2	Maximum ratings and operating conditions	4
3	Radiations	5
4	Electrical characteristics	6
4.1	Typical characteristics	9
5	Package information	11
5.1	Flat-10 package information	11
6	Ordering information	13
7	Other information	14
7.1	Date code	14
7.2	Product documentation	14
	Revision history	15

List of tables

Table 1.	Pin description	3
Table 2.	Absolute maximum ratings	4
Table 3.	Operating conditions	4
Table 4.	Radiations	5
Table 5.	Electrical characteristics in single-ended input	6
Table 6.	Flat-10 mechanical data	12
Table 7.	Product documentation	14
Table 8.	Document revision history	15

List of figures

Figure 1.	Pin localization	2
Figure 2.	Block diagram	2
Figure 3.	Serial interface	8
Figure 4.	Input register	8
Figure 5.	INL vs. Vcc (temp.=25 °C)	9
Figure 6.	DNL vs. Vcc (temp.=25 °C)	9
Figure 7.	INL vs. Vcc on full temp. range	9
Figure 8.	DNL vs. Vcc on full temp. range	9
Figure 9.	INL vs. temp. (Vcc=3.3V)	9
Figure 10.	DNL vs. temp. (Vcc=3.3V)	9
Figure 11.	INL vs. clock frequency (temp.=25 °C)	10
Figure 12.	DNL vs. clock frequency (temp.=25 °C)	10
Figure 13.	Flat-10 package outline	11

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