Current Mode PWM Controller

NCP12711



MSOP10, 3x3
CASE 846AE

The NCP12711 is a fixed−frequency peak−current−mode PWM controller containing all of the features necessary for implementing single−ended power converter topologies. The device operates from 4 V to 45 V without auxiliary winding and within its thermal capabilities. The controller contains a programmable oscillator capable of operating from 100 kHz to 1 MHz and integrates slope compensation to prevent subharmonic oscillations. The controller includes a programmable soft−start, input voltage UVLO protection, and an over−power protection (OPP) circuit which limits the total power capability of the circuit as the input voltage increases. The UVLO pin also features a shutdown comparator which allows for an external signal to disable switching and brings the controller into a low quiescent state. An onboard op−amp allows the implementation of primary−side regulated converters or non−isolated dc−dc converters.

The NCP12711 contains a suite of protection features including cycle−by−cycle peak−current limiting with smooth frequency increase and a timer−based overload protection. All protection features place the device into a low quiescent fault mode with a 1−s auto−recovery period to allow for system recovery if the fault condition is removed.

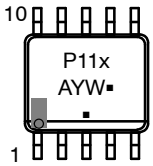
Common General Features

- Wide V_{cc} Input Range (4 – 45 V)
- Internal 7.5−V Regulator
- Current−Mode Control with Adjustable Slope Compensation
- 0% Duty Ratio Operation in No−Load Condition
- Internal Over Power Protection
- Single Resistor Programmable Oscillator – 100 kHz to 1 MHz
- Adjustable Soft−Start on Peak Current and Frequency
- Programmable Input Voltage UVLO with Hysteresis
- Shutdown Threshold for External Disable
- Overload Protection with 30 ms Overload Timer
- Internal Operational Amplifier
- Fault Auto−recovery Mode with 1−s Auto−recovery Period
- ±1 A Source / Sink Gate Driver

Typical Applications

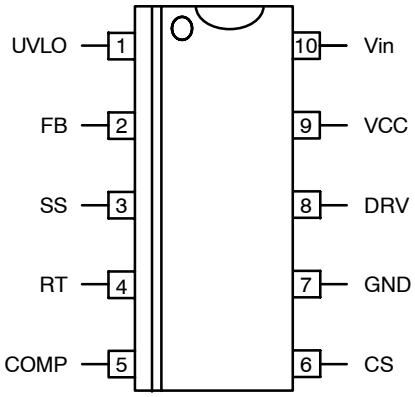
- Single−ended Flyback and Forward Converters for Electric Vehicles
- 4 – 45 V Input DC/DC Controller for Auxiliary Power

MARKING DIAGRAM



P11x	= Specific Device Code
x	= A
A	= Assembly Location
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCP12711ADNR2G	MSOP10, 3x3 (Pb−Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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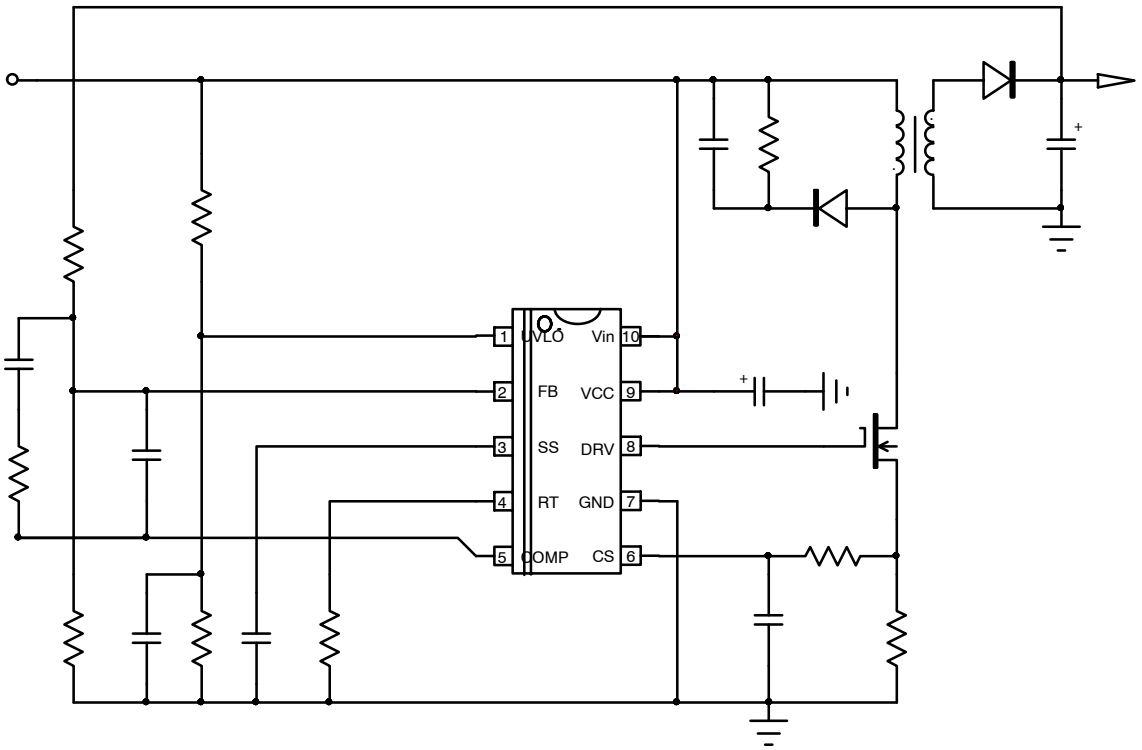


Figure 1. Low−Dissipation Wide−Range Application Non−Isolated Converter

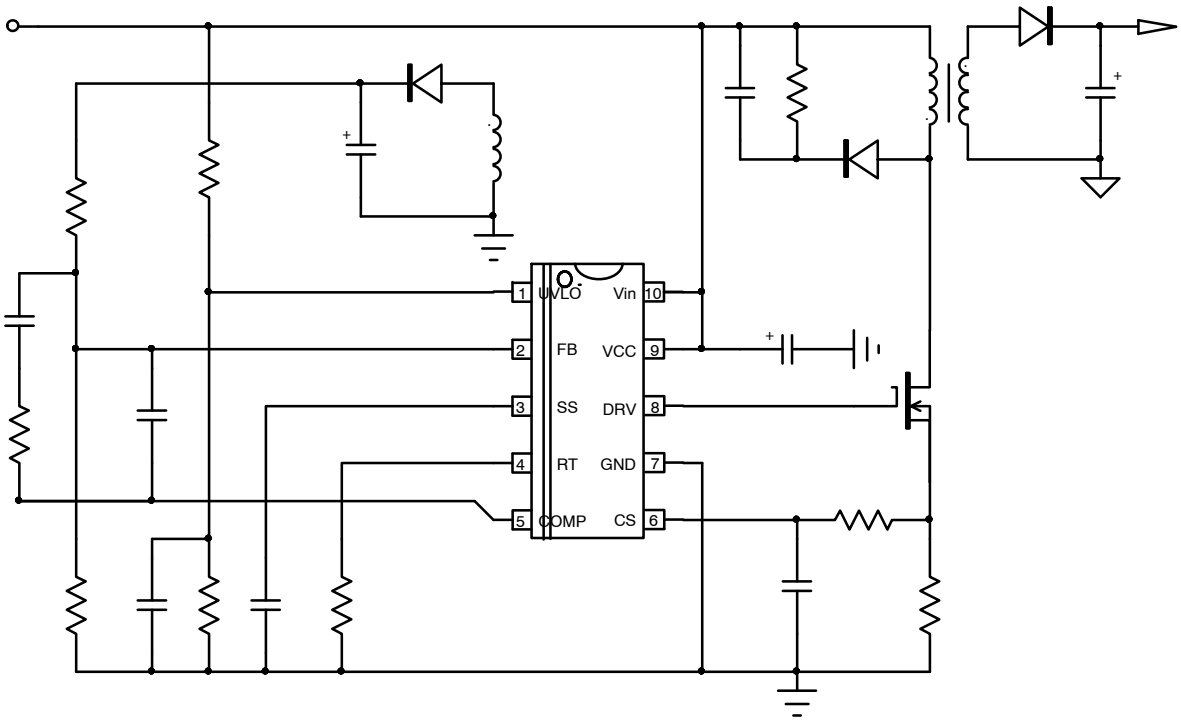


Figure 2. Primary−Side−Regulated Wide−Range−Application Isolated Converter

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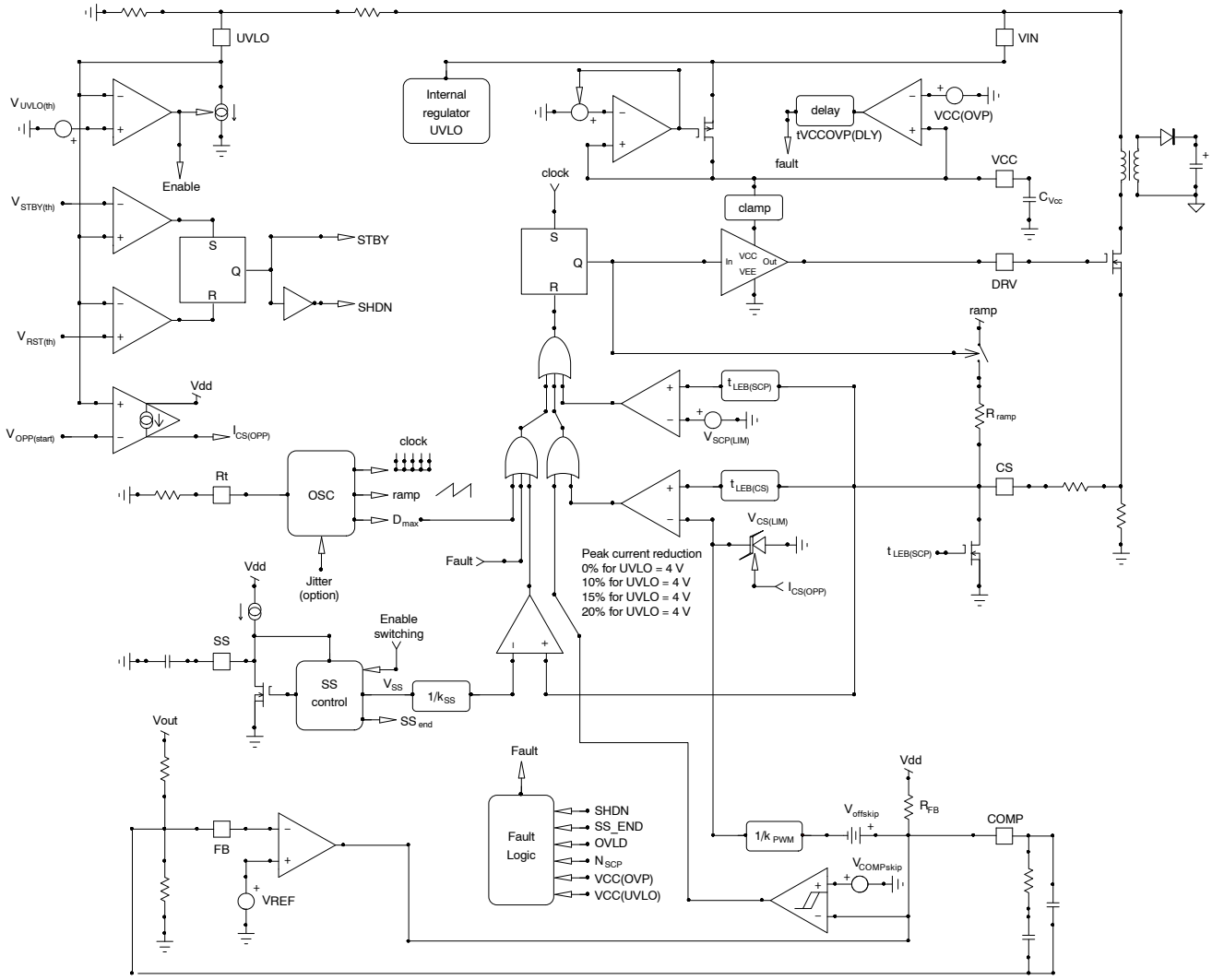


Figure 3. Block Diagram

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PIN DESCRIPTION

DFNW10	Pin Name	Pin Description
1	UVLO	The UVLO pin is the input to the standby and UVLO comparators. A resistor divider between the power supply input voltage and ground is connected to the UVLO pin to set the input voltage level at which the controller will be enabled. UVLO hysteresis is set by a 5−μA pull−down current source. An externally−supplied pull−down signal can also be used to disable the controller. The UVLO pin is also used to determine the over−power protection amount.
2	FB	The FB pin senses the voltage to be regulated via a resistive divider. A passive network connected between this pin and COMP allows to set poles and zeroes as suggested by the compensation strategy.
3	SS	A capacitor on this pin sets the soft−start sequence during which the peak current setpoint is gradually increased as well as the switching frequency.
4	RT	The RT pin sets the oscillator frequency in the controller. This pin requires a resistor to ground closely located to the controller. Typical R_T resistor values are in the range of 10 kΩ − 150 kΩ.
5	COMP	This is the op−amp output pin, loaded by the R_{FB} resistance.
6	CS	The CS pin is the current sense input for the PWM and current limit comparators. An external low−pass filter is recommended for improved noise immunity. The external filter resistor is also used to determine the amount of compensation ramp added to the current sense information.
7	GND	This pin is the controller ground.
8	DRV	The DRV pin is a high current output used to drive the external MOSFET gate. DRV has source and sink capability of 1 A.
9	VCC	The VCC pin provides bias to the controller via a linear regulator. An external decoupling capacitor to ground in the range of 1 − 10 μF is recommended. An auxiliary winding can help turn off the regulator and improve power dissipation in wide input range applications.
10	VIN	This is the controller supply input. If kept below $V_{CC(OVP)}$ it can be safely connected to VCC.

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
$V_{in(MAX)}$	Supply Voltage (Continuous)	−0.3 to 45	V
$I_{CC(MAX)}$	Supply Current V_{in} = 12 V V_{in} = 45 V	 35 10	mA
$V_{CC(MAX)}$	VCC pin	−0.3 to 30	V
$V_{DRV(MAX)}$	DRV Voltage (Note 1)	−0.3 V to $V_{DRV(high)}$	V
$I_{DRV(MAX)}$	DRV Current (Peak)	1.25	A
$V_{SIG(MAX)}$	Max Voltage on Signal Pins V_{Vcc} > 5.5 V V_{Vcc} < 5.5 V	 −0.3 to 5.5 −0.3 to V_{Vcc}	V
$I_{SIG(MAX)}$	Max Current on Signal Pins	10	mA
$R_{\theta J-A}$	Thermal Resistance Junction−to−Air	139	°C/W
$\Psi_{\theta J-T}$	Junction−to−Top Thermal Characterization Parameter	5.5	°C/W
$\Psi_{\theta J-B}$	Junction−to−Board Thermal Characterization Parameter	68.4	°C/W
T_{JMAX}	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	−55 to 150	°C
T_J	Operating Temperature Range	−40 to 125	°C
	ESD Capability (Notes 2, 3) Human Body Model per JEDEC Standard JESD22−A114E. Charge Device Model per JEDEC Standard JESD22−C101E.	 2000 1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum driver voltage is limited by the driver clamp voltage, $V_{DRV(high)}$, when V_{CC} exceeds the driver clamp voltage. Otherwise, the maximum driver voltage is V_{CC}.
2. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per JEDEC Standard JESD22−A114E
   Charge Device Model 1000 V per JEDEC Standard JESD22−C101E
3. This device contains latch−up protection and has been tested per JEDEC JESD78D, Class I and exceeds ±100 mA.

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RECOMMENDED OPERATING CONDITIONS

Symbol	Rating	Value	Unit
V_{in}	Supply Voltage	4.5 – 40	V
T_J	Operating Temperature Range	–40 to 125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{IN} = 12 V, V_{CC} = 12 V, V_{COMP} = open, C_{DRV} = 1 nF, R_T = 53.6 kΩ, V_{CS} = 0 V, V_{SS} = Open, V_{UVLO} = 1.2 V, V_{FB} = 0 V, for typical values T_J = 25°C, for min/max values, T_J is – 40°C to 125°C, unless otherwise noted)

Symbol	Characteristics	Test Condition	Min	Typ	Max	Unit
SUPPLY CIRCUIT						
$V_{CC(reg)}$ $V_{in(STR)}$ $V_{in(MIN)}$ $V_{CC(reset)}$	Supply Voltage V_{cc} Regulation Level Start–up Level (Part Switches) Minimum Operating Voltage Reset Voltage (All Faults Clear)	 I_{CC} = –5 mA V_{in} increasing V_{in} decreasing V_{CC} decreasing	 7.0 3.5 3.3 3.0	 7.5 3.7 3.5 3.3	 8.0 3.95 3.75 3.6	 V V V V
$V_{IN(hys)}$	Hysteresis between $V_{in(STR)}$ and $V_{in(MIN)}$		–	200	–	mV
I_{start}	Start–up Current	V_{CC} = $V_{CC(reg)}$ – 0.2 V	15	20	–	mA
$I_{VIN(LIM)}$	Start–up Current with V_{cc} = 0 V	V_{cc} pin shorted to ground	–	2.5	–	mA
$V_{CC(SC)}$	V_{CC} Threshold for Non–Short Circuit Detection		–	0.2	–	V
$I_{Vin(off)}$	Start–up Circuit Off–State Leakage Current	V_{in} = 45 V	–	–	95	μA
$V_{CC(OVP)}$	Supply Over–Voltage Protection		25	27	29	V
$V_{CC(OVP_HYS)}$	Hysteresis on Supply OVP		–	100	–	mV
$t_{VCCOVP(DLY)}$	VCC OVP Detection Filter Delay		–	7	–	μs
$I_{CC(SHDN)}$ $I_{CC(STBY)}$ $I_{CC(SHDNVI)}$ $I_{CC(STBYVI)}$ $I_{CC(EN)}$ $I_{CC(FLT)}$	Supply Current SHDN (VCC Pin) STBY (VCC Pin) SHDN (VIN and VCC Pins Shorted) STBY (VIN and VCC Pins Shorted) Enable Fault	 V_{UVLO} = 0 V V_{UVLO} = 0.4 V V_{UVLO} = 0 V V_{UVLO} = 0.4 V C_{DRV} = Open, V_{COMP} = 2 V V_{CS} = 0 V	 – – – – – –	 60 340 104 380 – –	 120 650 170 700 4 500	 μA μA μA μA mA μA
CURRENT SENSE						
$V_{CS(LIM)}$	Current Limit Comparator Threshold		237	250	263	mV
$t_{CS(DLY)}$	Propagation Delay From Current Sense Limit to DRV Low	Step V_{CS} from 0 – 0.35 V	–	25	75	ns
$V_{SCP(LIM)}$	Short Circuit Protection (SCP) Current Limit Threshold		–	325	–	mV
$t_{SCP(DLY)}$	Propagation Delay From Short Circuit Limit to DRV Low	Step V_{CS} from 0 – 0.44 V	–	25	75	ns
$t_{on,min}$	Minimum On–time Duration		–	135	170	ns
N_{SCP}	Short Circuit Counter	V_{CS} = 1 V	–	4	–	
$t_{LEB(CS)}$	CS Leading Edge Blanking (LEB)		60	110	155	ns
$t_{LEB(SCP)}$	SCP Leading Edge Blanking		35	60	90	ns
$R_{PD(LEB)}$	CS LEB Pull–down Resistance		–	27	55	Ω
$t_{CS(OVLD)}$	Overload Timer Duration	V_{CS} > 0.25 V	22.5	28.5	34.5	ms
$V_{CS(skip)}$	CS Skip Threshold in % of the Max CS Level	0% duty ratio – V_{COMP} < 325 mV	–	0	–	%
V_{ramp}	Compensation Ramp Peak Level		1.55	1.8	2.05	V
R_{ramp}	Internal Ramp Resistance to CS Pin		15	21	27	kΩ

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ELECTRICAL CHARACTERISTICS (V_{IN} = 12 V, V_{CC} = 12 V, V_{COMP} = open, C_{DRV} = 1 nF, R_T = 53.6 kΩ, V_{CS} = 0 V, V_{SS} = Open, V_{UVLO} = 1.2 V, V_{FB} = 0 V, for typical values T_J = 25°C, for min/max values, T_J is − 40°C to 125°C, unless otherwise noted) (continued)

Symbol	Characteristics	Test Condition	Min	Typ	Max	Unit
COMP SECTION						
K_{PWM}	PWM to COMP Gain Through Resistor Divider	V_{COMP} = 1.25 V / 2.9 V	7.6	8.0	8.4	
$t_{PWM(Dly)}$	Propagation Delay to DRV Low (Note 6)	V_{COMP} = 2 V, Step V_{CS} 0 − 0.35 V	–	25	75	ns
$V_{offskip}$	Internal Feedback Offset		0.3	0.64	0.91	V
$V_{COMP(skip)}$	0% Duty Ratio Level − 0−A Setpoint and No DRV	V_{COMP} is decreasing	–	325	–	mV
$V_{COMP(skip_hys)}$	Voltage Hysteresis between Skip and Skip_out Level	V_{COMP} is increasing	–	5	–	mV
R_{FB}	Internal Pull−Up Resistance		4	5	6	kΩ
$V_{COMP(open)}$	COMP Open Pin Voltage	V_{cc} = 3.6 V	3.15	3.45	–	V
I_{COMP}	COMP Output Current	V_{COMP} = 0	0.84	1	1.2	mA
D_{MAX}	Maximum Duty Ratio Limit (Note 6)	V_{COMP} = Open	86	90	94	%
D_{MIN}	Minimum Duty Ratio (Note 6)	V_{COMP} = 0	–	–	0	%
OPERATIONAL AMPLIFIER SECTION						
V_{ref}	Voltage Feedback Input	T_J = 25°C −40°C < T_J < 125°C	2.45 2.42	2.5 2.5	2.55 2.58	V
I_{IB}	Input Bias Current	V_{FB} = 3 V	–	0.01	–	μA
A_{OL}	Open−Loop Voltage Gain	V_{COMP} = 2 to 4 V	–	90	–	dB
BW	Unity Gain Bandwidth (T_j = 25°C)		–	1	–	MHz
PSRR	Power Supply Rejection Ratio		–	60	–	dB
I_{OPS}	Output Current (Output Resistance is R_{FB}) Sink	(V_{COMP} = 0.35 V, V_{FB} = 2.7 V)	–	10	–	mA
V_{OTH} V_{OTL}	Output Voltage Swing High State Low State	 COMP is open, V_{FB} = 2.3 V COMP is open, V_{FB} = 2.7 V	 – –	 4.8 0.03	 – 0.15	 V V
SOFT START						
$V_{SS(open)}$	Soft−Start Open Pin Voltage	V_{cc} = 3.6 V	2.80	3.35	–	V
$V_{SS(end)}$	Soft−Start End Threshold		1.85	2.00	2.15	V
I_{SS}	Soft−Start Current	0 < V_{SS} < $V_{SS(end)}$	12	15	18	μA
K_{SS}	Soft−Start to CS Divider		–	8	–	
$R_{SS(DIS)}$	Soft−Start Discharge Resistance		–	–	100	Ω
$f_{SW(SS)}$	Minimum Frequency for V_{SS} = 0 V	Clamp frequency	20	30	–	kHz
OSCILLATOR						
f_{OSC1}	Oscillator Frequency 1	R_T = 53.6 kΩ	185	200	215	kHz
f_{OSC2}	Oscillator Frequency 2	R_T = 130 kΩ	90	100	110	kHz
f_{OSC3}	Oscillator Frequency 3	R_T = 18.7 kΩ	450	500	550	kHz
f_{OSC4}	Oscillator Frequency 4	R_T = 8.66 kΩ	–	1000	–	kHz
UNDER−VOLTAGE LOCKOUT						
$V_{STBY(th)}$	Standby Threshold	V_{UVLO} increasing	0.3	0.35	0.4	V
$V_{RST(th)}$	Reset Threshold	V_{UVLO} decreasing	0.25	0.3	0.35	V
$V_{STBY(HYS)}$	Standby Hysteresis	V_{UVLO} decreasing	–	50	–	mV
$t_{STBY(DLY)}$	Standby Detection RC Filter		–	7	–	μs
$V_{UVLO(th)}$	UVLO Threshold	V_{UVLO} increasing	0.49	0.5	0.51	V
$I_{UVLO(HYS)}$	UVLO Hysteresis Current		4.5	5	5.5	μA
$t_{UVLO(DLY)}$	UVLO Detection Delay Filter	V_{UVLO} = $V_{UVLO(th)}$ − 50 mV	–	1.1	–	μs

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ELECTRICAL CHARACTERISTICS (V_{IN} = 12 V, V_{CC} = 12 V, V_{COMP} = open, C_{DRV} = 1 nF, R_T = 53.6 kΩ, V_{CS} = 0 V, V_{SS} = Open, V_{UVLO} = 1.2 V, V_{FB} = 0 V, for typical values T_J = 25°C, for min/max values, T_J is − 40°C to 125°C, unless otherwise noted) (continued)

Symbol	Characteristics	Test Condition	Min	Typ	Max	Unit
UNDER−VOLTAGE LOCKOUT						
$t_{UVLO(EN)}$	Enable Filter Delay	V_{UVLO} increasing	−	5	−	μs
OVER−POWER PROTECTION						
$V_{OPP(START)}$	UVLO Voltage Above Which OPP Applied		−	1		V
OPP_{red}	Maximum Peak Current Reduction	V_{UVLO} = 4 V	−	15	−	%
OPP_{clp}	Internal Peak Reduction Clamp on UVLO	$V_{CS} = V_{CS(LIM)}$ (1− OPP_{red})	−	4	−	V
$V_{OPP(0\%)}$	COMP Threshold Voltage Above Which OPP is Applied		−	1.4	−	V
$V_{OPP(100\%)}$	COMP Threshold Voltage for 100% OPP		−	2.6	−	V
GATE DRIVE						
$t_{DRV(rise)}$	DRV Rise Time	V_{DRV} = 1.2 V to 10.8 V, C_{DRV} = 1 nF	6	10	16	ns
$t_{DRV(fall)}$	DRV Fall Time	V_{DRV} = 10.8 V to 1.2 V, C_{DRV} = 1 nF	6	10	16	ns
$I_{DRV(SRC)}$	DRV Source Current	V_{DRV} = 6 V, Note 8	−	0.9	−	A
$I_{DRV(SNK)}$	DRV Sink Current	V_{DRV} = 6 V, Note 8	−	1.0	−	A
$V_{DRV(clamp)}$	DRV Clamp Voltage	V_{CC} = 20 V, R_{DRV} = 10 kΩ	8	10	12	V
$V_{DRV(MIN)}$	Minimum DRV Voltage	$V_{CC} = V_{CC(reg)}$ + 100 mV, R_{DRV} = 10 kΩ	6	−	−	V
FAULT PROTECTION						
t_{AR}	Auto−recovery Timer		0.8	1	1.2	s
THERMAL SHUTDOWN						
T_{SHDN}	Thermal Shutdown		150	165	180	°C
$T_{SHDN(hys)}$	Thermal Shutdown Hysteresis		−	25	−	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Disabling of overload timer refers to not acknowledging overload as a fault. The device will continue to switch indefinitely without going to fault mode.
5. Disabling Slope compensation means that no compensation ramp is applied.
6. Electrical characteristics apply to both COMP Architectures
7. OPP Current Gain disabled means that no OPP current is injected out of the CS pin
8. Guaranteed by design

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TYPICAL CHARACTERISTICS

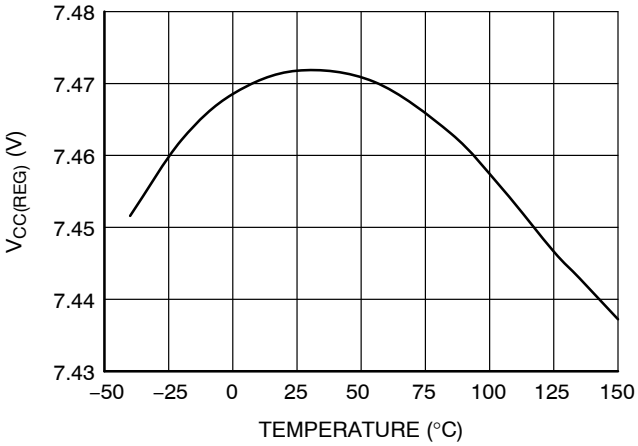


Figure 4. $V_{CC(REG)}$ vs. Temperature

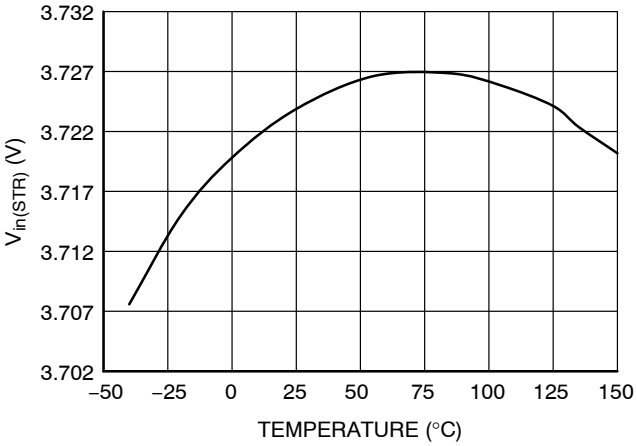


Figure 5. $V_{in(STR)}$ vs. Temperature

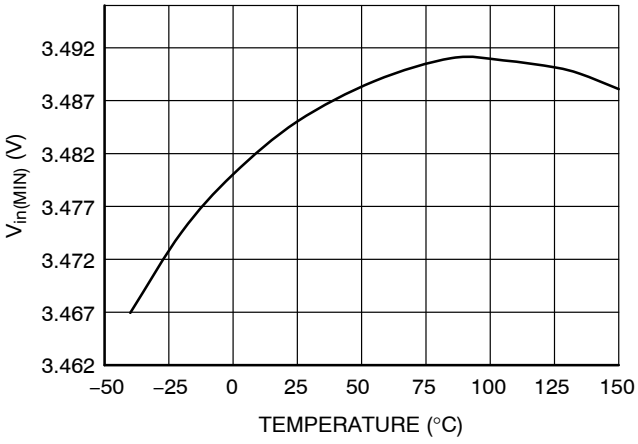


Figure 6. $V_{in(MIN)}$ vs. Temperature

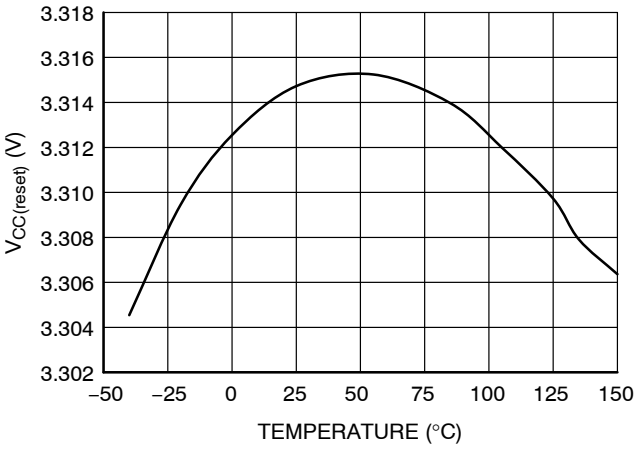


Figure 7. $V_{CC(reset)}$ vs. Temperature

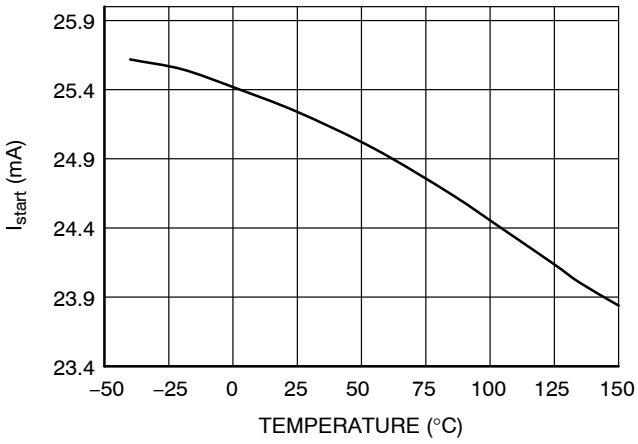


Figure 8. I_{start} vs. Temperature

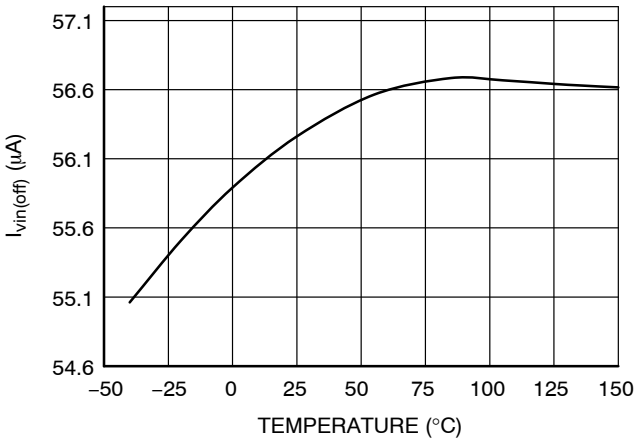


Figure 9. $I_{vin(off)}$ vs. Temperature

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TYPICAL CHARACTERISTICS (continued)

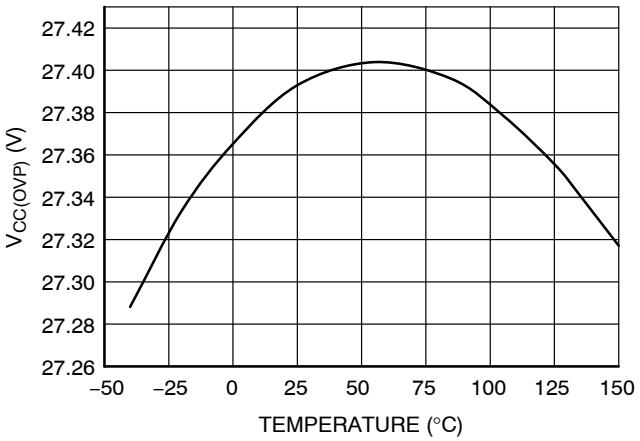


Figure 10. $V_{CC(OVP)}$ vs. Temperature

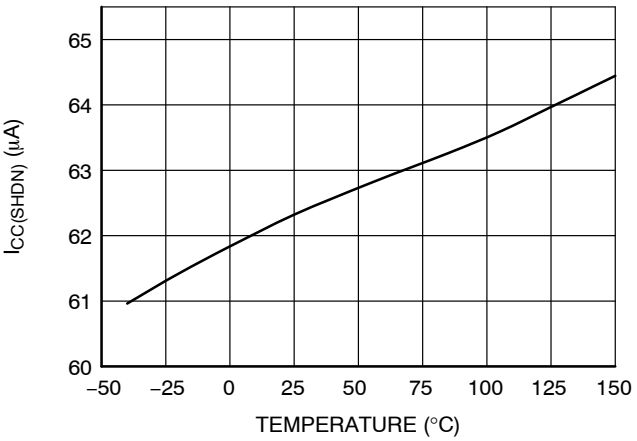


Figure 11. $I_{CC(SHDN)}$ vs. Temperature

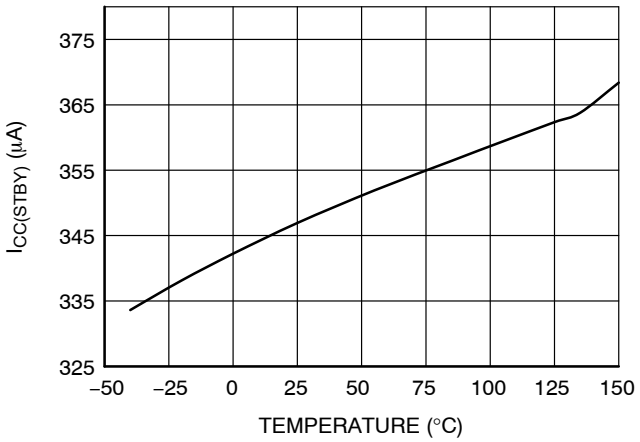


Figure 12. $I_{CC(STBY)}$ vs. Temperature

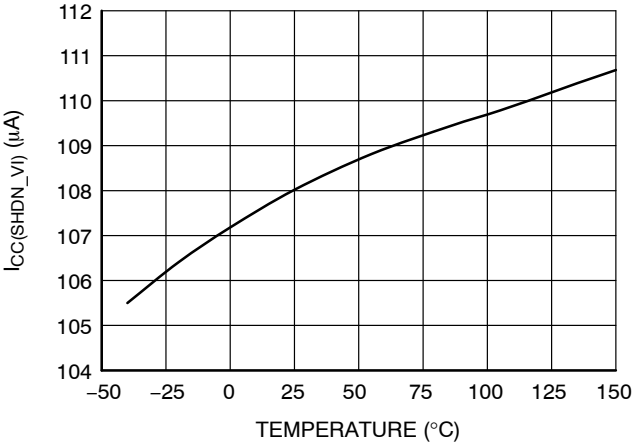


Figure 13. $I_{CC(SHDN_VI)}$ vs. Temperature

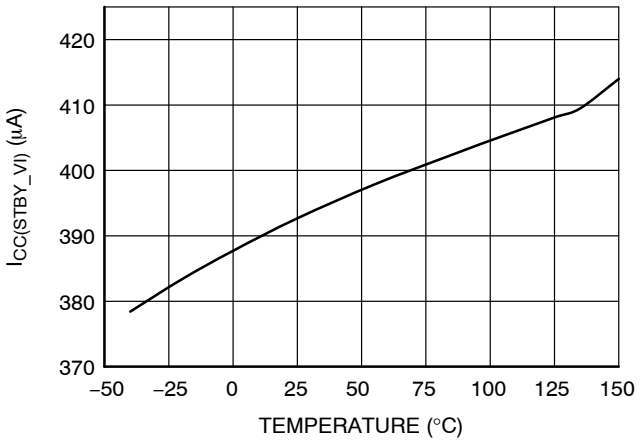


Figure 14. $I_{CC(STBY_VI)}$ vs. Temperature

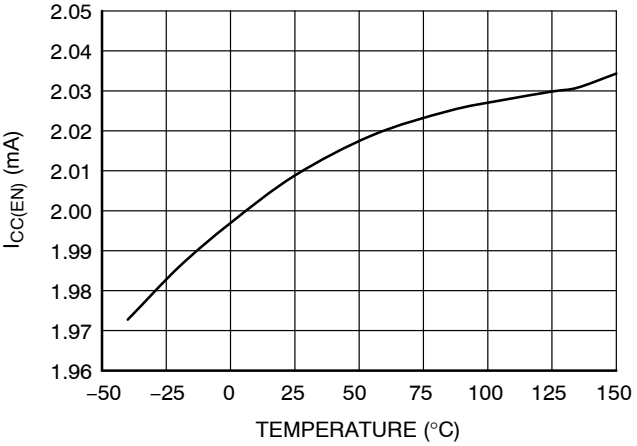


Figure 15. $I_{CC(EN)}$ vs. Temperature

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TYPICAL CHARACTERISTICS (continued)

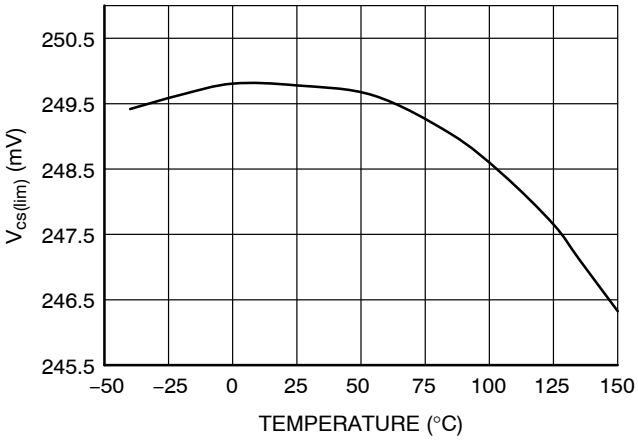


Figure 16. $V_{cs(lim)}$ vs. Temperature

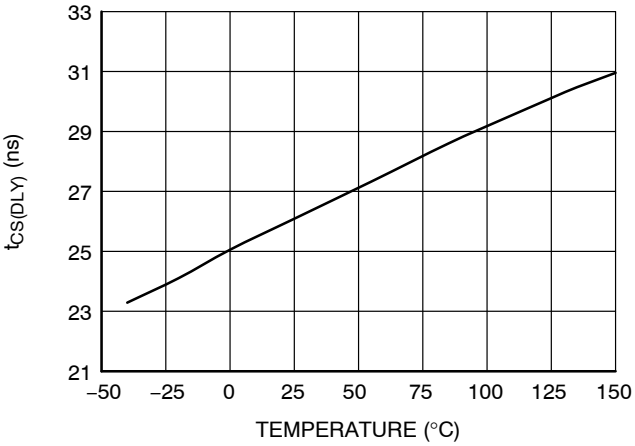


Figure 17. $t_{CS(DLY)}$ vs. Temperature

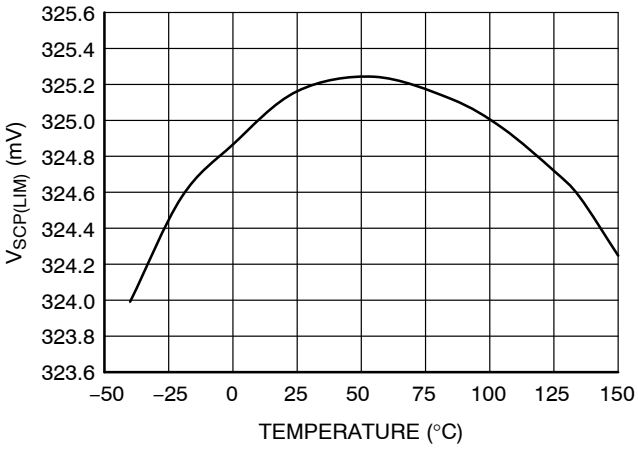


Figure 18. $V_{SCP(LIM)}$ vs. Temperature

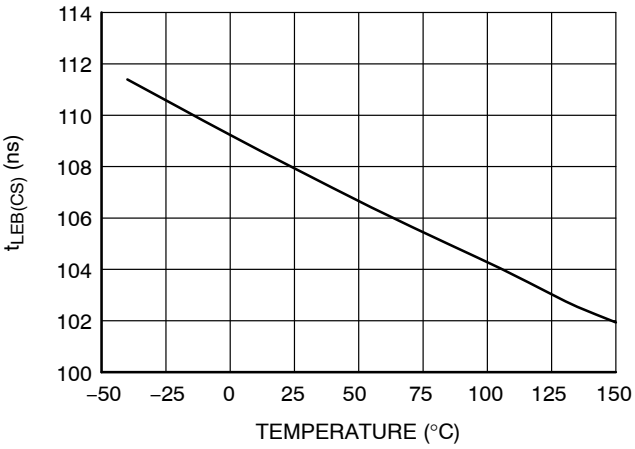


Figure 19. $t_{LEB(CS)}$ vs. Temperature

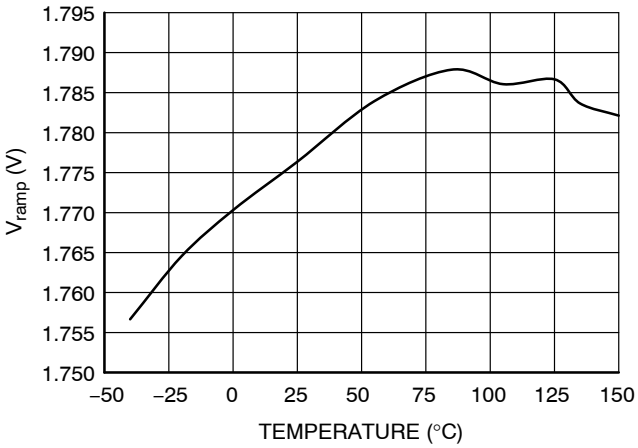


Figure 20. V_{ramp} vs. Temperature

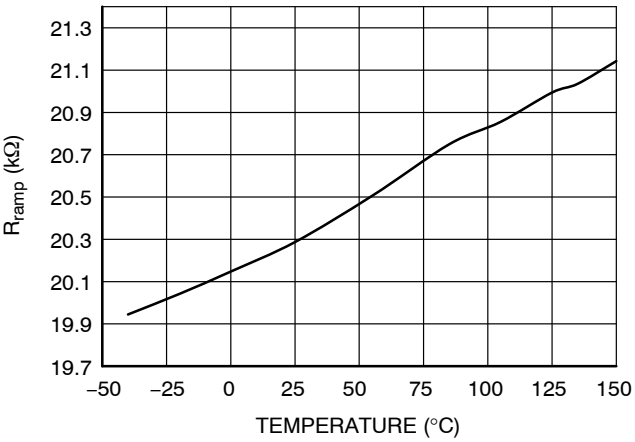


Figure 21. R_{ramp} vs. Temperature

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TYPICAL CHARACTERISTICS (continued)

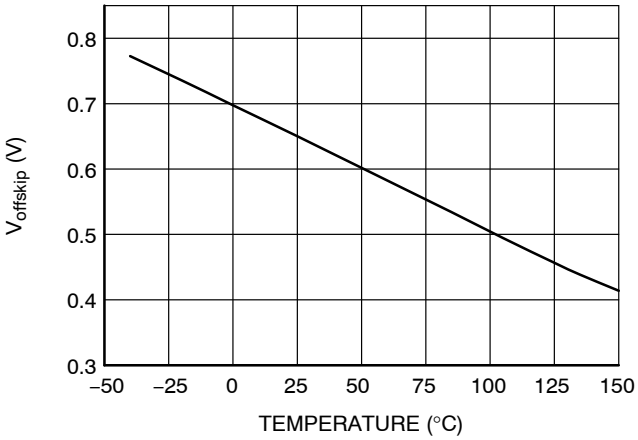


Figure 22. $V_{offskip}$ vs. Temperature

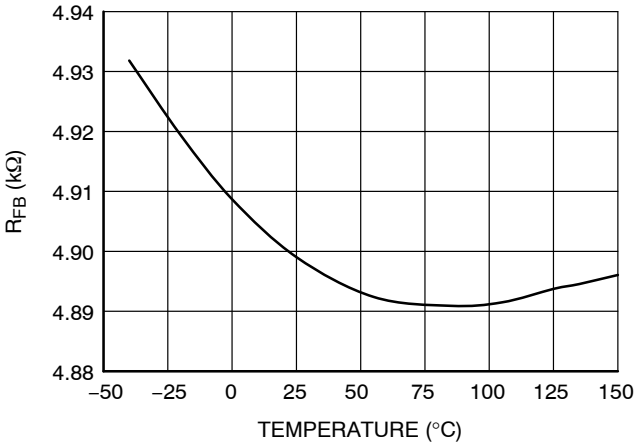


Figure 23. R_{FB} vs. Temperature

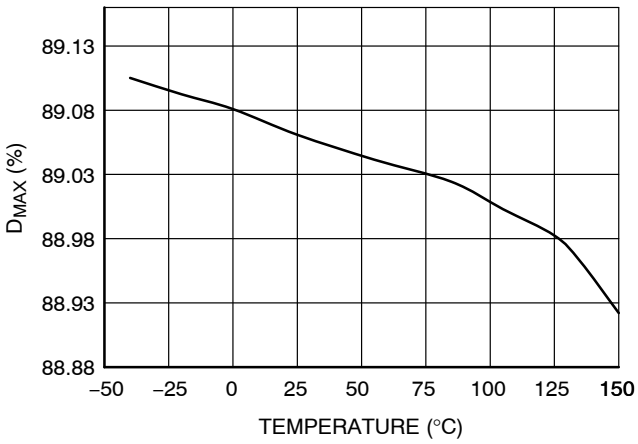


Figure 24. D_{MAX} vs. Temperature

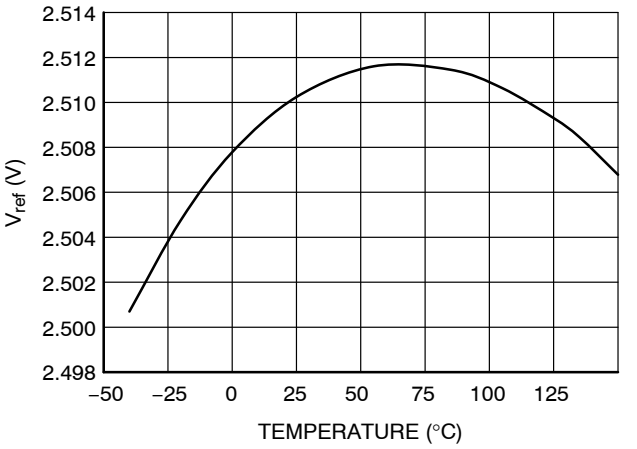


Figure 25. V_{ref} vs. Temperature

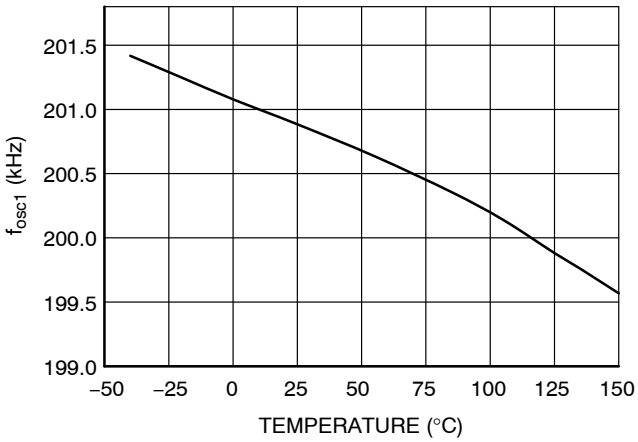


Figure 26. f_{osc1} vs. Temperature

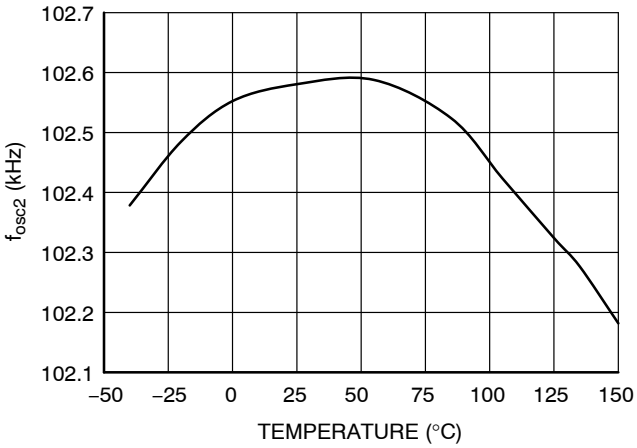


Figure 27. f_{osc2} vs. Temperature

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TYPICAL CHARACTERISTICS (continued)

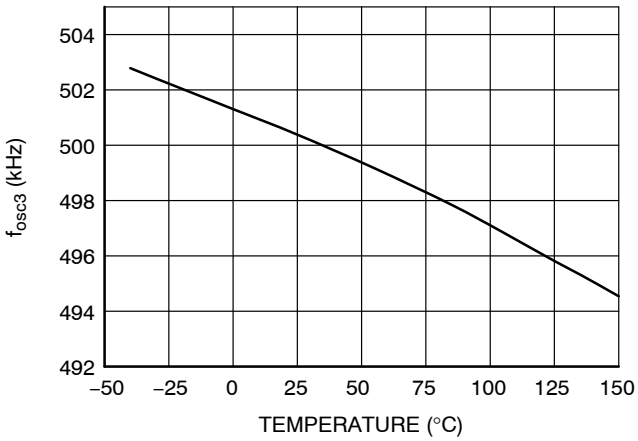


Figure 28. f_{osc3} vs. Temperature

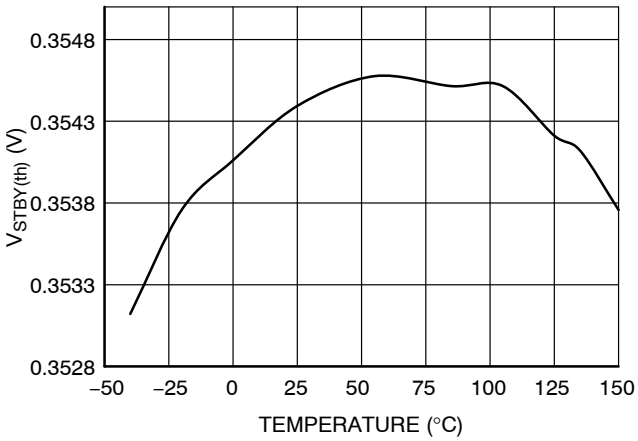


Figure 29. $V_{STBY(th)}$ vs. Temperature

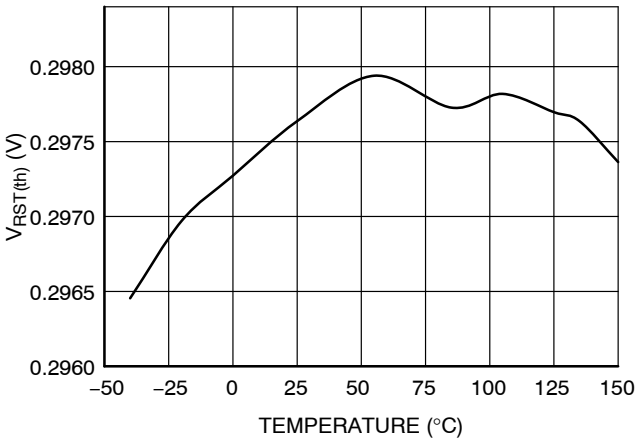


Figure 30. $V_{RST(th)}$ vs. Temperature

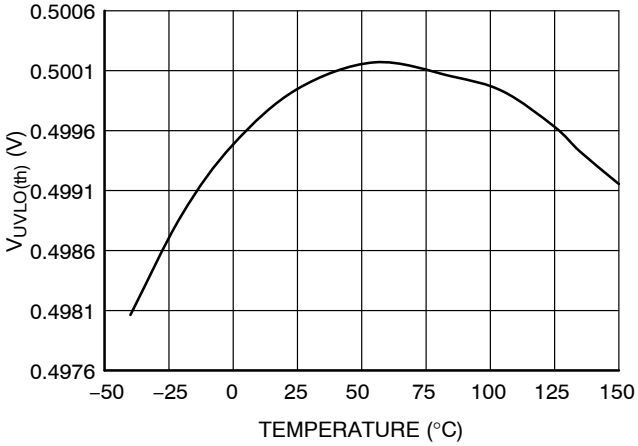


Figure 31. $V_{UVLO(th)}$ vs. Temperature

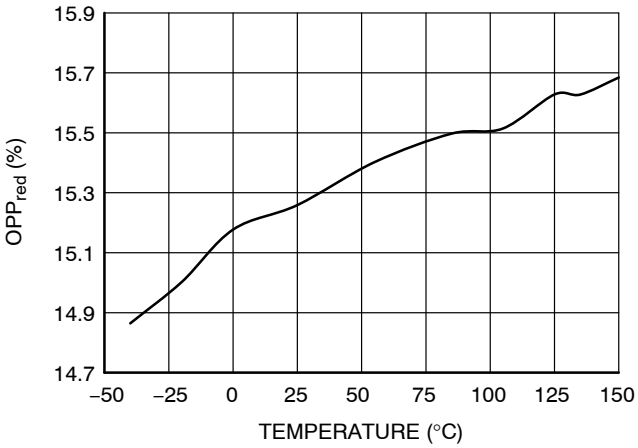


Figure 32. OPP_{red} vs. Temperature

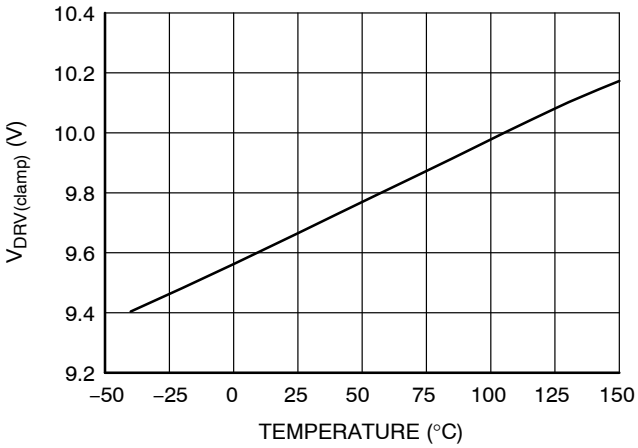


Figure 33. $V_{DRV(clamp)}$ vs. Temperature

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APPLICATION INFORMATION

NCP12711 implements a standard current−mode architecture where the switch−off event is dictated by the peak current setpoint. This component represents the ideal candidate where low part−count and cost effectiveness are key design parameters, particularly in dc−dc converters modules and open−frame power supplies. NCP12711 brings all the necessary components normally needed in today modern power supply designs.

- *Current−mode operation with internal slope compensation:* implementing peak current mode control at a fixed operating frequency, the NCP12711 includes an externally−adjustable slope compensation scheme. By sizing a single resistance connected in series with the CS pin, the designer has the ability to tailor the compensation level exactly to his needs.
- *0% duty ratio operation:* the loop can program a 0−A peak current setpoint when it imposes 640 mV on the error amplifier COMP pin. It means, the width of the DRV pulse is a minimum t_{on} (LEB + propagation delay). If V_{out} keeps increasing in this situation, the regulation is lost and the IC goes to skip mode with no DRV pulse. It ensures that the IC will safely skip cycles at minimum t_{on} during light load, preventing output runaway while keeping output ripple at a minimum.
- *Internal regulator:* the part includes an internal regulator powering the device from 4 to 45 V without the need to resort to an auxiliary winding. When power dissipation is at stake, it is possible to lift the VCC pin up via an auxiliary winding and permanently disable the regulator.
- *Input voltage monitoring:* the UVLO pin observes the input voltage through a resistive divider. This pin serves two purposes: a) it ensures the converter operates within the range it has been designed for and b) it routes this information to a power−limiting path for over−power protection (OPP).
- *Internal OPP:* the part internally buffers the UVLO voltage and reduces the maximum peak current setpoint at high input line. Please note that the OPP current starts from 0% when the UVLO voltage is 1.0 V, a low−line condition. It helps pass maximum power at the lowest input voltage despite some compensation at high line. OPP is also disabled during the start−up sequence or in light−load operation.
- *Internal soft−start:* a soft−start precludes the main power switch from being stressed upon start up and it reduces output voltage overshoots. In this controller, the soft−start can be adjusted by a simple capacitor to ground. Beside peak current smooth increase brought by this mechanism, the switching frequency starts from a low 30−kHz value and increases along the soft−start sequence. Soft−start is activated when a new startup sequence occurs or during an auto−recovery hiccup.
- *On−board op−amp:* an op−amp allows the implementation of non−isolated dc−dc converters but also isolated versions in which the rectified auxiliary voltage is used for regulation.
- V_{cc} *OVP:* an OVP protects the circuit against V_{cc} runaways. The fault must be present at least 7 μs to be validated. This OVP is auto−recovery.
- *Short−circuit protection:* short−circuit and especially over−load protections are difficult to implement when a strong leakage inductance between auxiliary and power windings affects the transformer (the auxiliary winding level does not properly collapse in presence of an output short). In this controller, every time the internal 0.25−V maximum peak current limit is activated (or less when OPP is active), an error flag is asserted and a time period starts, thanks to the programmable timer. When the timer has elapsed, the controller enters an auto−recovery mode with a 1−s recurrence.
- *Winding or diode short circuit protection:* in case the secondary−side winding (or even the rectifying diode) is shorted, the primary−side current can grow very quickly with possibly−lethal conditions in the converter. An extra comparator with a smaller LEB monitors if the peak current exceeds 25% of the maximum value (250 mV/R_{sense}) four consecutive times. At the end of this sequence, the converter enters auto−recovery mode.

Supplying the Controller

The component integrates a start−up current source supplied from the VIN pin and capable of sourcing up to 20 mA typically to the VCC pin. When V_{cc} reaches the regulation level of 7.5 V, the startup is a linear regulator which can continue to supply and regulate V_{cc} at 7.5 V. The recommended VCC capacitance to ensure stability of the regulator is 1 – 10 μF. This source is a dual−current type meaning that if for any reason the V_{cc} is shorted to ground, the current is safely limited to 2.5 mA, preventing any lethal runaway at a high input voltage. When the short circuit is released and V_{cc} exceeds a certain voltage level (200 mV typical), the source is back to its 20−mA setpoint. The 20−mA are typically specified for a 12−V level on the VIN pin but the part will deliver current as soon as a bias appears on the part. Figure 34 shows a simulated start−up sequence with VIN plateauing at 4 V for some time before taking off towards 15 V. The driving pulses follow the voltage and are clamped at the 7.5−V voltage later on.

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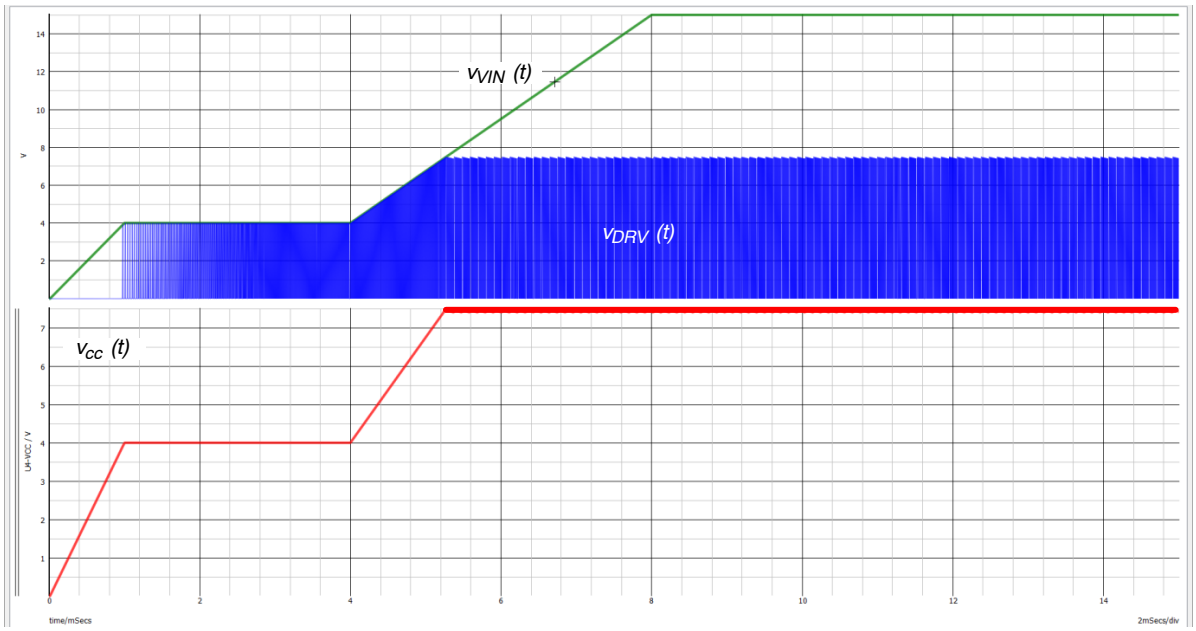


Figure 34. The LDO is Activated During the Start−up Sequence and Powers the Controller

As the LDO supplies the controller, it sees the average current absorbed by the controller. This current is approximately made of $I_{CC(EN)}$ plus the MOSFET driving current leading to a total current equal to:

$$I_{LDO} \approx I_{CC(EN)} + I_{DRV} \approx I_{CC(EN)} + f_{sw}Q_G \quad \text{(eq. 1)}$$

Assume you have selected a MOSFET featuring a 35−nC total gate charge Q_G and operate it at 250 kHz. The average current flowing in the LDO will be:

$$I_{LDO} \approx 4\ m + 250\ k \cdot 35\ n \approx 12.8\ mA \quad \text{(eq. 2)}$$

This current multiplied by the maximum voltage at the VIN pin will define the controller average power dissipation:

$$P_{LDO} = I_{LDO}V_{VIN} \quad \text{(eq. 3)}$$

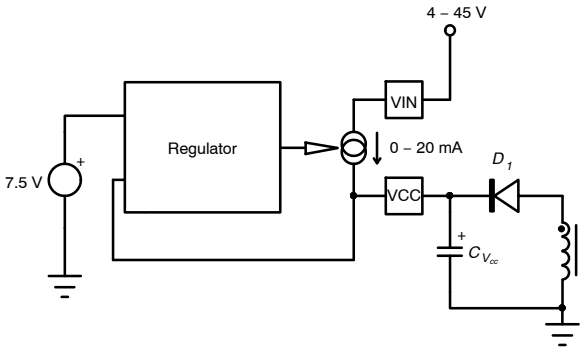
If we assume a $R_{\theta J-A}$ of 130°C/W when the part is soldered on a wide copper area, then the maximum VIN voltage at a 50°C ambient temperature will be:

$$V_{in,max} < \frac{T_j - T_A}{R_{\theta J-A}I_{LDO}} \quad \text{(eq. 4)}$$

Assume a junction temperature limit of 110°C and a maximum ambient of 60°C, then the maximum bias voltage for this circuit *while the LDO is permanently activated* would be:

$$V_{in,max} < \frac{110 - 60}{130 \times 12.8\ m} \approx 30\ V \quad \text{(eq. 5)}$$

Beyond this value, risks exist to damage the die by excessive power dissipation. To benefit from the full voltage range up to 45 V, it is recommended to a) reduce the dissipated power by lowering f_{sw} and adopting a low−Q_G power MOSFET and/or b) add an auxiliary winding to the transformer and use the LDO as a simple one−shot start−up source (Figure 35).



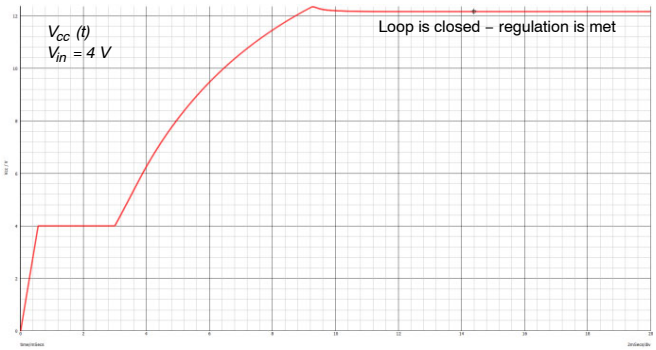


Figure 35. The LDO Can Be Associated with an Auxiliary Winding and Be Turned Off in Normal Operation

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Protecting the VCC Pin

The VCC pin is protected by an over−voltage detection circuitry which immediately reacts as soon as the bias on this pin exceeds 27 V typically (25 V minimum). When the fault happens and lasts more than 7 μs, all pulses are immediately stopped and the circuit remains silent for 1 s. It resumes operation via a soft−start sequence and goes back to normal mode if the fault has gone. This function is there to protect the controller in case you would accidentally supply it with a large voltage on the auxiliary winding for instance if the control loop fails. In some low−voltage applications, you can directly supply the controller from the input rail by shorting the VIN and VCC pins together (Figure 36).

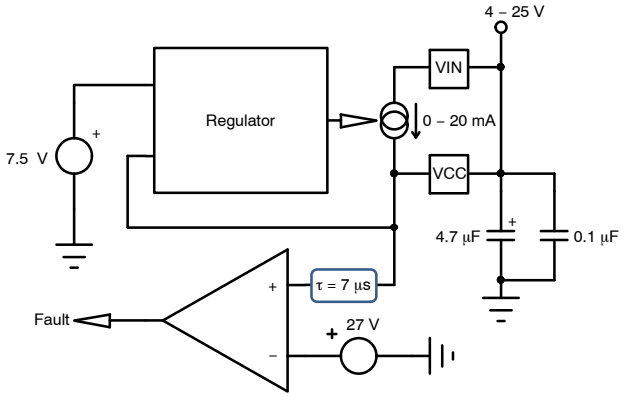


Figure 36. For Low−voltage Applications, it is Possible to Connect the VIN and VCC Pins Together. The OVP on the VCC Pin Remains Active and will Stop Pulses if the Input Rail Exceeds 27 V.

The short circuit between the pins bypasses the LDO and the whole circuit is fed by the input rail. Make sure the input rail voltage always remain below the OVP voltage otherwise the controller will stop working. In the example, the 25−V limit corresponds to the minimum of the OVP specification.

Monitoring the Input Voltage

It is important to check that the converter operates within an authorized input voltage range. For that purpose, the UVLO pin permanently monitors a scaled−down image of the input rail and turns the IC on or off accordingly. A simplified view of the internal circuitry is shown in Figure 37.

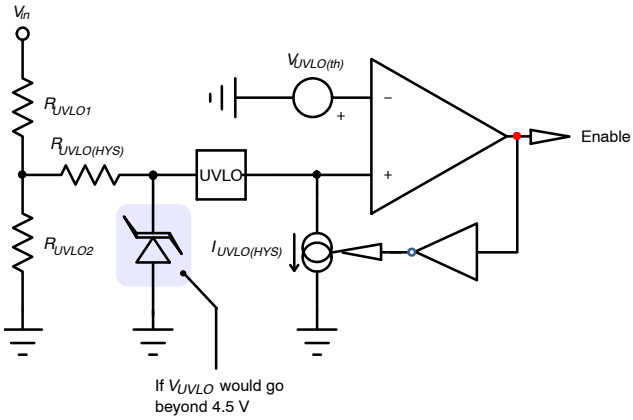


Figure 37. A Comparator Turns The IC On or Off Depending the VIN Pin Bias Level

The turn−on and –off voltages can be obtained using the following formulas:

$$V_{on} = [V_{UV(th)} + (R_{UVLO1} \parallel R_{UVLO2} + R_{HYS})\, I_{UV(HYS)}] \frac{R_{UVLO1} + R_{UVLO2}}{R_{UVLO2}} \quad \text{(eq. 6)}$$

$$V_{off} = (V_{UVLO(th)} - V_{UVLO(HYS)}) \frac{R_{UVLO1} + R_{UVLO2}}{R_{UVLO2}} \quad \text{(eq. 7)}$$

From these expressions, resistors setting the turn−on and −off levels are determined with the below equations in which R_{UVLO2} is arbitrarily fixed:

$$R_{UVLO(HYS)} = \frac{(V_{UVLO(th)} - V_{UVLO(HYS)})\, V_{on} + I_{UVLO(HYS)} R_{UVLO2} (V_{UVLO(th)} - V_{UVLO(hys)}) - V_{off} (V_{UVLO(th)} + I_{UVLO(HYS)} R_{UVLO2})}{I_{UVLO(HYS)} V_{off}} \quad \text{(eq. 8)}$$

$$R_{UVLO1} = \frac{R_{UVLO2} (V_{off} - V_{UVLO(th)} + V_{UVLO(HYS)})}{V_{UVLO(th)} - V_{UVLO(HYS)}} \quad \text{(eq. 9)}$$

As an example, if R_{UVLO2} = 10 kΩ and you select an 8−V turn−on voltage with a 6−V turn−off level, then R_{HYS} = 20 kΩ and R_{UVLO1} = 114 kΩ. The Excel sheet posted on the NCP12711 landing page automates the calculation of these resistors. As a final note, once the resistive divider is determined, it is important to verify that the maximum voltage on the UVLO pin does not approach or exceed its 5.5−V maximum rating at the maximum input voltage. Should it be the case, you will have to install a 4.7−V Zener diode at the UVLO pin to keep the pin voltage within its safe operating area.

Limiting the Power Excursion at High Input Voltage

It is a well−known phenomenon that the maximum power delivered by a flyback converter varies with the input voltage. Assuming a wide input range design, your converter can potentially exhibit more current for the output diode at high line than at low line with detrimental effects for

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reliability. This is because the converter is designed to deliver its nominal power at the lowest input voltage. Transition to DCM and propagation delays are the reason why the power capability changes with the input voltage.

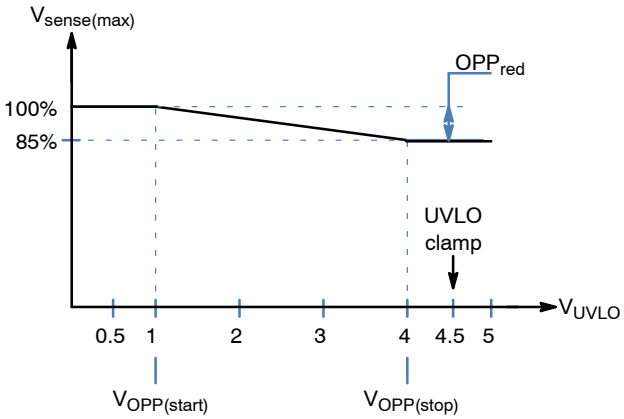


Figure 38. The Maximum Peak Current Reduces with the Input Voltage and Reaches 85% of its Nominal Value at the Highest Input Voltage

NCP12711 embarks an over−power protection (OPP) scheme which reduces the maximum peak current setpoint when the UVLO voltage varies from 1 V (low line) to 4 V where the OPP is no longer active. The peak setpoint will reduce by 15% when the UVLO hits 4 V (Figure 38). An option exists to turn OPP permanently off, please contact sales for that purpose.

Soft−Start Sequence

To limit the stress on primary− and secondary−sides, the NCP12711 incorporates a soft−start circuitry which smoothly increases the peak current setpoint cycle−by−cycle but also sweeps the switching frequency. The converter starts with an almost 0−A setpoint at a 30−kHz frequency and increases this value up to the nominal selection. A capacitor is charged by a 15−μA current source up to 2 V where the sequence has ended. The capacitor is thus selected based on the wanted soft−start duration:

$$C_{SS} = \frac{I_{SS} t_{SS}}{V_{SS(end)}} = \frac{15\,\mu \times 10\,m}{2} = 75\,nF \qquad \text{(eq. 10)}$$

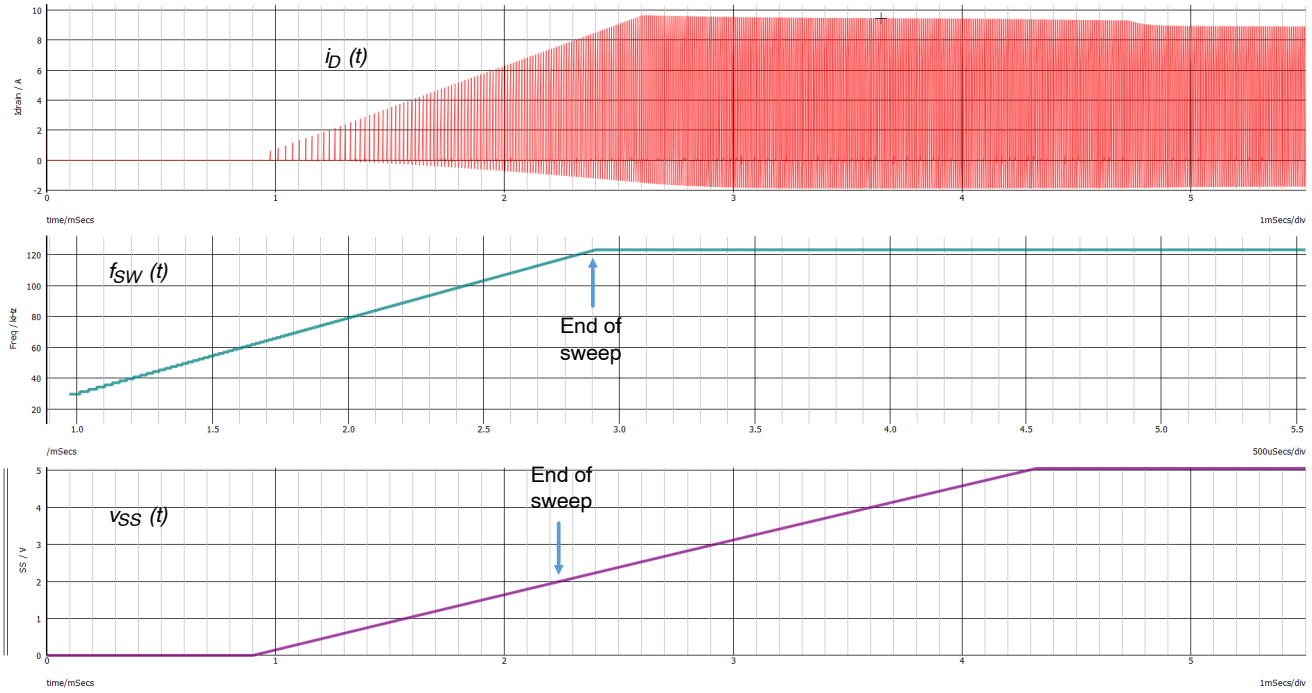


Figure 39. The Peak Current is Smoothly Ramped Up as Well as the Switching Frequency Which Starts from a Low 30 kHz

Figure 39 shows a typical start−up sequence highlighting current and frequency variations during this sequence. Please note the different time scale for the frequency plot.

The frequency sweep ensures the lowest possible stress at power up and is especially interesting when secondary−side synchronous rectification is used: in absence of output voltage, the MOSFET body diode plays the rectifier role until the control circuit takes the lead when sufficiently powered. In absence of a smooth frequency ramp−up, violent voltage spikes can appear across the synchronous MOSFET and may destroy it. A slow frequency increase ensures a limited stress until the synchronous circuit is fully operational.

Feedback and Current Sense

The controller hosts an operational amplifier (op−amp) useful for either non−isolated dc−dc or primary−side−operated isolated flyback converters. The

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output of this op−amp controls the peak current setpoint via a resistive divider associated with a series diode as shown in Figure 40. The voltage−to−peak−current−setpoint division ratio is 8 with a maximum value $V_{CS(LIM)}$ clamped at 250 mV. The maximum inductor current without active OPP is therefore defined as:

$$I_{L,max} = \frac{V_{CS(LIM)}}{R_{sense}} + \frac{V_{in}}{L_p} t_{prop} \quad \text{(eq. 11)}$$

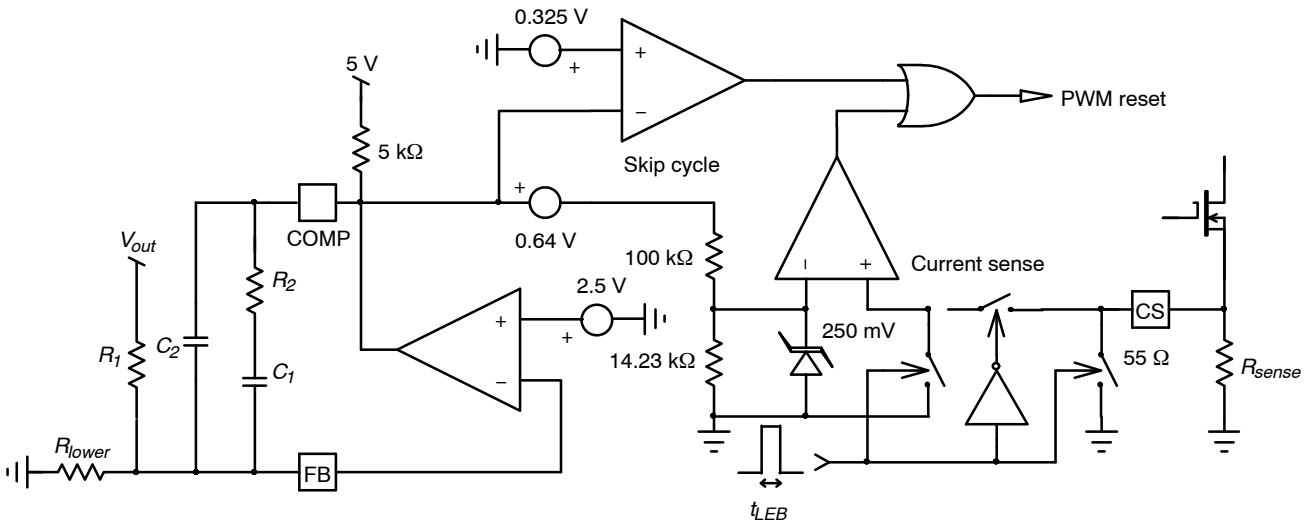


Figure 40. The Series Diode Introduces an Offset Making Sure Skip Cycle Occurs at a 0% Duty Ratio

In which t_{prop} represents the maximum propagation delay from the detection of the over−current event to the effective MOSFET gate pulldown. The IC contributes up to 75 ns to this figure but if you add a gate resistance, this number can grow significantly.

In a current−mode controller, the minimum on−time duration is set by the propagation delay and the leading−edge blanking duration. The sum of both variables gives the minimum t_{on}. When the load current is getting lighter, the op−amp pulls the COMP pin down in an attempt to reduce the peak current setpoint. The voltage on the COMP decreases until the minimum on−time is reached. With the NCP12711, this minimum t_{on} is around 135 ns and despite a COMP pin going further down, it cannot be reduced. Thus, there is always a little bit of energy that is transmitted cycle by cycle from the primary to the secondary side. An output voltage runaway in a flyback converter is therefore possible in a no−load condition. To avoid this situation, a diode drop (≈ 640 mV) is inserted with the feedback voltage setting the peak current. For the maximum peak value, the COMP pin will be biased at the following level:

$$V_{COMP} = V_{CS(LIM)} \times k_{PWM} + V_f = 0.25 \times 8 + 0.64 = 2.64\ V \quad \text{(eq. 12)}$$

On the opposite, the minimum current will be reached when V_{COMP} falls below 0.64 V. The dynamic on the COMP pin can therefore be depicted by the graph shown in Figure 41 with simulation data. At power up, the loop asks for the maximum peak current and regulates when the target is met. Considering a light−load condition, the loop will reduce the setpoint to a minimum so as to keep V_{out} in regulation. The output pulses can reduce down to the smallest possible ones and equal LEB plus propagation delay, including the MOSFET turn−off time. If the loop asks for less than this value, the peak current is frozen to this minimum value:

$$I_{p,min} = \frac{V_{in}}{L_p} (t_{LEB} + t_{prop}) \quad \text{(eq. 13)}$$

Assuming a 5−μH primary inductance L_p with a 40−V input voltage and a 150−ns pulse duration, the peak current cannot be below 1.2 A. If the load keeps decreasing, an output voltage runaway can happen as peak current can no longer be reduced: regulation is lost. To avoid an over−voltage situation, the controller hosts a skip cycle comparator which shuts pulses off when the feedback is out of its normal dynamic range. When V_{COMP} keeps going down in an attempt to regulate (with no action of course), it reaches 325 mV and all pulses are stopped. As V_{out} is now falling in lack of pulses, the COMP pin slightly goes up again and authorizes pulses until COMP goes low. This is skip cycle operation. Unlike other controller where skip is programmed at 10 – 15% peak current, here it only activates when the regulation is lost. Thus, if you do not want to see skip cycle in your application, either install a dummy output load (a bleeder) or reduce the output resistance of the feedback divider so that it draws enough current to maintain V_{COMP} above 640 mV.

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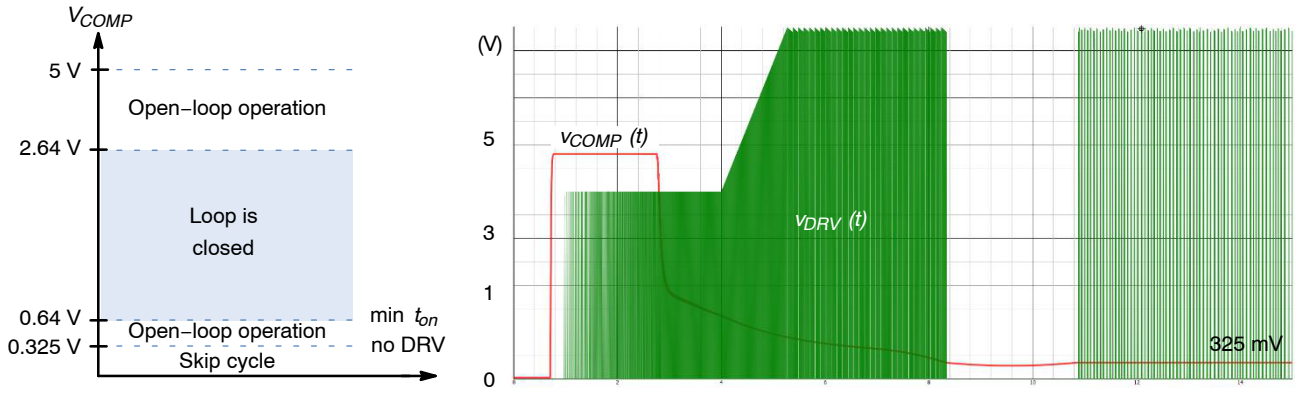


Figure 41. The COMP Pin Swings between 2.64 V and 0.64 V for a 0−A Peak Setpoint. Skip Cycle Operation Happens when the Loop Fails to Regulate at the Lowest Possible Peak Current Setpoint.

Slope Compensation

Current−mode power supplies are prone to sub−harmonic oscillations. This is because the inner current−loop gain crossover frequency is too high and there is no phase margin at this point. The condition happens when the converter operates in continuous conduction mode (CCM) with a duty ratio approaching 50%. A simple cure for these sub−harmonic oscillations is to inject a compensation ramp S_e which will reduce the current−loop gain. It can be done in several ways but the simplest one is to sum the ramp with the current sense information. NCP12711 integrates an artificial ramp derived from the oscillator. Once buffered, it biases the CS pin via a 20−kΩ resistor (Figure 42) only during the on−time. Inserting a resistance in series with the sensed voltage offers a simple means to adjust the compensation effort. If you do not want compensation, simply reduce this resistance or suppress it provided your PCB layout is clean.

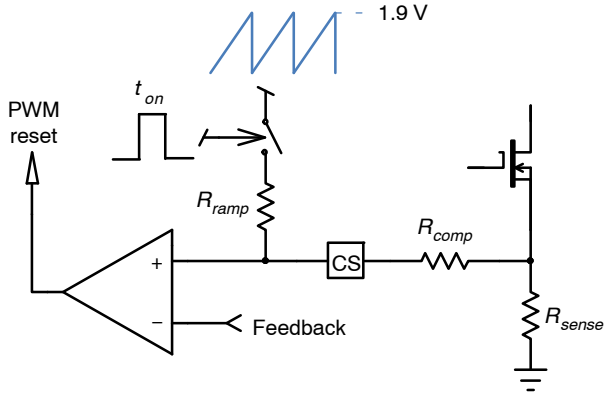


Figure 42. You Can Easily Adjust the Slope Compensation Level you Need by Inserting a Resistance in Series with the CS Pin

To determine the value of R_{comp}, you first need to determine the primary−side inductor current downslope S_f. Once scaled to volts per second via the sense resistance, we have:

$$S_f = \frac{V_{out} + V_f}{NL_p} R_{sense} \qquad \text{(eq. 14)}$$

In which V_f is the secondary−side rectifier drop, N is the 1:N transformer turns ratio, L_p the primary−side inductance and R_{sense} the current sensing resistance. The compensation slope is given in the data−sheet and depends on the selected switching period:

$$S_e = \frac{V_{ramp}}{D_{max} T_{sw}} \qquad \text{(eq. 15)}$$

Now, compute the division ratio value between S_e, the existing ramp level and what you want to inject. If we select a compensation level equal to 50% of the inductor downslope current, then the division ratio equals:

$$\text{divratio} = \frac{0.5 \times S_f}{S_e} = \frac{0.5 \cdot D_{max} R_{sence} T_{sw} (V_{out} + V_f)}{L_p N V_{ramp}} \qquad \text{(eq. 16)}$$

Then, the resistance to add in series with the CS pin is simply:

$$R_{comp} = \text{divratio} \times R_{ramp} \qquad \text{(eq. 17)}$$

Assume the following data: L_p = 5 µH, R_{sense} = 0.03 Ω, D_{max} = 90%, F_{sw} = 100 kHz, R_{ramp} = 20 kΩ, N = 1.25 and V_{ramp} = 1.9 V. Applying the above formulas to a 5−V converter leads to a compensation resistance value of 1.4 kΩ:

$V_{out} := 5\ V \quad N_{turns} := 1.25 \quad R_{ramp} := 20\ k\Omega \quad R_{sense} := 0.03\ \Omega$

$L_p := 5\ \mu H \quad D_{max} := 90\% \quad F_{sw} := 100\ kHz \quad k_{comp} := 50\%$

$V_{ramp} := 1.9\ V \quad T_{sw} := \frac{1}{F_{sw}} \quad V_f := 0.5\ V$

$S_e := \frac{V_{ramp}}{T_{sw}} = 0.19\ \frac{V}{\mu s} \qquad S_f := \frac{V_{out} + V_f}{N_{turns} \cdot L_p} \cdot R_{sense} = 0.026\ \frac{V}{\mu s}$

$$\text{divratio} := \frac{k_{comp} \cdot S_f}{S_e} = 0.069$$

$$R_{comp} := R_{ramp} \cdot \text{divratio} = 1.389 \times 10^3\ \Omega$$

$$\frac{k_{comp} \cdot R_{sense} \cdot T_{sw} \cdot (V_{out} + V_f)}{L_p \cdot N_{turns} \cdot V_{ramp}} \cdot R_{ramp} = 1.389\ k\Omega$$

Figure 43. The Compensation Resistance is Easily Determined with a few Calculation Steps

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Short Circuit Protection

If the loop asks for the maximum power, the peak−current setpoint is clamped to 250 mV (no OPP). When this happens, the controller arms an error flag signaling a fault condition. This naturally occurs during the start−up sequence until the converter regulates and resets the flag. A fault timer of 30 ms starts every time the error flag is asserted. When the timer reaches completion, all pulses are stopped and the part remains silent for 1 s. If the auxiliary winding disappears during the 1−s off−mode, the LDO takes over and supplies the part. At the end of the 1−s period, a fresh start−up sequence takes place with soft−start and frequency sweep. If the fault has disappeared, the converter recovers and resumes operation. If the fault is still present, a new 1−s off−mode takes place and the converter keeps ticking as long as the fault remains. Figure 44 describes a start−up sequence leading to a regulated output and suddenly followed by an output short circuit. The error flag is asserted immediately and the timer starts counting. During this time, the peak current is pushed to the maximum value. When the timer has elapsed, all pulses stop and the 1−s off−time period starts. Then the power supply attempts to resume operations (not shown). The overload timer is set to 30 ms but longer periods of time are available upon request to the factory. Please contact your sales person for more information.

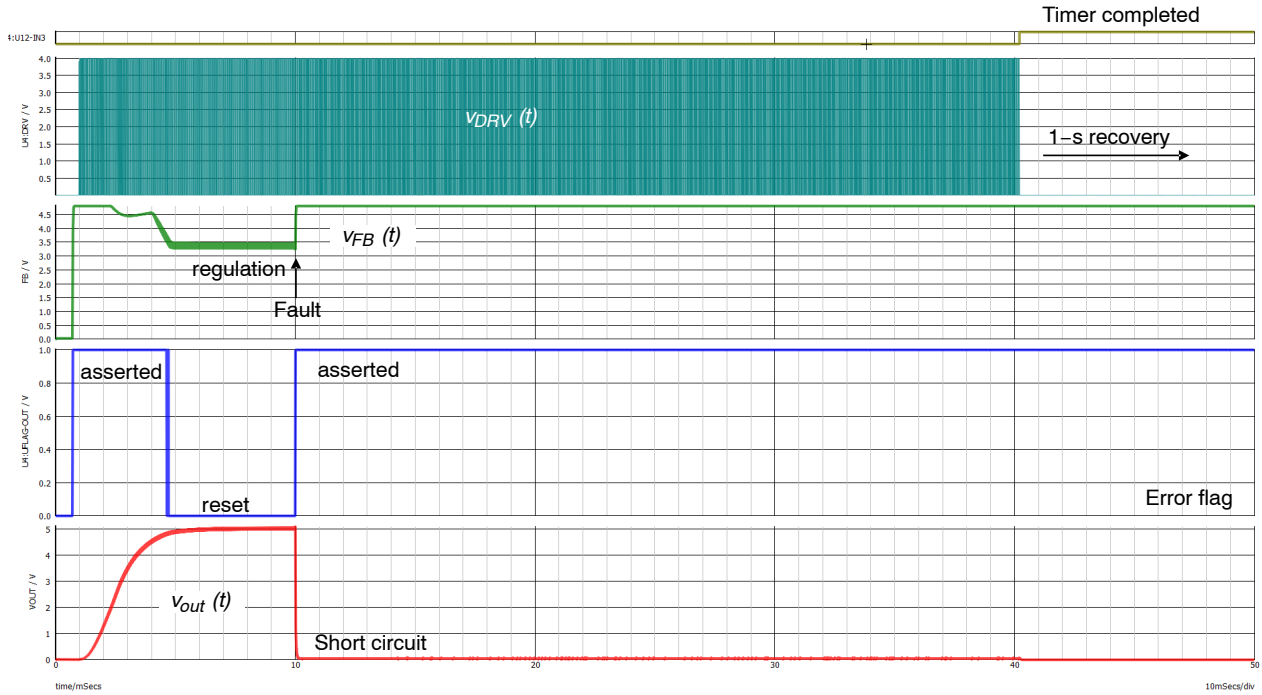


Figure 44. The Circuit Auto−recovers from a Short Circuit or an Overload Situation

In case the peak current measured at the CS pin largely exceeds the 250−mV voltage setpoint, a second over−current comparator trips. This second comparator benefits from a smaller LEB duration (60 ns versus 110 ns) and reacts in case the sensed voltage exceeds the 250−mV limit by 25%: $V_{SCP(LIM)}$. When such an event occurs, e.g. when the secondary diode fails shorted, the controller counts 4 consecutive events and stops all pulses immediately. The part then waits 1 s before attempting to restart. The internal circuitry appears in Figure 45.

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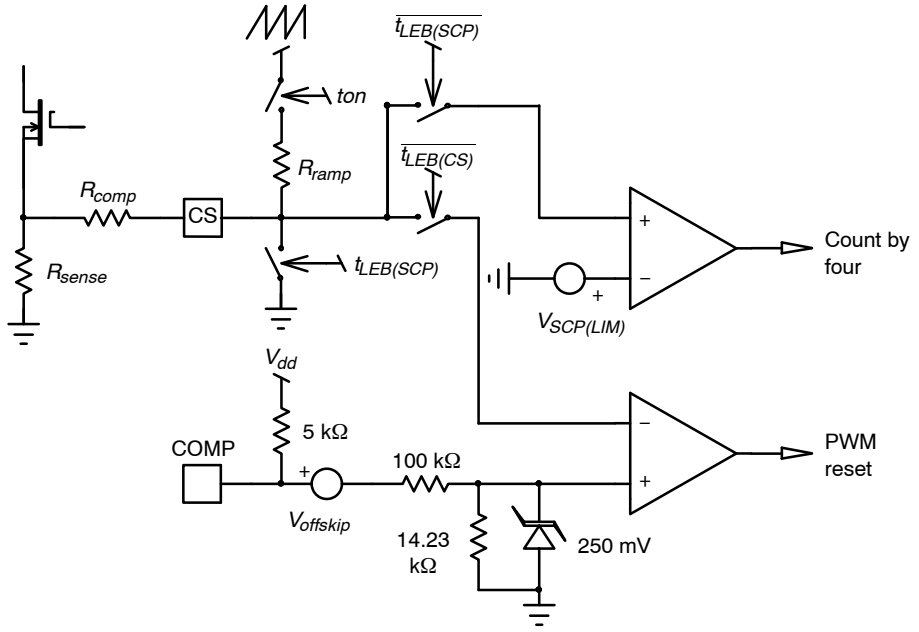


Figure 45. If the Current Sense Pin Exceeds the Maximum Cycle−by−cycle Limit by 25%, a Counter Records the Event and Stops All Pulses after 4 Consecutive Events

Operational Amplifier

The on−board op−amp exhibits a gain−bandwidth product (GBW) of 1.4 MHz with a low−frequency pole located at 53 Hz. It features an open−drain configuration loaded by the internal 5−kΩ pull−up resistor. With this circuit, it is possible to implement a type 2 compensator hosting a pole at the origin, one zero and one pole. Such configuration is shown in Figure 46 with its typical ac response in the right side. The type 2 lends itself well to stabilizing current−mode dc−dc converters. The characteristics of such compensator are described by the following transfer functions:

$$G(s) = -G_0 \frac{1 + \frac{\omega_z}{s}}{1 + \frac{s}{\omega_p}} \quad \text{(eq. 18)}$$

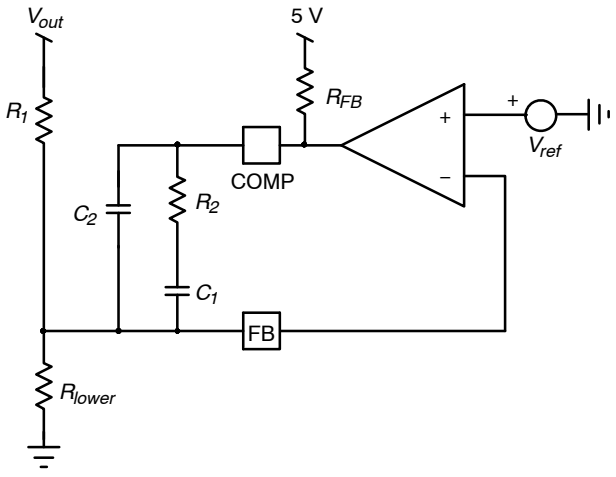
In which:

$$G_0 = \frac{R_2}{R_1}\frac{C_1}{C_1 + c_2} \approx \frac{R_2}{R_1} \quad \text{(eq. 19)}$$

$$\omega_z = \frac{1}{R_2 C_1} \quad \text{(eq. 20)}$$

$$\omega_p = \frac{1}{R_2 \frac{C_1 C_2}{C_1 + C_2}} \approx \frac{1}{R_2 C_1} \quad \text{(eq. 21)}$$

Approximated formulas are valid when we have $C_2 << C_1$.



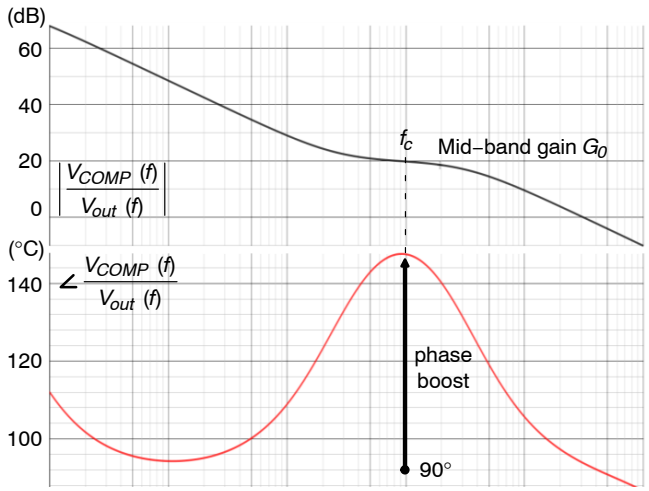


Figure 46. The On−board op−amp Lets you Realize a Type 2 Compensator which is Adequate for Stabilizing Current−mode dc−dc Converters

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The op−amp own characteristic can be neglected if the selected crossover frequency is moderate, around the kHz for instance. However, if you plan to extend crossover at 10 kHz or so, then it is important to verify the compensator response once the op−amp characteristic is accounted for especially if a high gain is required at crossover. A separate application note covers a compensation exercise in details.

NCP12711 lends itself well to opto−isolated applications also. Just ground the feedback pin and connect the opto−coupler collector to the COMP pin with a capacitor for the pole generation together with R_{FB}.

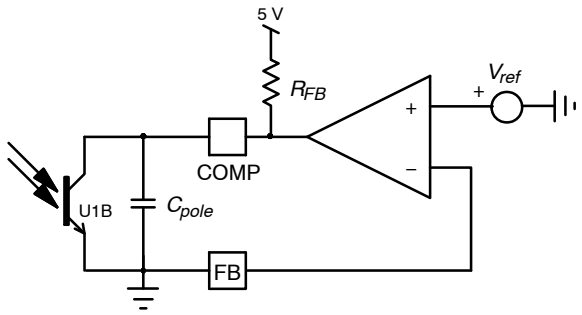


Figure 47. If you Tie the FB Pin to Ground, then an Opto−isolator Can Pull the COMP Pin Down for Regulation Purposes

Oscillator

The oscillator lets you select a switching frequency from 100 kHz up to 1 MHz. By pulling the R_t pin to ground via a resistance, it is possible to select the switching frequency. The curve from Figure 48 links the switching frequency with the resistance value. An approximate formula lets you also determine the resistance as follows:

$$R_t \approx \frac{8.9 \cdot 10^9}{F_{sw} - 30\ k} \qquad \text{(eq. 22)}$$

Assuming a wanted 100−kHz operation, you would select a resistance of

$$R_t = \frac{8.9 \cdot 10^9}{100\ k - 30\ k} \approx 127\ k\Omega \qquad \text{(eq. 23)}$$

A quick experiment on the prototype will let you know if you need to keep or slightly adjust this value. The following array suggest values for some typical switching frequencies:

Table 1.

Frequency (kHz)	R_t (kΩ)
100	127
150	74.2
200	52.4
250	40.5
300	33
350	27.8
400	24

For stability reasons, it is usually not recommended to decouple the R_t pin with a capacitor.

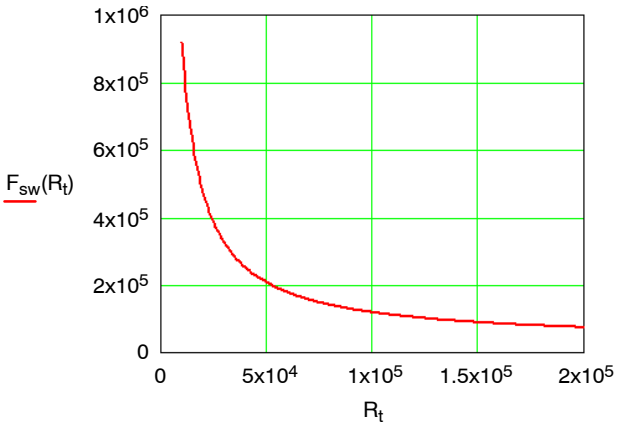


Figure 48. You Can Extract the R_t Resistance Value from the Graph or Compute it with the Approximate Expression

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Application Circuits

The NCP12711 can be used in a variety of applications. Figure 49 represents a 100−kHz flyback converter regulating the auxiliary winding at 12 V. This is a wide−range application since the board operates from a 4−V input voltage up to 45 V. the precision

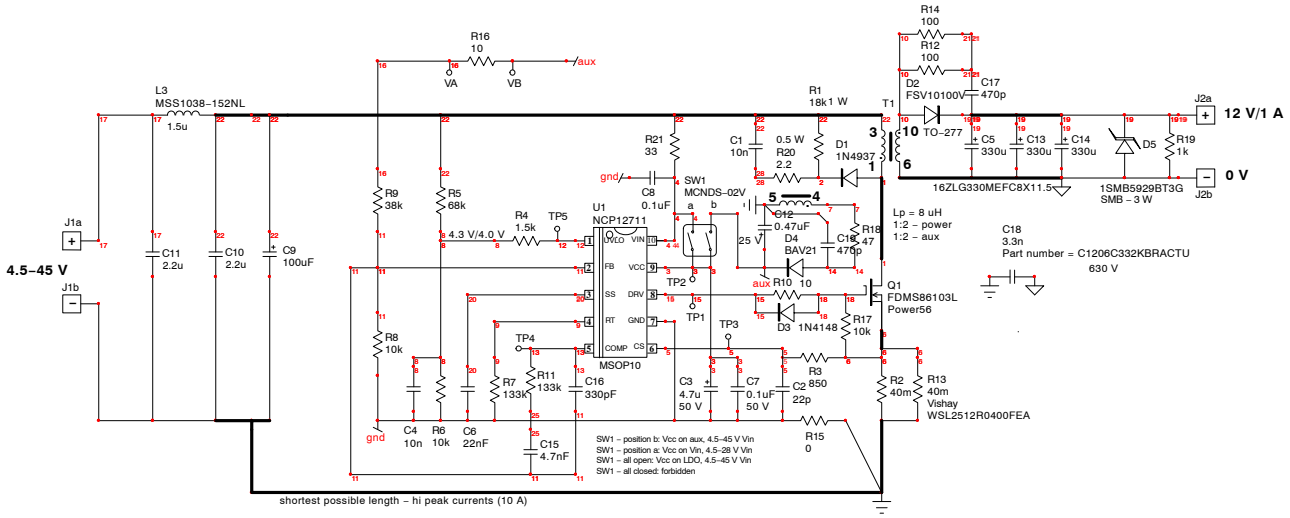


Figure 49. 4.5 − 45 V Input Voltage Isolated Flyback Converter Delivering 12 V/1 A

Figure 50 represents a 5−V/2−A application circuit operated from a 4.5−to−10−V input source, a typical industrial board−mounted module. A synchronous rectifier ensures a good overall efficiency. There is no auxiliary winding on this board.

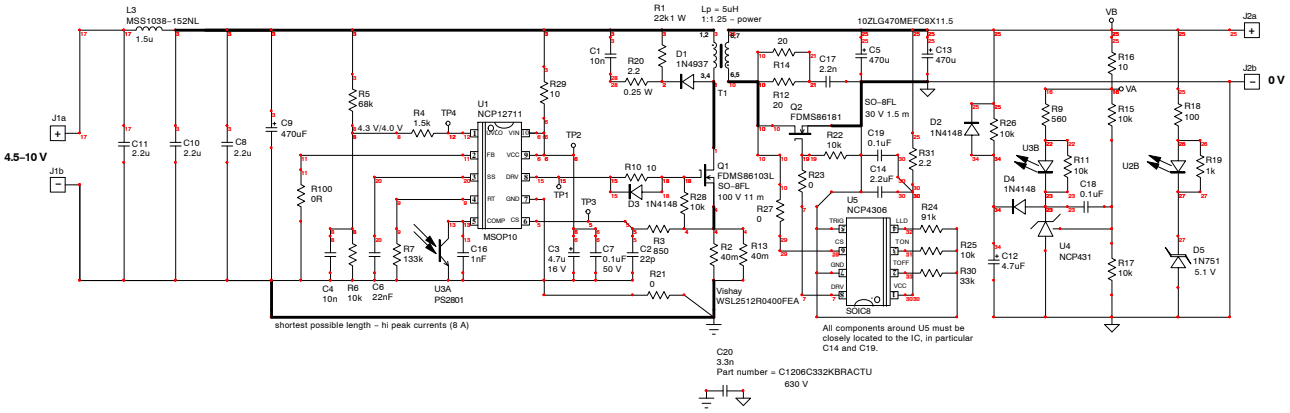


Figure 50. 4.5 − 10 V 5−V/2−A Opto−isolated dc−dc Flyback Module

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Considering NCP12711 for a non−isolated dc−dc converter such as a SEPIC or a boost is an option as shown in the below figure:

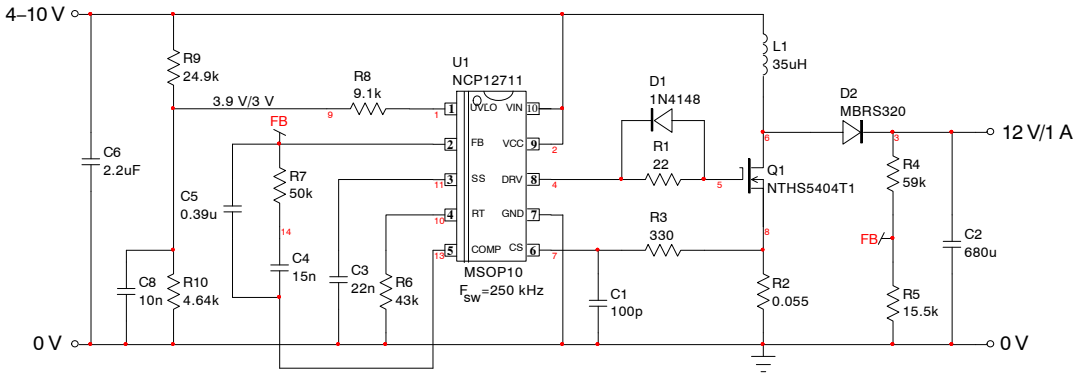


Figure 51. Here an Example of a 250−kHz−operated 12−W Boost Converterc delivers 12 V

Finally, it is also possible to use the NCP12711 as a high−side controller, for instance to build a primary−side−regulated flyback converter operated without an auxiliary winding:

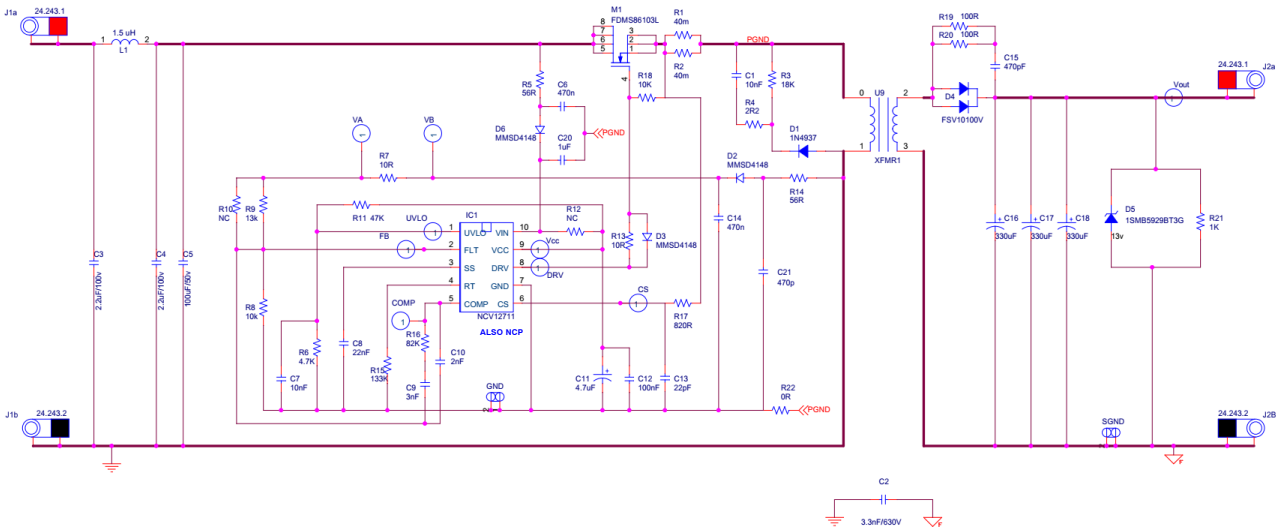


Figure 52. A 100−kHz−operated 12−W Flyback Converter Delivering 12 V without Auxiliary Winding

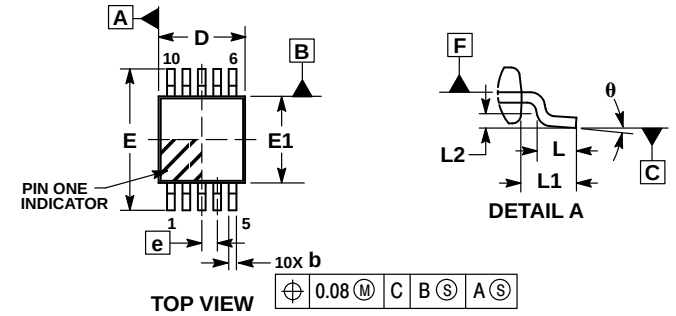
With a 12−V output, the reflected voltage imposes a maximum input voltage limited to 38 V. It can be increased if V_{out} takes on a lower value.

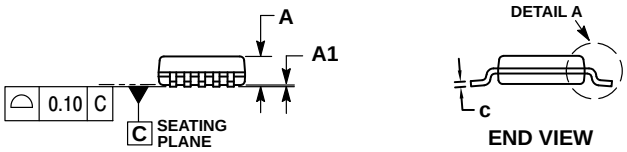
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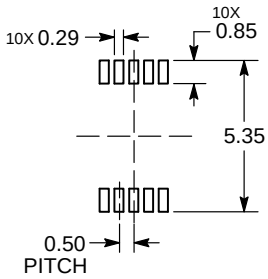




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 MM IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. DIMENSION E DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 MM PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	---	---	1.10
A1	0.00	0.05	0.15
A2	0.75	0.85	0.95
b	0.17	---	0.27
c	0.13	---	0.23
D	2.90	3.00	3.10
E	4.75	4.90	5.05
E1	2.90	3.00	3.10
e	0.50 BSC		
L	0.40	0.70	0.80
L1	0.95 REF		
L2	0.25 BSC		
θ	0°	---	8°

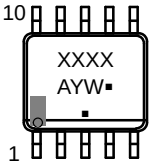
RECOMMENDED SOLDERING FOOTPRINT*



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*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present and may be in either location. Some products may not follow the Generic Marking.

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