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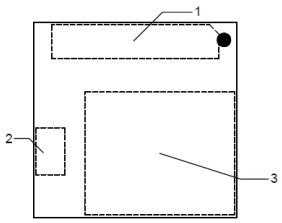
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Features

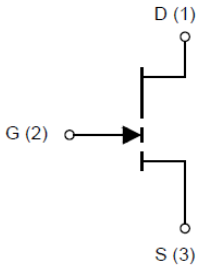
- 100V enhancement mode power transistor
- Bottom-side cooled configuration
- $R_{DS(on)}$ = 16 mΩ
- $I_{DS(max)}$ = 38 A
- Ultra-low FOM Island Technology® die
- Low inductance GaN*PX*® package
- Simple gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 V / +10 V)
- Very high switching frequency (> 10 MHz)
- Fast and controllable fall and rise times
- Reverse current capability
- Zero reverse recovery loss
- Small 4.6 x 4.4 mm^2 PCB footprint
- RoHS 3 (6+4) compliant



Package Outline



Circuit Symbol



Applications

- Enterprise and networking power
- Uninterruptable power supplies
- Industrial motor drives
- Solar power
- Fast battery charging
- Class D audio amplifiers
- Smart home
- Wireless Power Transfer

Description

The GS61004B is an enhancement mode GaN-on-Silicon power transistor. The properties of GaN allow for high current, high voltage breakdown, high switching frequency. GaN Systems innovates with industry leading advancements such as patented **Island Technology®** and **GaN*PX*®** packaging. **Island Technology®** cell layout realizes high-current die and high yield. **GaN*PX*®** packaging enables low inductance & low thermal resistance in a small package. The GS61004B is a bottom-cooled transistor that offer very low junction-to-case thermal resistance for demanding high power applications. These features combine to provide very high efficiency power switching.

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Absolute Maximum Ratings (T_{case} = 25 °C except as noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	T_J	-55 to +150	°C
Storage Temperature Range	T_S	-55 to +150	°C
Drain-to-Source Voltage	V_{DS}	100	V
Transient Drain to Source Voltage (Note 1)	$V_{DS(transient)}$	120	V
Gate-to-Source Voltage	V_{GS}	-10 to +7	V
Gate-to-Source Voltage - transient (Note 1)	$V_{GS(transient)}$	-20 to +10	V
Continuous Drain Current (T_{case}=25 °C)	I_{DS}	38	A
Continuous Drain Current (T_{case}=100 °C)	I_{DS}	26	A
Pulse Drain Current (Pulse width 50 µs, V_{GS} = 6V) (Note 2)	$I_{DS\ Pulse}$	60	A

(1) For $\leq$ 1 µs

(2) Defined by product design and characterization. Value is not tested to full current in production.

Thermal Characteristics (Typical values unless otherwise noted)

Parameter	Symbol	Value	Units
Thermal Resistance (junction-to-case) – bottom side	$R_{\Theta JC}$	1.2	°C /W
Thermal Resistance (junction-to-ambient) (Note 3)	$R_{\Theta JA}$	28	°C /W
Maximum Soldering Temperature (MSL3 rated)	T_{SOLD}	260	°C

(3) Device mounted on 1.6 mm PCB thickness FR4, 4-layer PCB with 2 oz. copper on each layer. The recommendation for thermal vias under the thermal pad are 0.3 mm diameter (12 mil) with 0.635 mm pitch (25 mil). The copper layers under the thermal pad and drain pad are 25 x 25 mm^2 each. The PCB is mounted in horizontal position without air stream cooling.

Ordering Information

Ordering code	Package type	Packing method	Qty	Reel Diameter	Reel Width
GS61004B-TR	GaN*PX*® bottom cooled	Tape-and-Reel	3000	13" (330mm)	12mm
GS61004B-MR	GaN*PX*® bottom cooled	Mini-Reel	250	7" (180mm)	12mm

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Electrical Characteristics (Typical values at T_J = 25 °C, V_{GS} = 6 V unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	$V_{(BL)DSS}$	100			V	V_{GS} = 0V, I_{DSS} = 25 µA
Drain-to-Source On Resistance	$R_{DS(on)}$		16	22	mΩ	V_{GS} = 6V, T_J = 25 °C I_{DS} = 13.5 A
Drain-to-Source On Resistance	$R_{DS(on)}$		37		mΩ	V_{GS} = 6 V, T_J = 150 °C I_{DS} = 13.5 A
Gate-to-Source Threshold	$V_{GS(th)}$	1.1	1.7	2.6	V	V_{DS} = V_{GS}, I_D = 3.15 mA
Gate-to-Source Current	I_{GS}		100		µA	V_{GS} = 6 V, V_{DS} = 0 V
Gate Plateau Voltage	V_{plat}		3.5		V	V_{DS} = 50 V, I_D = 38 A
Drain-to-Source Leakage Current	I_{DSS}		0.3	25	µA	V_{DS} =100 V, V_{GS} = 0 V T_J = 25°C
Drain-to-Source Leakage Current	I_{DSS}		50		µA	V_{DS} = 100 V, V_{GS} = 0 V T_J = 150 °C
Internal Gate Resistance	R_G		0.9		Ω	f = 5 MHz, open drain
Input Capacitance	C_{ISS}		260		pF	V_{DS} = 50 V V_{GS} = 0 V f = 100 kHz
Output Capacitance	C_{OSS}		110		pF	
Reverse Transfer Capacitance	C_{RSS}		5		pF	
Effective Output Capacitance Energy Related (Note 4)	$C_{O(ER)}$		140		pF	V_{GS} = 0 V V_{DS} = 0 to 50 V
Effective Output Capacitance Time Related (Note 5)	$C_{O(TR)}$		180		pF	
Total Gate Charge	Q_G		3.3		nC	V_{GS} = 0 to 6 V V_{DS} = 50 V I_{DS}= 38 A
Gate-to-Source Charge	Q_{GS}		1.5		nC	
Gate threshold charge	$Q_{G(th)}$		0.8		nC	
Gate switching charge	$Q_{G(sw)}$		1.4		nC	
Gate-to-Drain Charge	Q_{GD}		0.7		nC	
Output Charge	Q_{OSS}		9		nC	V_{GS} = 0 V, V_{DS} = 50 V
Reverse Recovery Charge	Q_{RR}		0		nC	
Output Capacitance Stored Energy	E_{OSS}		0.2		µJ	V_{GS} = 0 V, V_{DS} = 50 V f = 100 kHz

(4) $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}

(5) $C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}

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Electrical Performance Graphs

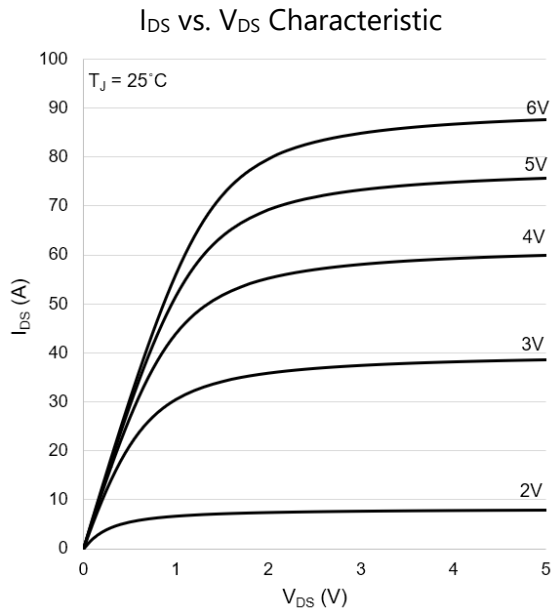


Figure 1: Typical I_{DS} vs. V_{DS} @ T_J = 25 °C

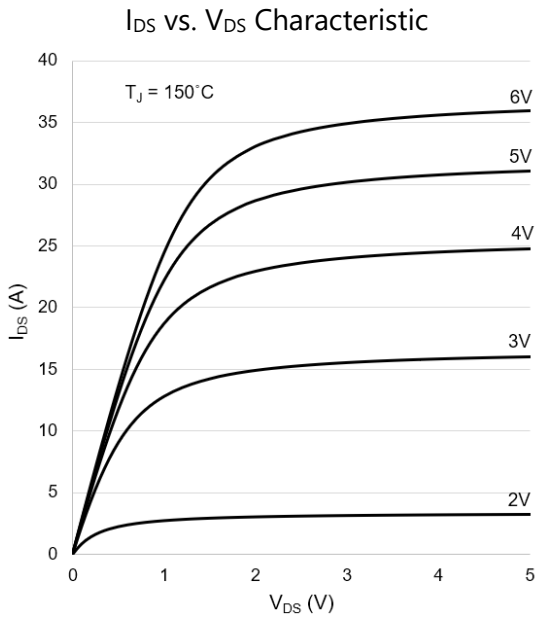


Figure 2: Typical I_{DS} vs. V_{DS} @ T_J = 150 °C

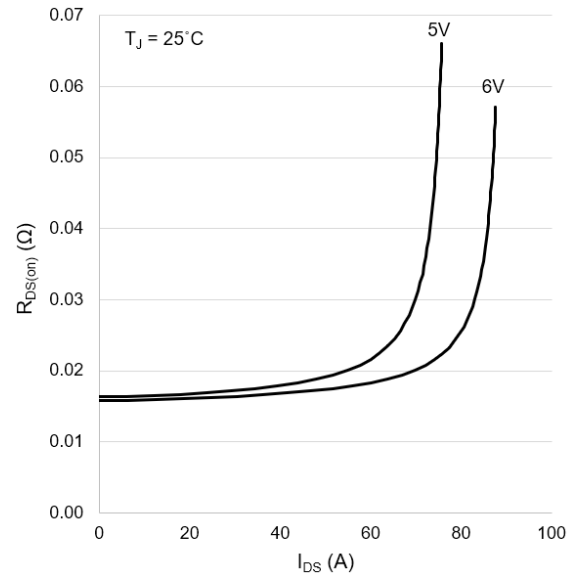


Figure 3: $R_{DS(on)}$ vs. I_{DS} at T_J = 25 °C

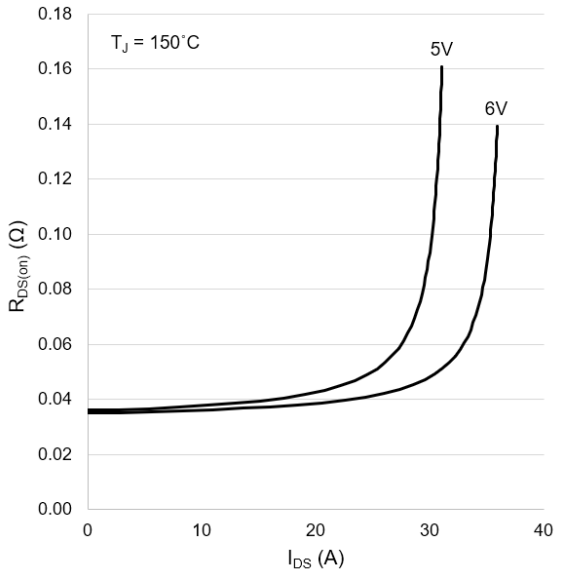


Figure 4: $R_{DS(on)}$ vs. I_{DS} at T_J = 150 °C

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Electrical Performance Graphs

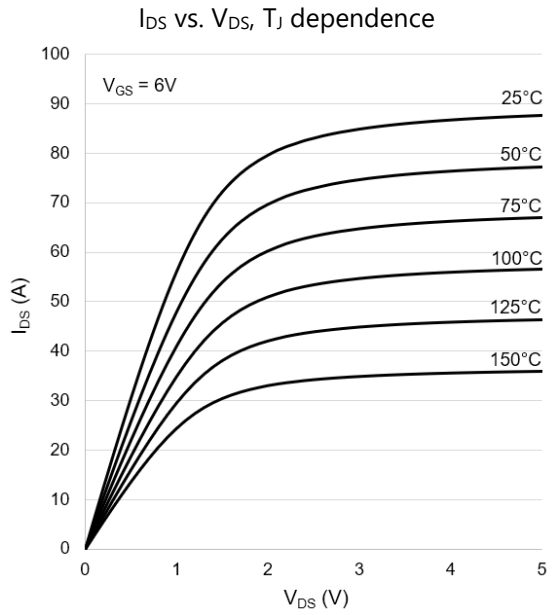


Figure 5: Typical I_{DS} vs. V_{DS} @ V_{GS} = 6 V

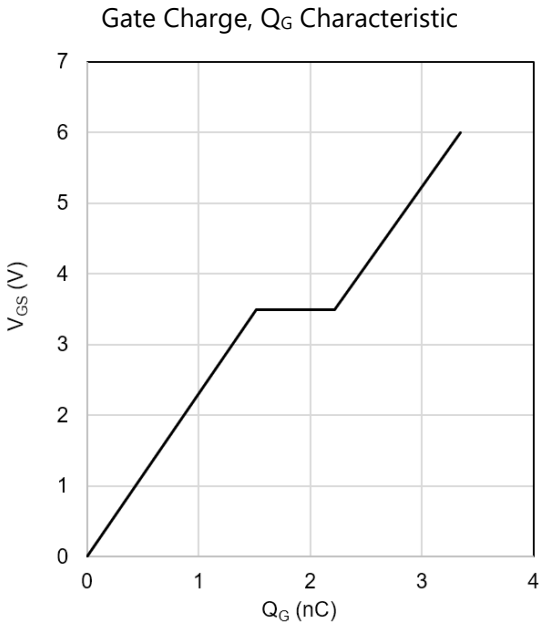


Figure 6: Typical V_{GS} vs. Q_G @ V_{DS} = 50 V

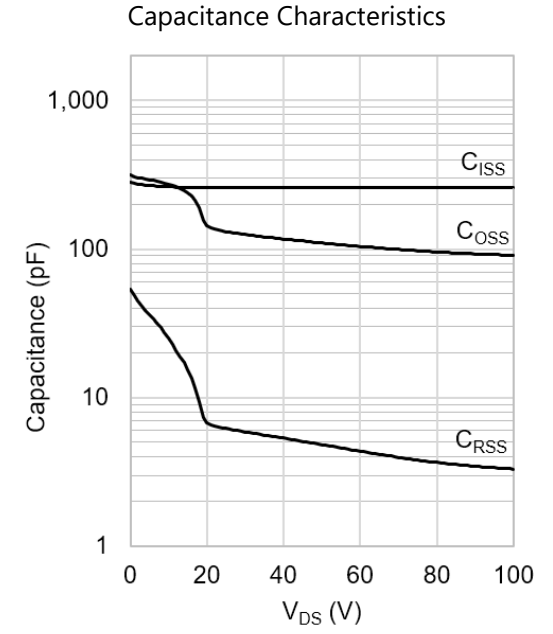


Figure 7: Typical C_{ISS}, C_{OSS}, C_{RSS} vs. V_{DS}

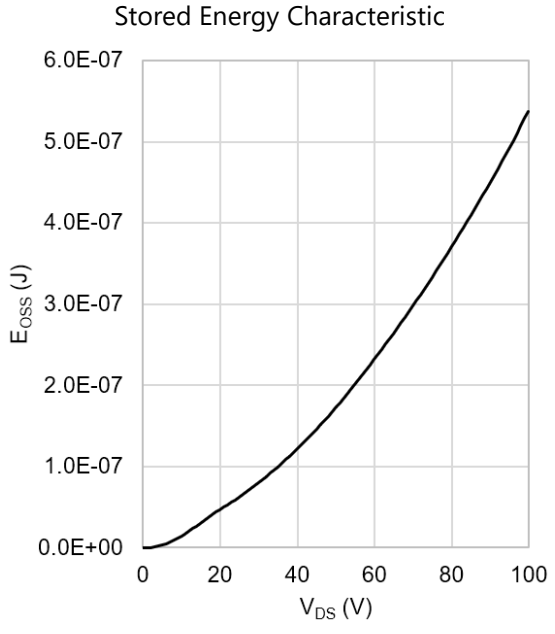


Figure 8: Typical C_{OSS} Stored Energy

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Electrical Performance Graphs

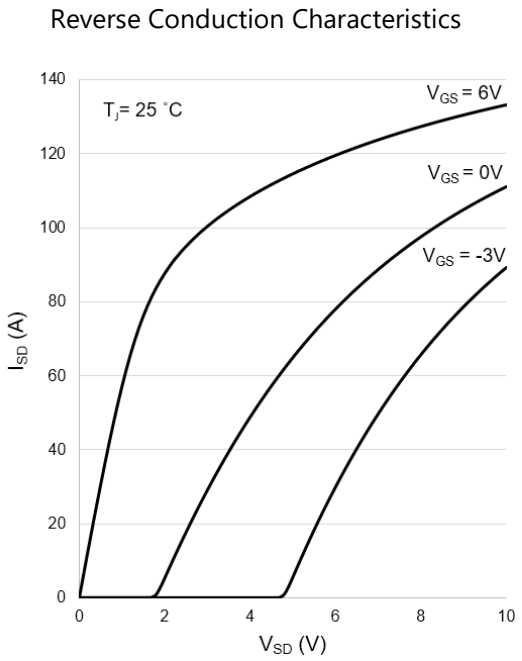


Figure 9: Typical I_{SD} vs. V_{SD} at 25 ˚C

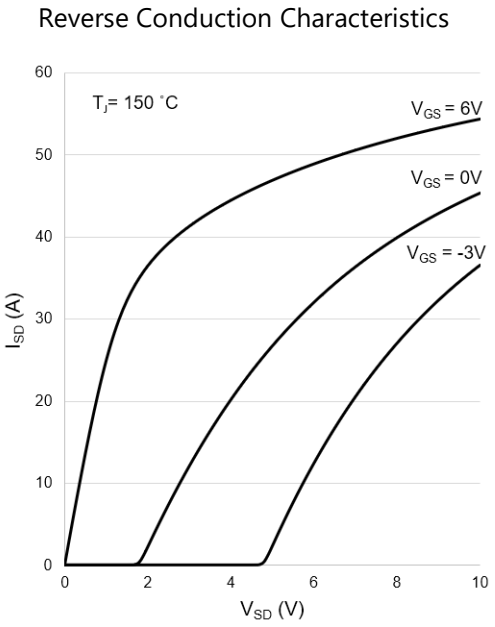


Figure 10: Typical I_{SD} vs. V_{SD} at 150 ˚C

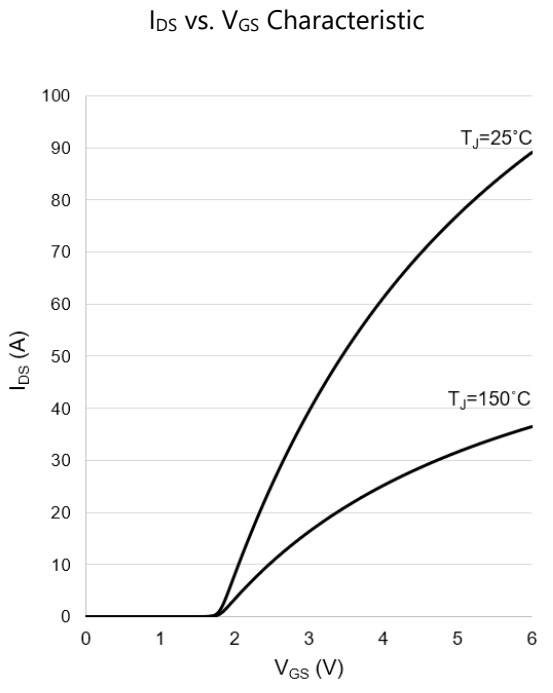


Figure 11: Typical I_{DS} vs. V_{GS}

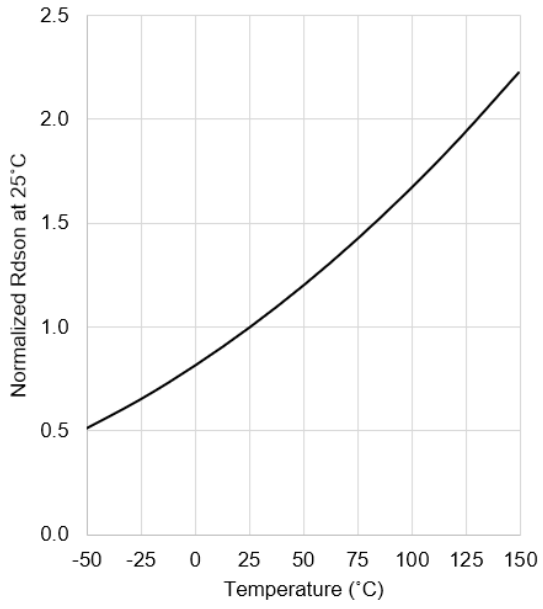


Figure 12: Normalized $R_{DS(on)}$ as a function of T_J

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Thermal Performance Graphs

I_{DS} - V_{DS} SOA

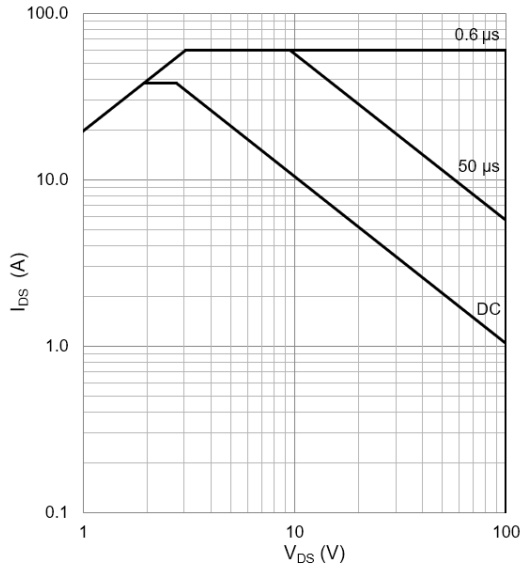


Figure 13: Safe Operating Area @ T_{case} = 25 °C

Power Dissipation – Temperature Derating

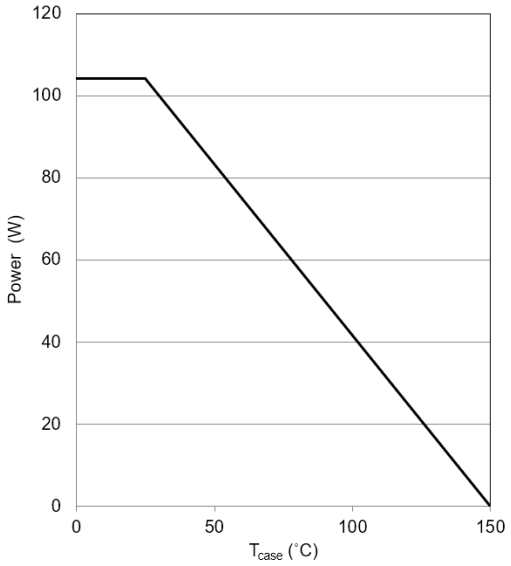


Figure 14: Derating vs. Case Temperature

Transient $R_{\theta JC}$

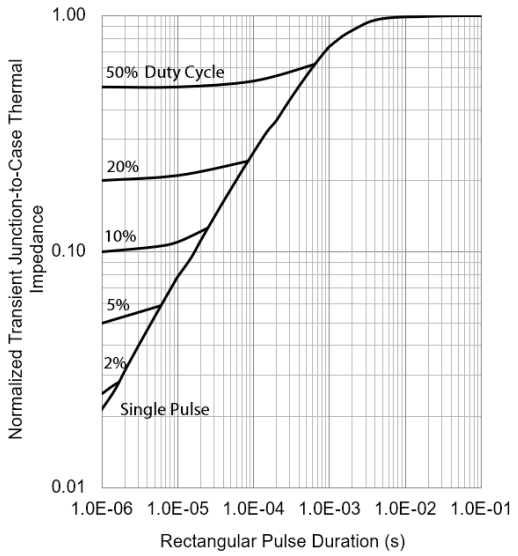


Figure 15: Transient Thermal Impedance
1.00 = Nominal DC thermal impedance

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Application Information

Gate Drive

The recommended gate drive voltage range, V_{GS}, is 0 V to + 6 V for optimal $R_{DS(on)}$ performance. Also, the repetitive gate to source voltage, maximum rating, $V_{GS(AC)}$, is +7 V to -10 V. The gate can survive non-repetitive transients up to +10 V and – 20 V for pulses up to 1 µs. These specifications allow designers to easily use 6.0 V or 6.5 V gate drive settings. At 6 V gate drive voltage, the enhancement mode high electron mobility transistor (E-HEMT) is fully enhanced and reaches its optimal efficiency point. A 5 V gate drive can be used but may result in lower operating efficiency. Inherently, GaN Systems E-HEMTs do not require negative gate bias to turn off. Negative gate bias, typically V_{GS} = -3 V, ensures safe operation against the voltage spike on the gate, however it may increase reverse conduction losses if not driven properly. For more details, please refer to the gate driver application note "GN001 How to Drive GaN Enhancement Mode Power Switching Transistors" at www.gansystems.com

Similar to a silicon MOSFET, the external gate resistor can be used to control the switching speed and slew rate. Adjusting the resistor to achieve the desired slew rate may be needed. Lower turn-off gate resistance, $R_{G(OFF)}$ is recommended for better immunity to cross conduction. Please see the gate driver application note (GN001) for more details.

A standard MOSFET driver can be used as long as it supports 6V for gate drive and the UVLO is suitable for 6V operation. Gate drivers with low impedance and high peak current are recommended for fast switching speed. GaN Systems E-HEMTs have significantly lower Q_G when compared to equally sized $R_{DS(on)}$ MOSFETs, so high speed can be reached with smaller and lower cost gate drivers.

Many non-isolated half bridge MOSFET drivers are not compatible with 6 V gate drive for GaN enhancement mode HEMT due to their high under-voltage lockout threshold. Also, a simple bootstrap method for high side gate drive will not be able to provide tight tolerance on the gate voltage. Therefore, special care should be taken when you select and use half bridge drivers. Alternatively, isolated drivers can be used for a high side device. Please see the gate driver application note (GN001) for more details.

Parallel Operation

Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible.

GaN enhancement mode HEMTs have a positive temperature coefficient on-state resistance which helps to balance the current. However, special care should be taken in the driver circuit and PCB layout since the device switches at very fast speed. It is recommended to have a symmetric PCB layout and equal gate drive loop length (star connection if possible) on all parallel devices to ensure balanced dynamic current sharing. Adding a small gate resistor (1-2 Ω) on each gate is strongly recommended to minimize the gate parasitic oscillation.

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Source Sensing

Although the device does not have a dedicated source sense pin, the GaN*PX*® packaging utilizes no wire bonds so the source connection is already very low inductance. By simply using a dedicated "source sense" connection with a PCB trace from the gate driver output ground to the Source pad in a kelvin configuration with respect to the gate drive signal, the function can easily be implemented. It is recommended to implement a "source sense" connection to improve drive performance.

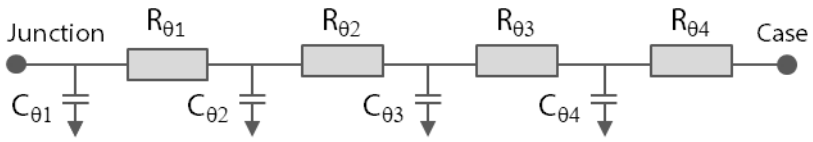
Thermal

The substrate is internally connected to the source/thermal pad a on the bottom side of the package. The transistor is designed to be cooled using the printed circuit board. The Drain pad is not as thermally conductive as the thermal pad. However, adding more copper under this pad will improve thermal performance by reducing the package temperature.

Thermal Modeling

RC thermal models are available to support detailed thermal simulation using SPICE. The thermal models are created using the Cauer model, an RC network model that reflects the real physical property and packaging structure of our devices. This thermal model can be extended to the system level by adding extra R_θ and C_θ to simulate the Thermal Interface Material (TIM) or Heatsink.

RC thermal model



RC breakdown of $R_{\Theta JC}$

R_θ (°C/W)	C_θ (W·s/°C)
$R_{\theta 1}$ = 0.045	$C_{\theta 1}$ = 2.5E-05
$R_{\theta 2}$ = 0.55	$C_{\theta 2}$ = 2.0E-04
$R_{\theta 3}$ = 0.57	$C_{\theta 3}$ = 1.9E-03
$R_{\theta 4}$ = 0.035	$C_{\theta 4}$ = 0.9E-04

For more detail, please refer to Application Note GN007 "Modeling Thermal Behavior of GaN Systems' GaN*PX*® Using RC Thermal SPICE Models" available at www.gansystems.com

Reverse Conduction

GaN Systems enhancement mode HEMTs do not have an intrinsic body diode and there is zero reverse recovery charge. The devices are naturally capable of reverse conduction and exhibit different characteristics depending on the gate voltage. Anti-parallel diodes are not required for GaN Systems transistors as is the case for IGBTs to achieve reverse conduction performance.

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On-state condition (V_{GS} = +6 V): The reverse conduction characteristics of a GaN Systems enhancement mode HEMT in the on-state is similar to that of a silicon MOSFET, with the I-V curve symmetrical about the origin and it exhibits a channel resistance, $R_{DS(on)}$, similar to forward conduction operation.

Off-state condition (V_{GS} ≤ 0 V): The reverse characteristics in the off-sate are different from silicon MOSFET as the GaN device has no body diode. In the reverse direction, the device starts to conduct when the gate voltage, with respect to the drain, (V_{GD}) exceeds the gate threshold voltage. At this point the device exhibits a channel resistance. This condition can be modeled as a "body diode" with slightly higher V_F and no reverse recovery charge.

If negative gate voltage is used in the off-state, the source-drain voltage must be higher than $V_{GS(th)}+V_{GS(off)}$ in order to turn the device on. Therefore, a negative gate voltage will add to the reverse voltage drop "V_F" and hence increase the reverse conduction loss.

Blocking Voltage

The blocking voltage rating, $V_{(BL)DSS.}$, is defined by the drain leakage current. The hard (unrecoverable) breakdown voltage is approximately 30% higher than the rated $V_{(BL)DSS}$. As a general practice, the maximum drain voltage should be de-rated in a similar manner as silicon MOSFETs. All GaN E-HEMTs do not avalanche and thus do not have an avalanche breakdown rating. The absolute maximum drain-to-source rating is 100 V and doesn't change with negative gate voltage.

Packaging and Soldering

The package material is high temperature epoxy-based PCB material which is similar to FR4 but has a higher temperature rating, thus allowing the device to be specified to 150 °C. The device can handle at least 3 reflow cycles.

It is recommended to use the reflow profile in IPC/JEDEC J-STD-020 REV D.1 (March 2008)

The basic temperature profiles for Pb-free (Sn-Ag-Cu) assembly are:

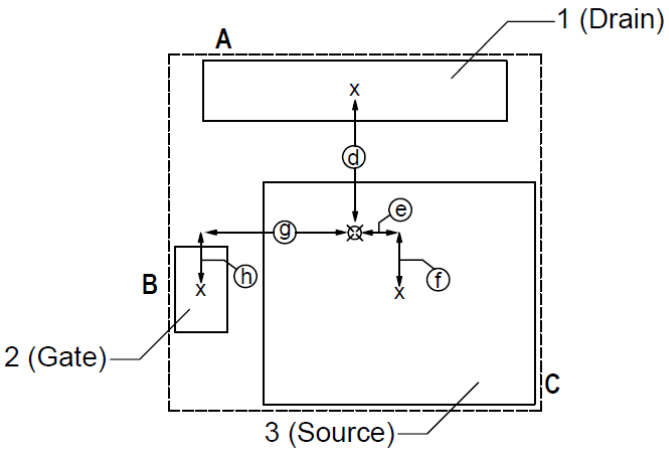
- Preheat/Soak: 60-120 seconds. T_{min} = 150 °C, T_{max} = 200 °C.
- Reflow: Ramp up rate 3°C/sec, max. Peak temperature is 260 °C and time within 5 °C of peak temperature is 30 seconds.
- Cool down: Ramp down rate 6 °C/sec max.

Using "No-Clean" soldering paste and operating at high temperatures may cause a reactivation of the "Non-Clean" flux residues. In extreme conditions, unwanted conduction paths may be created. Therefore, when the product operates at greater than 100 °C it is recommended to also clean the "No-Clean" paste residues.

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Recommended PCB Footprint



Pad sizes

	mm		Inches	
	X (width)	Y (height)	X (width)	Y (height)
A	3.75	0.75	0.148	0.030
B	0.65	1.05	0.026	0.041
C	3.35	2.75	0.132	0.108

Dimensions

	mm	Inches
d	1.75	0.069
e	0.55	0.022
f	0.75	0.030
g	1.90	0.075
h	0.70	0.028

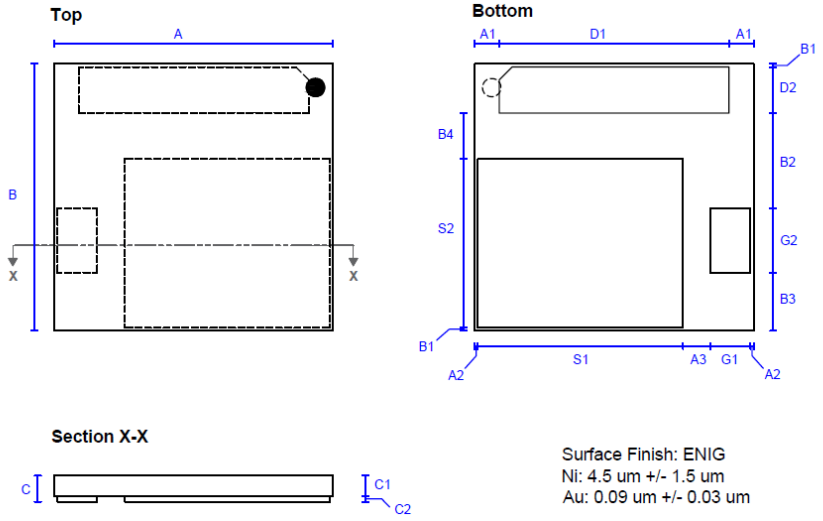
PCB pad openings

Package outline

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Package Dimensions



	mm	Inches*	
A	4.60	0.181	+/- 0.100 mm (0.004")
A1	0.43	0.017	+/- 0.050 mm (0.002")
A2	0.08	0.003	+/- 0.050 mm (0.002")
A3	0.45	0.018	
B	4.40	0.173	+/- 0.100 mm (0.004")
B1	0.08	0.003	+/- 0.050 mm (0.002")
B2	1.55	0.061	
B3	0.98	0.039	+/- 0.050 mm (0.002")
B4	0.75	0.030	
C	0.51	0.020	+/- 0.08mm (0.003")
C1	0.50	0.020	
C2	0.01	0.0004	
D1	3.75	0.148	
D2	0.75	0.030	
G1	0.65	0.026	
G2	1.05	0.041	
S1	3.35	0.132	
S2	2.75	0.108	

*Inch measurements are approximate values

Surface Finish: ENIG
Ni: 4.5 um +/- 1.5 um
Au: 0.09 um +/- 0.03 um

Part Marking

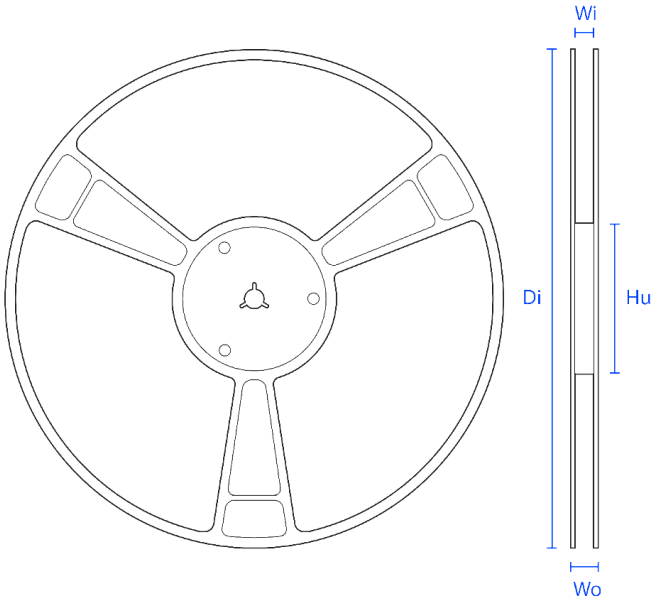


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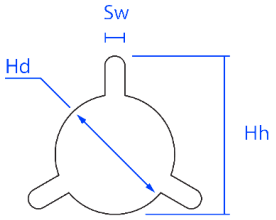
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Tape and Reel Information

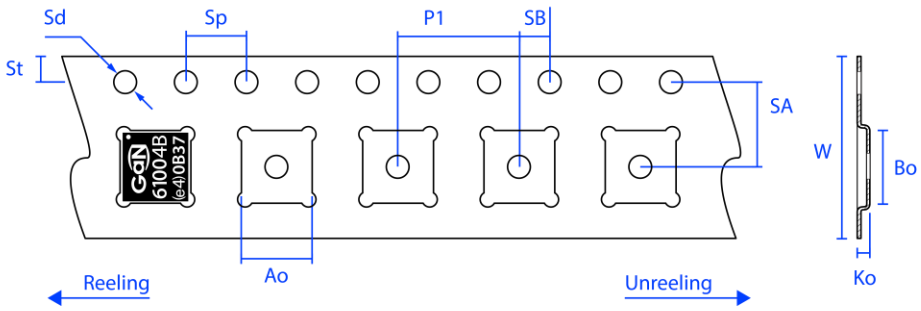


Dimensions (mm)

13 inch reel	Min	Max	7 inch reel	Min	Max
Di	328.5	331.5	Di	177.0	181.5
Wo		18.4	Wo	16.0	18.4
Wi	12.4	14.4	Wi	11.5	14.4
Hu	98.5	104.0	Hu	59.5	62.5
Hh	16.45	17.4	Hh	17.1	17.5
Sw	1.5	2.5	Sw	2.1	2.5
Hd	12.8	13.5	Hd	12.8	13.4



Note: Wo and Wi measured at hub



Dimensions (mm)

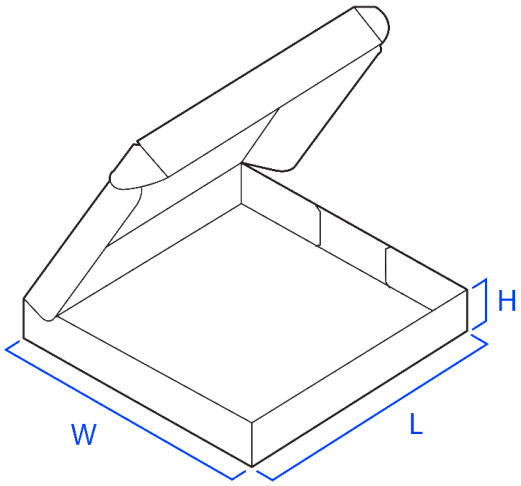
	Nominal	Tolerance
P1	8.00	+/- 0.1
W	12.00	+ 0.3 / - 0.1
Ko	0.83	+/- 0.1
Ao	4.67	+/- 0.05
Bo	4.80	+/- 0.05
Sp	4.00	+/- 0.2
Sd	1.50	+ 0.1 / - 0.0
St	1.75	+/- 0.1
SA	5.50	+/- 0.05
SB	2.00	+/- 0.05

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Tape and Reel Box Dimensions



Outside dimensions (mm)

13 inch reel			7 inch reel		
	Min	Max		Min	Max
W	197.0	203.5	W	337.0	342.0
L	204.0	218.5	L		355.0
H		32.0	H	50.0	53.0

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