ROHM SEMICONDUCTOR

Datasheet

Middle Power Class-D Speaker Amplifier series

20W+20W Full Digital Speaker Amplifier with built-in DSP

PERFECT PURE Bass+

BM5481MUV

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General Description

BM5481MUV is a Full Digital Speaker Amplifier with built-in DSP (Digital Sound Processor) designed for Flat-panel TVs in particular for space-saving and low-power consumption, delivers an output power of 20W+20W. This IC employs Bipolar, CMOS, and DMOS (BCD) process technology that eliminates turn-on resistance in the output power stage and internal loss due to line resistances up to an ultimate level. With this technology, the IC can achieve high efficiency. In addition, the IC is packaged in a compact reverse heat radiation type power package to achieve low power consumption and low heat generation and eliminates necessity of external heat-sink up to a total output power of 40W. This product satisfies both needs for drastic downsizing, low-profile structures and many function, high quality playback of sound system.

Key Specifications

- Supply voltage (VCC) 10V to 26V
- Speaker output power 20W+20W (Typ)
- (VCC=19V,RL=8Ω)THD+N
- Audio output voltage 0.07 [%] (Typ)
  (SVDD=3.3V,RL=10kΩ) 2 .0[Vrms] (Typ)

Applications

- Flat Panel TVs (LCD, Plasma)
- Home Audio
- Desktop PC
- Amusement equipments
- Electronic Music equipments, etc.

Package

Package	W(Min) x D(Typ) x H(Max)
VQFN48V7070P	7.00mm x 7.00mm x 1.00mm

VQFN48V7070P

Features

- This IC includes the DSP (digital sound processor) 0for Audio signal processing for Flat TVs.
  P^2Bass+(pseudo bass), 16 Band P-EQ,
  Level DRC, 2 Band DRC, Surround, etc.
- This IC has one input systems of digital audio interface. (No needs of Master Clock)
  - I^2S / LJ / RJ format
  - LRCLK: 32k/44.1k/48KHz
  - BCLK: 32fs / 48fs / 64fs
  - SDATA: 16 / 20 / 24bit
- With wide range of power supply voltage.
- The monaural output that can reduce the number of external parts can be used.
- With high efficiency and low heat dissipation contributing to miniaturization, slim design, and also power saving of the system.
- Eliminates pop-noise generated during the power supply on/off. High quality muting performance is realized by using the soft-muting technology.
- This IC is built-in with various protection functions for highly reliability design.
  - High temperature protection
  - Over voltage protection, Under voltage protection
  - Output short protection
  - DC voltage protection
  - Clock stop protection
- Small package
- The Audio output amplifier of the unnecessary output coupling capacitor.
  - Adjust gain (Via external parts)
  - 2Vrms output (SVDD=3.3V, RL =10kΩ) or 35mW output (SVDD=3.3V, RL =32Ω)

Typical Application Circuit

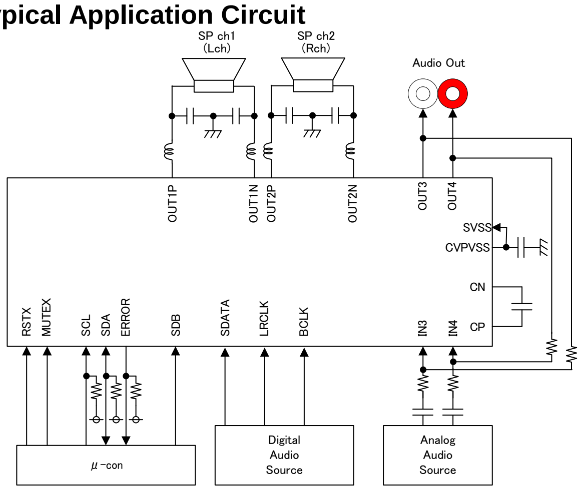

Figure 1. Typical application circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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Pin configuration and Block diagram

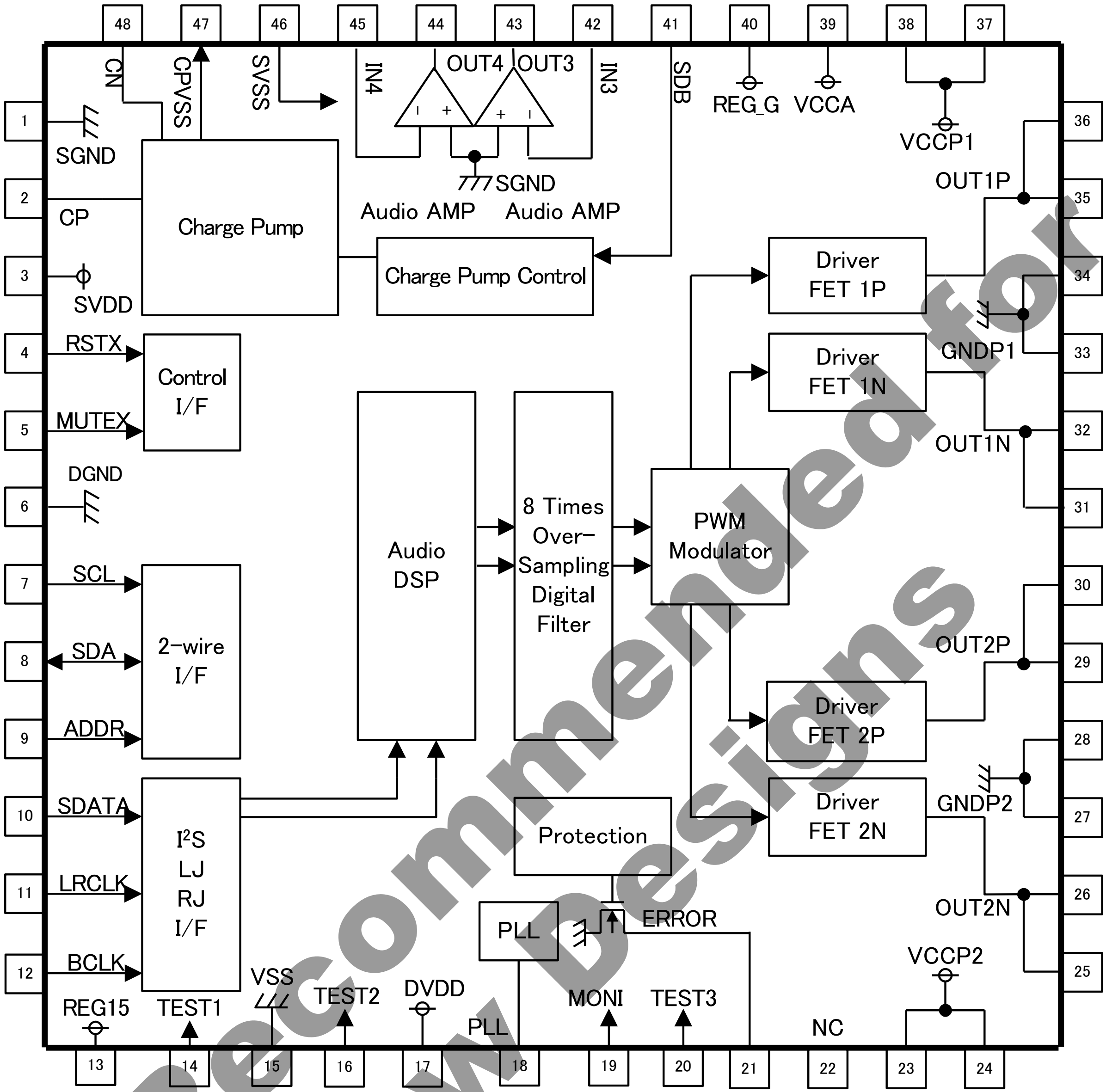

Figure 2. Pin configuration and Block diagram (Top View)

Pin Description

No.	Name	I/O	No.	Name	I/O	No.	Name	I/O	No.	Name	I/O
1	SGND	-	13	REG15	O	25	OUT2N	O	37	VCCP1	-
2	CP	I	14	TEST1	I	26	OUT2N	O	38	VCCP1	-
3	SVDD	-	15	VSS	-	27	GNDP2	-	39	VCCA	-
4	RSTX	I	16	TEST2	O	28	GNDP2	-	40	REG_G	O
5	MUTEX	I	17	DVDD	-	29	OUT2P	O	41	SDB	I
6	DGND	-	18	PLL	O	30	OUT2P	O	42	IN3	O
7	SCL	I	19	MONI	I/O	31	OUT1N	O	43	OUT3	O
8	SDA	I/O	20	TEST3	I	32	OUT1N	O	44	OUT4	O
9	ADDR	I	21	ERROR	O	33	GNDP1	-	45	IN4	I
10	SDATA	I	22	NC	-	34	GNDP1	-	46	SVSS	I
11	LRCLK	I	23	VCCP2	-	35	OUT1P	O	47	CPVSS	O
12	BCLK	I	24	VCCP2	-	36	OUT1P	O	48	CN	O

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Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Limit	Unit	Conditions
Supply voltage	VCC	-0.3 to 30	V	Pin 23,24,37,38, 39(Note1)(Note2)
	DVDD	-0.3 to 4.5	V	Pin 17 (Note1)
	SVDD	-0.3 to 4.5	V	Pin 3(Note1)
Power dissipation	Pd	4.30	W	(Note3)
		4.80	W	(Note4)
Input voltage 1	VIN1	-0.3 to DVDD+0.3	V	Pin 4, 5, 7 - 12, 14, 16, 19, 20, 21(Note1)
Input voltage 2	VIN2	-3.5 to 3.5	V	Pin 42, 45 (Note1)(Note5)
Input voltage 3	VIN3	-4.5 to 0.3	V	Pin 46, 47 (Note1)
Input voltage 4	VIN4	-0.3 to SVDD+0.3	V	Pin 2, 41(Note1)
Terminal voltage 1	VPIN1	-0.3 to 7.0	V	Pin 40(Note1)
Terminal voltage 2	VPIN2	-0.3 to 30	V	Pin 25, 26, 29, 30, 31, 32, 35, 36(Note1) (Note6)
Terminal voltage 3	VPIN3	-3.5 to 3.5	V	Pin 43, 44(Note1) (Note5)
Terminal voltage 4	VPIN4	(SVSS-0.3) to 0.3	V	Pin 48(Note1)
Operating temperature range	Topr	-25 to +85	°C	
Storage temperature range	Tstg	-55 to +150	°C	
Maximum junction temperature	Tjmax	+150	°C	

(Note1) The voltage that can be applied reference to GND (Pin 1, 6, 15, 27, 28, 33, 34).
(Note2) Do not, however exceed Pd and Tjmax=150°C.
(Note3) 74.2mm × 74.2mm × 1.6mm, FR4, 4-layer glass epoxy board (Copper area 34.09mm2)
Derating in done at 34.4 mW/°C for operating above Ta＝25°C. There are thermal via on the board.
(Note4) 74.2mm × 74.2mm × 1.6mm, FR4, 4-layer glass epoxy board (Copper area 5505mm2)
Derating in done at 38.4 mW/°C for operating above Ta＝25°C. There are thermal via on the board.
(Note5) It should be ≦SVDD and ≧SVSS.
(Note6) It should use it below this ratings limit including the AC peak waveform (overshoot) for all conditions.
At only undershoot, it is admitted using at ≦10nse and ≦30V by the VCC reference. (Please refer following figure.)

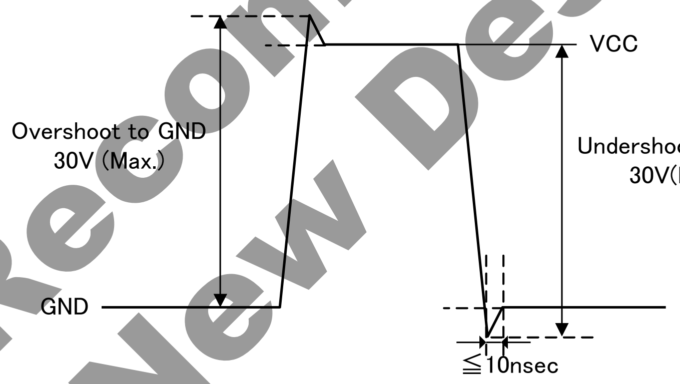

Figure 3

Recommended Operating Ratings (Ta=25°C)

Item	Symbol	Limit	Unit	Conditions
Supply voltage	VCC	10 to 26	V	Pin 23,24,37,38, 39(Note1) (Note2)
	DVDD	3 to 3.6	V	Pin 16(Note1)
	SVDD	3 to 3.6	V	Pin 3(Note1)
Minimum load impedance 1	R_{L1}	5.4	Ω	Pin 25, 26, 29, 30, 31, 32, 35, 36 VCC = 18V to 26V(Note7)
		3.6	Ω	Pin 25, 26, 29, 30, 31, 32, 35, 36 VCC < 18V(Note7)
Minimum load impedance 2	R_{L2}	16	Ω	Pin 43, 44

(Note7) Do not, however exceed Pd.

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Electrical Characteristics

(Unless otherwise specified Ta=25°C, VCC=18V, DVDD=3.3V, SVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, SDB=0V, f=1 kHz, R_{L1}=8Ω, R_{L2}=10kΩ, RI=RF=10kΩ, DSP: Through, fs=48 kHz, MCLK=256fs, Snubber circuit for output terminal: R=5.6Ω, C=1200pF)

Item	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Total circuit						
Circuit current 1 (Normal mode)	I_{CC1}	-	45	90	mA	Pin 23,24,37,38,39, No load
	I_{DD1}	-	20	40	mA	Pin 17, -∞dBFS input, No load
Circuit current 2 (Reset mode)	I_{CC2}	-	100	200	μA	Pin 23,24,37,38,39, No load RSTX=0V, MUTEX=0V, SDB=0V
	I_{DD2}	-	2.5	7.0	mA	Pin 17, -∞dBFS input, No load RSTX=0V, MUTEX=0V, SDB=0V
Open-drain terminal Low level voltage	V_{ERR}	-	-	0.8	V	Pin 21, I_O=0.5mA
Regulator output voltage 1	V_{REG_G}	4.2	5.1	5.6	V	Pin 40
Regulator output voltage 2	V_{REG15}	1.3	1.5	1.7	V	Pin 13
High level input voltage	V_{IH}	2.5	-	3.3	V	Pin 4, 5, 7 - 12, 14, 16, 19, 20, 41
Low level input voltage	V_{IL}	0	-	0.8	V	Pin 4, 5, 7 - 12, 14, 16, 19, 20, 41
Input current (Input pull-up terminal)	I_{UP}	-150	-100	-50	μA	Pin 10 – 12, 19, VIN = 0V
Input current (Input pull-down terminal)	I_{DN}	35	70	105	μA	Pin 4, 5, 9, VIN = 3.3V
Input current (SCL, SDA terminal)	I_{IL}	-1	0	-	μA	Pin 7, 8, VIN = 0V
Input current (SCL, SDA terminal)	I_{IH}	-	0	1	μA	Pin 7, 8, VIN = 3.3V
Speaker amplifier output						
Maximum output power 1	P_{O1}	-	10	-	W	VCC=13.5V,THD+n=10% (Note8)
Maximum output power 2	P_{O2}	-	20	-	W	VCC=19V,THD+n=10% (Note8)
Total harmonic distortion 1	THD1	-	0.07	-	%	P_O=1W, BW=20 to 20kHz(AES17) (Note8)
Crosstalk 1	CT1	60	80	-	dB	VCC=13.5V, P_O=1W, BW=IHF-A (Note8)
Output noise voltage 1	V_{NO1}	-	80	-	μVrms	-∞dBFS input, BW=IHF-A (Note8)
PWM sampling frequency	f_{PWM1}	-	256	-	kHz	fs=32 kHz (Note8)
	f_{PWM2}	-	352.8	-	kHz	fs=44.1 kHz (Note8)
	f_{PWM3}	-	384	-	kHz	fs=48 kHz (Note8)
Audio amplifier output						
Maximum output power 3	P_{O3}	-	35	-	mW	SVDD=3.3V,THD+n=1%,R_{L2}=32Ω (Note8) (Note9)
Maximum output voltage	V_{Om}	-	2	-	Vrms	SVDD=3.3V,THD+n=1%,R_{L2}=10kΩ (Note8) (Note9)
Total harmonic distortion 2	THD2	-	0.05	-	%	P_O=1mW, BW=20 to 20kHz, R_{L2}=32Ω (Note8) (Note9) (Note10)
Total harmonic distortion 3	THD3	-	0.02	-	%	V_O=1Vrms,BW=20 to 20kHz, R_{L2}=10kΩ (Note8) (Note9) (Note10)
Crosstalk 2	CT2	60	80	-	dB	f=1kHz, P_O=10mW BW=1kHz BPF, R_{L2}=32Ω (Note8) (Note9)
Crosstalk 3	CT3	60	80	-	dB	f=1kHz, Vo=200mVp-p, BW=1kHz BPF, R_{L2}=10kΩ (Note8) (Note9)
Output noise voltage 2	V_{NO2}	-	20	-	μVrms	Rg=0Ω, BW=IHF-A , R_{L2}=32Ω (Note8) (Note9)
Output noise voltage 3	V_{NO3}	-	20	-	μVrms	Rg=0Ω, BW=IHF-A , R_{L2}=10kΩ (Note8) (Note9)
PSRR	PSRR	-	-55	-	dB	f=1kHz, 100mV_{P-P} - ripple, BW=1kHz BPF (Note8) (Note9)

(Note8) These items show the typical performance of device and depend on board layout, parts, and power supply.
The standard value is in mounting device and parts on surface of ROHM's board directly.

(Note9) MUTEX=0V, SDB=3.3V

(Note10) Either ch input.

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Typical Performance Curves Speaker output(Ta=25°C, VCC=18V, DVDD=3.3V, SVDD=3.3V, RSTX=0V/3.3V, MUTEX=0V/3.3V, SDB=0V, f=1 kHz,
DSP: Through, fs=48 kHz, MCLK=256fs, Snubber circuit for output terminal: [8Ω] R=5.6Ω, C=1200pF, [6,4Ω] R=5.6Ω, C=3300pF)
Measured by ROHM designed 4 layer board.

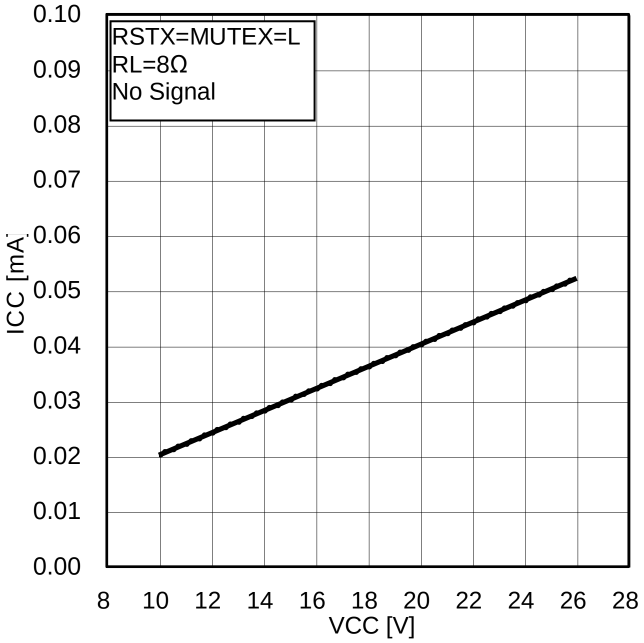

Figure 4. Power supply voltage- Current consumption

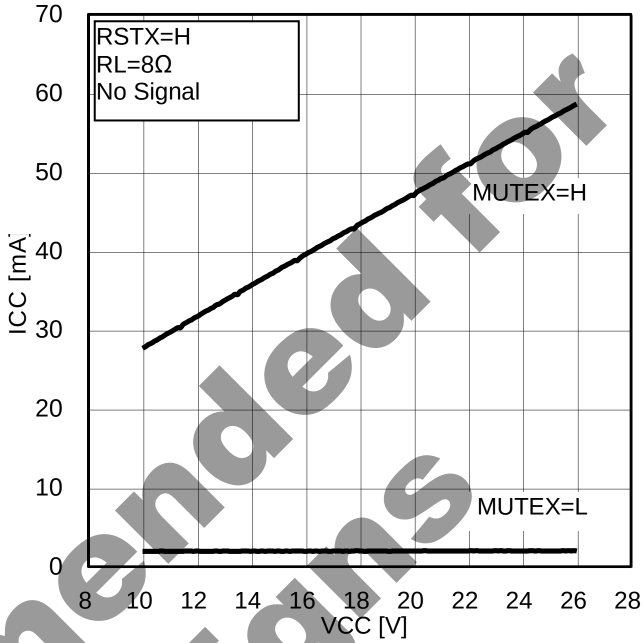

Figure 5. Power supply voltage- Current consumption

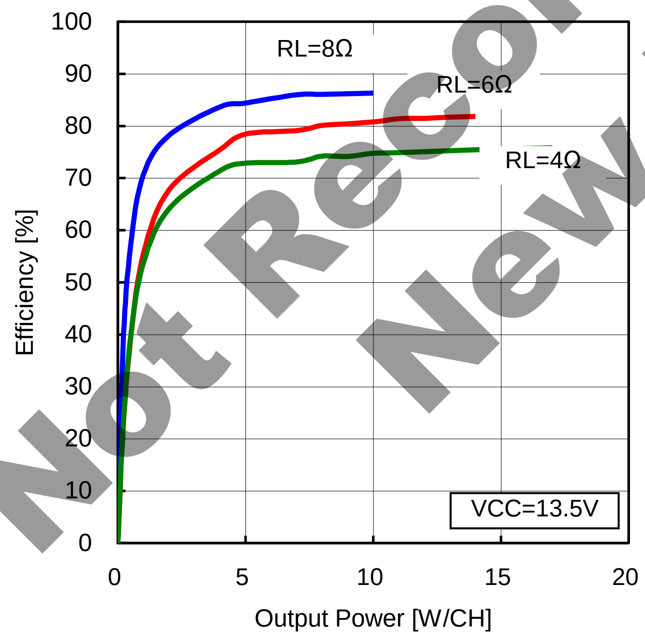

Figure 6. Output power – Efficiency

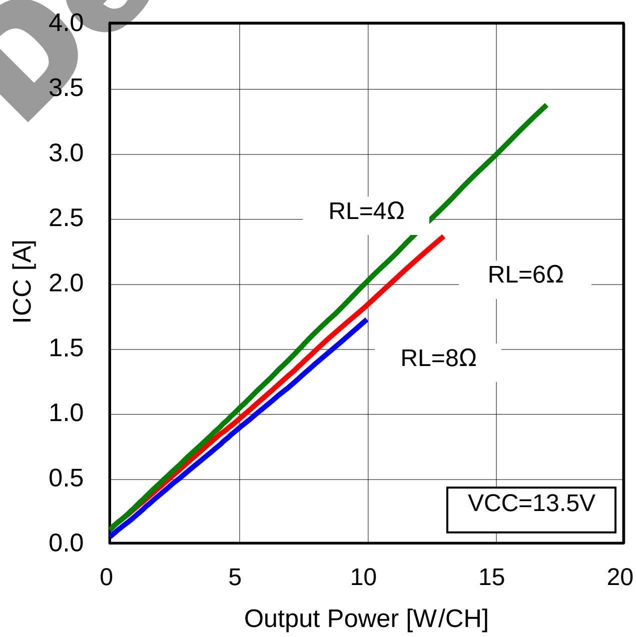

Figure 7. Output power - Current consumption

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Typical Performance Curves Speaker output(Ta=25°C, VCC=18V, DVDD=3.3V, SVDD=3.3V, RSTX=0V/3.3V, MUTEX=0V/3.3V, SDB=0V, f=1kHz,
DSP: Through, fs=48kHz, MCLK=256fs, Snubber circuit for output terminal: [8Ω] R=5.6Ω, C=1200pF, [6,4Ω] R=5.6Ω, C=3300pF)
Measured by ROHM designed 4 layer board.

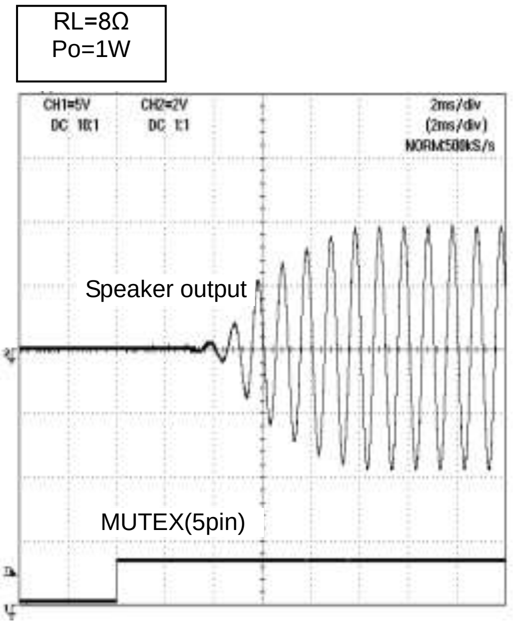

Figure 8. Waveform at soft start

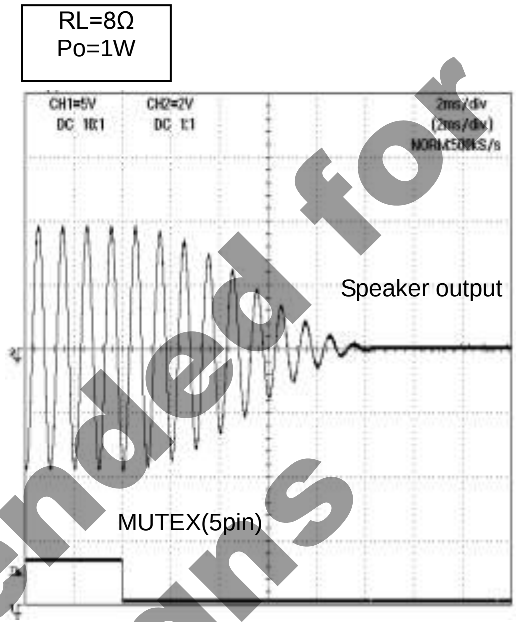

Figure 9. Waveform at soft mute

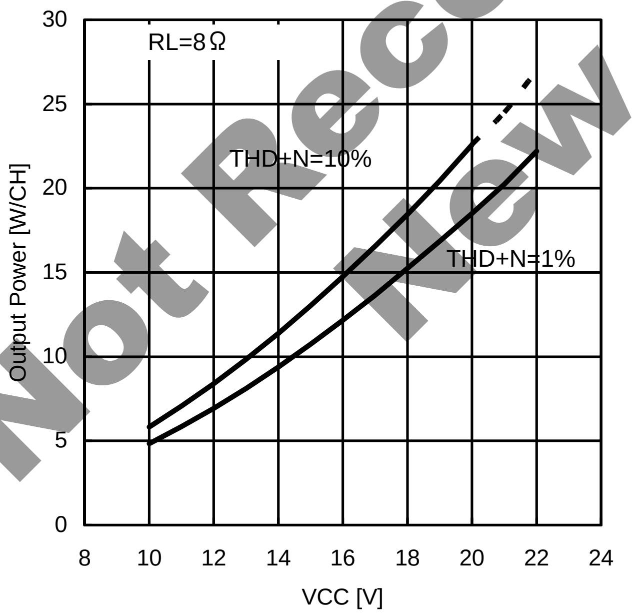

Figure 10. Output voltage - Power voltage (R_{L1}=8Ω)

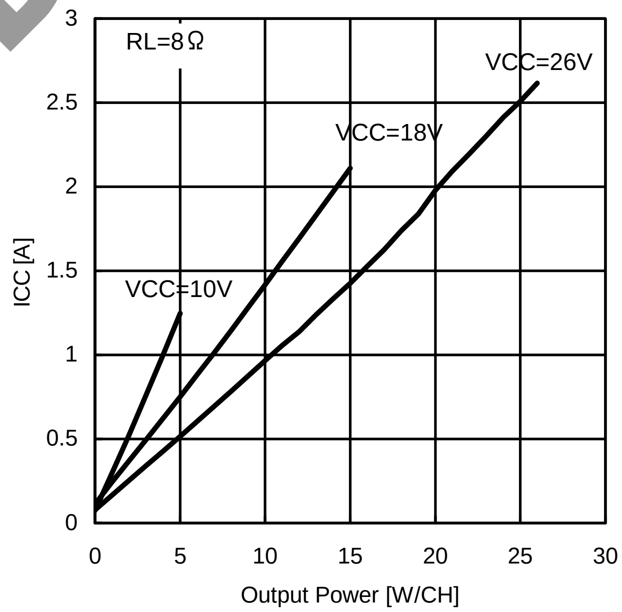

Figure 11. Output power - Current consumption (R_{L1}=8Ω)

※Dotted line means internal dissipation is over package power.

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Typical Performance Curves Speaker output(Ta=25°C, VCC=18V, DVDD=3.3V, SVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, SDB=0V, f=1kHz, DSP: Through, fs=48kHz, MCLK=256fs, Snubber circuit for output terminal: [8Ω] R=5.6Ω, C=1200pF, [6,4Ω] R=5.6Ω, C=3300pF)
Measured by ROHM designed 4 layer board.

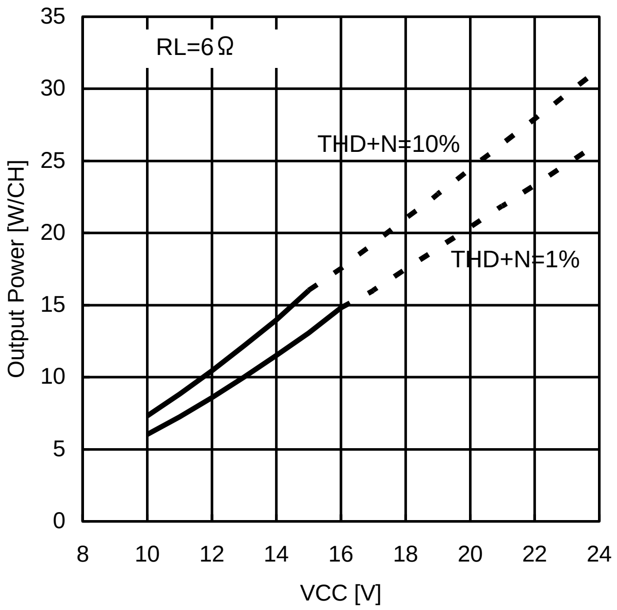

Figure 12. Output voltage - Power voltage (R_{L1}=6Ω)

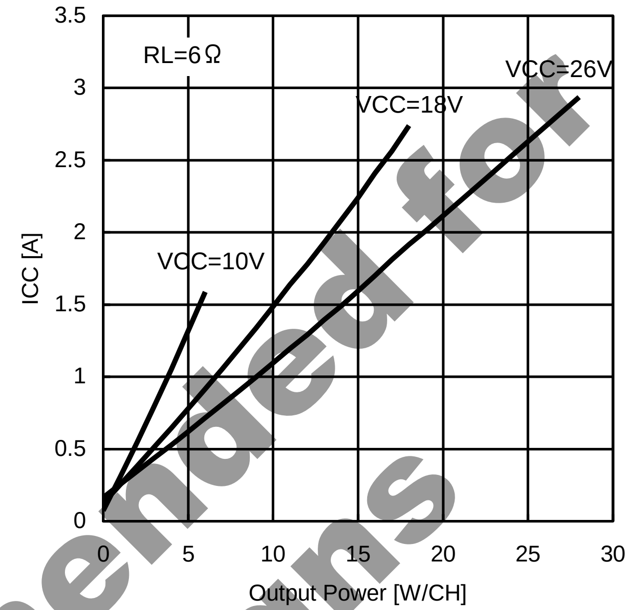

Figure 13. Output power - Current consumption (R_{L1}=6Ω)

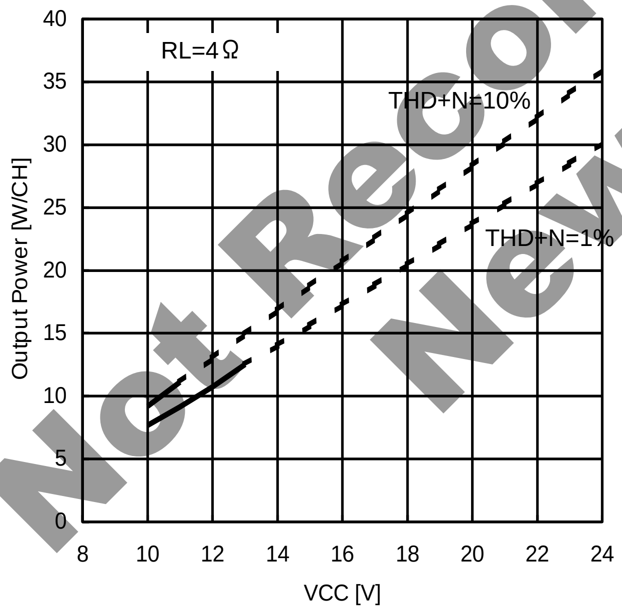

Figure 14. Output Voltage – Power Voltage (R_{L1}=4Ω)

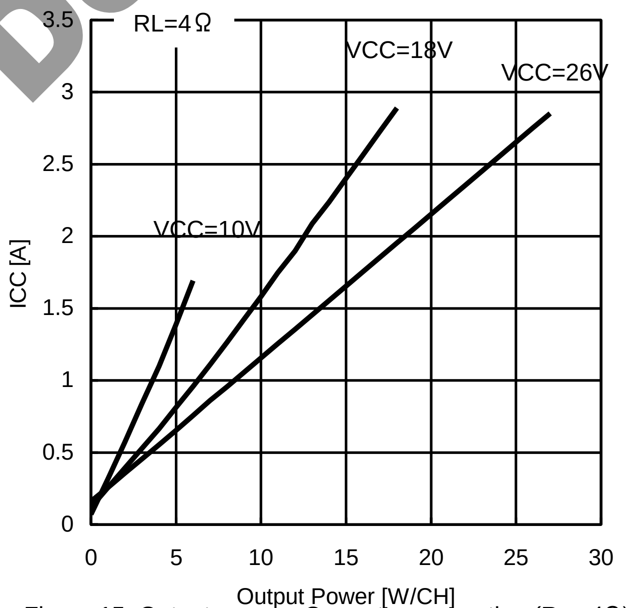

Figure 15. Output power - Current consumption (R_{L1}=4Ω)

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※Dotted line means internal dissipation is over package power.

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Typical Performance Curves Speaker output(R_{L1}=8Ω, Ta=25°C, VCC=18V, DVDD=3.3V, SVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, SDB=0V, f=1kHz,
DSP: Through, fs=48kHz, MCLK=256fs, Snubber circuit for output terminal: R=5.6Ω, C=1200pF)
Measured by ROHM designed 4 layer board.

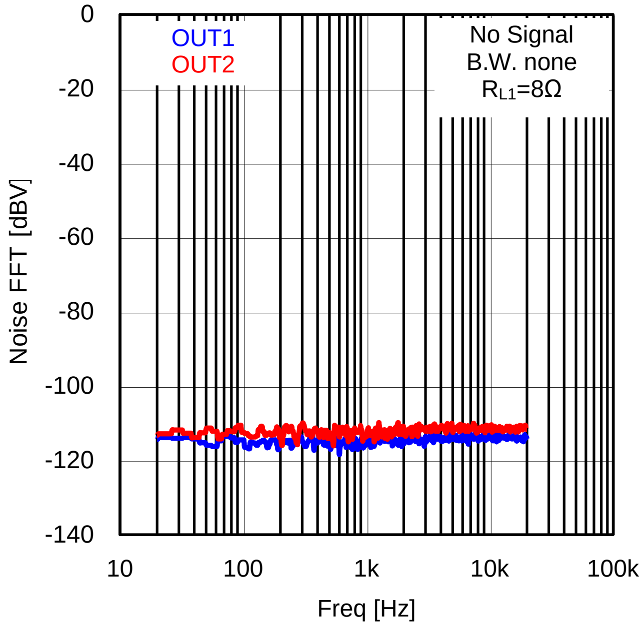

Figure 16. FFT of output noise voltage

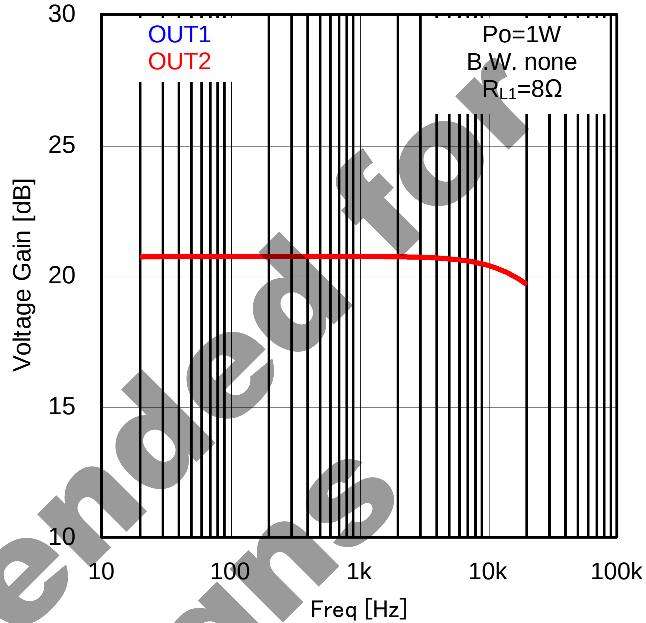

Figure 17. Frequency – Output power

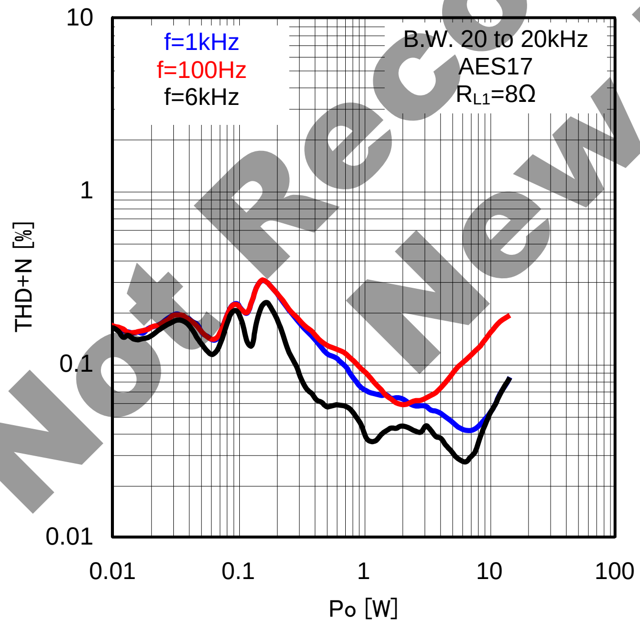

Figure 18. Output Power - THD+N

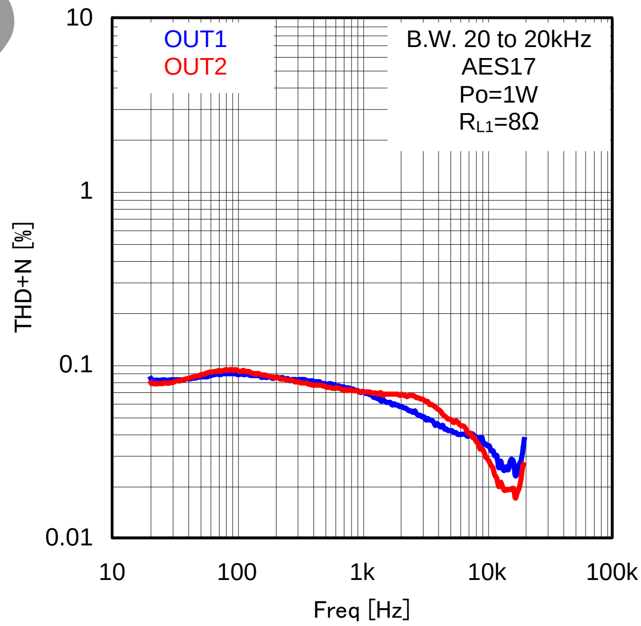

Figure 19. Frequency - THD+N

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Typical Performance Curves Speaker output(R_{L1}=8Ω, Ta=25°C, VCC=18V, DVDD=3.3V, SVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, SDB=0V, f=1 kHz,
DSP: Through, fs=48 kHz, MCLK=256fs, Snubber circuit for output terminal: R=5.6Ω, C=1200pF)
Measured by ROHM designed 4 layer board.

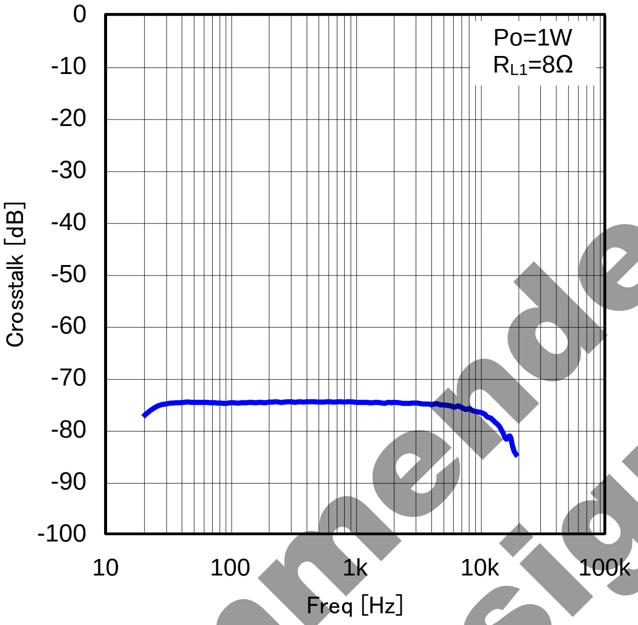

Figure 20. Frequency - Crosstalk

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Typical Performance Curves Speaker outputR_{L1}=6Ω, Ta=25°C, VCC=18V, DVDD=3.3V, SVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, SDB=0V, f=1 kHz,
DSP: Through, fs=48 kHz, MCLK=256fs, Snubber circuit for output terminal: R=5.6Ω, C=3300pF)
Measured by ROHM designed 4 layer board.

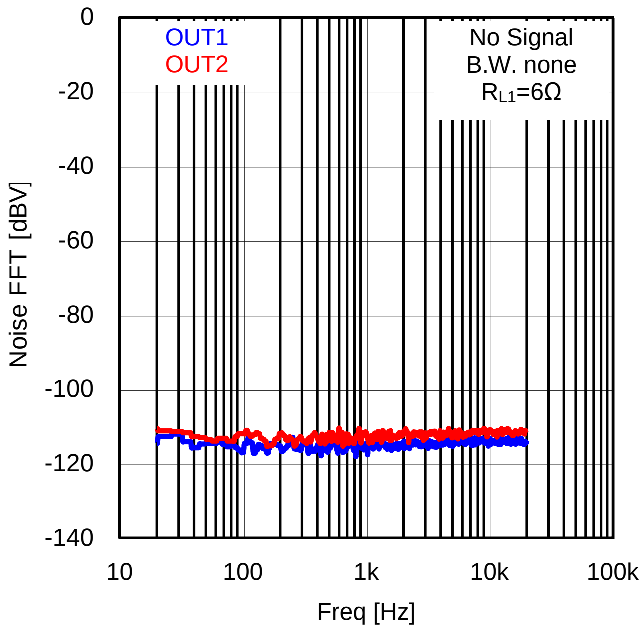

Figure 21. FFT of output noise voltage

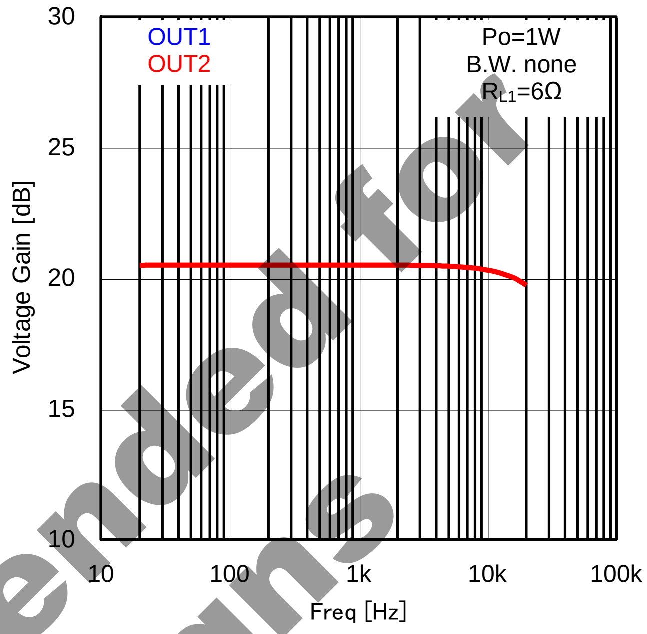

Figure 22. Frequency – Output power

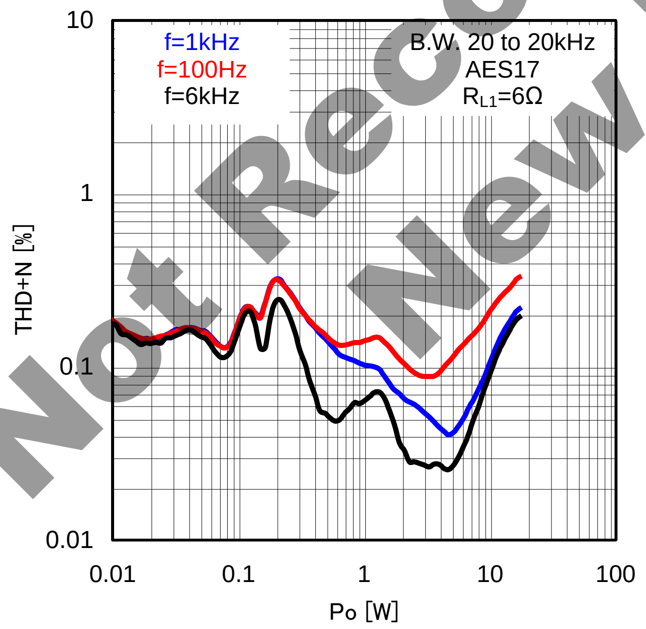

Figure 23. Output Power - THD+N

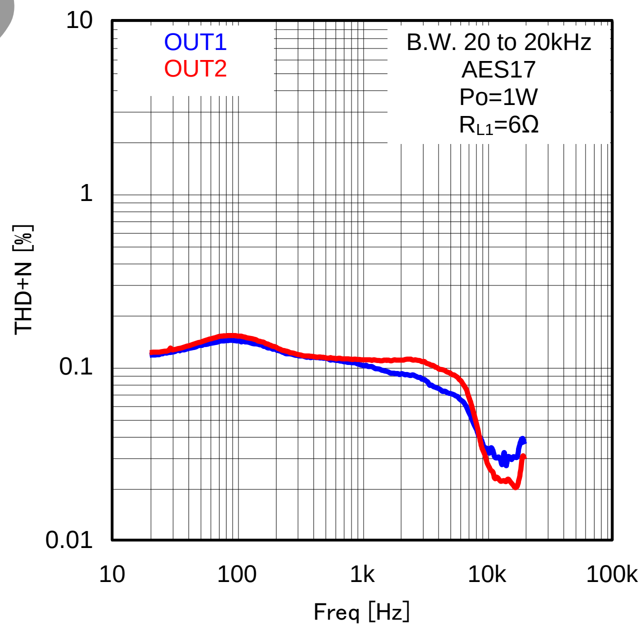

Figure 24. Frequency - THD+N

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Typical Performance Curves Speaker output(R_{L1}=6Ω, Ta=25°C, VCC=18V, DVDD=3.3V, SVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, SDB=0V, f=1 kHz,
DSP: Through, fs=48 kHz, MCLK=256fs, Snubber circuit for output terminal: R=5.6Ω, C=3300pF)
Measured by ROHM designed 4 layer board.

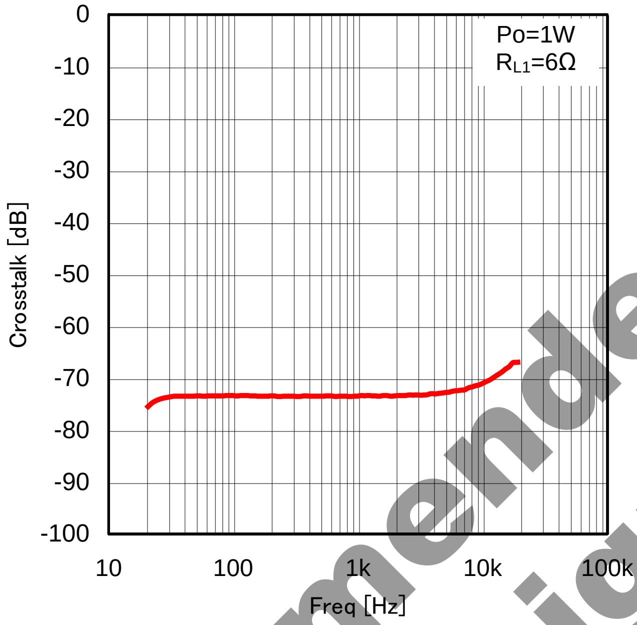

Figure 25. Frequency - Crosstalk

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Typical Performance Curves Speaker output(R_{L1}=4Ω, Ta=25°C, VCC=18V, DVDD=3.3V, SVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, SDB=0V, f=1 kHz,
DSP: Through, fs=48 kHz, MCLK=256fs, Snubber circuit for output terminal: R=5.6Ω, C=3300pF)
Measured by ROHM designed 4 layer board.

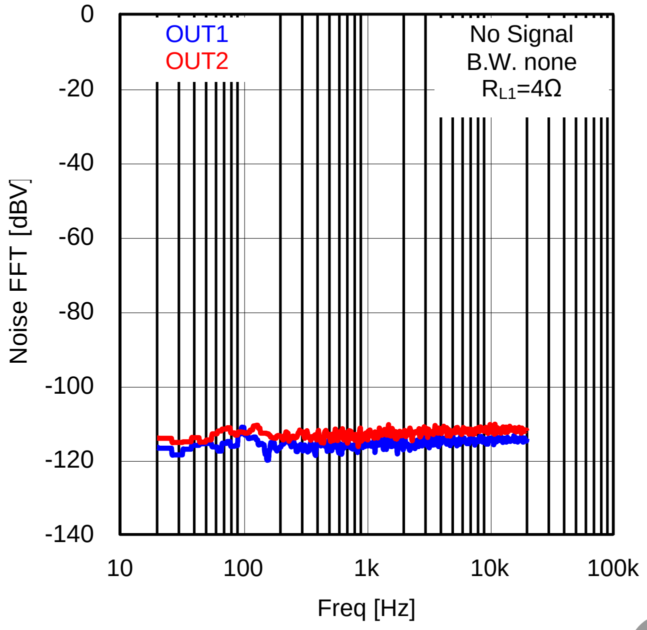

Figure 26. FFT of output noise voltage

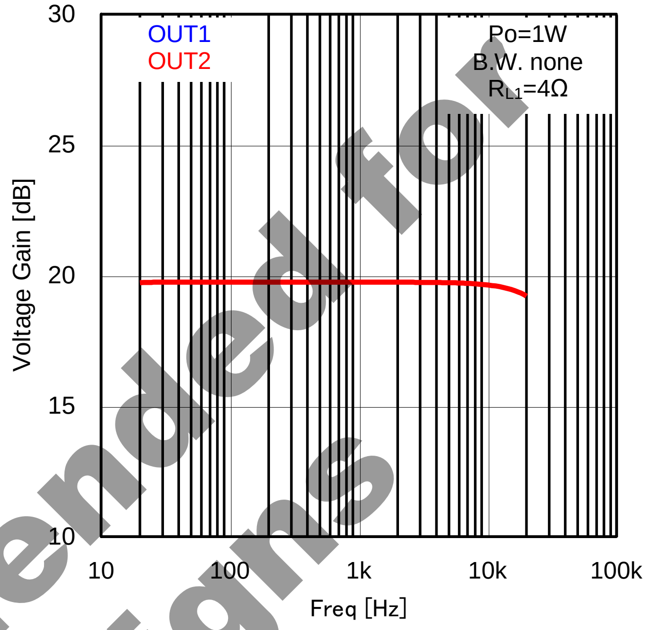

Figure 27. Frequency – Output power

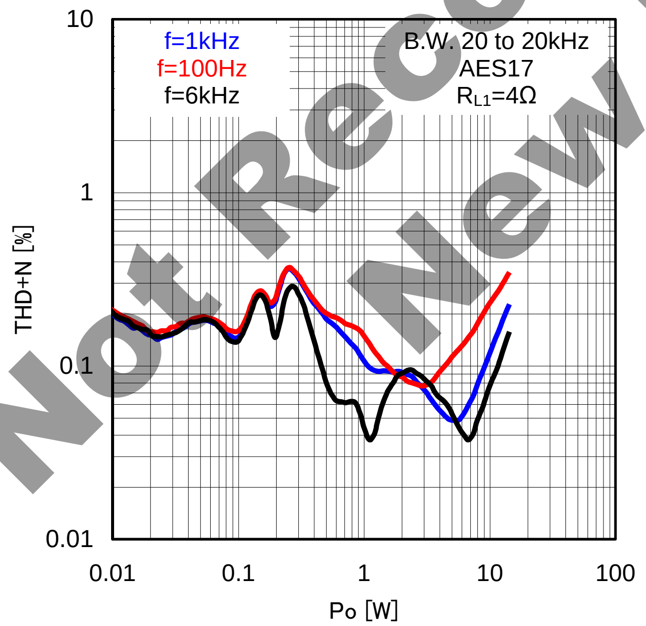

Figure 28. Output Power - THD+N

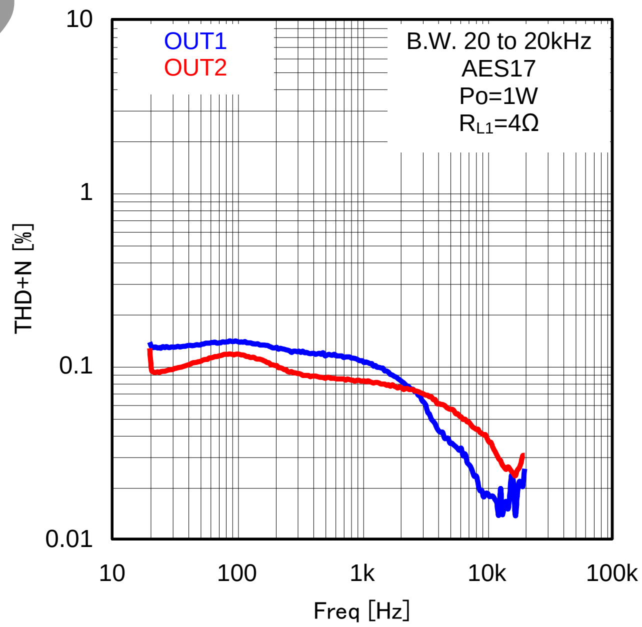

Figure 29. Frequency - THD+N

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Typical Performance Curves Speaker output(R_{L1}=4Ω, Ta=25°C, VCC=18V, DVDD=3.3V, SVDD=3.3V, RSTX=3.3V, MUTEX=3.3V, SDB=0V, f=1 kHz,
DSP: Through, fs=48 kHz, MCLK=256fs, Snubber circuit for output terminal: R=5.6Ω, C=3300pF)
Measured by ROHM designed 4 layer board.

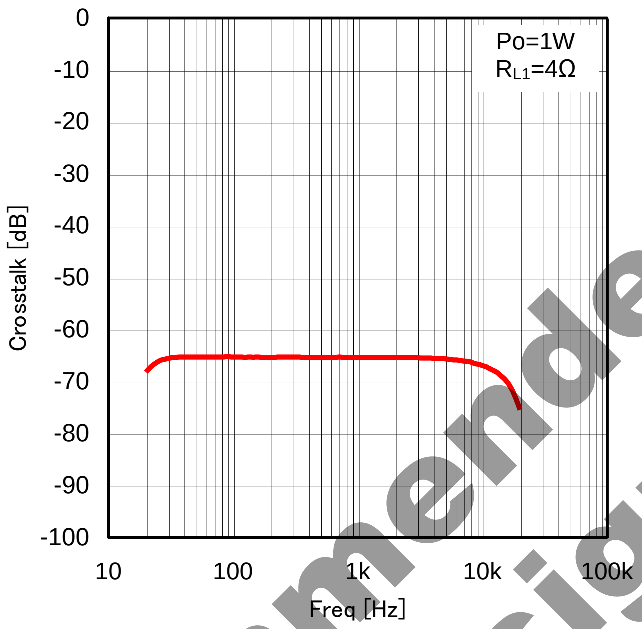

Figure 30. Frequency - Crosstalk

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Typical Performance Curves Audio output(Ta=25°C, VCC=18V, DVDD=3.3V, SVDD=3.3V, MUTEX=0V, RSTX=3.3V, SDB=3.3V, f=1 kHz, RI=RF=10kΩ)
Measured by ROHM designed 4 layer board.

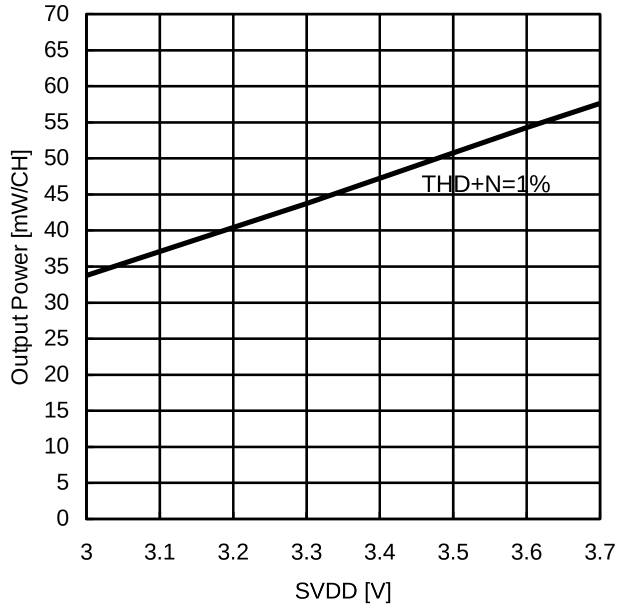

Figure 31. Output voltage - Power voltage (RL2=16Ω)

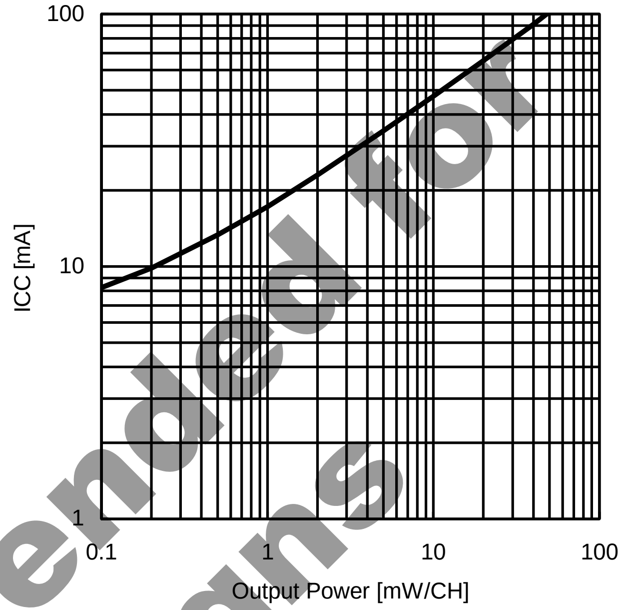

Figure 32. Output power - Current consumption (RL2=16Ω)

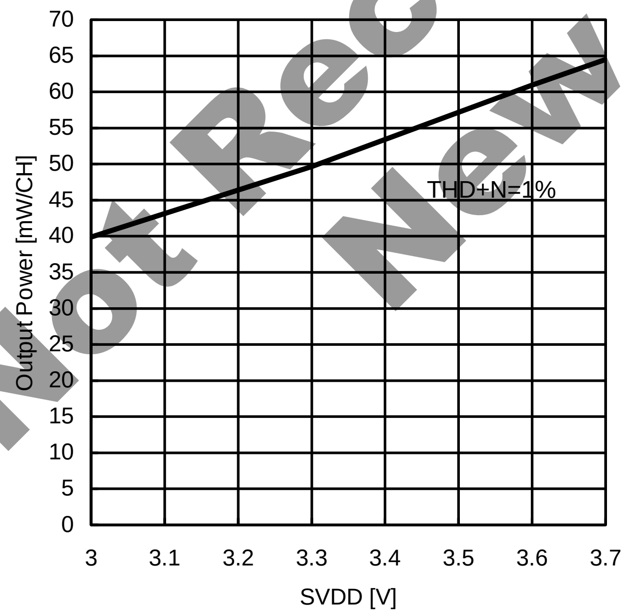

Figure 33. Output voltage - Power voltage (RL2=32Ω)

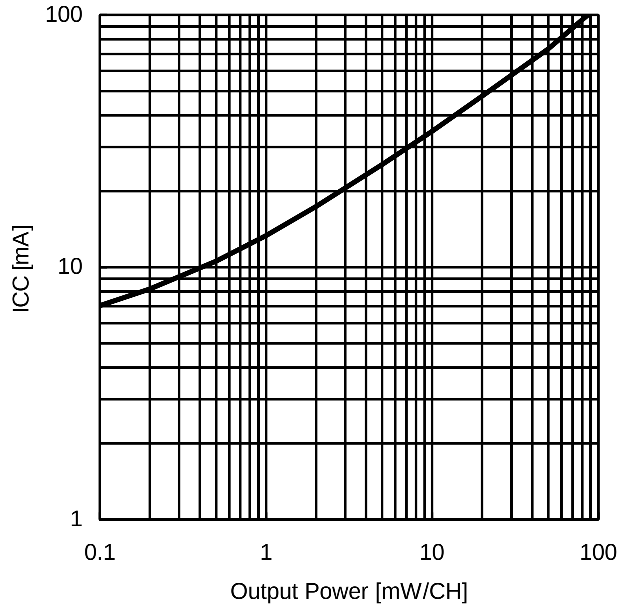

Figure 34. Output power - Current consumption (RL2=32Ω)

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Typical Performance Curves Audio output(Ta=25°C, VCC=18V, DVDD=3.3V, SVDD=3.3V, MUTEX=0V, RSTX=3.3V, SDB=3.3V, f=1 kHz, RI=RF=10kΩ)

Measured by ROHM designed 4 layer board.

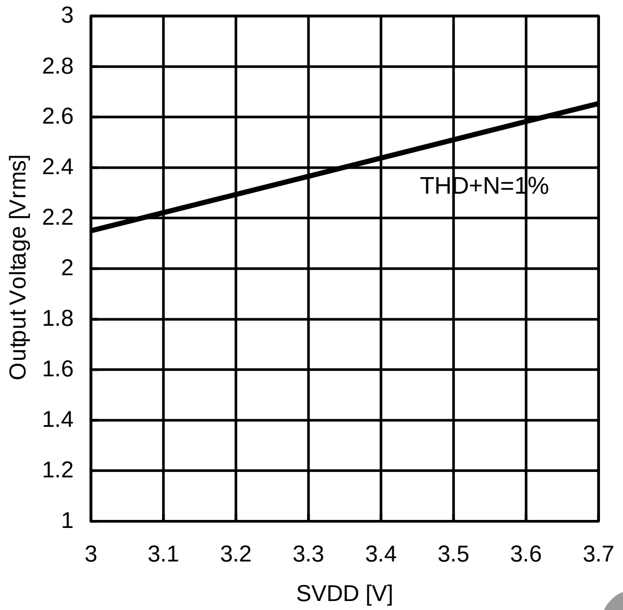

Figure 35. Output voltage - Power voltage (R_{L2}=10kΩ)

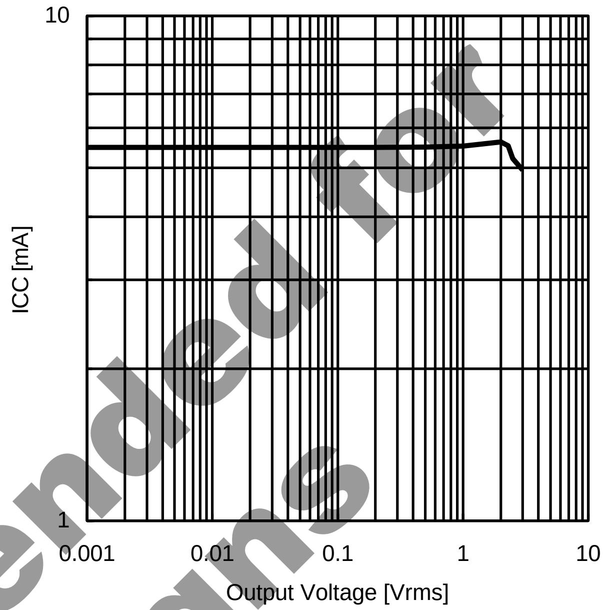

Figure 36. Output voltage - Current consumption (R_{L2}=10kΩ)

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Typical Performance Curves Audio output(Ta=25°C, VCC=18V, DVDD=3.3V, SVDD=3.3V, R_{L2}=32Ω, MUTEX=0V, RSTX=3.3V, SDB=3.3V, f=1 kHz, Ri=Rf=10kΩ)
Measured by ROHM designed 4 layer board.

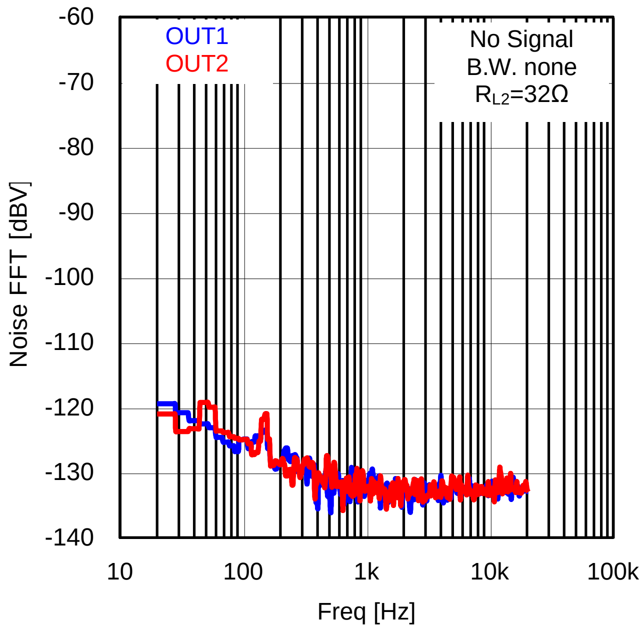

Figure 37. FFT of output noise voltage

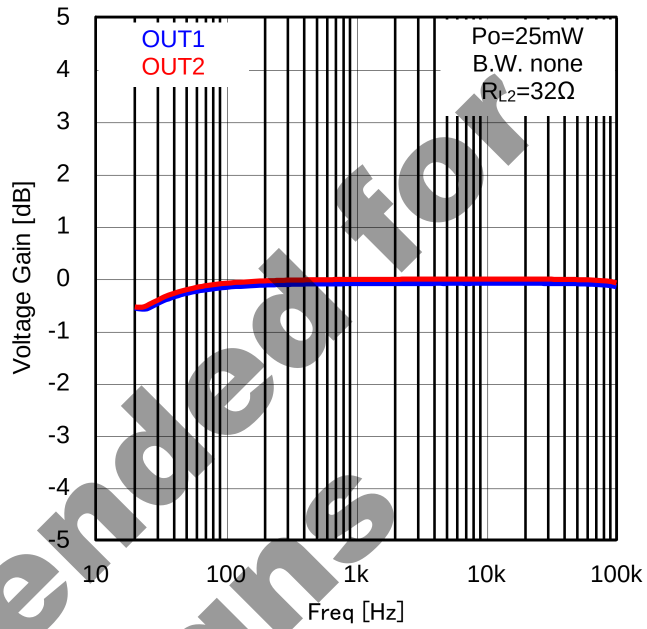

Figure 38. Frequency – Voltage gain

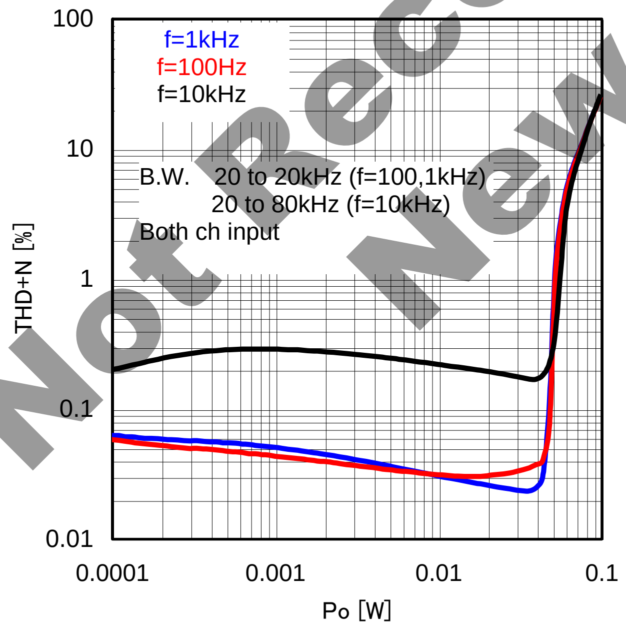

Figure 39. Output Power - THD+N

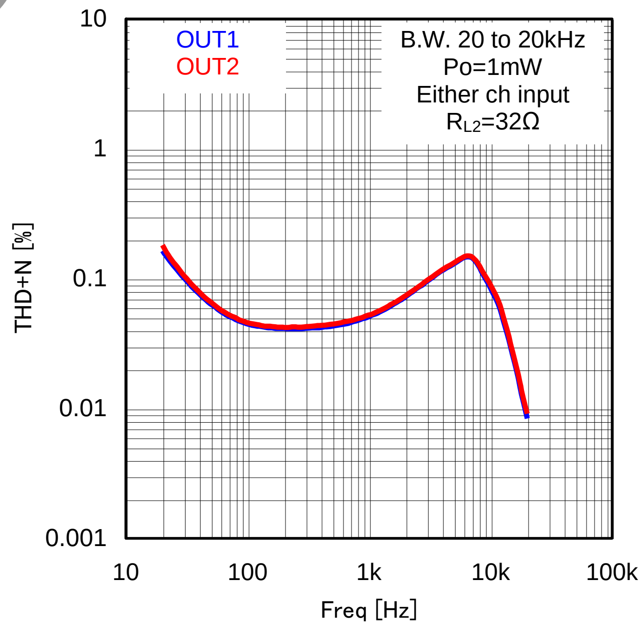

Figure 40. Frequency - THD+N

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Typical Performance Curves Audio output(Ta=25°C, VCC=18V, DVDD=3.3V, SVDD=3.3V, R_{L2}=32Ω, MUTEX=0V, RSTX=3.3V, SDB=3.3V, f=1kHz, Ri=Rf=10kΩ)
Measured by ROHM designed 4 layer board.

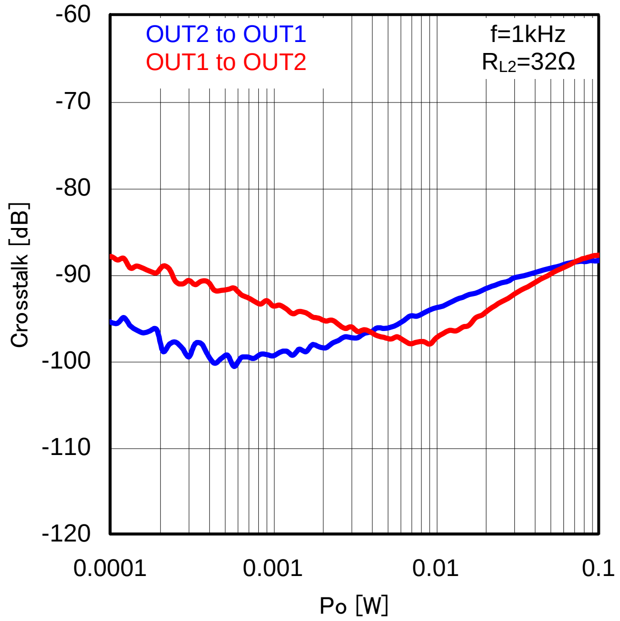

Figure 41. Output Power – Crosstalk

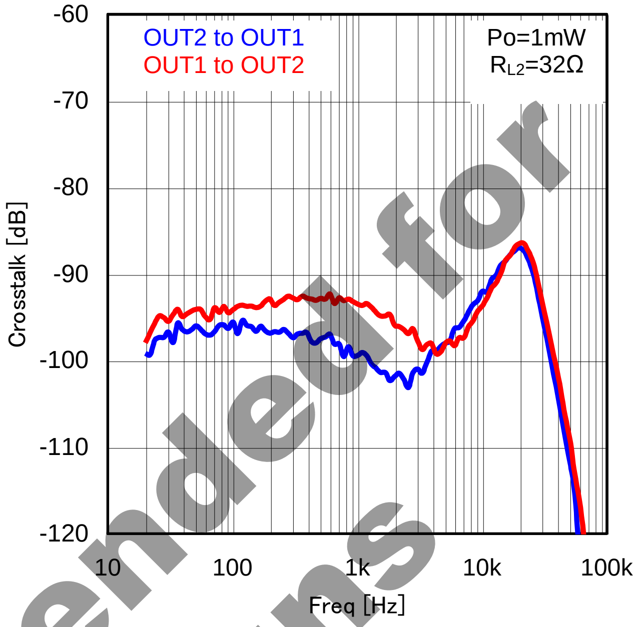

Figure 42. Frequency - Crosstalk

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Typical Performance Curves Audio output(Ta=25°C, VCC=18V, DVDD=3.3V, SVDD=3.3V, R_{L2}=10kΩ, MUTEX=0V. RSTX=3.3V, SDB=3.3V, f=1kHz, Ri=Rf=10kΩ)

Measured by ROHM designed 4 layer board.

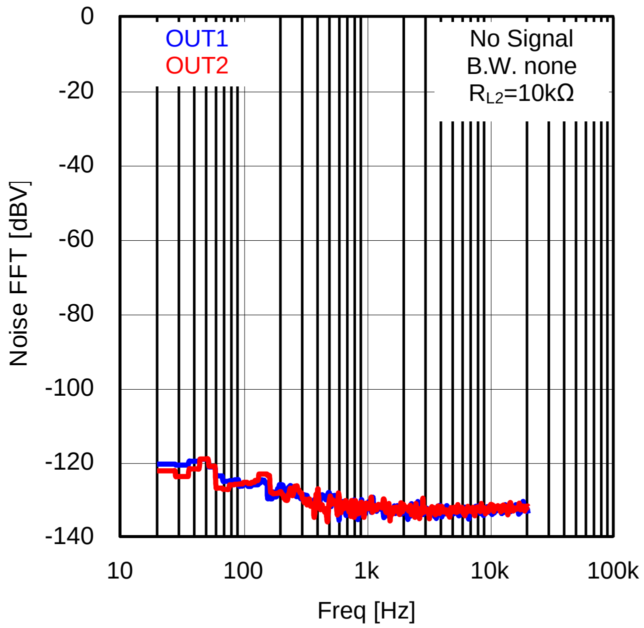

Figure 43. FFT of output noise voltage

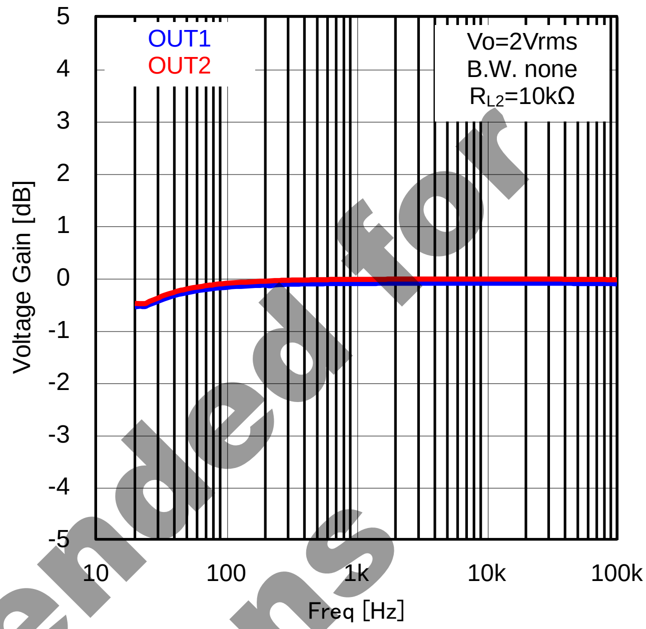

Figure 44. Frequency – Voltage gain

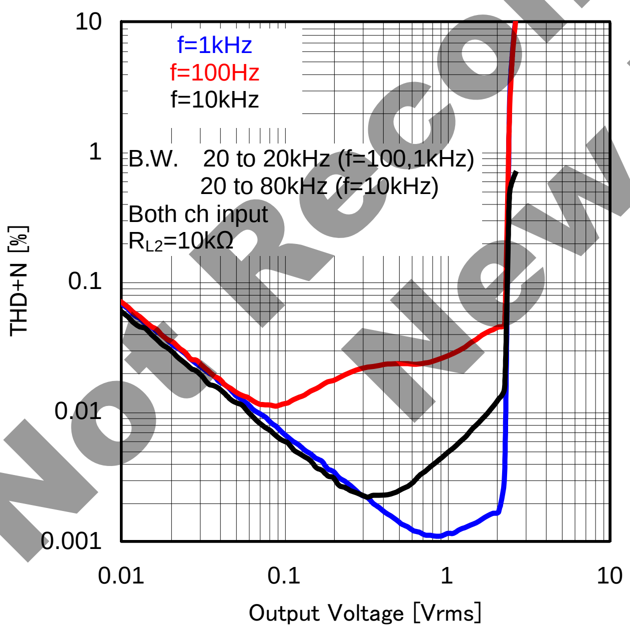

Figure 45. Output Power - THD+N

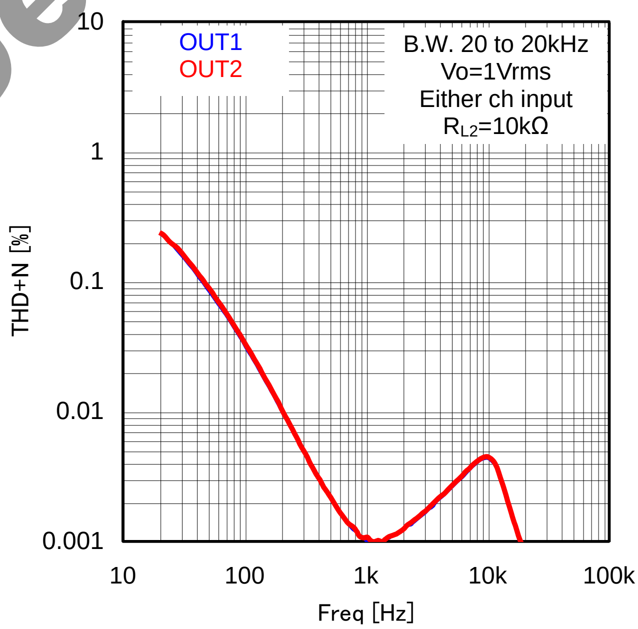

Figure 46. Frequency - THD+N

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Typical Performance Curves Audio output(Ta=25°C, VCC=18V, DVDD=3.3V, SVDD=3.3V, R_{L2}=10kΩ, MUTEX=0V. RSTX=3.3V, SDB=3.3V, f=1kHz, Ri=Rf=10kΩ)
Measured by ROHM designed 4 layer board.

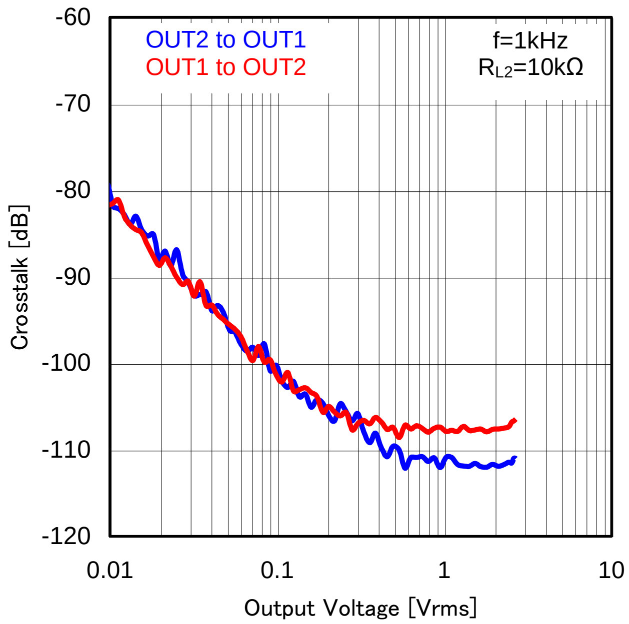

Figure 47. Output Power – Crosstalk

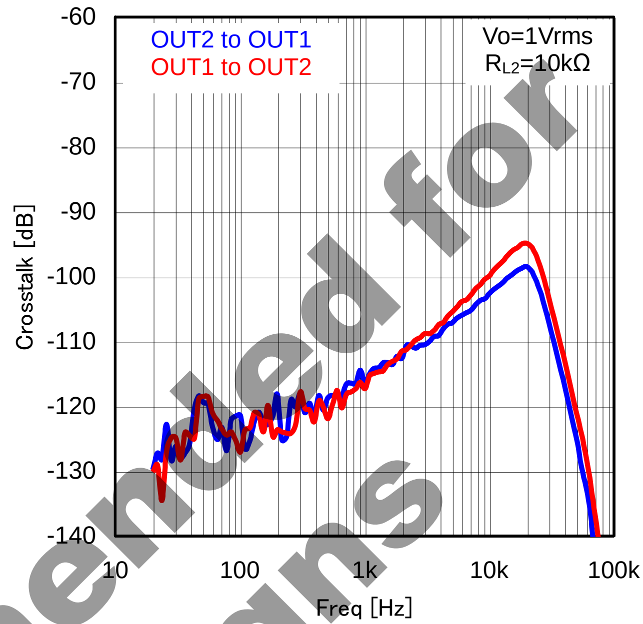

Figure 48. Frequency - Crosstalk

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Typical Performance Curves Audio output(Ta=25°C, VCC=18V, DVDD=3.3V, SVDD=3.3V, R_{L2}=32Ω, MUTEX=0V.
RSTX=3.3V, SDB=3.3V, f=1kHz, Ri=Rf=10kΩ)
Measured by ROHM designed 4 layer board

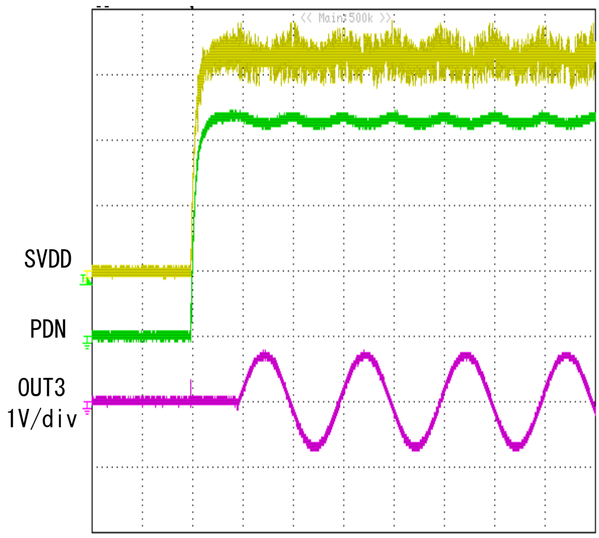

Figure 49. SVDD turn on

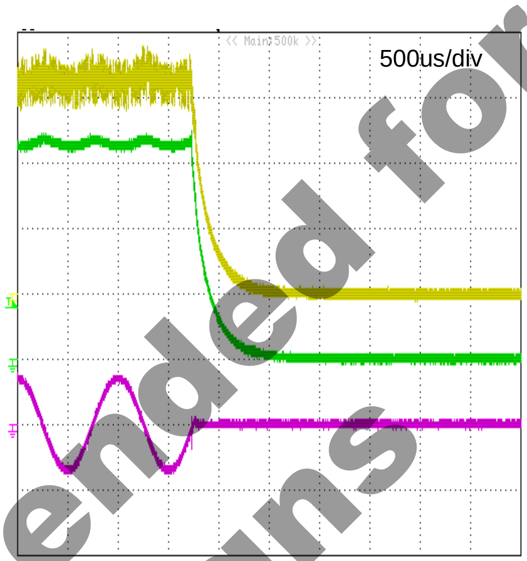

Figure 50. SVDD turn off

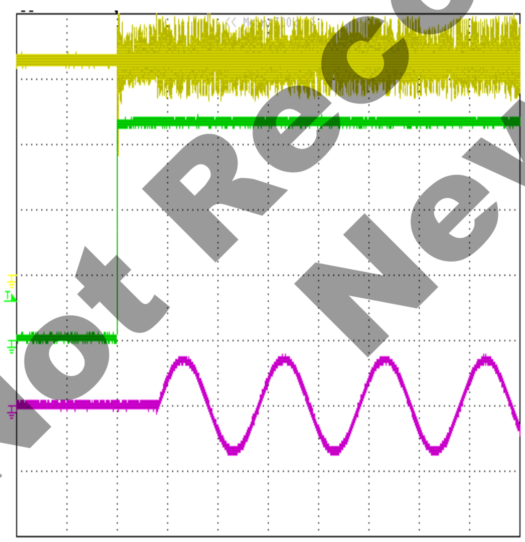

Figure 51. PDN turn on

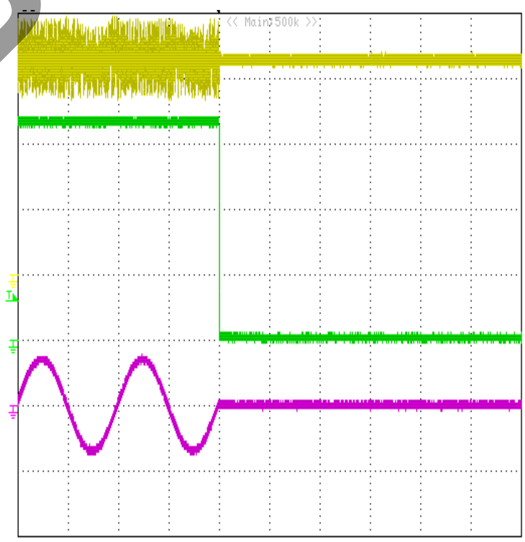

Figure 52. PDN turn off

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Typical Performance Curves Audio output(Ta=25°C, VCC=18V, DVDD=3.3V, SVDD=3.3V, R_{L2}=10kΩ, MUTEX=0V. RSTX=3.3V, SDB=3.3V, f=1kHz, Ri=Rf=10kΩ)
Measured by ROHM designed 4 layer board

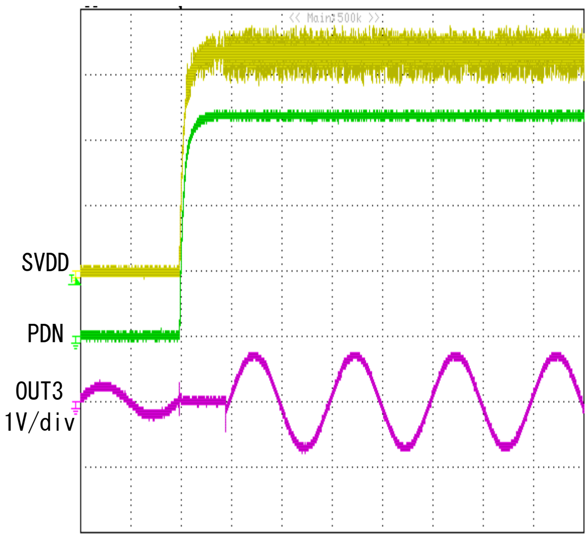

Figure 53. SVDD turn on

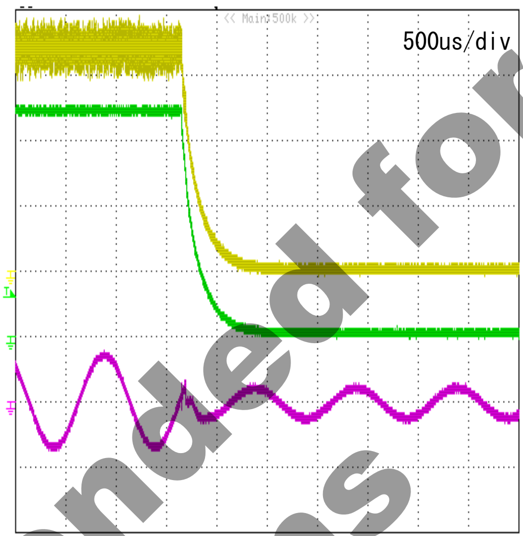

Figure 54. SVDD turn off

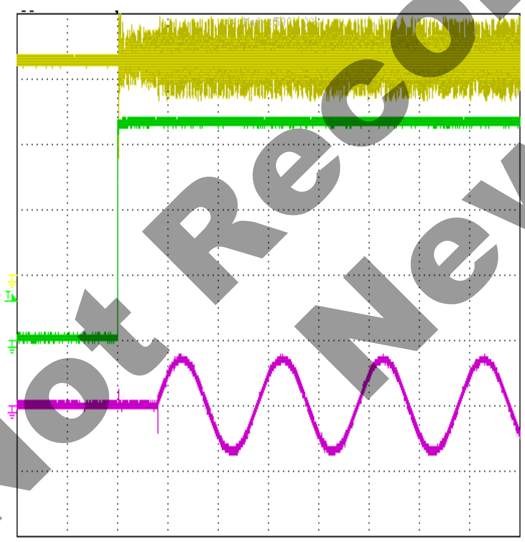

Figure 55. PDN turn on

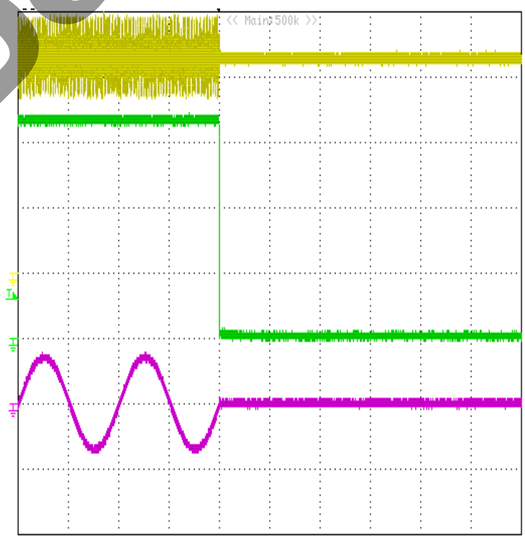

Figure 56. PDN turn off

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Digital Block Functional Overview

No.	Function	Specification
1	DC cut HPF	・1^{st} order HPF ・Fc : 1Hz
2	Pre-scalar	・Lch / Rch become same set point. ・+48dB to -79dB (0.5dB step)、-∞dB ・default 0dB
3	Channel Mixer	・Lch <= Mute, Lch(default), Rch, (L+R)/2, L-R ・Rch <= Mute, Lch, Rch(default), (L+R)/2, L-R ・Lch/Rch are independent phase reversal control available.
4	LEVEL DRC	・When the small signal is detected continuously during the fixed time, this function is soft mute transition. ・There is soft transition function. ・LEVEL DRC Detect level : -30dB to -96dB,12step ・Soft MUTE transition time : 0.125sec to 8sec,16step ・MUTE release time : 1msec to 40msec,8step
5	Surround	・Emphasizes the stereo. ・There is a pseudo-stereo effect.(Add a stereo to mono sound)
6	P^2Bass+ (Perfect Pure Bass+)	・This function make pseudo bass sound with the speaker which cannot make low frequency sound. ・Generation frequency : 68Hz to 1200Hz, 16step
7	16-Band Parametric Equalizer	・Parametric Equalizer has built-in coefficient calculation circuit. ・Only 4 factors is required.(Frequency/Gain/Quality factor/Filter type) ・The Filter types which can be selected is Peaking/Low-shelf/High-shelf/Low-pass/High-pass/All-pass. ・Lch/Rch become same set point. There is soft transition function. ・The set point of F0: Divide between into 61 from 20 Hz to 20 kHz. ・The set point of Gain: ±18dB (0.5dB step) ・A big gain may be unable to be set up when exceeding the factor span of DSP (±4) at the time of a gain selecting. ・Q(Quality factor) : 0.33 to 8.2, 29step. ・It is also possible to set up a factor directly.
8	Fine Master Volume	・Lch / Rch become same set point. ・+24dB to -103dB (0.125dB step)、-∞dB ・There is soft transition function.
9	Balance	・1dB step ・There is soft transition function. (Lch/Rch:0dB/-∞dB,0dB/-126dB,0dB/-125dB,・・,0dB/0dB,・・,-125dB/0dB, -126dB/0dB,-∞dB/0dB)
10	2 Band DRC	・Non clip output is achieved. ・Lch/Rch becomes the same control. ・Low-pass and a high region become an independent control. ・Threshold level : +12dB to -32dB (0.5dB step) ・The set point of Cross-over frequency : Divide between into 61 from 20 Hz to 20 kHz. ・The voice below the set-up detect level is decreased gently.
11	Post-Scalar	・Lch / Rch become same set point. ・+48dB to -79dB (0.5dB step)、-∞dB
12	Fine Post-Scalar	・Lch / Rch become independent set point. ・+0.7dB to -0.8dB (0.1dB step)
13	DC cut HPF	・1^{st} order HPF ・Fc : 1Hz
14	Clipper	・Lch / Rch become same set point. ・Clip level : +3dB to 22.5dB (-0.1dB step)

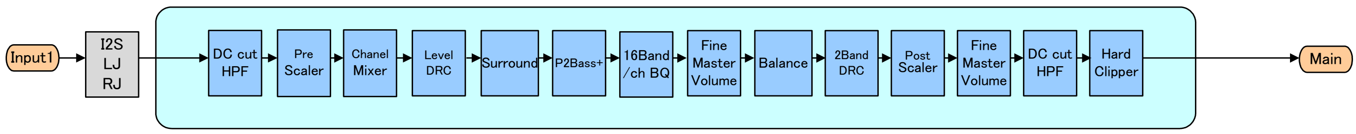

Figure 57. DSP Block diagram

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RSTX pin, MUTEX pin function

RSTX (4pin)	MUTEX (5pin)	DSP block condition	Speaker output condition
L	L	Reset ON	HiZ_Low (Low consumption)
H	L	Normal operation (Mute ON)	HiZ_Low (Mute ON)
H	H	Normal operation (Mute OFF)	Normal operation (Mute OFF)
L	H	Don't use.	

※RSTX is set Low, internal registers are initialized.
※VCCP1, VCCP2< 2.5V, IC latched by protection circuit and ERROR terminal condition are initialized.
※If DVDD is under 3V, RSTX is set Low once for 10ms(min), and set High again. Then DSP is needed to set parameter again.

SDB pin function

SDB (41pin)	Audio amplifier output (43pin,44pin)
L	HiZ_Low (Low consumption)
H	Normal operation

The negative power supply circuit starts when H level is input to SDB, and power is downed at the SDB=L level.

Input Digital sound sampling frequency (fs) explanation

PWM sampling frequency of Speaker output and Soft-mute transition time depends on sampling frequency (fs) of the digital sound input. These transition times are changed by sending select address &h15 [1:0].

Sampling frequency of the Digital sound input (fs)	Speaker output PWM sampling frequency	Soft-mute Transition time	
		Mute ON	Mute OFF
48kHz	384kHz	85.4msec	10.7msec
		42.7msec	10.7msec
		21.4msec	10.7msec
		10.7msec	10.7msec
44.1kHz	352.8kHz	92.9msec	11.7msec
		46.5msec	11.7msec
		23.3msec	11.7msec
		11.7msec	11.7msec
32 kHz	256kHz	128.1msec	16.1msec
		64.1msec	16.1msec
		32.1msec	16.1msec
		16.1msec	16.1msec

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2 wire Bus control signal specification

1) Electrical characteristics and Timing of Bus line and I/O stage

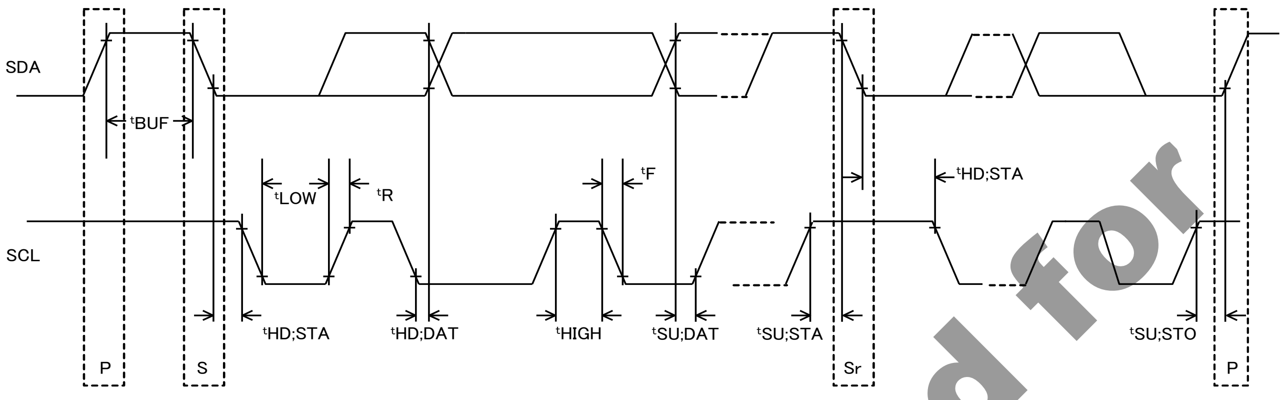

Figure 58

SDA and SCL bus line characteristics (Unless otherwise specified Ta=25°C, VCC=13V)

	Parameter	Symbol	High speed mode		Unit
			Min	Max	
1	SCL clock frequency	fSCL	0	400	kHz
2	Bus free time between「Stop」condition and「Start」condition	tBUF	1.3	–	μS
3	Hold-time of (sending again)「Start」condition. After this period the first clock pulse is generated.	tHD;STA	0.6	–	μS
4	SCL clock's LOW state Hold-time	tLOW	1.3	–	μS
5	SCL clock's HIGH state Hold-time	tHIGH	0.6	–	μS
6	Set-up time of sending again「Start」condition	tSU;STA	0.6	–	μS
7	Data hold time	tHD;DAT	0 (Note1)	–	μS
8	Data set-up time (Note2)	tSU;DAT	500/250/150	–	ns
9	Rise-time of SDA and SCL signal	tR	20+0.1Cb	300	ns
10	Fall-time of SDA and SCL signal	tF	20+0.1Cb	300	ns
11	Set-up time of「Stop」condition	tSU;STO	0.6	–	μS
12	Capacitive load of each bus line	Cb	–	400	pF

The above-mentioned numerical values are all the values corresponding to VIH min and the VIL max level.
(Note1) To exceed an undefined area on the fall-edge of SCL (VIH min of the SCL signal), the transmitting set should internally offer the holding time of 300ns or more for the SDA signal.
(Note2) SCL and SDA pin is not corresponding to threshold tolerance of 5V.
Please use it within 4.5V of the absolute maximum rating.

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2) Command interface

2 wire Bus control is used for command interface between hosts CPU. It not only writes but also it is possible to read it excluding a part of register. In addition to "Slave Address " , set and write 1 byte of "Select Address " to read out the data. 2 wire bus Slave mode format is illustrated below.

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	Data	A	P

S : Start Condition
Slave Address : The data of eight bits in total is sent putting up bit of Read mode (H) or Write mode (L) after slave address (7bit) set with the terminal ADDR. (MSB first)
A : The acknowledge bit adds to data that the acknowledge is sent and received in each byte.
When data is correctly sent and received, "L"is sent and received.
There was no acknowledgement for "H".
Select Address : The select address in one byte is used.(MSB first)
Data : Data byte is sent and received data(MSB first)
P : Stop Condition

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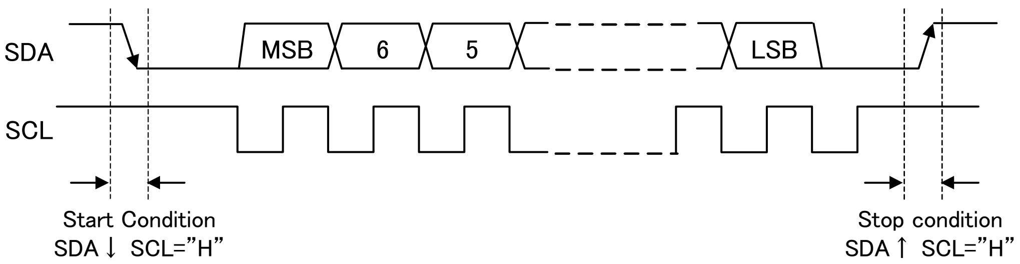

Figure 59

3) Slave Address

・While ADDR pin is"L"

MSB … LSB

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	0	1/0

・While ADDR pin is"H"

MSB … LSB

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	1	1/0

4) Writing of data

・Basic format

S	Slave Address	A	Select Address	A	Data	A	P

(cyan box) : Master to Slave, (white box) : Slave to Master

・Auto-increment format

S	Slave Address	A	Select Address	A	Data 1	A	Data 2	A	Data 3…N	A	P

(cyan box) : Master to Slave, (white box) : Slave to Master

5) Reading of data

First of all, the address (20h in the example) for reading is written in the register of the D0h address at the time of reading. In the following stream, data is read after the slave address. Please do not return the acknowledge when you end the reception.

S	Slave Address	A	Req_Addr	A	Select Address	A	P
(ex.)	80h		D0h		20h		

S	Slave Address	A	Data 1	A	Data 2	A		A	Data N	Ā	P
(ex.)	81h		**h		**h				**h		

(cyan box) : Master to Slave, (white box) : Slave to Master, A : With Acknowledge, Ā : Without Acknowledge

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Format of digital audio input

- LRCLK: It is L/R clock input signal.
  It corresponds to 32kHz/44.1kHz/48kHz with those clock (fs) that are same to the sampling frequency (fs).
  The audio data of a left channel and a right channel for one sample is input to this section.

- BCLK: It is Bit Clock input signal.
  It is used for the latch of data in every one bit by sampling frequency's 48 times frequency (48fs) or 64 times sampling frequency (64fs). However if the 48fs being selected, the input will be Right-justified data format and held static.

- SDATA: It is Data input signal.
  It is amplitude data. The data length is different according to the resolution of the input digital data.
  It corresponds to 16/ 20/ 24 bit.

The digital input has I2S, Left-justified and Right-justified formats.
The figure below shows the timing chart of each transmission mode.

Bit clock 64fs

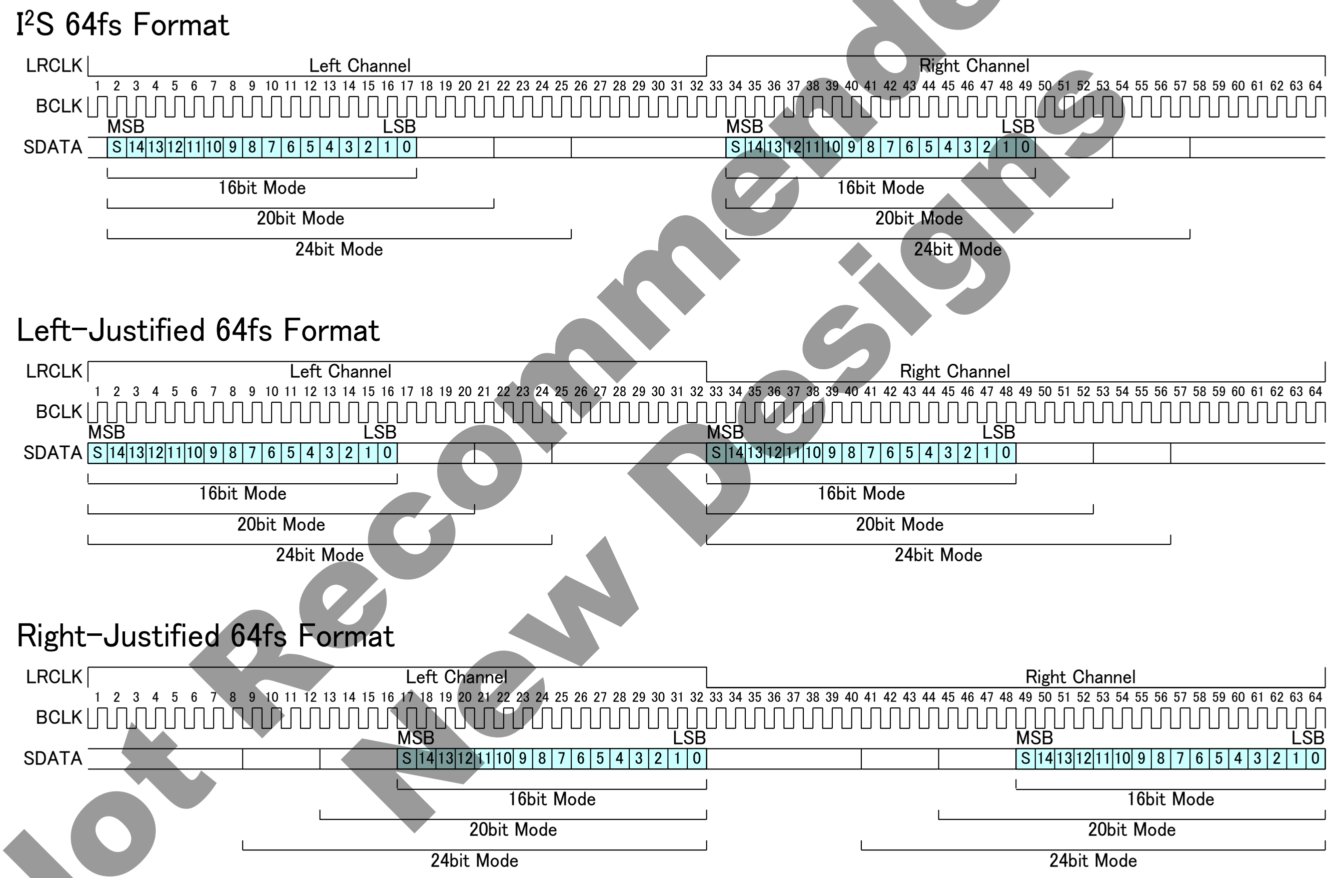

Figure 60

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Bit clock 48fs

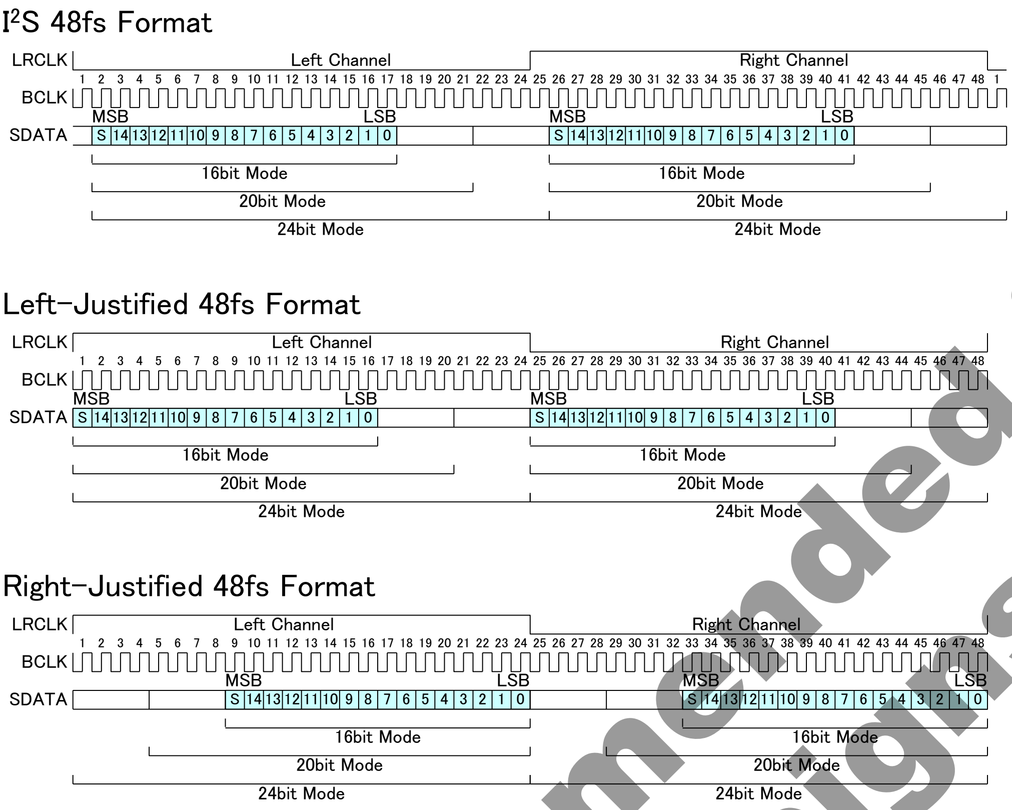

Figure 61

Bit clock 32fs

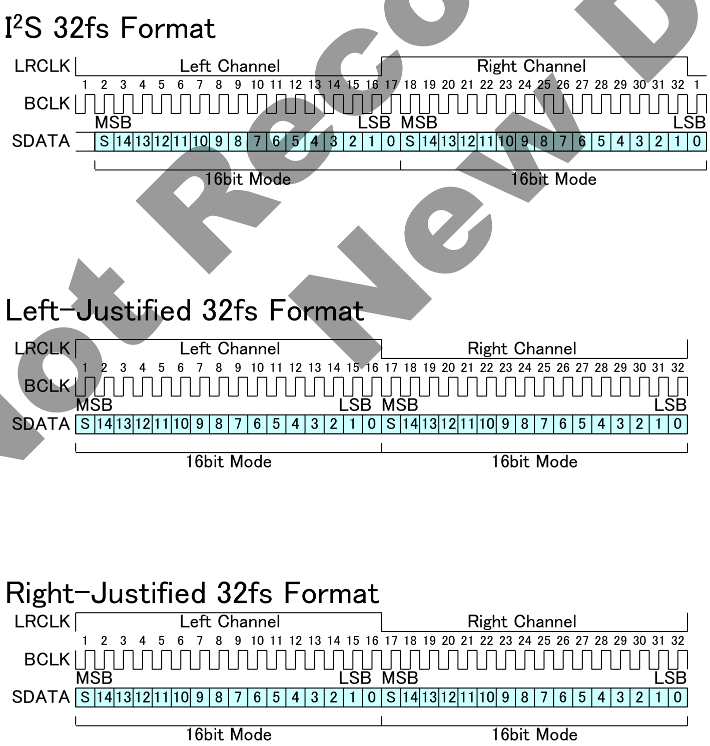

Figure 62

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Format setting for Digital Audio Interface

Please set Bit clock fs , Data strength and Format by transmitting command according to inputted Digital Serial Audio signal.

Bit clock

Default = 0

Select Address	Value	Explanation of operation
&h03[5:4]	0	64fs
	1	48fs
	2	32fs

Data Format

Default = 0

Select Address	Value	Explanation of operation
&h03[3:2]	0	IIS format
	1	Left-justified format
	2	Right-justified format

Data strength

Default = 2

Select Address	Value	Explanation of operation
&h03[1:0]	0	16 bit
	1	20 bit
	2	24 bit

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Audio Interface format and timing

Recommended timing and operating conditions (BCLK, LRCLK, SDATA)

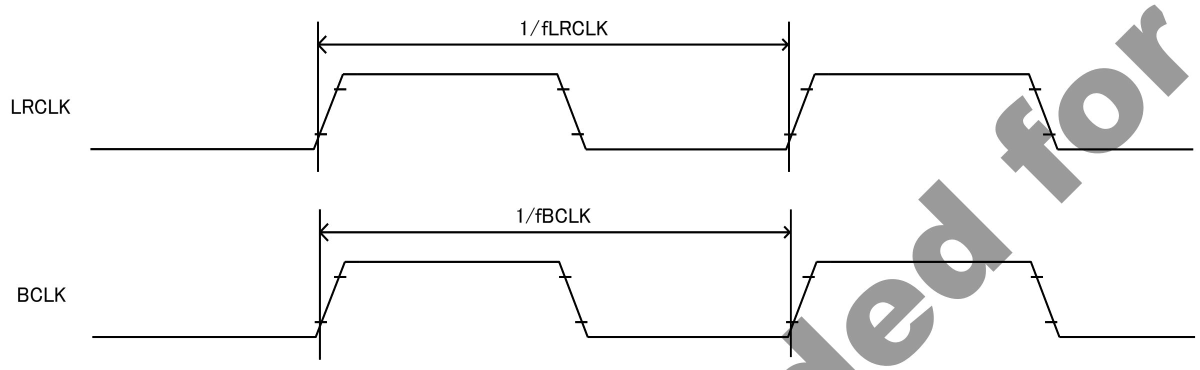

Figure 63. Clock timing

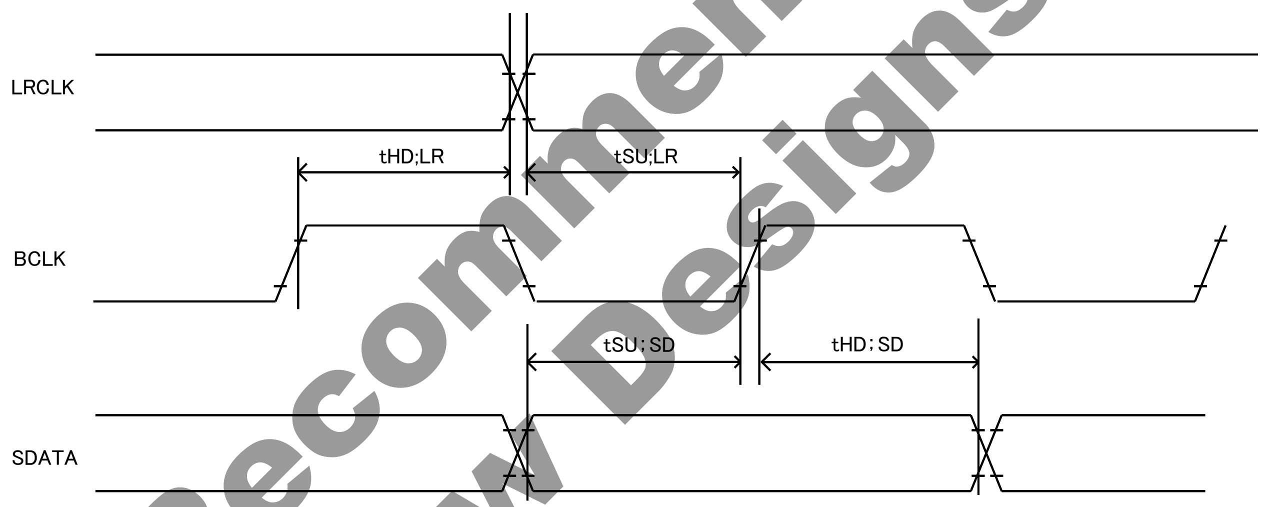

Figure 64. Audio Interface timing

No.	Parameter	Symbol	Limit		Unit
			Min	Max	
1	LRCLK frequency	fLRCLK	32	48	kHz
2	BCLK frequency	fBCLK	2.048	3.072	MHz
3	Setup time, LRCLK(Note1)	tSU;LR	20	–	ns
4	Hold time, LRCLK(Note1)	tHD;LR	20	–	ns
5	Setup time, SDATA	tSU;SD	20	–	ns
6	Hold time, SDATA	tHD;SD	20	–	ns
7	LRCLK, DUTY	dLRCLK	40	60	%
8	BCLK, DUTY	dBCLK	40	60	%

(Note1) This regulation is to keep rising edge of LRCK and rising edge of BCLK from overlapping.

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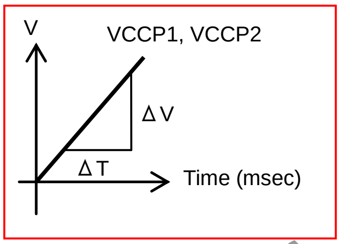
Power supply start-up sequence

＊Important precaution for Ramp up procedure
Ramp up speed of VCCP1 and VCCP2 must be less than ΔV/ΔT=7（V/msec）.If ramp up speed of VCCP1 and VCCP2 exceeds this time, there is a possibility of malfunction of short detection circuit.
Under this condition, start up with output terminal grounding may cause destruction.



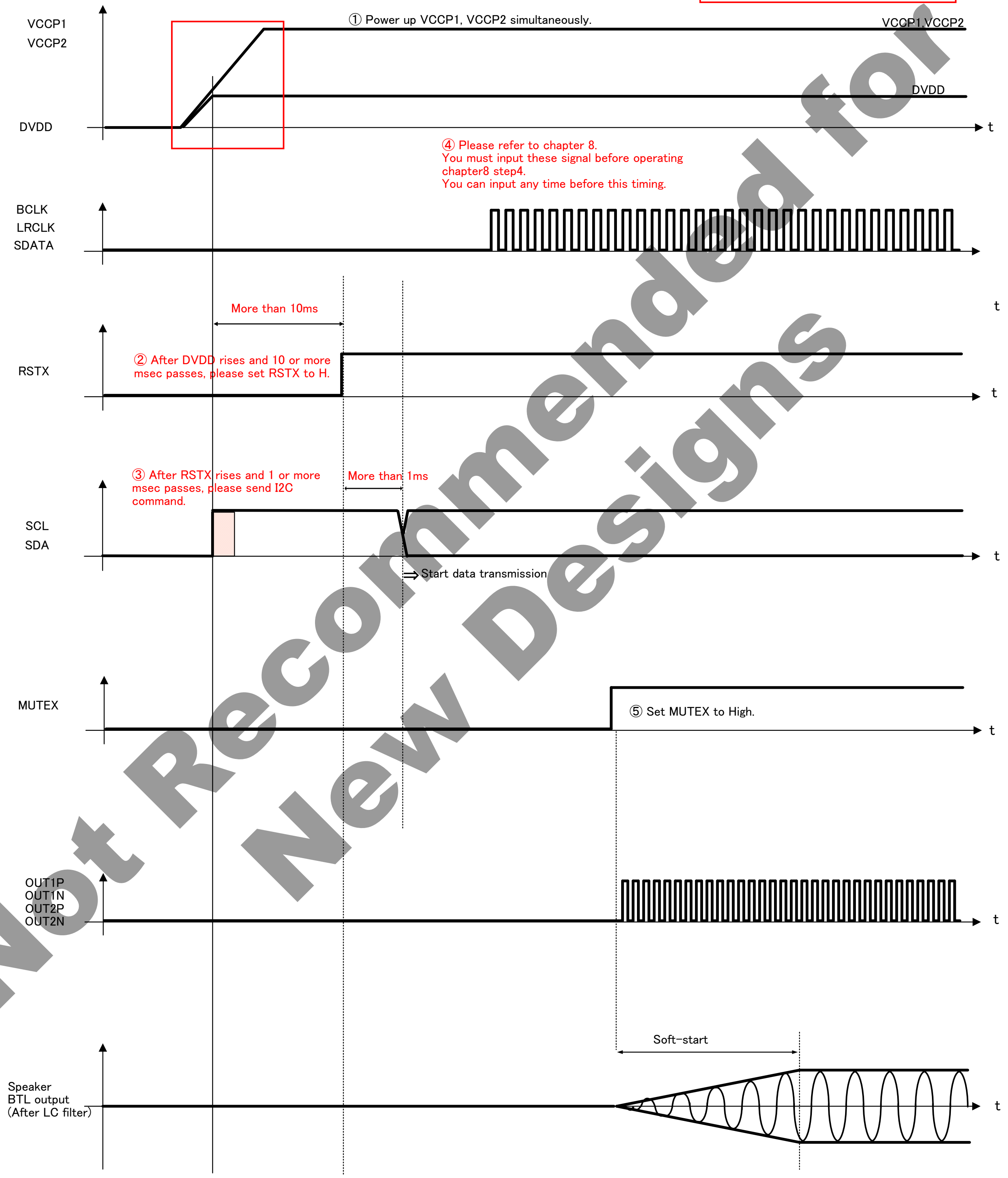


Figure 65

※To avoid POP noise or canceling error protection of IC, please set RSTX is L⇒H before MUTEX is L⇒H regularly.

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Power supply shut-down sequence

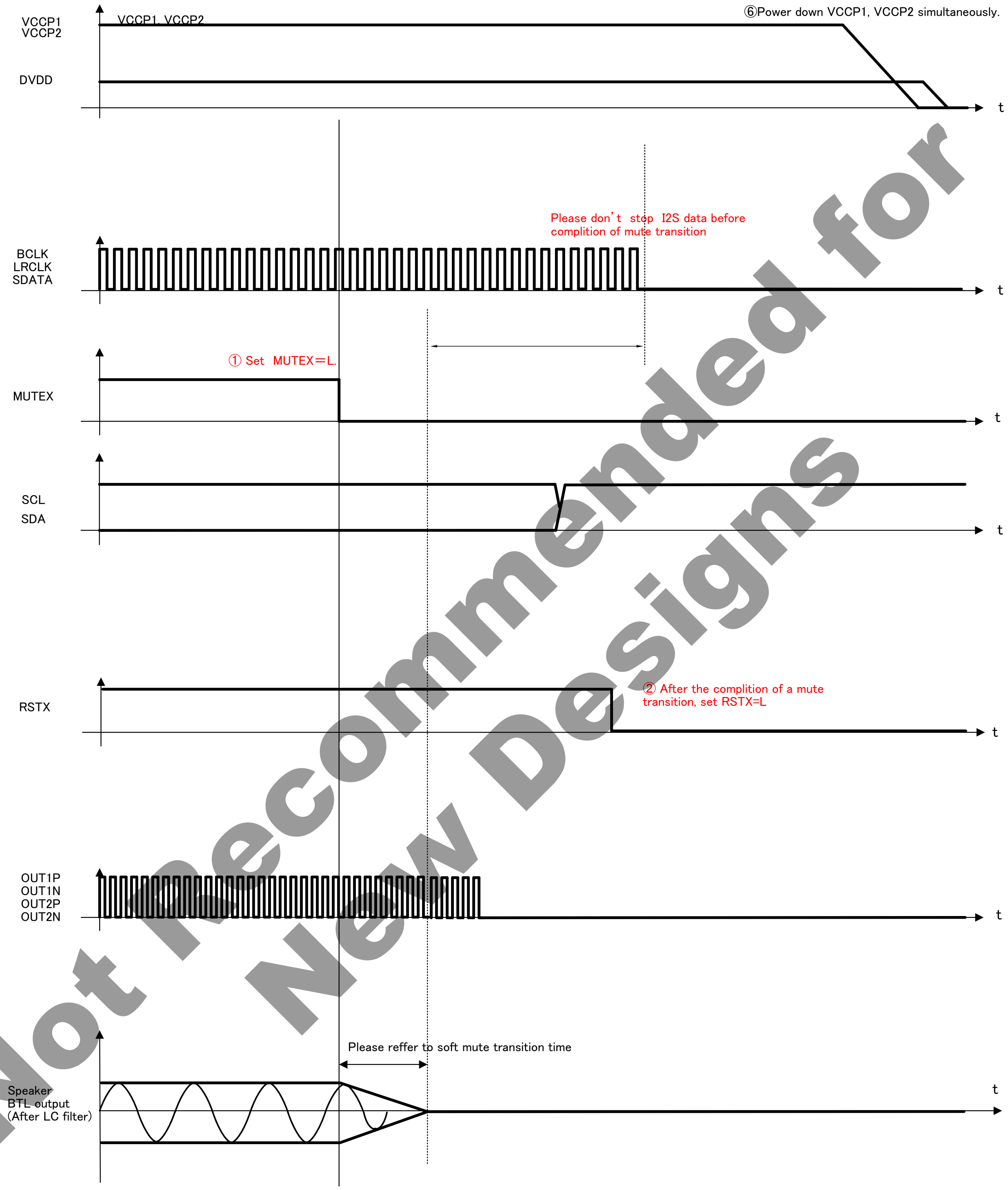

Figure 66

※To avoid POP noise or canceling error protection of IC, please set MUTEX is H⇒L and keep mute transition time before RSTX is H⇒L regularly.
※To avoid POP noise, please set RSTX is H⇒L time before DVDD Power down.

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About the protection function

Protection function	Detecting & Releasing condition		Speaker PWM output	ERROR output
Output short protection	Detecting condition	Detecting current = 7.2A (TYP)	HiZ_Low (Latch) *1	L (Latch)
DC voltage protection	Detecting condition	PWM output Duty=0% or 100% for 12µsec(TYP)and over	HiZ_Low (Latch) *1	L (Latch)
High temperature protection	Detecting condition	Chip temperature to be above 150°C (TYP)	HiZ_Low	H
	Releasing condition	Chip temperature to be below 120°C (TYP)	Normal operation	
Under voltage protection	Detecting condition	Power supply voltage to be below 8.1V (TYP)	HiZ_Low	H
	Releasing condition	Power supply voltage to be above 9.1V (TYP)	Normal operation	
Over voltage protection	Detecting condition	Power supply voltage to be above 29.5V (TYP)	HiZ_Low	H
	Releasing condition	Power supply voltage to be below 28.5V (TYP)	Normal operation	
Clock stop protection	Detecting condition	BCLK signal have stopped among constant period. LRCLK signal have stopped among constant period. BCLK frequency is under constant value. BCLK frequency is over constant value. ※Please refer to chapter 6 about constant value.	HiZ_Low	H
	Releasing condition	LRCLK signal haven't stopped among constant period and BCLK continues 30 or more msec of condition within constant frequency.	Normal operation	

* The ERROR pin is Nch open-drain output.
(Note1) Once an IC is latched, the circuit is not released automatically even after an abnormal status is removed.
The following procedures ① or ② is available for recovery.
①After MUTEX pin is made Low once over the soft mute transition time, MUTEX pin is returned to High again.
②Turning on the power supply again (VCCP1, VCCP2<2.5V, 10ms(min)).

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1)Output short protection (Short to the power supply)

This IC has the output short protection circuit that stops the PWM output when the PWM output is short-circuited to the power supply due to abnormality.

Detecting condition - It will detect when MUTEX pin is set High and the current that flows in the PWM output pin becomes 7.2A(TYP) or more. The PWM output instantaneously enters the state of HiZ-Low if detected, and IC does the latch.

Releasing method - ①After MUTEX pin is set Low once over the soft mute transition time(see page 23/106), MUTEX pin is returned to High again.
②Turning on the power supply again (VCCP1, VCCP2<2.5V, 10ms(min)).

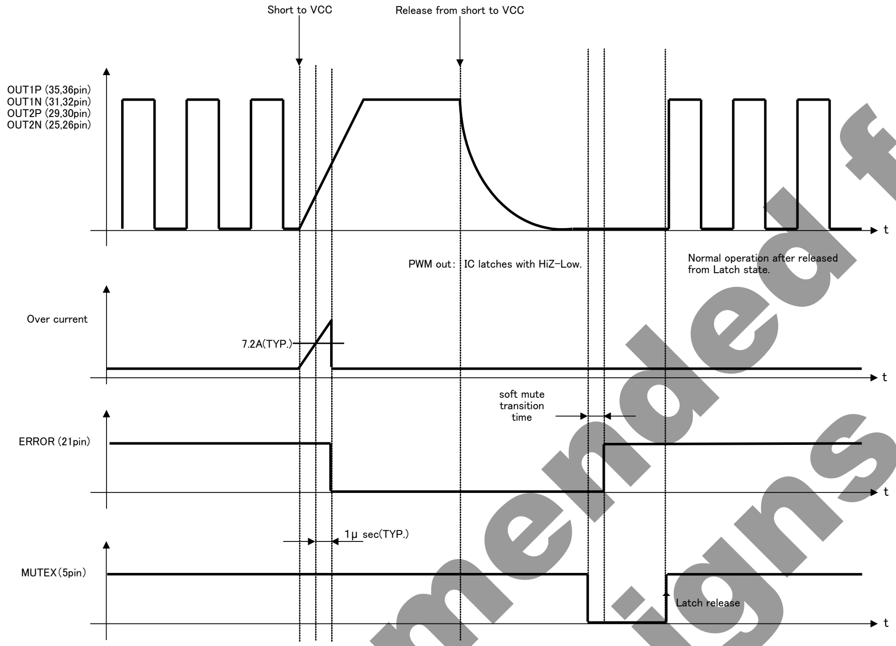

Figure 67

2)Output short protection (Short to GND)

This IC has the output short protection circuit that stops the PWM output when the PWM output is short-circuited to GND due to abnormality.

Detecting condition - It will detect when MUTEX pin is set High and the current that flows in the PWM output terminal becomes 7.2A(TYP) or more. The PWM output instantaneously enters the state of HiZ-Low if detected, and IC does the latch.

Releasing method – ①After MUTEX pin is set Low once over the soft mute transition time(see page 23/106), MUTEX pin is returned to High again.
②Turning on the power supply again (VCCP1, VCCP2<2.5V, 10ms(min)).

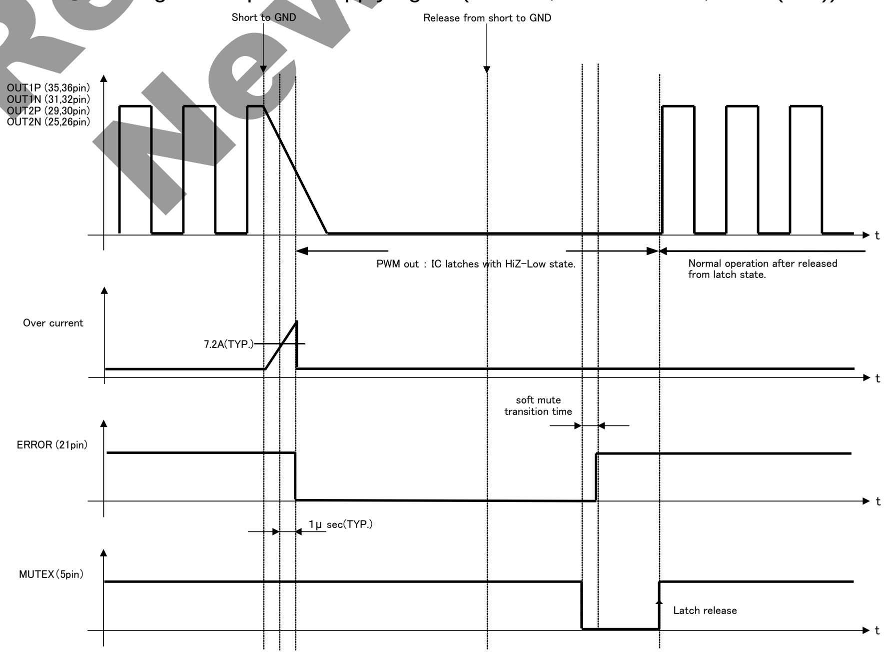

Figure 68

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3)DC voltage protection in the speaker

When the DC voltage in the speaker is impressed due to abnormality, this IC has the protection circuit where the speaker is defended from destruction.

Detecting condition - It will detect when MUTEX pin is set High and PWM output Duty=0% or 100% over 12μsec.(fs=48kHz) Once detected, The PWM output instantaneously enters the state of HiZ-Low, and IC does the latch.

Releasing method – ①After MUTEX pin is set Low once over the soft mute transition time(see page 23/106), MUTEX pin is returned to High again.
②Turning on the power supply again (VCCP1, VCCP2<2.5V, 10ms(min)).

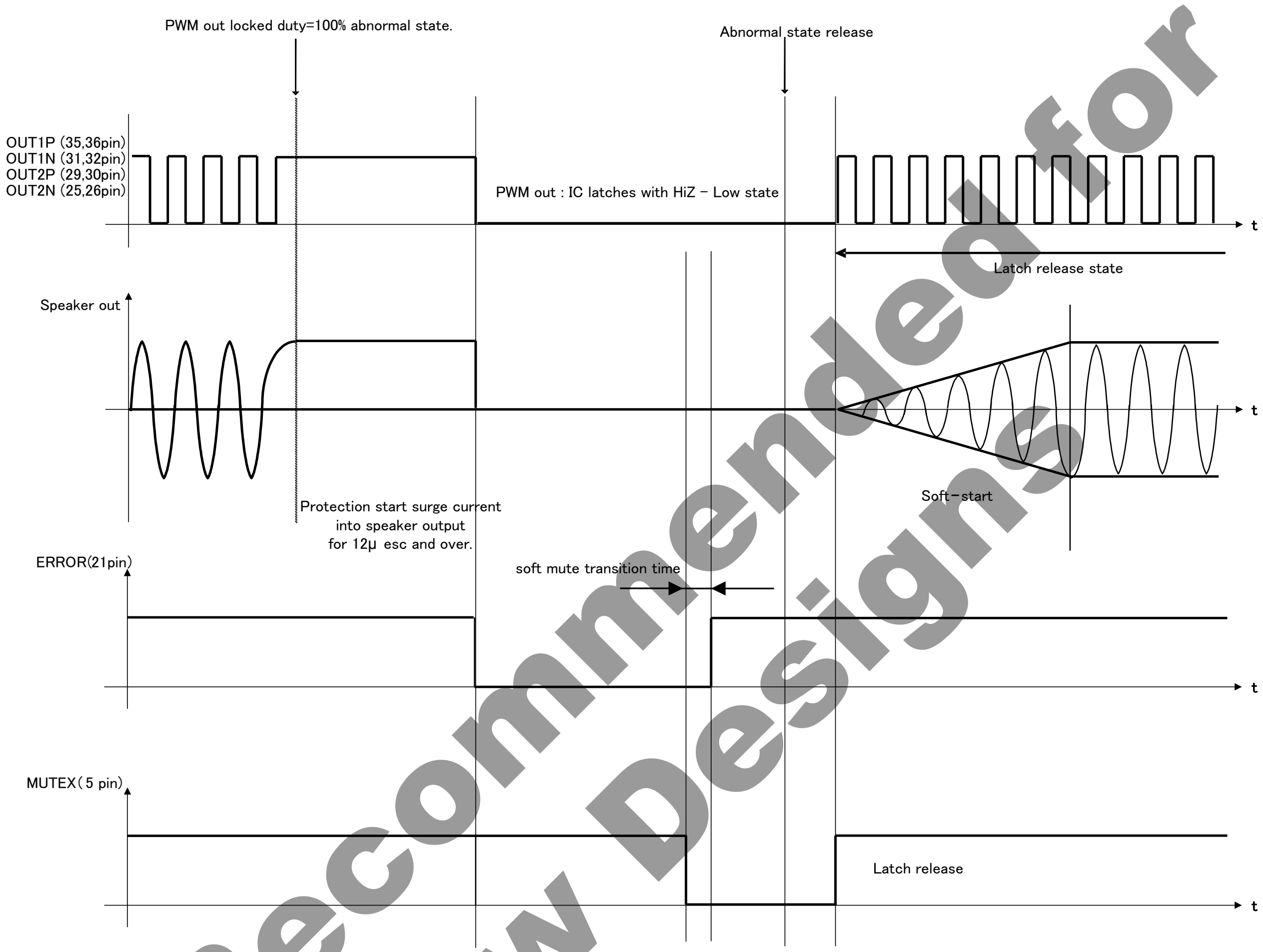

Figure 69

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4)High temperature protection

This IC has the high temperature protection circuit that prevents thermal reckless driving under an abnormal state for the temperature of the chip to exceed Tjmax=150°C.

Detecting condition - It will detect when MUTEX pin is set High and the temperature of the chip becomes 150°C(TYP) or more. The speaker output is muted when detected.

Releasing condition - It will release when MUTEX pin is set High and the temperature of the chip becomes 120°C(TYP) or less. The speaker output is outputted when released.

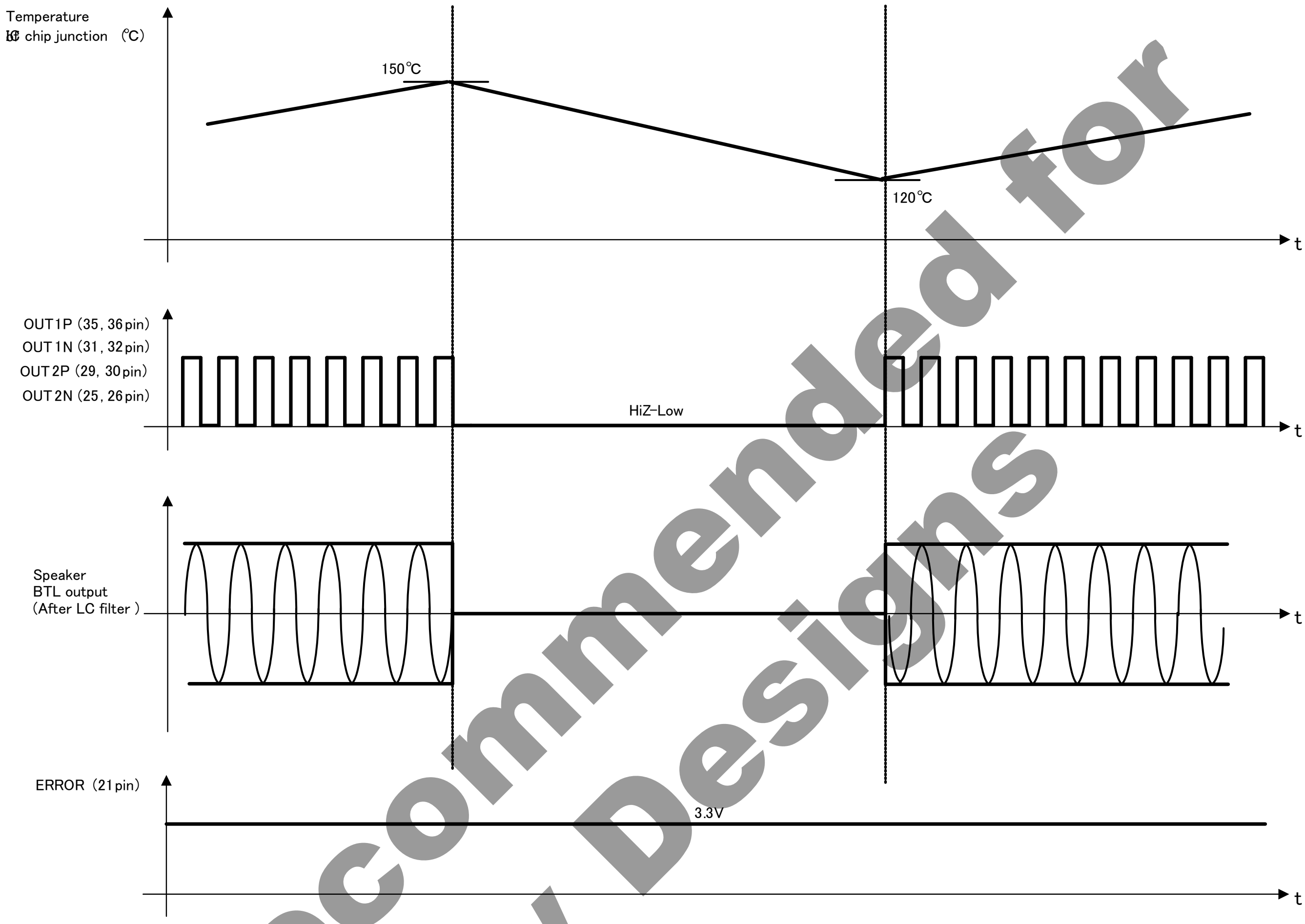

Figure 70

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5)Under voltage protection

This IC has the under voltage protection circuit that make speaker output mute once detecting extreme drop of the power supply voltage.

Detecting condition – It will detect when MUTEX pin is set High and the power supply voltage becomes lower than 8.1V. The speaker output is muted when detected.

Releasing condition – It will release when MUTEX pin is set High and the power supply voltage becomes more than 9.1V. The speaker output is outputted when released.

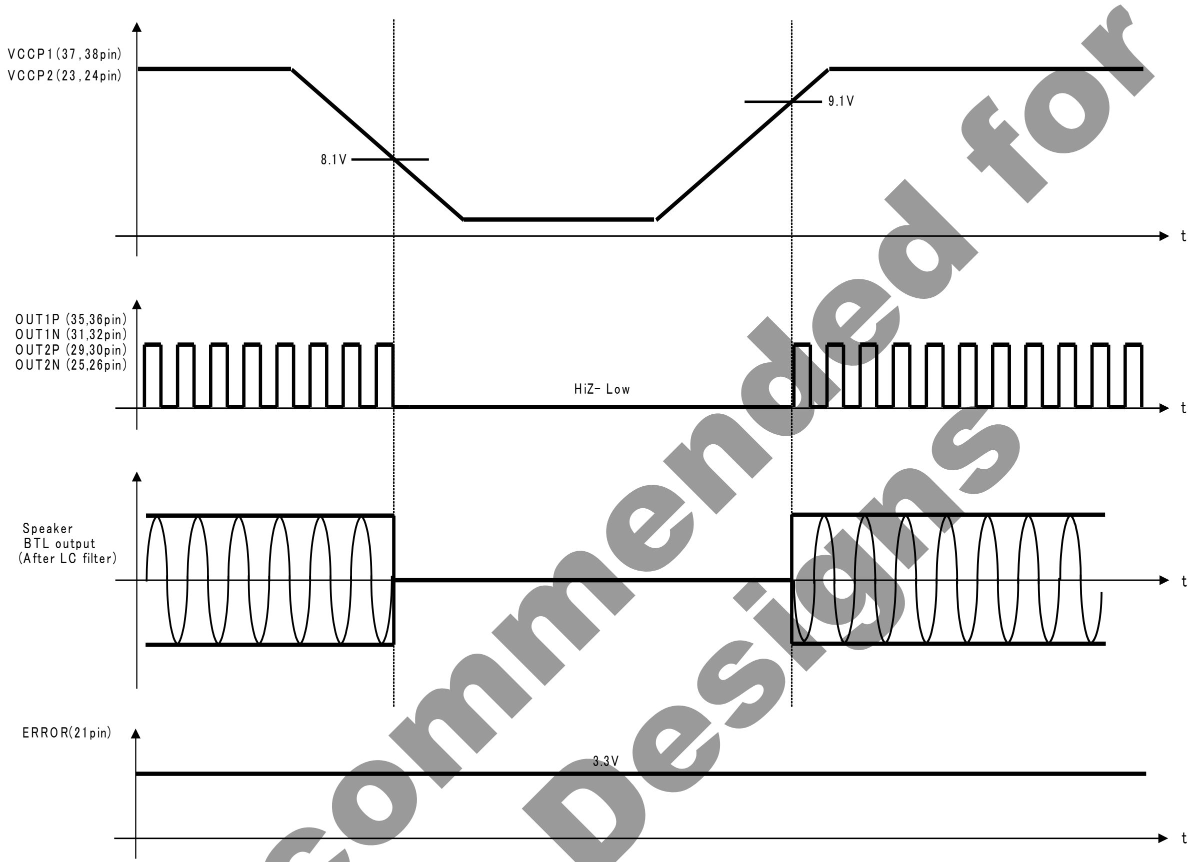

Figure 71

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6)Over voltage protection

This IC has the over voltage protection circuit that make speaker output mute once detecting extreme drop of the power supply voltage.

Detecting condition – It will detect when MUTEX pin is set High and the power supply voltage becomes more than 29.5V. The speaker output is muted when detected.

Releasing condition – It will release when MUTEX pin is set High and the power supply voltage becomes less than 28.5V. The speaker output is outputted when released.

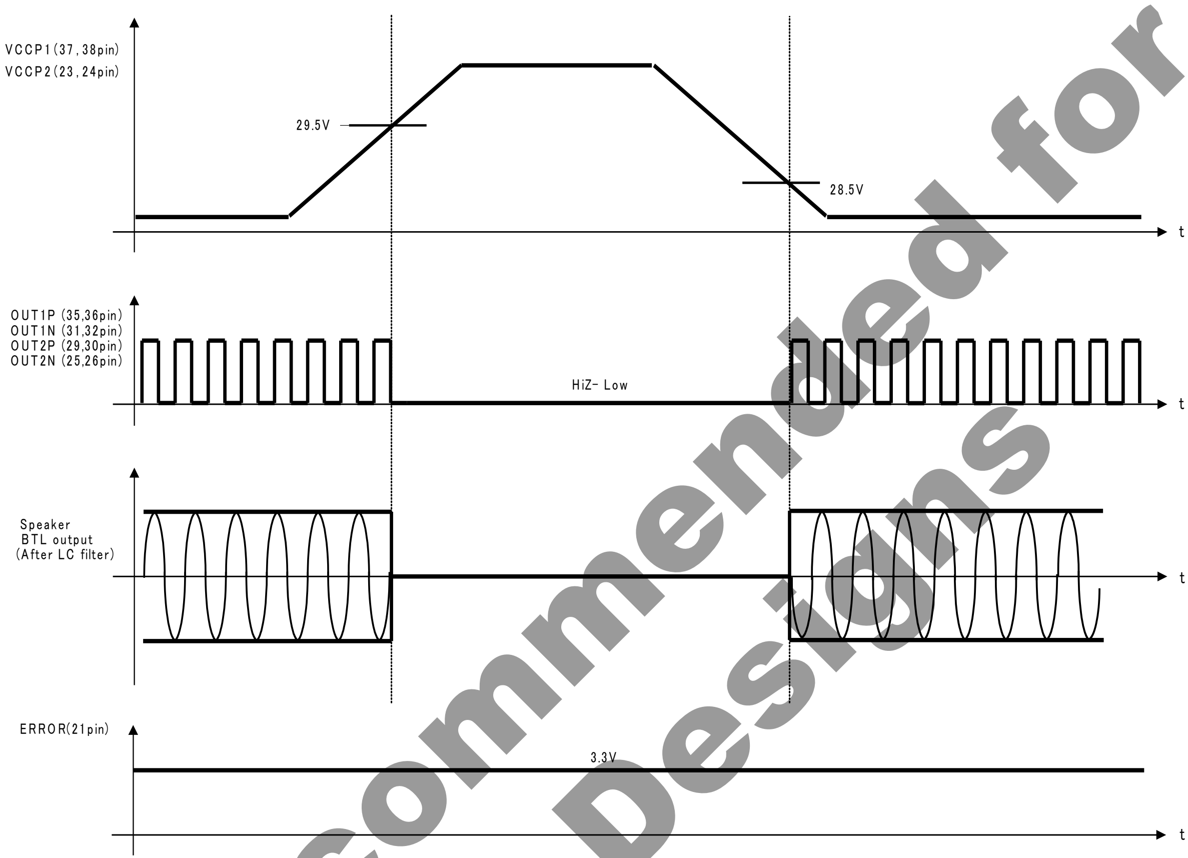

Figure 72

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7)Clock stop protection

This IC has the clock stop protection circuits that make the speaker output mute when the BCLK and LRCLK frequency of the digital sound input are decreased or low frequency.

Detecting condition - BCLK frequency is low or stop, LRCLK frequency is stop. The speaker output is muted.

Releasing condition – BCLK and LRCK are OK over 60msec(max).

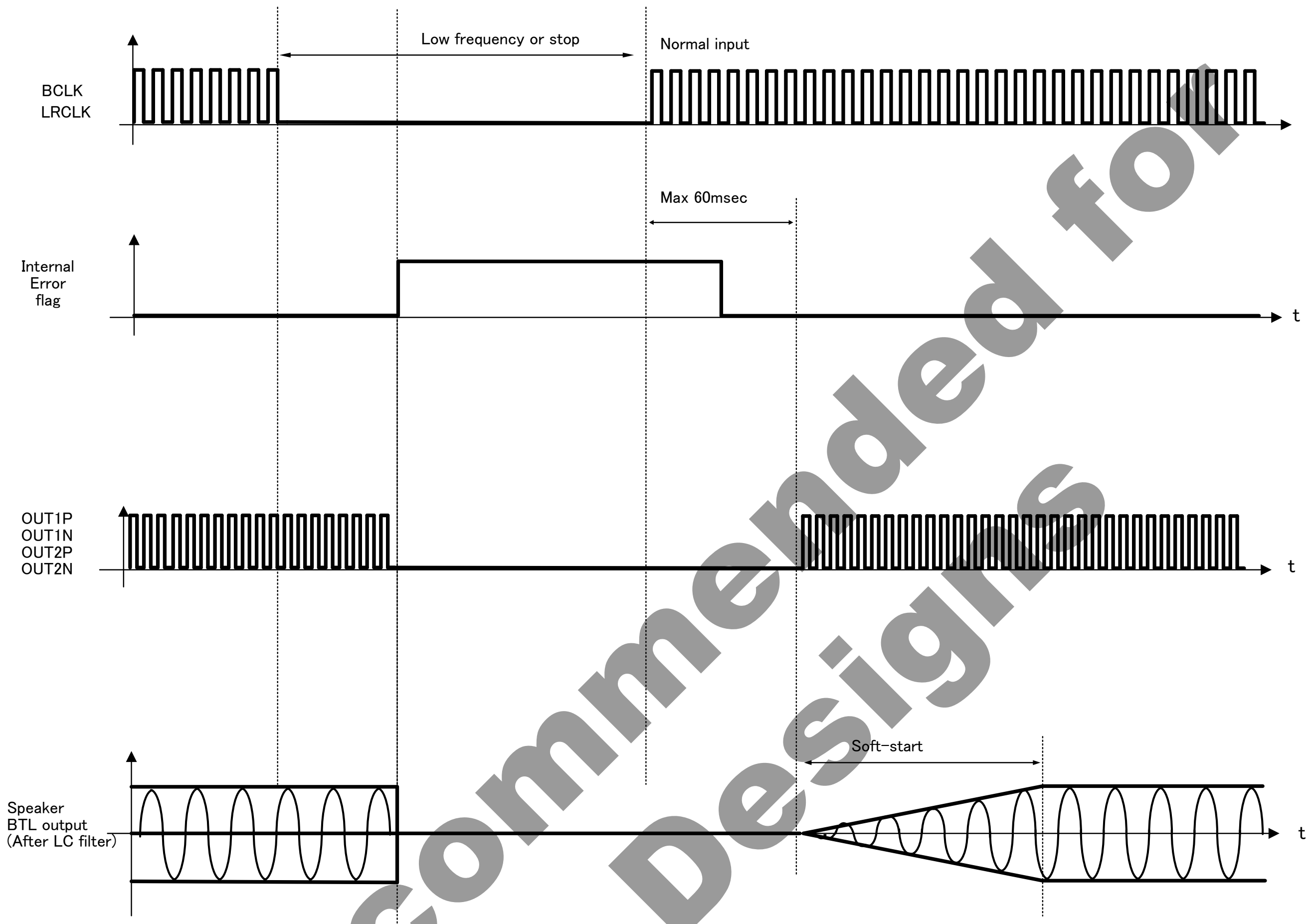

Figure 73

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Functional descriptions of DSP Block

1. Digital Sound Processing(DSP)

The digital sound processing (DSP) part of BM5481 is composed of the special hard ware which is the optimal for FPD-TV, the Mini/Micro Compo. BM5481MUV does the following processing using this special DSP.

DC cut HPF、Pre-scalar、Channel mixer、Level DRC、Surround、P^{2}Bass+、16 Band P-EQ、Fine Master Volume、Balance Volume、2 Band DRC、Post-scalar、Fine Post-scalar、Hard Clipper

The outline and signal flow of the DSP part

Data width:	32 bit (DATA RAM)
Machine cycle:	20.3ns (1024fs, fs=48kHz)
Multiplier:	32×24 → 56 bit
Adder:	56＋56 → 56 bit
Data RAM:	512×32 bit
Coefficient RAM:	512×24 bit
Sampling frequency :	fs=32k,44.1k,48kHz

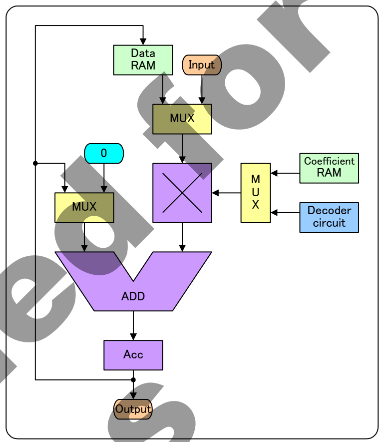

Figure 74

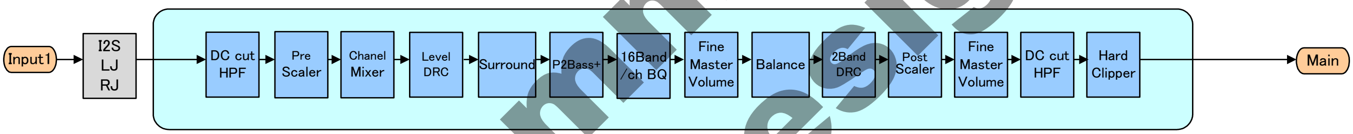

Figure 75

The digital signal from 16 bits to 24 bits is inputted to the DSP but extends 8bit(+48dB) as the overflow margin to the upper side. When doing the processing which exceeds this range, it processes a clip in the DSP. Incidentally, in case of the 2nd IIR-type (BQ) filter which is often used generally as the digital filter, because it consumes a lot of overflow margins, the output of the multiplier and the adder inside needs note.

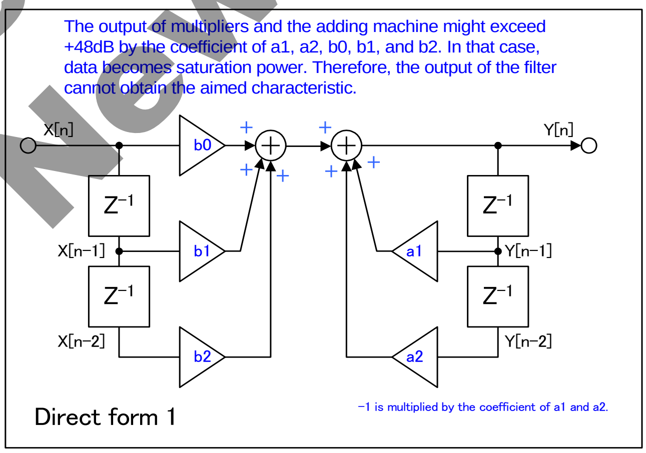

Figure 76

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The management of audio data is as follows by each block.

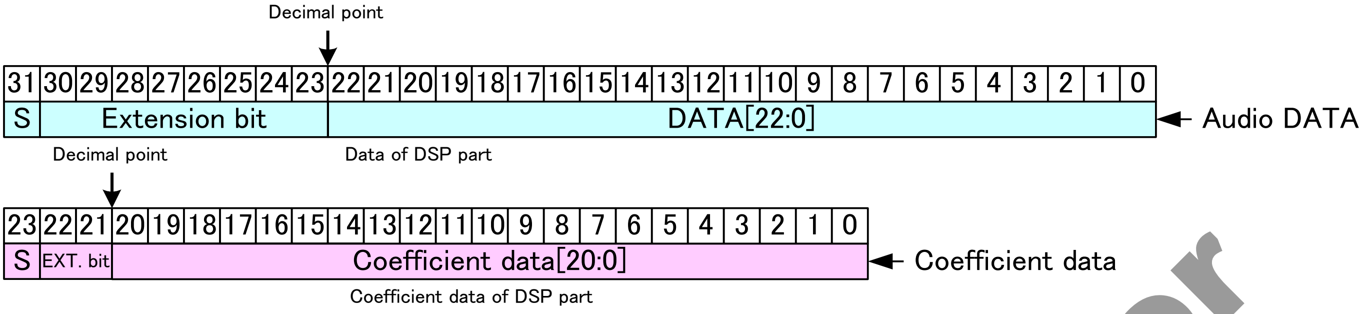

Figure 77

1-1 Bypass

It passes in the each function of the DSP by the command. Because it left the set value of the each function can be passed in, it is possible to do the confirmation of ON/OFF of the sound effect easily.
The effect which is possible about the bypass , 1) LEVEL DRC, 2) Surround 3) P^{2}Bass + (Pseudo Bass) , 4) 16Band BQ, 5) 2Band DRC and the whole DSP can be passed.

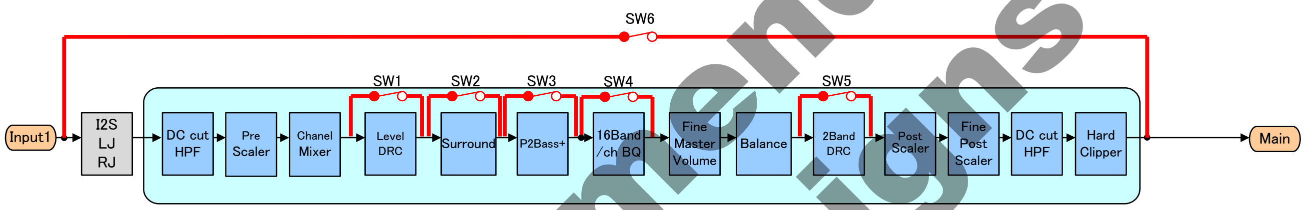

Figure 78

Default = 00h

Select Address	bit	Explanation of operation (*) '1' bypasses each function.
&h02 [5:0]	5	Bypass of LEVEL DRC (SW1) 0:Normal 1:Bypass
	4	Bypass of Surround (SW2) 0:Normal 1:Bypass
	3	Bypass of P^{2}Bass+ (SW3) 0:Normal 1:Bypass
	2	Bypass of 16Band BQ (SW4) 0:Normal 1:Bypass
	1	Bypass of 2band DRC (SW5) 0:Normal 1:Bypass
	0	Bypass of DSP (SW6) 0:Normal 1:Bypass

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1-2. Pre-scalar

To overflow when the level sometimes is full scale entry in case of the digital signal which is inputted to the sound DSP and does surround and equalizer processing, it adjusts an entry gain with Pre-scalar. The adjustable-range can be set from +48 dB to -79 dB with the 0.5-dB step. (Lch/Rch concurrency control)
Pre-scalar doesn't have a soft transfer feature.

Default = 60h

Select Address	Explanation of operation
&h16 [7:0]	(see table below)

Command Value	Gain
00	+48dB
01	+47.5dB
⋮	⋮
60	0dB
61	-0.5dB
62	-1dB
⋮	⋮
FE	-79dB
FF	-∞

1-3. Channel setup with a phase inversion function (Channel Mixer 1)

It sets a mixing in the sound on the left channel and the right channel of the digital signal which was inputted to the DSP. It makes a stereo signal a monaural here. Also, the phase-inversion, the mute on each channel can be set.

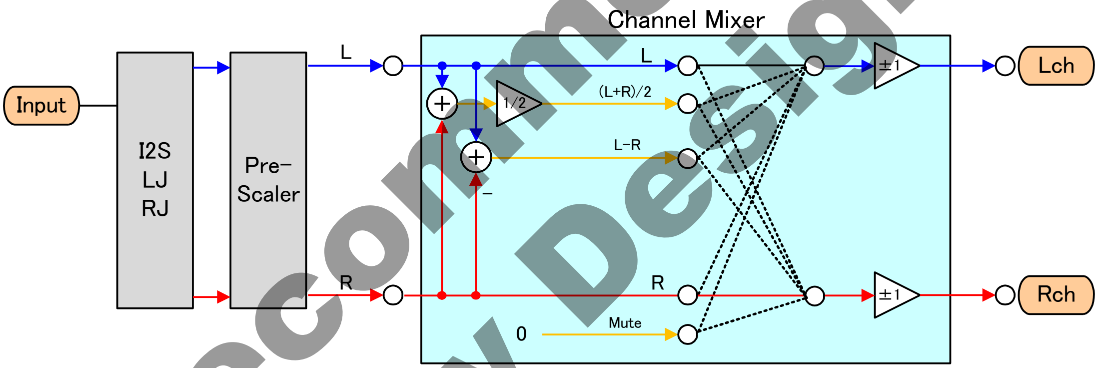

Figure 79

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DSP Input : The data inputted into Lch of DSP is inverted.

Default = 0

Select Address	Value	Explanation of operation
&h17[7]	0	Normal
	1	Invert

DSP Input : The data inputted into Lch of DSP is mixed.

Default = 1

Select Address	Value	Explanation of operation
&h17 [6:4]	0	Mute
	1	Lch data input
	2	Rch data input
	3	(Lch + Rch) / 2
	4	Lch-Rch
	5	-
	6	-
	7	-

DSP input : The data inputted into Rch of DSP is inverted.

Default = 0

Select Address	Value	Explanation of operation
&h17 [3]	0	Normal
	1	Invert

DSP Input : The data inputted into Rch of DSP is mixed.

Default = 2

Select Address	Value	Explanation of operation
&h17 [2:0]	0	Mute
	1	Lch data input
	2	Rch data input
	3	(Lch + Rch) / 2
	4	Lch-Rch
	5	-
	6	-
	7	-

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1-4. 1st HPF for DC cut (Front)

It cuts the DC offset component of the digital signal which is inputted to the sound DSP with this HPF. The cut off frequency fc of HPF is using 1 Hz and the degree is using the 1st filter.

Default = 1

Select Address	Value	Explanation of operation
Input1 &h18 [1]	0	Not use DC cut HPF
	1	Use DC cut HPF

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1-5. Surround

Surround 1 emphasizes the stereo feeling, and is suitable for the music source.
Surround 2 is effective of a pseudo stereo. Because the monaural voice is pseudo made a stereo, it is suitable for the talk show etc. of the studio recording.

Surround1 function ON/OFF

Default = 0

Select Address	Value	Explanation of operation
&h40[7]	0	Surround1 OFF
	1	Surround1 ON

Surround2 function ON/OFF

Default = 0

Select Address	Value	Explanation of operation
&h40 [6]	0	Surround2 OFF
	1	Surround2 ON

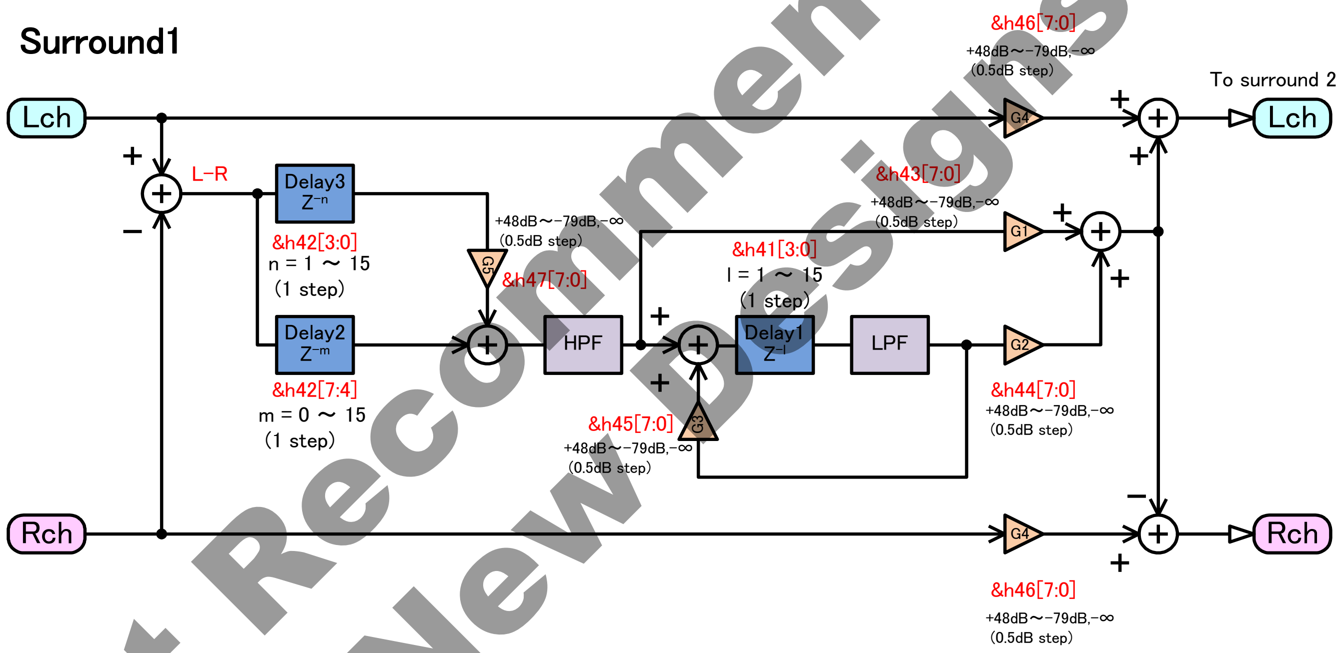

Figure 80

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Surround1 Delay value of feedback part setting for surround effect 1 (Delay1)

Default = 2h

Select Address	Explanation of operation
&h41 [3:0]	The command value becomes the amount of the delay. One sample delay is about 21μs. "0" is a set prohibition.

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Surround1　Delay value of input part setting for surround effect 1 (Delay2)

Default = 2h

Select Address	Explanation of operation
&h42 [7:4]	The command value becomes the amount of the delay. One sample delay is about 21µs.

Surround1　Delay value of input part setting for surround effect 1 (Delay3)

Default = 1h

Select Address	Explanation of operation
&h42 [3:0]	The command value becomes the amount of the delay. One sample delay is about 21µs. “0” is a set prohibition.

Surround1　Additive gain setting for surround effect 1 (G1, G2, G3)

Default =66h(G1),70h(G2),70h(G3)

Select Address	Explanation of operation
G1 : &h43 [7:0] G2 : &h44 [7:0] G3 : &h45 [7:0]	

Command	Gain
00	+48dB
01	+47.5dB
⋮	⋮
60	0dB
61	-0.5dB
62	-1dB
⋮	⋮
FE	-79dB
FF	-∞

Surround1　Additive gain setting for surround effect 1 (G4)

Default = 60h

Select Address	Explanation of operation
&h46 [7:0]	

Command	Gain
00	+48dB
01	+47.5dB
⋮	⋮
60	0dB
61	-0.5dB
62	-1dB
⋮	⋮
FE	-79dB
FF	-∞

Surround1　Additive gain setting for surround effect 1 (G5)

Default = FFh

Select Address	Explanation of operation
&h47 [7:0]	

Command	Gain
00	+48dB
01	+47.5dB
⋮	⋮
60	0dB
61	-0.5dB
62	-1dB
⋮	⋮
FE	-79dB
FF	-∞

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Surround1 HPF

Default=3h

Select Address	Explanation of operation
&h48 [7:4]	(see table below)

Command	Cut off freq.	Command	Cut off freq.
0	Through	8	1200Hz
1	330Hz	9	1500Hz
2	390Hz	A	-
3	470Hz	B	-
4	560Hz	C	-
5	680Hz	D	-
6	820Hz	E	-
7	1000Hz	F	-

Surround1 LPF

Default=5h

Select Address	Explanation of operation
&h48 [3:0]	(see table below)

Command	Cut off freq.	Command	Cut off freq.
0	Through	8	5600Hz
1	1500Hz	9	6800Hz
2	1800Hz	A	-
3	2200Hz	B	-
4	2700Hz	C	-
5	3300Hz	D	-
6	3900Hz	E	-
7	4700Hz	F	-

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Surround2

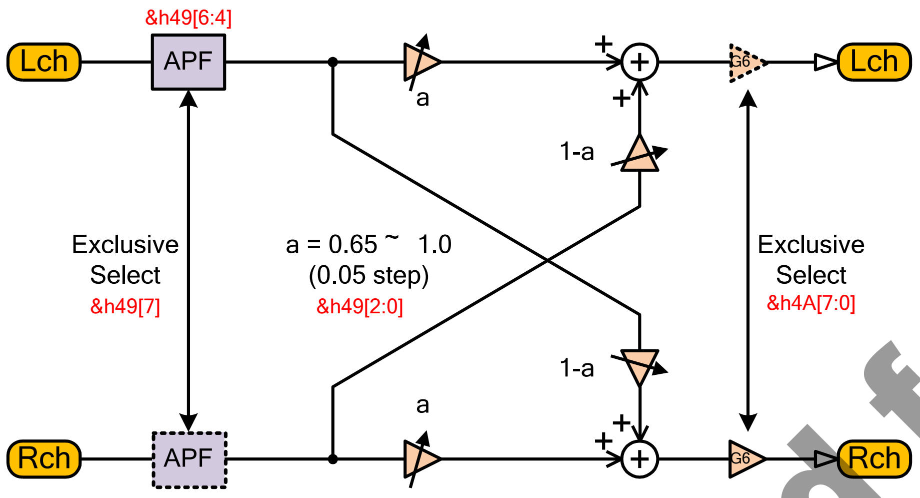

Figure 81

Surround2 APF(All Pass Filter)select
Select which channel of L/Rch to insert APF.

Default = 0

Select Address	Value	Explanation of operation
&h49 [7]	0	Lch
	1	Rch

Surround2 APF(All Pass Filter)Cut off frequency

Default = 0

Select Address	Value	Explanation of operation
&h49 [6:4]	0	22Hz
	1	47Hz
	2	100Hz
	3	220Hz
	4	470Hz

Surround2　LR mixing gain
Change the LR mix gain in surround effect 2. The sound extends to the setting of about big gain.

Default = 2h

Select Address	Explanation of operation
&h49 [2:0]	(see table below)

Command	Gain	Command	Gain
0	x0	4	x0.2
1	x0.05	5	x0.25
2	x0.1	6	x0.3
3	x0.15	7	x0.35

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Surround Output gain
Change the gain of the channel opposite to the channel selected with &h49[7].

Default = 60h

Select Address	Explanation of operation
&h4A [7:0]	(see table below)

Command	Gain
00	+48dB
01	+47.5dB
⋮	⋮
60	0dB
61	-0.5dB
62	-1dB
⋮	⋮
FE	-79dB
FF	-∞

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1-6. Pseudo bass (P^2Bass+)

A Pseudo bass function is a function which turns into that it is possible to emphasize low frequency sound effectively also to the low speaker of low-pass reproduction capability.
In order to be audible as the fundamental wave is sounding in false by adding 2 double sound and 3 time sound to a fundamental wave, the reproduction capability of the band of a fundamental wave becomes possible.
Although use independently is also possible for a pseudo bass function, low-pitched sound can be emphasized more by combining with P^2Bass function.
Moreover, since it is possible to change the band to emphasize, optimizing to the frequency characteristic of the speaker to be used is possible.

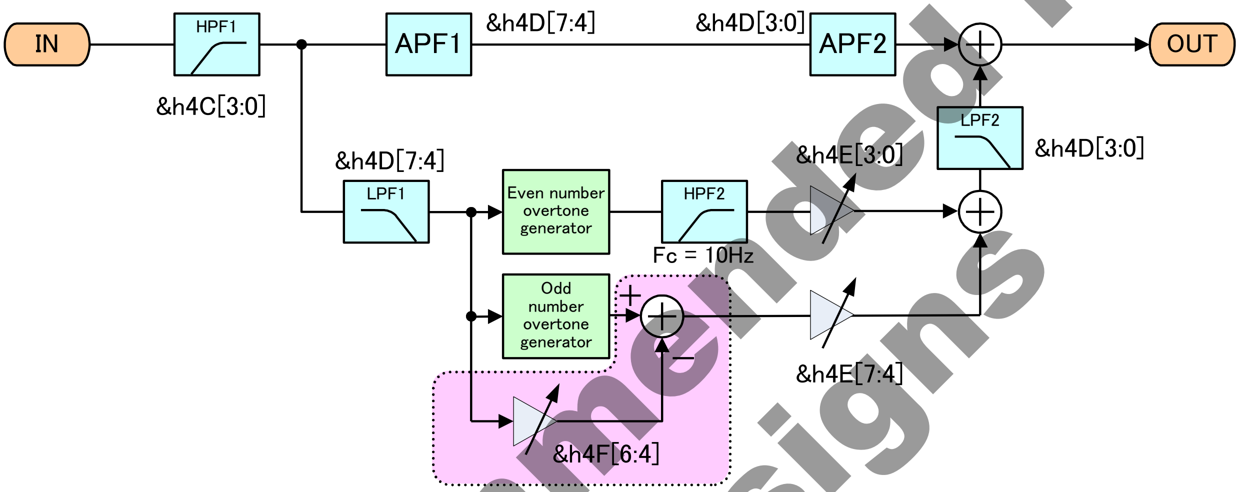

Figure 82

Pseudo bass ON/OFF
The effect of the bass emphasis of a pseudo bass (overtone) is used.
Default = 0

Select Address	Value	Explanation of operation
&h4C [7]	0	Not use pseudo bass (overtone)
	1	Use pseudo bass (overtone)

Setting of pseudo bass input HPF1(The super-low element of the fundamental harmonic input to the overtone generator can be cut.)
Default = 0h

Select Address	Explanation of operation
&h4C [3:0]	(see table below)

Command	Frequency	Command	Frequency
0	OFF	8	82Hz
1	22Hz	9	100Hz
2	27Hz	A	120Hz
3	33Hz	B	150Hz
4	39Hz	C	180Hz
5	47Hz	D	220Hz
6	56Hz	E	270Hz
7	68Hz	F	330Hz

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Pseudo bass input LPF1 selection. (The low element of the fundamental harmonic that the overtone generator inputs is extracted)

Default = 0h

Select Address	Explanation of operation
&h4D [7:4]	(see table below)

Command	Frequency	Command	Frequency
0	68Hz	8	330Hz
1	82Hz	9	390Hz
2	100Hz	A	470Hz
3	120Hz	B	560Hz
4	150Hz	C	680Hz
5	180Hz	D	820Hz
6	220Hz	E	1000Hz
7	270Hz	F	1200Hz

LPF2 setting for 2 overtones and 3 overtones. (The harmonic content of the overtone is suppressed with this LPF)

Default = 0h

Select Address	Explanation of operation
&h4D [3:0]	(see table below)

Command	Frequency	Command	Frequency
0	68Hz	8	330Hz
1	82Hz	9	390Hz
2	100Hz	A	470Hz
3	120Hz	B	560Hz
4	150Hz	C	680Hz
5	180Hz	D	820Hz
6	220Hz	E	1000Hz
7	270Hz	F	1200Hz

Additive gain setting for 3 overtones
When the input of the fundamental wave component is assumed to be 0dB, the output of the fundamental wave component from the overtone generator becomes -3dB.
(Output = Input - 3dB)

Default = 7h

Select Address	Explanation of operation
&h4E [7:4]	(see table below)

Command	Gain	Command	Gain
0	$-\infty$	8	7dB
1	0dB	9	8dB
2	1dB	A	9dB
3	2dB	B	10dB
4	3dB	C	11dB
5	4dB	D	12dB
6	5dB	E	13dB
7	6dB	F	14dB

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Additive gain setting for 2 overtones
When the input of the fundamental wave component is assumed to be 0dB, the output from the overtone generator becomes -6dB.

(Output = Input - 6dB)
Default = 7h

Select Address	Explanation of operation			
	Command	Gain	Command	Gain
&h4E [3:0]	0	-∞	8	1dB
	1	-6dB	9	2dB
	2	-5dB	A	3dB
	3	-4dB	B	4dB
	4	-3dB	C	5dB
	5	-2dB	D	6dB
	6	-1dB	E	7dB
	7	0dB	F	8dB

Subtraction gain setting for 3 overtones (recommendation value: -6dB or -4dB)
Default = 5h

Select Address	Explanation of operation			
	Command	Gain	Command	Gain
&h4F [6:4]	0	-∞	4	-6dB
	1	-12dB	5	-4dB
	2	-10dB	6	-2dB
	3	-8dB	7	0dB

Setting at blind time of odd-order overtone generation circuit
The high frequency signal that cannot be attenuated with LPF is included in the LPF1 outgoing signal input to the overtone generation circuit. It is set the blind time to do an unnecessary zero-cross point masking.

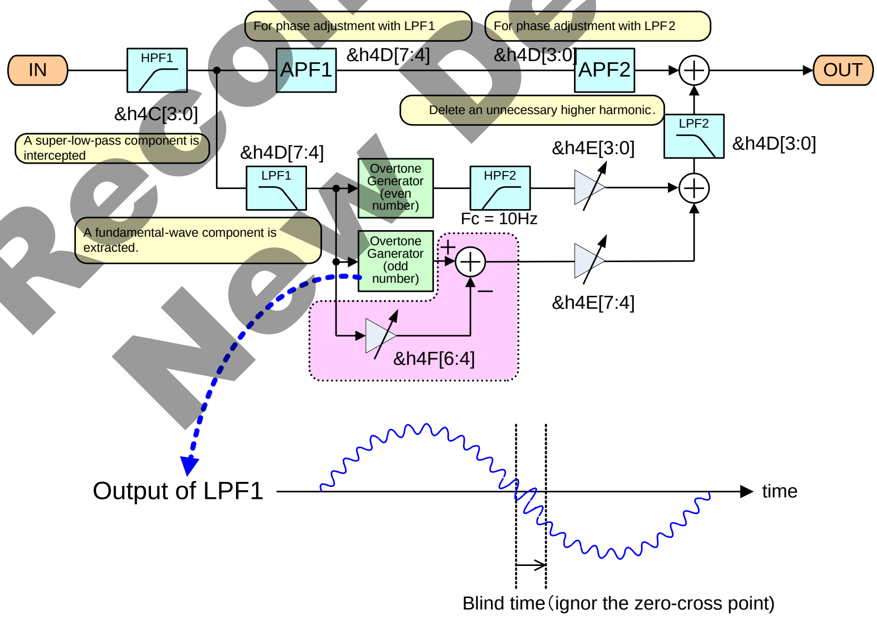

Figure 83

Default = 1

Select Address	Value	Explanation of operation
&h4F [1:0]	0	1.25ms (Fc of LPF1 = 47Hz to 180Hz)
	1	0.625ms (Fc of LPF1 = 220Hz to 390Hz)
	2	0.3125ms (Fc of LPF1 = 470Hz to 800Hz)

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1-7. Parametric Equalizer

In this IC, the following block has the feature of the parametric equalizer.
16Band BQ, Crossover filter of 2Band DRC block and BQ of the smooth transition.
The shape is used peaking filter, low shelf filter, high shelf filter, lowpass filter, highpass filter and all path filter.
The setting is to choose F, Q, Gain, and changes into the coefficient of the digital filter in the IC and it transfers to the coefficient RAM. 16Band BQ have the soft transfer feature. Incidentally, the detailed order of the parameter setting refer to the following PEQ setting method.
The coefficient RAM which stores a filter coefficient owns four banks and the command can choose it. The coefficient RAM for the parametric equalizer can set a coefficient to the bank-memory but the bank-memory during sound reconstruction.
But when a coefficient is written to BQ for smooth transition, write a coefficient to same bank for sound reconstruction.

Select of bank memory for coefficient RAM used to reproduce

Default = 0h

Select Address	Value	Explanation of operation
&h60[3:2]	0	BANK1
	1	BANK2
	2	BANK3
	3	BANK4

Select of bank memory used to set coefficient

Default = 0h

Select Address	Value	Explanation of operation
&h60 [1:0]	0	BANK1
	1	BANK2
	2	BANK3
	3	BANK4

L/R independence selection

Default = 0h

Select Address	Value	Explanation of operation
&h60 [4]*	0	L/R same
	1	L/R independence(Usable only BANK1、BANK2)

*Notes when &h60 4 is set
Please set all the parametric equalizers setting again, when you change the setting of &h60[4].
The re-setting parametric equalizers are 18 parametric equalizers of BQ1-16, DRC APF, and DRC HPF.
And, please set all BANK setting again, since the placement of BANK is changed, too.

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Sampling frequency selection of coefficient automatic calculated circuit

Default = 0h

Select Address	Value	Explanation of operation
&h50 [1:0]	0	For 48kHz
	1	For 44.1kHz
	2	For 32kHz

Select of PEQ setting

Only when choose 60[4]=1

Default = 0h

Select Address	Value	Explanation of operation
&h51 [7]	0	Lch
	1	Rch

When it is &h60[4]=1, and uses the L/R independence setting, and uses smooth transition,
Please synchronize Lch/Rch setting of &h51[7] and channel setting of &h 53[5:4].
Example 1 : When it set Lch at independently L/R: &h 53[5:4] =1 in case of &h60[4]=1 and &h51[7]=0.
Example 2 : When it set Rch at independently L/R: &h 53[5:4] =2 in case of &h60[4]=1 and &h51[7]=1.

Default = 00h

Select Address	Explanation of operation							
&h51[4 : 0]	Command	PEQ	Command	PEQ	Command	PEQ	Command	PEQ
	0	16Band BQ (1)	8	16Band BQ (9)	10	2Band DRC HPF	18	-
	1	16Band BQ (2)	9	16Band BQ (10)	11	2Band DRC APF	19	-
	2	16Band BQ (3)	A	16Band BQ (11)	12	-	1A	-
	3	16Band BQ (4)	B	16Band BQ (12)	13	-	1B	-
	4	16Band BQ (5)	C	16Band BQ (13)	14	-	1C	-
	5	16Band BQ (6)	D	16Band BQ (14)	15	-	1D	-
	6	16Band BQ (7)	E	16Band BQ (15)	16	-	1E	-
	7	16Band BQ (8)	F	16Band BQ (16)	17	-	1F	-

16Band BQ : BQ is Bi-Quad-type digital filter.
2 Band DRC HPF/APF : The crossover filter of 2Band DRC block should be set to high path filter and all pass filter.

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Select of filter type

Default = 0h

Select Address	Value	Explanation of operation
&h52[2:0]	0	Peaking Filter
	1	Peaking Filter(Equal Q type)
	2	Low Shelf Filter
	3	High Shelf Filter
	4	Low Pass Filter
	5	High Pass Filter
	6	All Pass Filter
	7	Filter through

Select of smooth transition

Default = 0h

Select Address	Value	Explanation of operation
&h53 [6]	0	Use smooth transition
	1	Not use smooth transition

Select channel of smooth transition

Default = 0h

Select Address	Value	Explanation of operation
&h53 [5:4]	0	Lch and Rch
	1	Lch
	2	Rch

Setting of smooth transition time

Default = 3h

Select Address	Value	Explanation of operation
&h53 [3:2]	0	2.7ms
	1	5.3ms
	2	10.7ms
	3	21.3ms

Setting of smooth transition wait time

Default = 0h

Select Address	Value	Explanation of operation
&h53 [1:0]	0	2.7ms
	1	5.3ms
	2	10.7ms
	3	21.3ms

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Setting of frequency (F_0)

Default = 0Eh

Select Address	Explanation of operation
&h54 [5:0]	

Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency
00	20Hz	08	50Hz	10	125Hz	18	315Hz	20	800Hz	28	2kHz	30	5kHz	38	12.5kHz
01	22Hz	09	56Hz	11	140Hz	19	350Hz	21	900Hz	29	2.2kHz	31	5.6kHz	39	14kHz
02	25Hz	0A	63Hz	12	160Hz	1A	400Hz	22	1kHz	2A	2.5kHz	32	6.3kHz	3A	16kHz
03	28Hz	0B	70Hz	13	180Hz	1B	450Hz	23	1.1kHz	2B	2.8kHz	33	7kHz	3B	18kHz
04	32Hz	0C	80Hz	14	200Hz	1C	500Hz	24	1.25kHz	2C	3.15kHz	34	8kHz	3C	20kHz
05	35Hz	0D	90Hz	15	220Hz	1D	560Hz	25	1.4kHz	2D	3.5kHz	35	9kHz	3D	-
06	40Hz	0E	100Hz	16	250Hz	1E	630Hz	26	1.6kHz	2E	4kHz	36	10kHz	3E	-
07	45Hz	0F	110Hz	17	280Hz	1F	700Hz	27	1.8kHz	2F	4.5kHz	37	11kHz	3F	-

Setting of quality factor (Q)

Default = 13h

Select Address	Explanation of operation
&h55 [4:0]	

Command	Q	Command	Q	Command	Q	Command	Q
00	0.33	08	1.2	10	5.6	18	1.932
01	0.39	09	1.5	11	6.8	19	0.51
02	0.47	0A	1.8	12	8.2	1A	0.601
03	0.56	0B	2.2	13	0.707	1B	0.9
04	0.68	0C	2.7	14	0.541	1C	2.563
05	0.75	0D	3.3	15	1.307	1D	-
06	0.82	0E	3.9	16	0.518	1E	-
07	1.0	0F	4.7	17	0.707	1F	-

Second butterworth is set to 13h. (BQx1) Fourth butterworth is set to 14h, 15h. (BQx2)
Sixth butterworth is set to 16h, 17h, 18h. (BQx3) Eighth butterworth is set to 19h, 1Ah, 1Bh, 1Ch. (BQx4)

Setting of gain (Gain)

Default = 40h

Select Address	Explanation of operation
&h56 [6:0]	

Command	Gain
1C	-18dB
⋮	⋮
38	-1dB
39	-0.5dB
40	0dB
41	+0.5dB
42	+1dB
⋮	⋮
64	+18dB

When the each coefficient (b0,b1,b2,a1,a2) exceeds ±4, it is not possible to set it.

Transfer start setting to coefficient RAM

Default = 0

Select Address	Value	Explanation of operation
&h57 [0]	0	Transfer stop
	1	Transfer start (After transferring is completed, it becomes 0 by the automatic operation.)

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Setting of smooth transition start

Default = 0

Select Address	Value	Explanation of operation
&h58 [0]	0	Stop the smooth transition operation
	1	Start the smooth transition operation (After the transition is completed, it becomes 0 by the automatic operation)

* This register cannot read-out.

Read-out smooth transition status

Select Address	Explanation of operation
&h59 [0]	"1" is read while software is changing. "0" is read usually.

[attention] The data of coefficient RAM can be read. Set values such as F, Q, and Gain cannot be read.

【Example of coefficient setting procedure 1】

Ex) Set fc=1kHz, Q=1.0, Gain=+6dB, and Filter type=Peaking Filter to 16Band BQ1 by using the soft transition function.
Sampling frequency: fs=48kHz, Smooth transition time: 21.3ms, Smooth transition wait time: 2.7ms Bank memory: BANK1 ,L/R same

1)&h60[4]=0h	:Select L/R same
2) &h60[1:0] = 0h	:Select BANK1(for writing)
&h60[3:2] = 0h	:Select BANK1(for reading)
3) &h50[1:0] = 0h	:Select sampling frequency to 48kHz
4) &h51[4:0] = 00h	:Select 16 Band BQ1
5) &h52[2:0] = 00h	:Select Peaking Filter
6) &h53[7:0] = 0Ch	
&h53[6] = 0h	: Use smooth transition
&h53[5:4] = 0h	:Select L/R smooth transition
&h53[3:2] = 3h	:Set smooth transition time to 21.3ms
&h53[1:0] = 0h	:Set smooth transition wait time to 2.7ms
7) &h54[5:0] = 22h	:Set frequency to 1kHz (f0)
8 &h55[4:0] = 07h	: Set quality factor to 1.0
9) &h56 [6:0] = 4Ch	: Set gain level to +6dB
10) &h57[0] = 1h	: Transferring start to coefficient RAM for smooth transition (After transferring is completed, it is cleared automatically to 0h.)

11) Even the transferring completion waits for about 150μs.

12) &h58[0] = 1h	: Smooth transition start (After smooth transition is completed, it is cleared automatically to 0h.)

13) About 24ms (21.3ms + 2.7ms) stands by to the smooth transition completion. Or, it stands by until 0 is read, and command &h59[0] is cleared to 0h.

【Example of coefficient setting procedure 2】

Ex) Set fc=200Hz, Q=0.707 and Filter type=Low Pass Filter to 16Band BQ2 by not using the soft transition function.
Sampling frequency: fs=44.1kHz, Bank memory: BANK1 ,L/R same

1) &h60[4] = 0h	:Select L/R same
2) &h60[1:0] = 0h	:Select BANK1(for writing)
3) &h50[1:0] = 1h	:Select sampling frequency to 44.1kHz
4) &h51[4:0] = 01h	:Select 16 Band BQ2
5) &h52[2:0] = 04h	:Select Low Pass Filter
6) &h53[6] = 1h	: Not Use smooth transition
7) &h54[5:0] = 14h	:Set frequency to 200Hz (f0)
8) &h55[4:0] = 17h	: Set quality factor to 0.707
9) &h56[6:0] = 40h	: Because Low Pass Filter was selected, the setting of the gain can be omitted.
10) &h57[0] = 1h	: Transferring start to coefficient RAM for smooth transition (After transferring is completed, it is cleared automatically to 0h.)

11) Even the transferring completion waits for about 150μs.

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【Example of coefficient setting procedure 3】

Ex) Set fc=2kHz, Q=0.56, and Filter type=Low Pass Filter to the ch. L of 16Band BQ3, and Set fc=3.15kHz, Q=0.68, and Filter type=High Pass Filter to the ch. R of 16Band BQ3 by using the soft transition function.
Sampling frequency: fs=48kHz, Smooth transition time: 21.3ms, Smooth transition wait time: 2.7ms Bank memory: BANK1 ,L/R independence.

1)&h60[4]=1h	:Select L/R independence
2)&h60[1:0]=0h	: Select BANK1(for writing)
&h60[3:2]=0h	: Select BANK1(for reading)
3)&h50[1:0]=0h	: Select sampling frequency to 48kHz
4)&h51[7:0]=02h	
&h51[7]=0h	:Select ch. L
&h51[4:0]=02h	:Select 16Band BQ3
5)&h52[2:0]=04h	:Select Low Pass Filter
6)&h53[7:0]=0Ch	
&h53[6]=0h	:Use smooth transition
&h53[5:4]=0h	:Select L/R smooth transition
&h53[3:2]=3h	:Set smooth transition time to 21.3ms
&h53[1:0]=0h	:Set smooth transition wait time to 2.7ms
7)&h54[5:0]=28h	:Set frequency to 2kHz (f0)
8)&h55[4:0]=03h	: Set quality factor to 0.56
9)&h56[6:0]=40h	: Because Low Pass Filter was selected, the setting of the gain can be omitted.
10)&h57[0]=1h	: Transferring start to coefficient RAM for smooth transition (After transferring is completed, it is cleared automatically to 0h.)

11) Even the transferring completion waits for about 150μs.

12)&h51[7:0]=82h	
&h51[7]=1h	:Select ch. R
&h51[4:0]=02h	:Select 16Band BQ3
13)&h52[2:0]=05h	:Select High Pass Filter
14)&h54[5:0]=2Ch	:Set frequency to 3.15kHz (f0)
15)&h55[4:0]=04h	: Set quality factor to 0.68
16)&h56[6:0]=40h	: Because High Pass Filter was selected, the setting of the gain can be omitted.0
17)&h57[0]=1h	: Transferring start to coefficient RAM for smooth transition (After transferring is completed, it is cleared automatically to 0h.)

18) Even the transferring completion waits for about 150μs.

19)&h58[0]=1h	: Smooth transition start (After smooth transition is completed, it is cleared automatically to 0h.)

20) About 24ms (21.3ms + 2.7ms) stands by to the smooth transition completion. Or, it stands by until 0 is read, and command &h59[0] is cleared to 0h.

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1-8. Volume

Volume is from+24dB to -103dB, and can be selected by the step of 0.125dB. At the time of switching of Volume, smooth transition is performed. Soft transition duration is optional with the command.
It becomes the following formula at the transition from AdB to BdB. C is smooth transition duration selected by &h15[7:6] command.

$$\text{Transition time} = \left|\left(10^{\frac{A}{20}} - 10^{\frac{B}{20}}\right) * C \ \text{ms}\right|$$

Setting of soft transition time

Default = 0

Select Address	Value	Explanation of operation
&h15 [7:6]	0	21.3ms
	1	42.7ms
	2	85.3ms

Setting of volume

Default = FFh

Select Address	Explanation of operation
&h11 [7:0]	(see table below)

Command	Gain
00	+24dB
01	+23.5dB
⋮	⋮
30	0dB
31	-0.5dB
32	-1dB
⋮	⋮
FE	-103dB
FF	-∞

Setting of fine volume
This command becomes effective by sending the following command after setting.
When using this command, it is possible to set a volume in 0.125dB carving.

Setting of fine volume

Default = 0h

Select Address	Value	Explanation of operation
&h10 [1:0]	0	0dB
	1	-0.125dB
	2	-0.25dB
	3	-0.375dB

【Note1】
It is possible to use with the 0.5-dB step in changing only &h11[7:0] when &h10[1:0]=0.

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【Note2】

It is possible to use with the 0.125-dB step in setting both &h10[1:0] and &h11[7:0].

In case of &h10[1:0]=0, it becomes the set value of &h11[7:0].
In case of &h10[1:0]=1, it becomes the -0.125dB set value of &h11[7:0].
In case of &h10[1:0]=2, it becomes the -0.25dB set value of &h11[7:0].
In case of &h10[1:0]=3, it becomes the -0.375dB set value of &h11[7:0].

Because it is fixed by the transfer of &h11 in any case, the soft transfer can be beforehand begun in the set value for the direct following of the purpose in setting &h11 after setting in &h10.

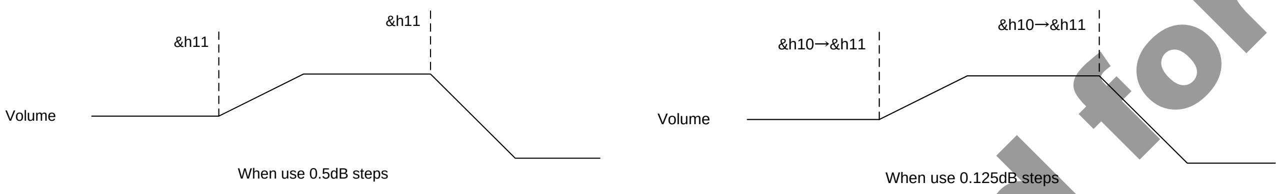

Figure 84

1-9. Balance

As for balance, it is possible to be attenuated at 1dB step width from volume setting value. The switch operation becomes a smooth transition. When the balance changes, smooth transition is done. Smooth transition duration becomes the same formula as the volume.

Setting of L/R balance

Default = 80h

Select Address	Explanation of operation
&h12 [7:0]	(see table below)

Command	Lch	Rch
00	0dB	−∞
01	0dB	−126dB
⋮	⋮	⋮
7E	0dB	−1dB
7F	0dB	0dB
80	0dB	0dB
81	−1dB	0dB
⋮	⋮	⋮
FE	−126dB	0dB
FF	−∞	0dB

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1-10. 2 band DRC

This DRC is used in order to prevent speaker protection and the clip output of a large audio signal.
In addition to two bands of DRC for low and high frequency, there is DRC for the whole frequency in the latter part. Non clip output is possible.
DRC for low frequency band and DRC for high frequency band can set up two threshold value levels. Moreover, it is possible to also change slope.

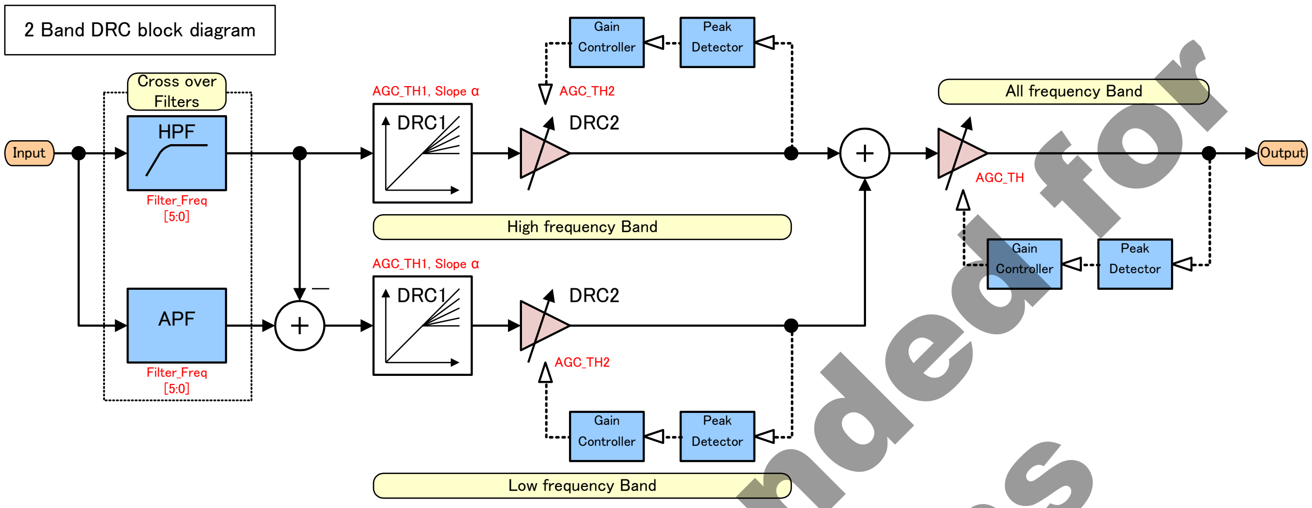

Figure 85

DRC transition figure

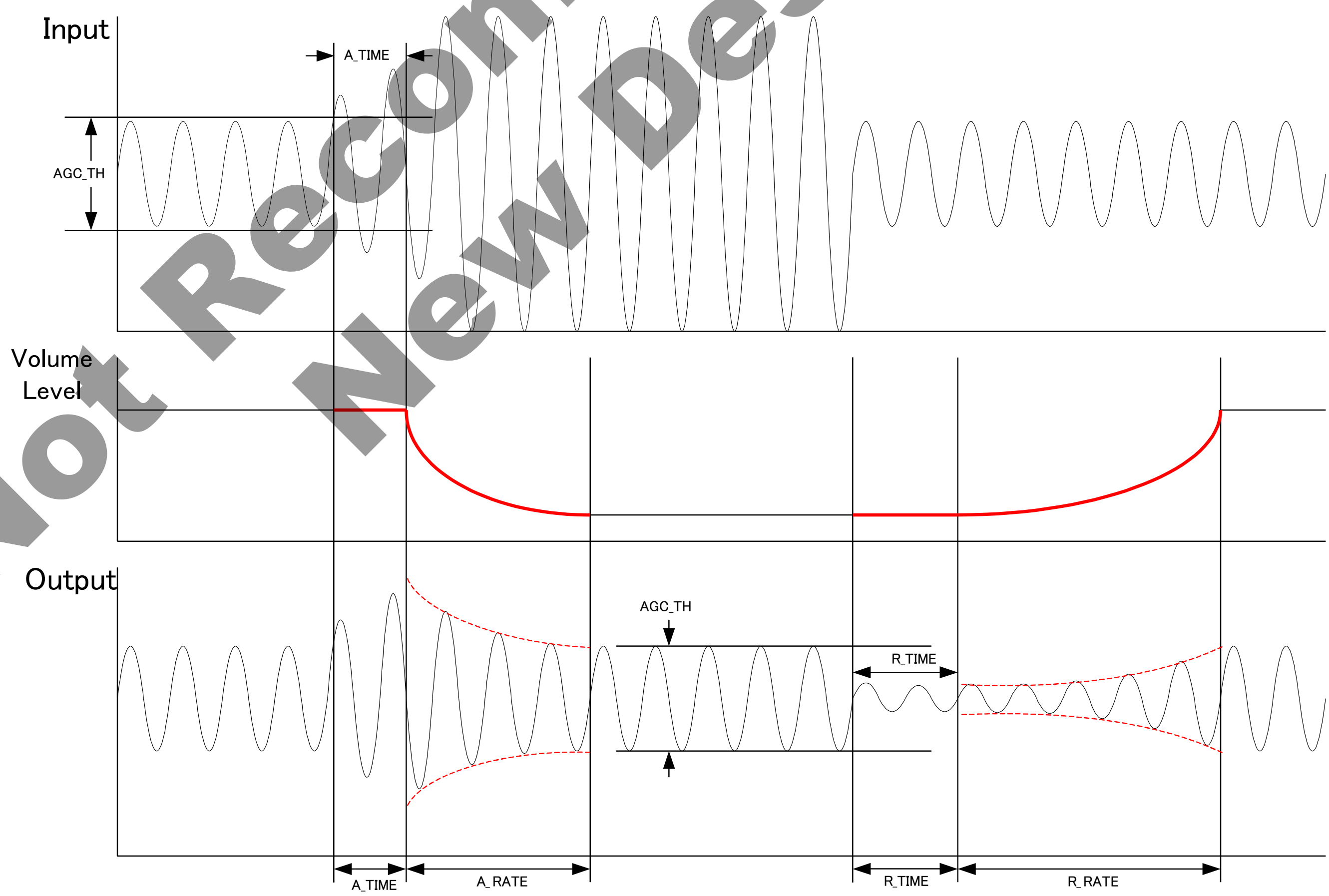

Figure 86

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DRC input-and-output gain characteristics

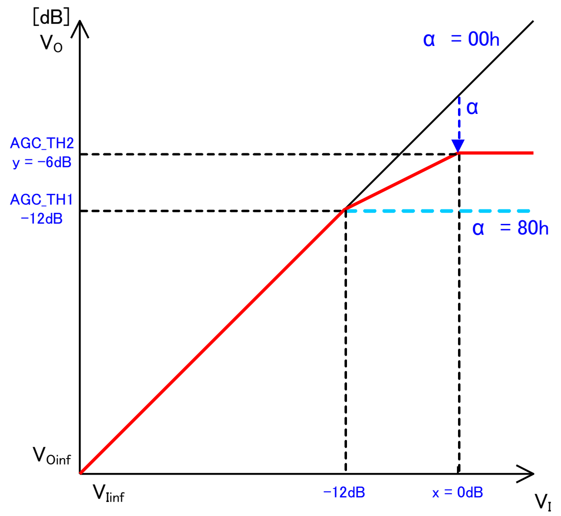

Figure 87

The formula which asks for Slope alpha is described below.

Alpha changes into 8bit Hex data of the complement of 2 the value calculated by calculation.

$$\alpha = \frac{10^{\frac{y}{20}} - 10^{\frac{x}{20}}}{10^{\frac{TH}{20}} - 10^{\frac{x}{20}}} \times 128$$

TH is AGC_TH1. x is input level. y is output level.

Ex) It asks for alpha at the time of AGC_TH1 = −12dB, x = 0dB y = −6dB

$$\alpha = \frac{10^{\frac{-6}{20}} - 10^{\frac{0}{20}}}{10^{\frac{-12}{20}} - 10^{\frac{0}{20}}} \times 128$$

$\alpha = 85.266 \rightarrow 55_H$

55_H calculated is set as &h25 or &h2A

Volume Curve

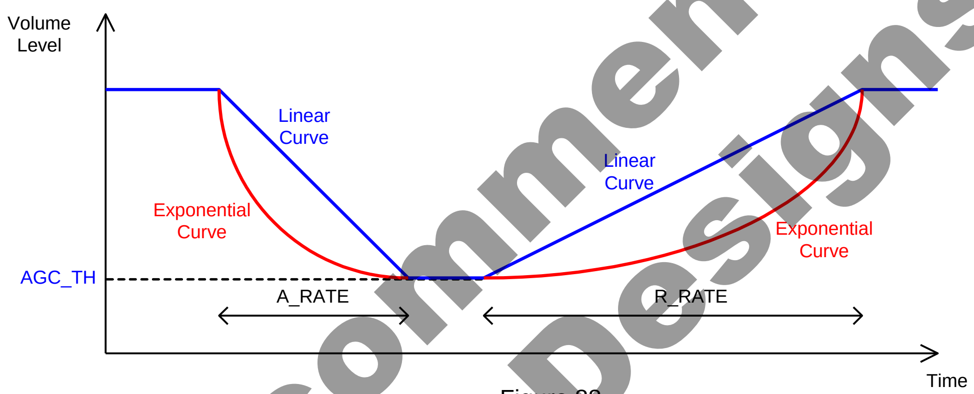

Figure 88

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ON/OFF setting of DRC for all frequency band.

OFF is through output.

Default = 1

Select Address	Value	Explanation of operation
&h20 [3]	0	Not use
	1	Use

ON/OFF setting of DRC1 for high frequency band. (DRC which can perform slope variable)

OFF is through output.

Default = 1

Select Address	Value	Explanation of operation
&h20 [7]	0	Not use
	1	Use

ON/OFF setting of DRC2 for high frequency band. (Compressor)

OFF is through output.

Default = 1

Select Address	Value	Explanation of operation
&h20 [6]	0	Not use
	1	Use

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ON/OFF setting of DRC1 for low frequency band. (DRC which can perform slope variable)

OFF is through output.

Default = 1

Select Address	Value	Explanation of operation
&h20 [5]	0	Not use
	1	Use

ON/OFF setting of DRC2 for low frequency band. (Compressor)

OFF is through output.

Default = 1

Select Address	Value	Explanation of operation
&h20 [4]	0	Not use
	1	Use

The volume curve at the time of an attack (A_RATE) is selected.

Default = 0

Select Address	Value	Explanation of operation
&h21[7]	0	Linear curve
	1	Exponential curve

The volume curve at the time of a release (R_RATE) is selected.

Default = 0

Select Address	Value	Explanation of operation
&h21 [6]	0	Linear curve
	1	Exponential curve

The choice of the DRC composition

It uses a standard in 2Band DRC but it is possible to use as 1Band DRC, too.

To make the composition of 1Band DRC, it chooses through setting in HPF and APF of the crossover filter.

【Procedure】

1) &h51 = 10h : Select HPF of the 2Band DRC.
2) &h52 = 07h : Select Filter through.
3) &h57 = 01h : It starts a transfer to the coefficient RAM.
4) &h51 = 11h : Select APF of 2Band DRC.
5) &h52 = 07h : Select Filter through.
6) &h57 = 01h : It starts a transfer to the coefficient RAM.

To set the crossover filter which divides the high frequency band and the low frequency band of 2Band DRC, therefore, it is referred to the chapter 1-7.

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Setting of DRC AGC_TH for all bands.
When using according to either of the DRC for the high area or the DRC for the low area bigger AGC_TH setting, the distortion in the crossover point can be suppressed.

Default = 40h

Select Address	Explanation of operation
&h38 [6:0]	

Command	Threshold
00	-32dB
⋮	⋮
3F	-0.5dB
40	0dB
41	+0.5dB
⋮	⋮
58	+12dB

Setting of DRC A_RATE for all bands. (The compression curve transition time in attack)

Default = 3h

Select Address	Explanation of operation
&h3A [6:4]	

Command	A_RATE time	Command	A_RATE time
0	1ms	4	5ms
1	2ms	5	10ms
2	3ms	6	20ms
3	4ms	7	40ms

Setting of DRC R_RATE for all bands. (The expansion curve transition time in release)

Default = Bh

Select Address	Explanation of operation
&h3A [3:0]	

Command	R_RATE time	Command	R_RATE time
0	0.125s	8	2s
1	0.1825s	9	2.5s
2	0.25s	A	3s
3	0.5s	B	4s
4	0.75s	C	5s
5	1s	D	6s
6	1.25s	E	7s
7	1.5s	F	8s

Setting of DRC A_TIME for all bands. (Setting of detection time for attack operation)

Default = 1h

Select Address	Explanation of operation
&h3B [7:4]	

Command	A_TIME time	Command	A_TIME time
0	0ms	8	6ms
1	0.5ms	9	7ms
2	1ms	A	8ms
3	1.5ms	B	9ms
4	2ms	C	10ms
5	3ms	D	20ms
6	4ms	E	30ms
7	5ms	F	40ms

Setting of DRC R_TIME for all bands. (Setting of detection time for release operation)

Default = 3h

Select Address	Explanation of operation
&h3B [2:0]	

Command	R_TIME time	Command	R_TIME time
0	5ms	4	100ms
1	10ms	5	200ms
2	25ms	6	300ms
3	50ms	7	400ms

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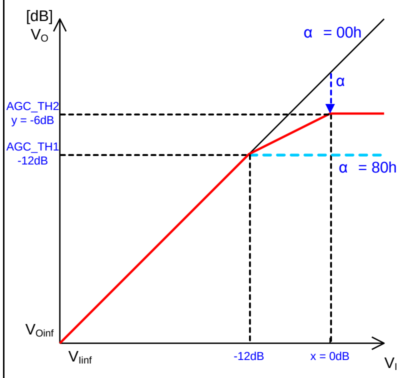
Slope (α) setting of DRC1 for high frequency band

Default = 80h

Select Address	Explanation of operation
&h29 [7:0]	(see figure and formula below)



The formula which asks for Slope alpha is described below.
Alpha changes into 8bit Hex data of the complement of 2 the value calculated by calculation.

$$\alpha = \frac{10^{\frac{y}{20}} - 10^{\frac{x}{20}}}{10^{\frac{TH}{20}} - 10^{\frac{x}{20}}} \times 128$$

TH is AGC_TH1. x is input level. y is output level.

Ex) It asks for alpha at the time of AGC_TH1 = -12dB, x = 0dB y = -6dB

$$\alpha = \frac{10^{\frac{-6}{20}} - 10^{\frac{0}{20}}}{10^{\frac{-12}{20}} - 10^{\frac{0}{20}}} \times 128$$

$$\alpha = 85.266 \rightarrow 55_H$$

55H calculated is set as &h61 or &h69

AGC_TH1 setting of DRC1 for high frequency band

Please set below to the setting value of AGC_TH2.

Default = 40h

Select Address	Explanation of operation
&h28 [6:0]	(see table below)

Command	Threshold
00	-32dB
⋮	⋮
3F	-0.5dB
40	0dB
41	+0.5dB
⋮	⋮
58	+12dB

AGC_TH2 setting of DRC2 for high frequency band

Default = 40h

Select Address	Explanation of operation
&h2C [6:0]	(see table below)

Command	Threshold
00	-32dB
⋮	⋮
3F	-0.5dB
40	0dB
41	+0.5dB
⋮	⋮
58	+12dB

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High frequency band A_RATE setting (It is the transition time of a compression curve at the time of an attack.)
DRC1 and DRC2 for high frequency band are individually setting.
Default = 3h

Select Address	Explanation of operation
DRC1 &h2A [6:4] DRC2 &h2E [6:4]	

Command	A_RATE time	Command	A_RATE time
0	1ms	4	5ms
1	2ms	5	10ms
2	3ms	6	20ms
3	4ms	7	40ms

High frequency band R_RATE setting (It is the transition time of an extension curve at the time of release.)
DRC1 and DRC2 for high frequency band are individually setting.
Default = Bh

Select Address	Explanation of operation
DRC1 &h2A [3:0] DRC2 &h2E [3:0]	

Command	R_RATE time	Command	R_RATE time
0	0.125s	8	2s
1	0.1825s	9	2.5s
2	0.25s	A	3s
3	0.5s	B	4s
4	0.75s	C	5s
5	1s	D	6s
6	1.25s	E	7s
7	1.5s	F	8s

A_TIME1 setting of DRC1 for high frequency band (Detection time setting of attack operation)
DRC1 and DRC2 for high frequency band are individually setting.
Default = 1h

Select Address	Explanation of operation
DRC1 &h2B [7:4] DRC2 &h2F [7:4]	

Command	A_TIME time	Command	A_TIME time
0	0ms	8	6ms
1	0.5ms	9	7ms
2	1ms	A	8ms
3	1.5ms	B	9ms
4	2ms	C	10ms
5	3ms	D	20ms
6	4ms	E	30ms
7	5ms	F	40ms

R_TIME setting of DRC for high frequency band (Detection time setting of release operation)
DRC1 and DRC2 for high frequency band are individually setting.
Default = 3h

Select Address	Explanation of operation
DRC1 &h2B [2:0] DRC2 &h2F [2:0]	

Command	R_TIME time	Command	R_TIME time
0	5ms	4	100ms
1	10ms	5	200ms
2	25ms	6	300ms
3	50ms	7	400ms

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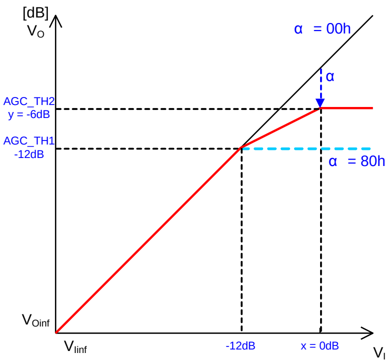
Slope (α) setting of DRC1 for low frequency band

Default = 80h

Select Address	Explanation of operation
&h31 [7:0]	(see below)



The formula which asks for Slope alpha is described below.
alpha changes into 8bit Hex data of the complement of 2 the value calculated by calculation.

$$\alpha = \frac{10^{\frac{y}{20}} - 10^{\frac{x}{20}}}{10^{\frac{TH}{20}} - 10^{\frac{x}{20}}} \times 128$$

TH is AGC_TH1. x is input level. y is output level.

Ex) It asks for alpha at the time of AGC_TH1 = −12dB, x = 0dB y = −6dB

$$\alpha = \frac{10^{\frac{-6}{20}} - 10^{\frac{0}{20}}}{10^{\frac{-12}{20}} - 10^{\frac{0}{20}}} \times 128$$

$\alpha = 85.266 \rightarrow 55_H$

55H calculated is set as &h61 or &h69

AGC_TH1 setting of DRC1 for low frequency band

Please set below to the setting value of AGC_TH2.

Default = 40h

Select Address	Explanation of operation
&h30 [6:0]	(see table below)

Command	Threshold
00	-32dB
⋮	⋮
3F	-0.5dB
40	0dB
41	+0.5dB
⋮	⋮
58	+12dB

AGC_TH2 setting of DRC2 for low frequency band

Default = 40h

Select Address	Explanation of operation
&h34 [6:0]	(see table below)

Command	Threshold
00	-32dB
⋮	⋮
3F	-0.5dB
40	0dB
41	+0.5dB
⋮	⋮
58	+12dB

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Low frequency band A_RATE setting (It is the transition time of a compression curve at the time of an attack.)
DRC1 and DRC2 for low frequency band are individually setting.
Default = 3h

Select Address	Explanation of operation
DRC1 &h32 [6:4] DRC2 &h36[6:4]	see table below

Command	A_RATE time	Command	A_RATE time
0	1ms	4	5ms
1	2ms	5	10ms
2	3ms	6	20ms
3	4ms	7	40ms

Low frequency band R_RATE setting (It is the transition time of an extension curve at the time of release.)
DRC1 and DRC2 for low frequency band are individually setting.
Default = Bh

Select Address	Explanation of operation
DRC1 &h32 [3:0] DRC2 &h36 [3:0]	see table below

Command	R_RATE time	Command	R_RATE time
0	0.125s	8	2s
1	0.1825s	9	2.5s
2	0.25s	A	3s
3	0.5s	B	4s
4	0.75s	C	5s
5	1s	D	6s
6	1.25s	E	7s
7	1.5s	F	8s

A_TIME1 setting of DRC1 for low frequency band (Detection time setting of attack operation)
DRC1 and DRC2 for low frequency band are individually setting.
Default = 1h

Select Address	Explanation of operation
DRC1 &h33 [7:4] DRC1 &h37 [7:4]	see table below

Command	A_TIME time	Command	A_TIME time
0	0ms	8	6ms
1	0.5ms	9	7ms
2	1ms	A	8ms
3	1.5ms	B	9ms
4	2ms	C	10ms
5	3ms	D	20ms
6	4ms	E	30ms
7	5ms	F	40ms

R_TIME setting of DRC for low frequency band (Detection time setting of release operation)
DRC1 and DRC2 for low frequency band are individually setting.
Default = 3h

Select Address	Explanation of operation
DRC1 &h33 [2:0] DRC2 &h37 [2:0]	see table below

Command	R_TIME time	Command	R_TIME time
0	5ms	4	100ms
1	10ms	5	200ms
2	25ms	6	300ms
3	50ms	7	400ms

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【Question】
What is the purpose of DRC for all frequency bands?

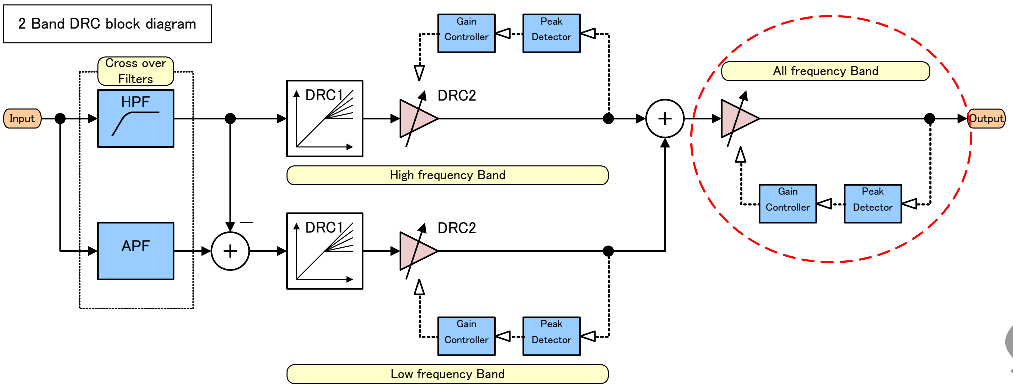

Figure 89

【Answer】
The purpose is for keeping constant the output level in the crossover point of low frequency band and high frequency band. A frequency characteristic figure with a cross over frequency 1.2kHz of DRC for low frequency band and DRC for high frequency band is shown below.

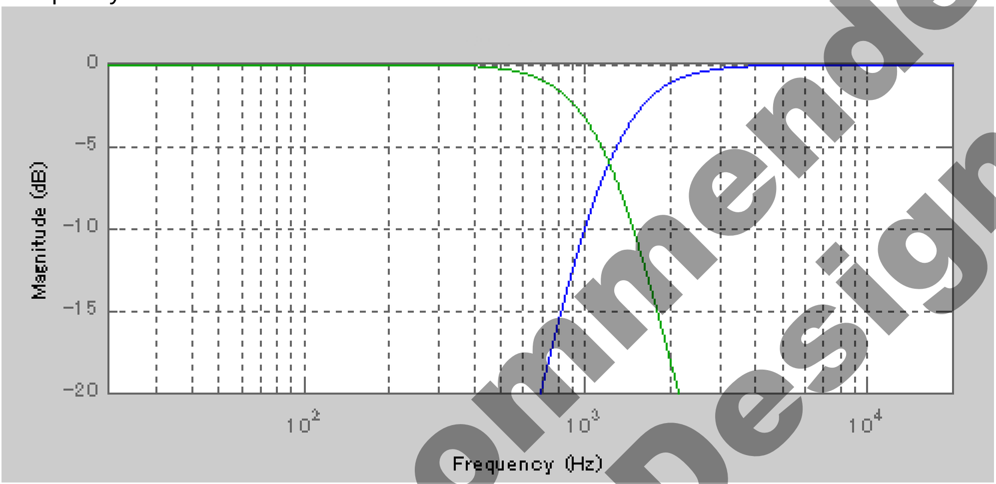

Figure 90

Next, the graph of AGC_TH=0dB, cross over frequency = 1.2kHz, and the frequency vs. output gain when not using all the DRC for all frequency bands is shown.

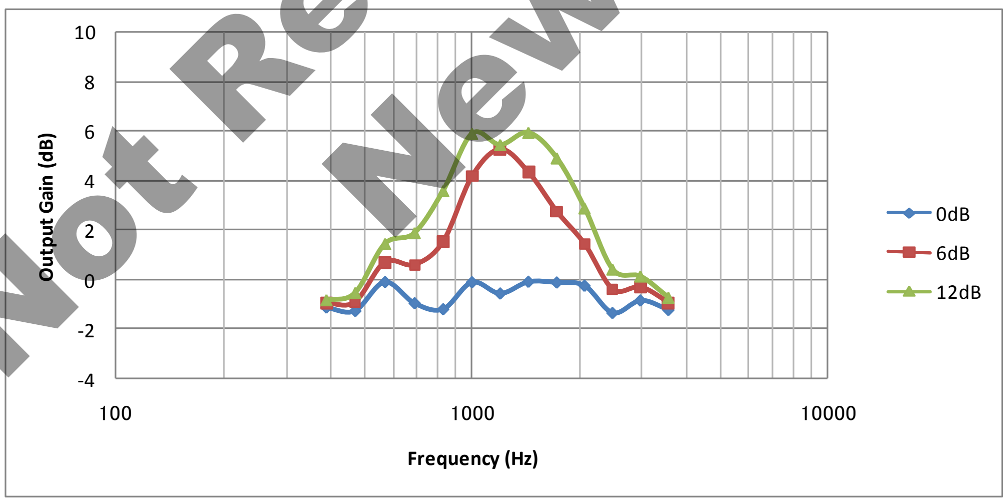

Figure 91

Input level 0dB is a flat. However, on an input level of +6dB or +12dB, it is over 0dB of a compression level near the cross over frequency.
In order to prevent this phenomenon, DRC for all frequency bands is used. However, when this phenomenon does not exist in a problem, I think that it is not necessary to use DRC for all frequency bands.
AGC_TH of DRC for all frequency band sets up AGC_TH2 value of the higher one, when AGC_TH2 differ by DRC for high frequency band, and DRC for low frequency band.

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【Question】
Recommendation value setting of 2 band DRC？

【Answer】
The recommendation value of 2 band DRC was examined to speaker protection using FPD TV.

- A_RATE : 4ms
- R_RATE : 2s or more
- A_TIME : 0.5ms
- R_TIME : 50ms or more

It is not uncomfortable to a music source to arrange all DRC (low frequency band, high frequency band, all frequency band) with the same value.

【Question]
When master volume is increased, why is it that only the sound of a high region becomes large?
【Answer】
It investigated about the cross over frequency and the relation of AGC_TH2 of DRC for high frequency band.
Its sound energy decreases, so that music data becomes high frequency. When a cross over frequency is set up highly, unless it lowers AGC_TH2 of DRC for high frequency band, when master volume is increased, the effect by limit cannot be heard.

The red line shows the Peak level.

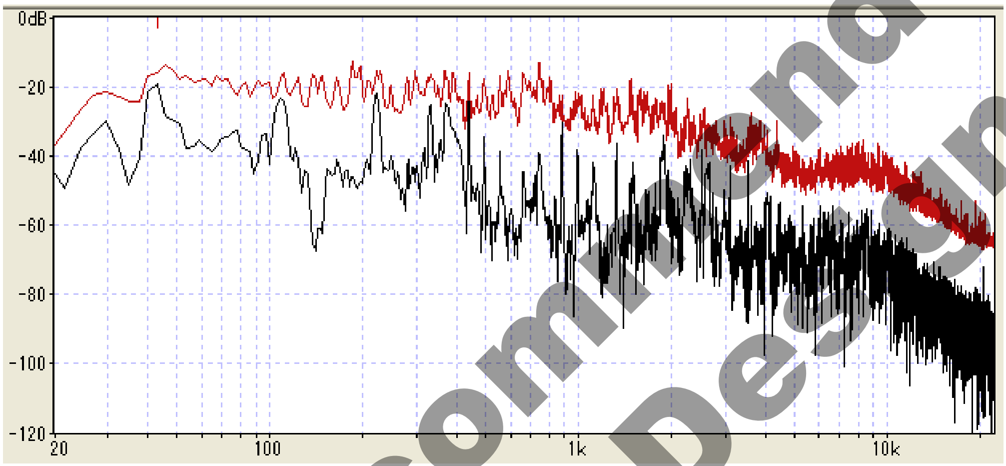

Figure 92

About the amount of adjustments of AGC_TH2 of DRC for high frequency band.

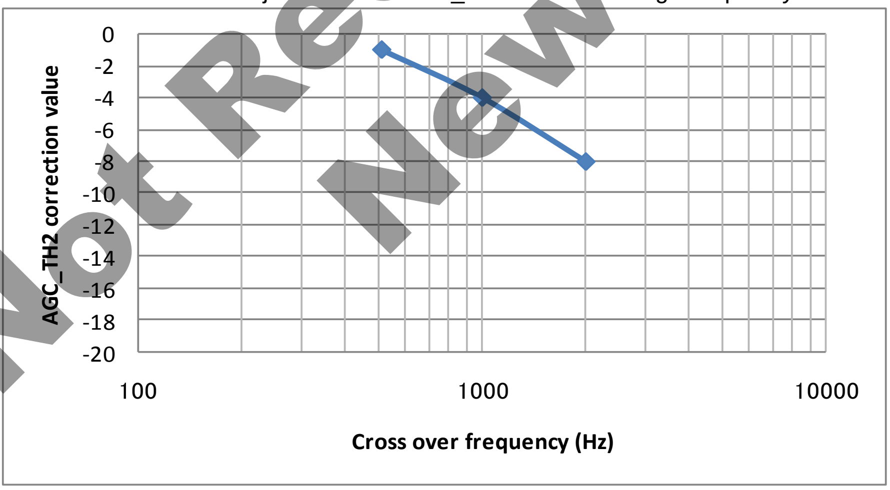

Figure 93

Please use as a standard of the adjustment value from AGC_TH2 value of DRC for low frequency band.
Moreover, the amount of adjustments decreases by setting up a cross over frequency lowness.

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1-11. Post-scalar

To prevent from an overflow in the DSP, it adjusts a gain with the scalar. An adjustable range can be set up at a 0.5dB step from +48dB to -79dB. Post-scalar does not have a smooth transition function.
(Same control of Lch/Rch.)

Default = 60h

Select Address	Explanation of operation	
&h13 [7:0]	Command	Gain
	00	+48dB
	01	+47.5dB
	⋮	⋮
	60	0dB
	61	-0.5dB
	62	-1dB
	⋮	⋮
	FE	-79dB
	FF	-∞

1-12. Fine Post-scalar

An adjustable range can be set up at a 0.1dB step from +0.7dB to –0.8dB. Fine Post-scalar does not have a smooth transition function.
(Independent control of Lch/Rch.)

Default=8h

Select Address	Explanation of operation			
Lch &h14 [7:4] Rch &h14 [3:0]	Command	Gain	Command	Gain
	0	-0.8dB	8	0dB
	1	-0.7dB	9	+0.1dB
	2	-0.6dB	A	+0.2dB
	3	-0.5dB	B	+0.3dB
	4	-0.4dB	C	+0.4dB
	5	-0.3dB	D	+0.5dB
	6	-0.2dB	E	+0.6dB
	7	-0.1dB	F	+0.7dB

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1-13. Hard Clipper

When measuring the rated output of the television, THD+N measures in 10%. It can be made to clip with any output amplitude by using a clipper function. For example, the rated output of 10W or 5W can be gained using the amplifier of 15W output.

Hard clip

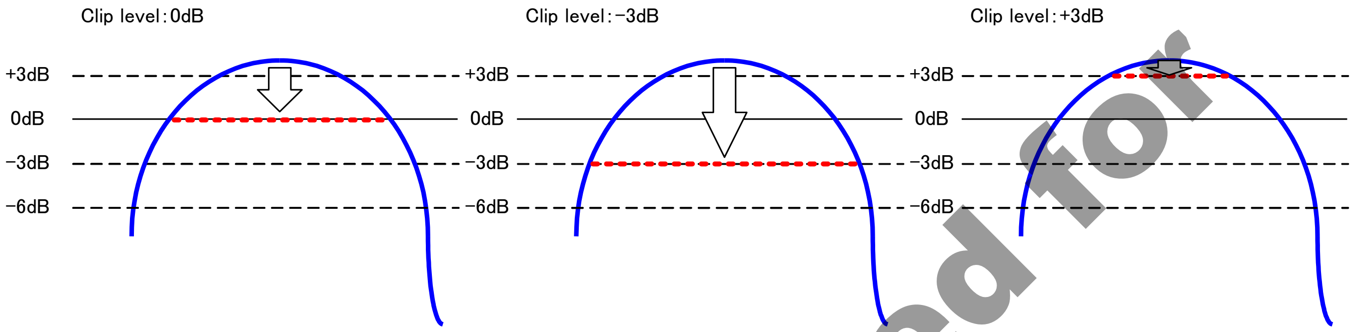

Figure 94

Clipper setting

Default = 1

Select Address	Value	Explanation of operation
&h1A [0]	0	Clipper function is not used.
	1	Hard clipper function is used.

Clip level selection

Default = E1h

Select Address	Explanation of operation
&h1B [7:0]	

Command	Gain
00	-22.5dB
⋮	⋮
E0	-0.1dB
E1	0dB
E2	+0.1dB
⋮	⋮
FF	+3dB

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1-14. DC cut HPF (Back)

DC offset element of the digital signal outputted from audio DSP is cut by this HPF.
The cutoff frequency fc of HPF uses the 1Hz filter, and the degree uses the first-order filter.

Default = 1

Select Address	Value	Explanation of operation
&h18 [0]	0	Not use
	1	Use

1-15. RAM clear

The data RAM of DSP and coefficient RAM are cleared.
40us or more is required until all the data is cleared.

Clear of the data RAM

Default = 1

Select Address	Value	Explanation of operation
&h01 [7]	0	Normal
	1	Clear operation

Clear of coefficient RAM

Default = 1

Select Address	Value	Explanation of operation
&h01 [6]	0	Normal
	1	Clear operation

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1-16. Audio Output Level Meter

It is possible to output the peak level of the PCM data inputted into a PWM processor.
A peak value can be read using the 2-wire command interface as 16 bit data of an absolute value.
The interval holding a peak value can be selected from six steps (50ms step) from 50ms to 300ms.
A peak hold result can be selected from L channel, R channel, and a monophonic channel {(Lch+Rch) /2}.

Audio Output Level Meter block diagram

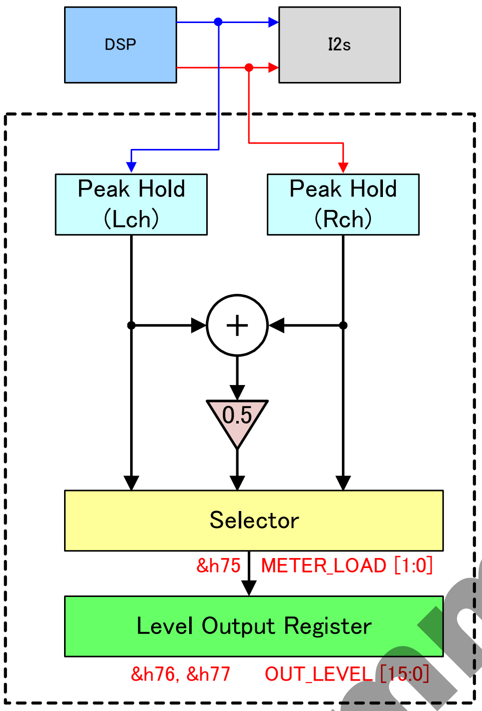

Figure 95

Setting of the peak level hold time interval of Audio Output Level Meter

Default = 00h

<table>
<tr><th>Select Address</th><th>Explanation of operation</th></tr>
<tr><td>&h74 [2:0]</td><td>
<table>
<tr><th>Command</th><th>Hold time</th></tr>
<tr><td>0</td><td>50ms</td></tr>
<tr><td>1</td><td>100ms</td></tr>
<tr><td>2</td><td>150ms</td></tr>
<tr><td>3</td><td>200ms</td></tr>
<tr><td>4</td><td>250ms</td></tr>
<tr><td>5</td><td>300ms</td></tr>
</table>
</td></tr>
</table>

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The signal of Audio Level Meter read-back is selected.
A value will be taken into a read-only register if a setting value is written in.
In order to update this register value, it is necessary to write in a setting value again.

Default = 0

Select Address	Value	Explanation of operation
&h75 [1:0]	0	The peak level of L channel
	1	The peak level of R channel
	2	The peak level of monophonic channel {(Lch+Rch) /2}

Read-back of Audio Output Level
&h76 (upper 8 bits) and a &h77 (lower 8 bits) commands are read for the maximum within the period appointed by the command &h74 using the 2-wire interface.

(Example)
When FFFFh is read, mean 1.0 (0dBFs).
When 8000h is read, mean 0.5 (-6dBFs).

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2. Setting and reading method of parametric equalizer

It explains a detailed sequence of the setting method and the reading method of the parametric equalizer separately for usage.

2-1 PEQ coefficient setting

The parametric equalizer consists of Bi-quad filter as follows. Each coeffiect of Bi-quad filter can be written directly. It is S2.21 format, and setting range is $-4 \leqq x < +4$.
Moreover, the coefficient address is shown in Table 1.

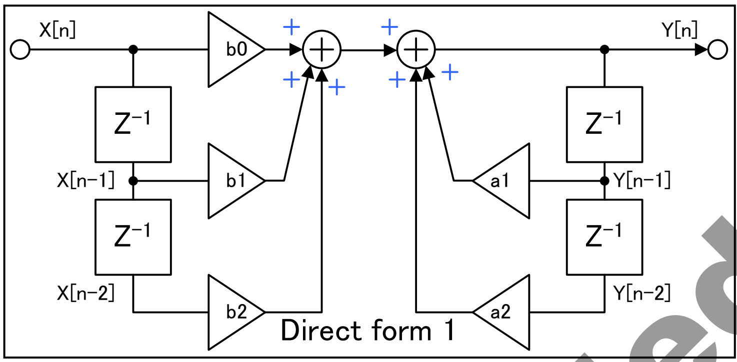

Figure 96

2-1-1 Writing sequence (It sets up in number order)

1. BANK1 to 4 is appointed. (&h60[1:0])
2. Address setting (&h61) (Note1)Table 1 is referred to.
3. 24bit coefficient Upper[23:16]bit setting (&h62[7:0])
4. 24bit coefficient Middle[15:8]bit setting (&h63[7:0])
5. 24bit coefficient Lower [7:0]bit setting (&h64[7:0])
6. The writing of coefficients are performed. (&h65[0] = 1) (Note2)

(Note2)After writing complete of coefficients is cleared automatically. It is not necessary to transmit h65[0] =L. Coefficient writing takes about 100μsec.100μsec should not change an address setup and several 24-bit setup after coefficient write-in execution.

(ex) When 0x3DEDE7 is written in BANK1, same L/Rch, 16band BQ1 b0

1. &h60 = 0*h (BANK1 is appointed.)
2. &h61 = 00h (16band BQ1 b0 is appointed)
3. &h62 = 3Dh (Upper[23:16] is setting)
4. &h63 = EDh (Middle[15:8] is setting)
5. &h64 = E7h (Lower[7:0] is setting)
6. &h65 = 01h (Coefficient transfer) (Note3)

(Note3)After writing complete of coefficients is cleared automatically.

7. 100μsec or more μsec wait

The writing of other coefficients is performed.

2-1-2 Read-back sequence (It sets up in number order)

1. BANK1 to 4 is appointed. (&h60[3:2])
2. Address setting (&h61) (Note4)Table 1 is referred to.
3. Setting of a read-back register address (&hD0)
4. Read-back of the 24bit coefficient Upper[23:16]bit (&h66[7:0])
5. Read-back of the 24bit coefficient Middle[15:8]bit (&h67[7:0])
6. Read-back of the 24bit coefficient Lower[7:0]bit (&h68[7:0])

2-1-3 When the coefficient of PEQ is set up directly and a soft transition is performed

1. Set PEQ coefficient to soft transition address whose address is 50-54.Please refer to Table 1.
   Since in the case of &h60[4]=1(Enable L/R independent setting) and &h53 [5:4] =0 a soft transition is carried out and it is set to LR simultaneous , please write a coefficient in both LR address.
   In the case of &h53[5:4]=1, coefficient is set to only Lch address.
   In the case of &h53[5:4]=2, coefficient is set to only Rch address.
2. Select PEQ channel that is performed soft transition by setting &h51[4:0] address.
3. &h58[0]=1h：Start soft transition (After the completion of soft transition this register is automatically cleared by 0 h)
4. Wait soft transition completion(about 24msec), or read command &h59 [0], and stand by until it is cleared by 0 h.

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Table 1. Specified coefficient

&h61[6:0]	Specified coefficient	&h61[6:0]	Specified coefficient	&h61[6:0]	Specified coefficient
00	16BandBQ1 b0	23	16BandBQ8 b0	46	16BandBQ15 b0
01	16BandBQ1 b1	24	16BandBQ8 b1	47	16BandBQ15 b1
02	16BandBQ1 b2	25	16BandBQ8 b2	48	16BandBQ15 b2
03	16BandBQ1 a1	26	16BandBQ8 a1	49	16BandBQ15 a1
04	16BandBQ1 a2	27	16BandBQ8 a2	4A	16BandBQ15 a2
05	16BandBQ2 b0	28	16BandBQ9 b0	4B	16BandBQ16 b0
06	16BandBQ2 b1	29	16BandBQ9 b1	4C	16BandBQ16 b1
07	16BandBQ2 b2	2A	16BandBQ9 b2	4D	16BandBQ16 b2
08	16BandBQ2 a1	2B	16BandBQ9 a1	4E	16BandBQ16 a1
09	16BandBQ2 a2	2C	16BandBQ9 a2	4F	16BandBQ16 a2
0A	16BandBQ3 b0	2D	16BandBQ10 b0	50	Smooth BQ b0
0B	16BandBQ3 b1	2E	16BandBQ10 b1	51	Smooth BQ b1
0C	16BandBQ3 b2	2F	16BandBQ10 b2	52	Smooth BQ b2
0D	16BandBQ3 a1	30	16BandBQ10 a1	53	Smooth BQ a1
0E	16BandBQ3 a2	31	16BandBQ10 a2	54	Smooth BQ a2
0F	16BandBQ4 b0	32	16BandBQ11 b0	55	DRC_HPF b0
10	16BandBQ4 b1	33	16BandBQ11 b1	56	DRC_HPF b1
11	16BandBQ4 b2	34	16BandBQ11 b2	57	DRC_HPF b2
12	16BandBQ4 a1	35	16BandBQ11 a1	58	DRC_HPF a1
13	16BandBQ4 a2	36	16BandBQ11 a2	59	DRC_HPF a2
14	16BandBQ5 b0	37	16BandBQ12 b0	5A	DRC_APF b0
15	16BandBQ5 b1	38	16BandBQ12 b1	5B	DRC_APF b1
16	16BandBQ5 b2	39	16BandBQ12 b2	5C	DRC_APF b2
17	16BandBQ5 a1	3A	16BandBQ12 a1	5D	DRC_APF a1
18	16BandBQ5 a2	3B	16BandBQ12 a2	5E	DRC_APF a2
19	16BandBQ6 b0	3C	16BandBQ13 b0		
1A	16BandBQ6 b1	3D	16BandBQ13 b1		
1B	16BandBQ6 b2	3E	16BandBQ13 b2		
1C	16BandBQ6 a1	3F	16BandBQ13 a1		
1D	16BandBQ6 a2	40	16BandBQ13 a2		
1E	16BandBQ7 b0	41	16BandBQ14 b0		
1F	16BandBQ7 b1	42	16BandBQ14 b1		
20	16BandBQ7 b2	43	16BandBQ14 b2		
21	16BandBQ7 a1	44	16BandBQ14 a1		
22	16BandBQ7 a2	45	16BandBQ14 a2		

When L/R independent, Lch:&h61[7]=0, Rch: &h61[7]=1
When L/R same, &h61[7] is not reflected.

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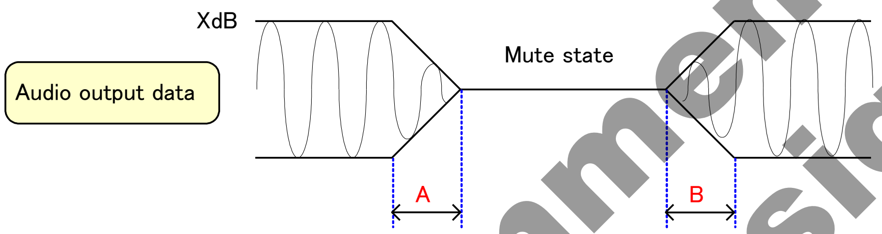
3. The mute function by a terminal

BM5481MUV has a mute function of audio DSP by a terminal.
It is possible to perform mute of the output from Audio DSP by setting a MUTEX terminal to "L."

Transition time setting at the time of mute is as follows.
Smooth transition mute time setting
The transition time when changing to a mute state is selected.
The soft transition time at the time of mute release is 10.7ms fixed.
Default = 3

Select Address	Value	Explanation of operation
&h15 [1:0]	0	10.7ms
	1	21.4ms
	2	42.7ms
	3	85.4ms

&h15[1:0] Mute time setting
It is only operated by mute terminal.



&h15[1:0] setting

Command	A	B
0	10.7ms	10.7ms
1	21.4ms	10.7ms
2	42.7ms	10.7ms
3	85.4ms	10.7ms

Figure 97

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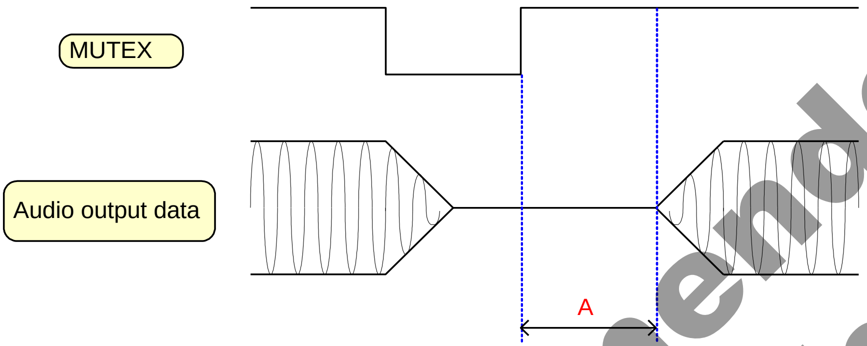
Smooth transition mute release time setting

Time after detecting mute release until it actually begins mute release operation is set up.

Default = 0

Select Address	Value	Explanation of operation
&h15 [5:4]	0	0ms
	1	100ms
	2	200ms
	3	300ms

Operation of mute delay &h15[5:4]



Command	A
0	0ms
1	100ms
2	200ms
3	300ms

Figure 98

【Question】

When mute release is performed, what happens during mute operation?
Moreover, when there is release delay time, what happens?

【Answer】

When mute release is performed during mute operation, mute release operation is started in an instant.
(When delay setting is 0) Return time at this time becomes shorter than mute release time (for example, 10ms).
Next, when there is setting of release delay time, a delay timer starts a count from the time of performing mute release, and mute release operation is started after delay time completing.
When mute release time setting is set to 10ms, it is designing so that a mute release curve may draw f curve.

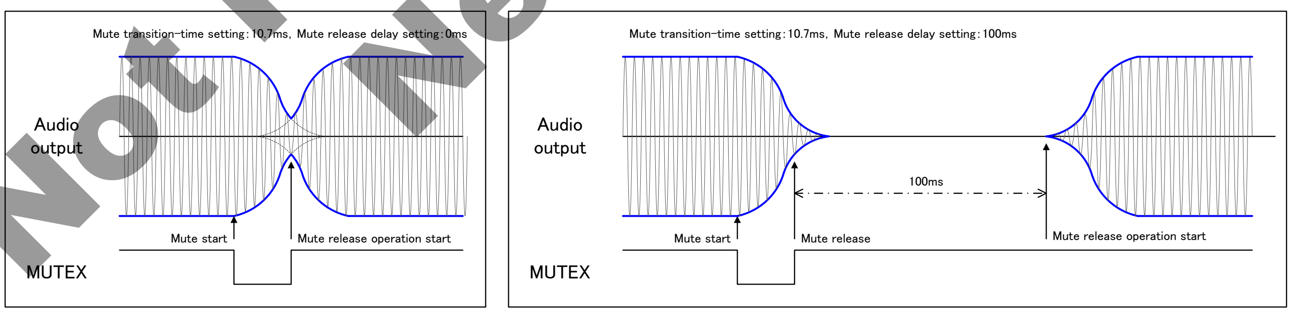


Figure 99

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4. Small signal input detection function

There is a function which detects the audio data input of a non-signal or a small signal. This function is used in order to reduce the standby power consumption of an audio set. Setting of a detection level and detection time can be performed.
If the signal below a setting detection level continues in both L channel and R channel, a small signal detection flag will become "H". A detection result can be read from command &h72 [2:0].
The point which acts as a monitor of the small signal becomes input data of audio DSP block.

Block diagram

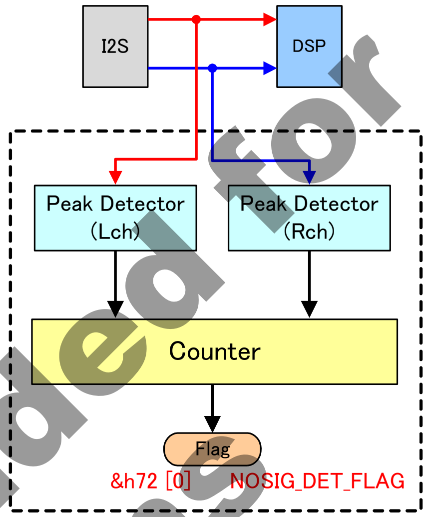

Figure 100

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Detection level setting

Default = 00h

Select Address	Explanation of operation
&h70 [4:0]	

Command	Level	Command	Level	Command	Level
00	-∞	08	-77dB	10	-69dB
01	-96dB	09	-76dB	11	-68dB
02	-92dB	0A	-75dB	12	-67dB
03	-88dB	0B	-74dB	13	-66dB
04	-84dB	0C	-73dB	14	-65dB
05	-80dB	0D	-72dB	15	-64dB
06	-79dB	0E	-71dB	16	-62dB
07	-78dB	0F	-70dB	17	-60dB

Detection time setting

Default = 0

Select Address	Value	Explanation of operation
&h71 [1:0]	0	42.7ms
	1	85.4ms
	2	170.7ms
	3	341.4ms

* Sampling frequency is value of Fs = 48kHz. In the case of Fs = 44.1kHz, it will be about 1.09 times the setting value.

Detection flag read-back (Read Only)

Select Address	Value	Explanation of operation
&h72 [0]	0	Un-detecting.
	1	Detecting

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5. LEVEL DRC

When the signal below a setting detection level and continues the setting time in both L channel and R channel, Mute function will be run. (Smooth transition mute)
Mute threshold level has hysteresis of 6dB. Small signal detect is run back channel mixer block.

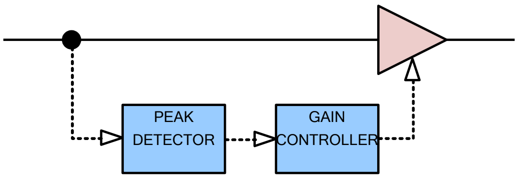

Figure 101

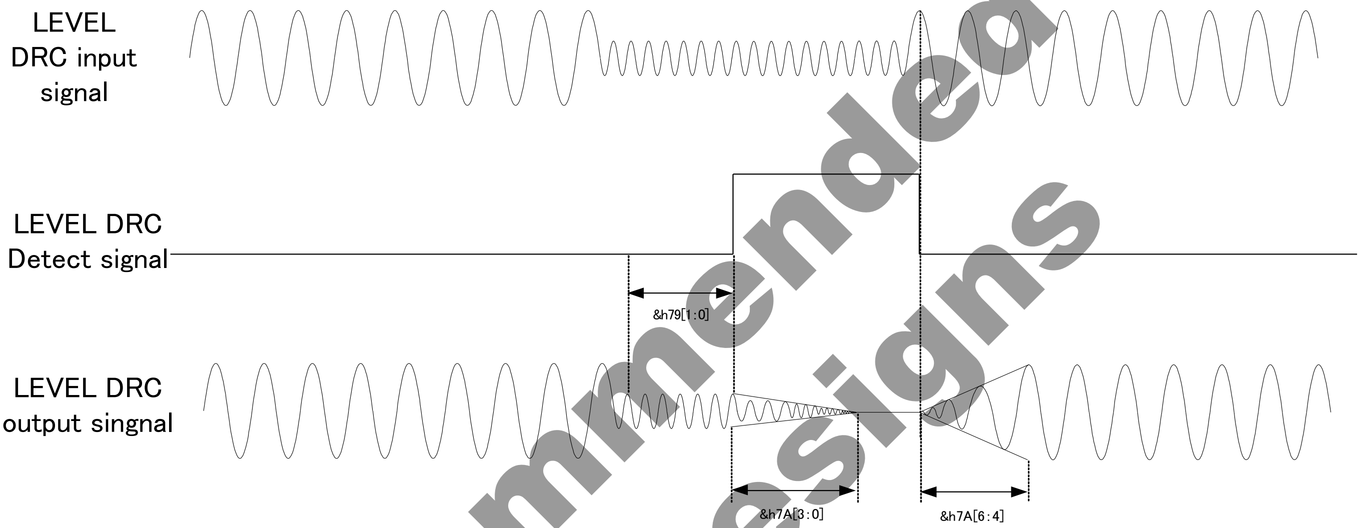

Figure 102

LEVEL DRC ON/OFF

Default = 1

Select Address	Value	Explanation of operation
&h78 [4]	0	OFF
	1	ON

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LEVEL DRC Detect level setting
Release level is +6dB of this setting.

Default=0h

Select Address	Explanation of operation
&h78 [3:0]	

Command	Level	Command	Level
0	-96dB	8	-48dB
1	-90dB	9	-42dB
2	-84dB	A	-36dB
3	-78dB	B	-30dB
4	-72dB	C	-
5	-66dB	D	-
6	-60dB	E	-
7	-54dB	F	-

Detect time setting

Default=3h

Select Address	Explanation of operation
&h79 [1:0]	

Command	Time
0	42.7ms
1	85.4ms
2	170.7ms
3	341.4ms

*Above is the value of FS=48kHz. FS=44.1kHz：Above value×1.09

LEVEL DRC smooth transition mute release time setting

Default=3h

Select Address	Explanation of operation
&h7A [6:4]	

Command	Time	Command	Time
0	1ms	4	5ms
1	2ms	5	10ms
2	3ms	6	20ms
3	4ms	7	40ms

*Above is the value of FS=48kHz. FS=44.1kHz：Above value×1.09

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LEVEL DRC smooth transition mute time setting

Default=Bh

Select Address	Explanation of operation
&h7A [3:0]	(see table below)

Command	Time	Command	Time
0	0.125S	8	2S
1	0.1825S	9	2.5S
2	0.25S	A	3S
3	0.5S	B	4S
4	0.75S	C	5S
5	1S	D	6S
6	1.25S	E	7S
7	1.5S	F	8S

*Above is the value of FS=48kHz. FS=44.1kHz：Above value×1.09

LEVEL DRC Detect signal read out(Read Only)

Select Address	Value	Explanation of operation
&h7B [0]	0	No detect
	1	Detect

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6. Clock stop detection and detection of BCLK frequency begin too low or too high or asynchronous state detection

6-1 Clock stop detection

BM5481MUV needs some clock source for generating proper clock to process Audio data.
By stopping these cock sources, these clocks to process Audio data also stop.
To prevent noise sounds, we need to detect BCLK or LRCLK stop condition.
As we detect stop flag that is to be valid, output is gone to mute state (mute instantly).

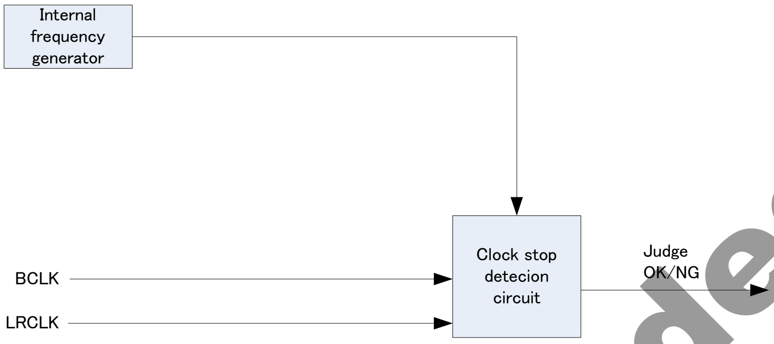

Figure 103

Each detect condition is set by below command. We can check detected result by reading back flag register.
These flags are cleared only by sending specified commands.

LRCLK stop detection time
Default = 2h(LRCK)

Select Address	Value	Operation
LRCLK &h07 [2:0]	0	10µs~20µs
	1	20µs~40µs
	2	50µs~100µs
	3	100µs~200µs
	4	200µs~400µs
	5	300µs~600µs
	6	400µs~800µs
	7	500µs~1000µs

※Detection time has the above-mentioned variation within the limits.

BCLK stop detection time
Default = 0h(BCK)

Select Address	Value	Operation
BCLK &h08 [6:4]	0	10µs~20µs
	1	20µs~40µs
	2	50µs~100µs
	3	100µs~200µs
	4	200µs~400µs
	5	300µs~600µs
	6	400µs~800µs
	7	500µs~1000µs

※Detection time has the above-mentioned variation within the limits.

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Stop detection flag read back register (Read Only)

Select Address	Value	Operation
&h09 [5]	0	Normal
	1	Detection of LRCLK stop flag
&h09 [4]	0	Normal
	1	Detection of BCLK stop flag

Stop detection flag clear register (Write Only)

Select Address	Operation
&h09 [1]	LRCLK stop detection flag is cleared by writing 1.
&h09 [0]	BCLK stop detection flag is cleared by writing 1.

※When using a clock shutdown auto return facility (Chapter 17), the above-mentioned flag is cleared automatically.

LRCLK stop flag valid or invalid selection
Default = 0h

Select Address	Value	Operation
&h07 [3]	0	Valid
	1	Invalid

BCLK stop flag valid or invalid selection
Default = 0h

Select Address	Value	Operation
&h08 [7]	0	Valid
	1	Invalid

6-2 Synchronous blank detection

As for synchronous blank detecting function, it detects as synchronous blank error when it counts between the rising edges of LRCK with internal clock (49.152MHz), and it shifts more than the definite value, and whether PLL is normally locked is judged.

Input sampling frequency	32kHz、44.1kHz、48kHz
Count value (Start of counting from 0)	1023

As for the detection result, reading from the register is possible. As a result of the judgment as synchronous blank once, it is not cleared until a clear command is transmitted even if the state of the clock returns normally. Moreover, the setting of the detection approval frequency is also possible, and if the error more than the predetermined number is detected, the flag (&h06[1]) becomes "1" by the command.

Synchronous blank flag reading register (Read Only)

Select Address	Value	Explanation of operation
&h06 [1]	0	Normal
	1	Synchronous blank detect

Synchronous blank flag clear register(Write Only)

Select Address	Explanation of operation
&h06 [0]	When "1" is written, the synchronous blank flag is cleared.

※When the clock stop automatic return function (Chapter 7) is used, these flags are cleared by the automatic operation.

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Synchronous blank count setting
Default = 2h

Select Address	Explanation of operation
&h06 [6:4]	1 or more is set. (It should be set from 1 to 7) If synchronous blank more than the set number of count is detected, & h06[1] becomes "1".

6-3 BCLK high or low speed detection

BCLK high or low speed detection function is that judge BCLK speed being too high or low by measuring by using internal clock(12MHz to 25MHz).
When using a BCLK speed detection, speed failure detection can be more correctly performed by making a command set reflect about an input sample rate.
When you validate sample rate setting, please be sure to set up the sample ring rate inputted with &h0c [1:0] command. A high speed and the low-speed detection flag can set up validity and the disabled, respectively, and if the validated flag is materialized, mute (mute instantly) will be carried out.

Valid or invalid frequency value setting up by &h0C[1:0] command.
Default = 0h

Select Address	Value	Operation
&h0A [3]	0	Valid
	1	Invalid

Setting of sampling rate
Default = 0h

Select Address	Value	Operation
&h0C [1:0]	0	48kHz
	1	44.1kHz
	2	32kHz

The constraints of a high speed or a low-speed condition
Default = 0h

Select Address	Value	Operation
&h0A [2]	0	±10%
	1	±20%

We can check detection result by reading back.
The result judged that is once unusual is not cleared until it transmits a clear command, even if the condition of a clock returns to normal. We can set up
We can set up the constraints of the count of formation, and it does not set a flag until it detects it by count continuation.

BCLK high speed flag(Read Only)

Select Address	Value	Operation
&h0A [1]	0	Normal
	1	High speed detection flag

BCLK low speed flag(Read Only)

Select Address	Value	Operation
&h0B [1]	0	Normal
	1	Low speed detection flag

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High speed detection clears register(Write Only)

Select Address	Operation
&h0A [0]	If “1” writes in, a high speed detection flag will be cleared.

※When using a clock shutdown auto return facility (Chapter 7), the above-mentioned flag is cleared automatically.

Low speed detection clear register(Write Only)

Select Address	Operation
&h0B [0]	If “1” writes in, a high speed detection flag will be cleared.

※When using a clock shutdown auto return facility (Chapter 7), the above-mentioned flag is cleared automatically.

A constraint of the count of judging with high speed flag detection
Default = 2h

Select Address	Operation
&h0A [6:4]	Please set up one or more. (1-7 are set up) A will become "&h0A[1]=1" if the BCLK high speed condition more than the count of setting up is detected continuously.

A constraint of the count of judging with low speed flag detection
Default = 2h

Select Address	Operation
&h0B [6:4]	Please set up one or more. (1-7 are set up) A will become "&h0B[1]=1" if the BCLK low speed condition more than the count of setting up is detected continuously.

High speed detection flag valid or invalid
Default = 0h

Select Address	Value	Operation
&h0A [7]	0	Valid
	1	Invalid

Low speed detection flag valid or invalid
Default = 0h

Select Address	Value	Operation
&h0B [7]	0	Valid
	1	Invalid

The frequency range of BCLK by which high speed detection or low speed detection is carried out becomes below.

Setting1	Setting2	Low speed	High speed
10%(&h0A[2]=0)	48kHz(&h0C[1:0]=0)	Under 20.0k to 41.3kHz	Over 55.6k to 111.4kHz
	44.1kHz(&h0C[1:0]=1)	Under 18.9k to 38.0kHz	Over 51.1k to 102.4kHz
	32kHz(&h0C[1:0]=2)	Under 13.7k to 27.6kHz	Over 37.1k to 74.3kHz
20%(&h0A[2]=1)	48kHz(&h0C[1:0]=0)	Under 19.2k to 38.4kHz	Over 62.4k to 128.4kHz
	44.1kHz(&h0C[1:0]=1)	Under 17,6k to 35.3kHz	Over 57.3k to 114.7kHz
	32kHz(&h0C[1:0]=2)	Under 12.8k to 25.6kHz	Over 41.6k to 83.2kHz

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7. Auto recovery from clock error function

Detection flag and a BCLK high speed, and low speed detection flag formation, it will be in a mute condition (mute instantly) about an output.
In that case, if the clock error auto return facility is enabled, when it returns to a normal input, a mute condition will be canceled automatically.
When the clock error auto return facility is repealed, it is necessary to control a series of operations called a mute-on and flag clear command transmission, an internal-RAM-data clear, and mute release from an external microcomputer.
Since it is invalid immediately after a wake-up, &h0D[6] =1 is set up before mute release, and it recommends validating.

Valid or invalid auto recover from clock error
Default = 0h

Select Address	Value	Operation
&h0D [6]	0	Invalid
	1	Valid

Each error flag can be read from the following addresses. When 1 is read from a read address, the error flag stands. Moreover, a flag is not cleared until it writes 0 in the target address, even if error status will be canceled, once a flag leaves.

Error flag read register

Select Address	Operation
&h0E [6]	Asynchronous flag
&h0E [4]	LRCLK stop flag
&h0E [3]	BCLK stop flag
&h0E [2]	BCLK high speed detection flag
&h0E [1]	BCLK low speed detection flag

8. The wake-up Procedure of power-up

It recommends starting power-up in the following Procedures.

1. Power up
○ Wait over 10msec
2. Release reset(RSTX=H)
3. &h0C[1:0]=*h : Sampling rate(Please set up 0h in the case of 48kHz, set up 1h in the case of 44.1kHz and 2h in 32kHz.)
○ Please input BCLK and LRCLK
4. &hE9=10h : changing clock to normal state
○ Wait over 5msec
5. &h0x01=00h : Set RAM clear OFF
6. &h0D[6]=1h : Valid auto recover from clock error
7. &h0E[7:1]=0h : Clear error flag
8. &h92[4:0]=11h : PWM setting1
9. &h93[4:0]=1Ch : PWM setting2
10. &h94[4:0]=15h : PWM setting3
11. &h95[4:0]=04h : PWM setting4
12. Please set up DSP function such as volume, PEQ, DRC, and Scalar etc.
13. MUTEX=H : Release mute

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9. The operating procedure in a status with an unstable clock

In the segment where the input of I2S signal of BCLK, LRCLK, and SDATA may become unstable, please set to MUTEX=L and carry out mute.

1.MUTEX=L

○ After stabilizing I2S input, it is 20 ms or more WAIT.

2.MUTEX=H

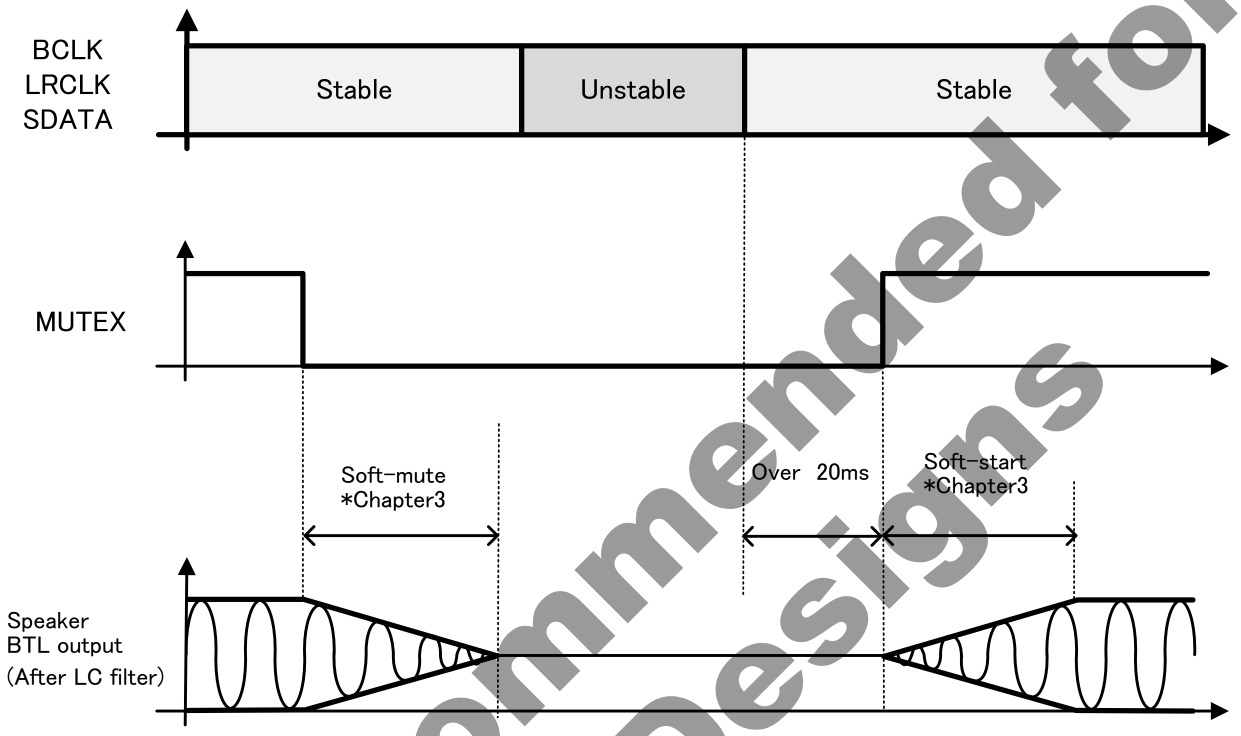

Figure 104

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Functional descriptions of Audio amplifier Block

The conventional line amplifier composition is occupied to Figure 59. In this composition, the signal is output by using the middle point bias circuit based on the middle point bias. Therefore, VDD Voltage limits the maximum output range of the line amplifier.

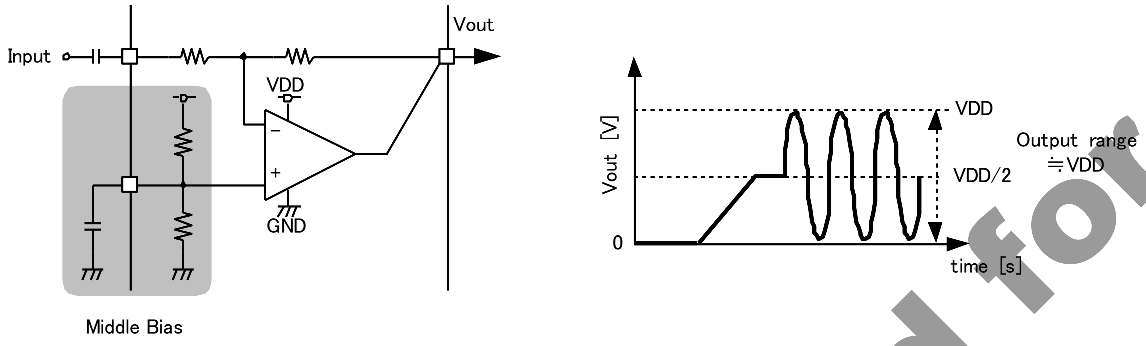

Figure 105. The conventional line amplifier composition

The composition of this IC is occupied to Figure 60. In this composition, the signal is output by using a negative voltage based on the ground level. Therefore, the amplifier can output between from –VDD to VDD. And it is possible to drive 2Vrms(5.65Vp-p) with single supply voltage 3.3V.

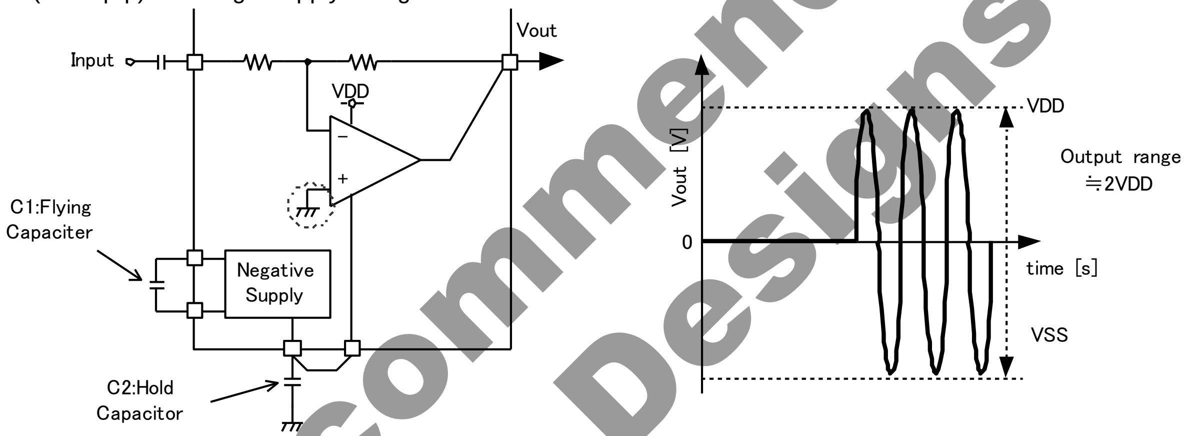

Figure 106. The composition of this IC

[CHARGE PUMP / CHARGE PUMP CONTROL]

The negative power supply circuit is composed of the regulated charge-pump. This circuit outputs the negative voltage (CPVSS) from power-supply voltage (SVDD).

・The flying capacitor and the hold capacitor
The flying capacitor (C1) and the hold capacitor (C2) greatly influence the characteristic of the charge pump. Therefore, please connect the capacitor with an excellent temperature characteristic and voltage characteristic of 1.0uF(and low ESR) as much as possible near IC.

・Over current Protection
This charge pump has the over current protection function. If the terminal of charge pump(CP, CN, CPVSS) is the stage of illegal operation(short ground etc.), this function shutdown IC, and protect by the damage.

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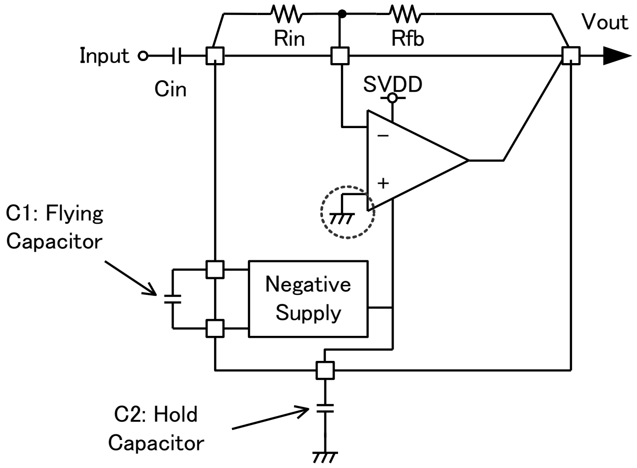
[Audio amplifier]

The Audio amplifier is driven by power-supply voltage (SVDD) and negative voltage (CPVSS) based on ground (SGND). Therefore, the amplifier can output 2Vrms for RL=10kohm with the single supply voltage 3.3V. And it can change the path gain by external resistors (Rin and Rfb).



Rin	Rfb	GAIN
10kΩ	10kΩ	-1.0V/V
10kΩ	15kΩ	-1.5 V/V
10kΩ	20kΩ	-2.0 V/V
4.7kΩ	47kΩ	-10.0 V/V

Figure 107

・GND of loads
Please layout GND line of loads independently not to have common impedance with GND of signals. It makes distortion and crosstalk worse.

・Power control
L channel and R channel of the line amplifier can be dependently controlled by SDB logic. When the SVSS voltage setup wait (t_{SON}=400us), the line amplifier does not operate to protect from illegal operation. And in addition, the over current protection circuit is built in. The amplifier is shutdown when the over current occurs because of the output short-circuit etc., and IC is protected from being destroyed.

Control of the Audio amplifier

SDB	L channel	R channel
L	Power down	Power down
H	Power on	Power on

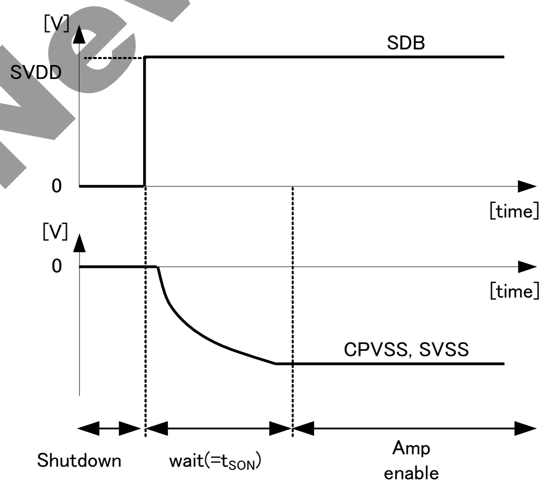


Figure 108. The area of audio amplifier can operate

SVSS connect with CPVSS in IC. But, please connect SVSS with CPVSS on the application board.

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・Input coupling capacitor
Input DC level is 0V(SGND). The input coupling capacitor is necessary for the connection with the signal source device. The signal decrease happens in the low frequency because of composing the high-pass filter by this input coupling capacitor and the input impedance.
The input impedance is Rin (external resistor). The cutoff frequency of this high-pass filter becomes the following formula.

$$f_c = \frac{1}{2\pi R_{in} C_{in}} \qquad (2)$$

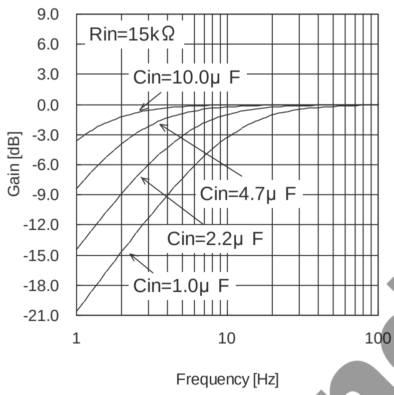

Figure 109. Frequency response by the input coupling capacitor(Reference data : at Rin=15kΩ)

And, the degradation of THD+N happens because of the input coupling capacitor. Therefore, please consider these about the selection of parts.

・State of terminal when power down
The state of the terminal changes by the power control of the audio amplifier. The time constant can be reduced when the input coupling capacitor is charged.
The input voltage changes while charging up the input coupling capacitor. Therefore, do not operate the audio amplifier while charging.

This charge time constant becomes the following formula (3) by using the input coupling capacitor and the input impedance. And the calculation value of the convergence to the wait time is indicated in Figure 63.

$$\tau = R_{in} C_{in} \qquad (3)$$

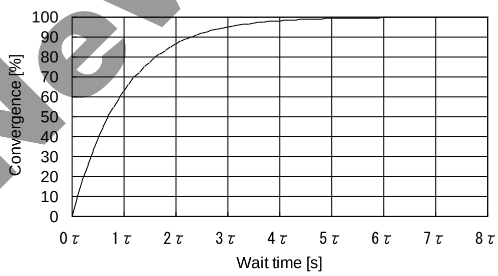

Figure 110. Wait time and convergence (Reference)

[UVLO / SHUTDOWN CONTROL]

This IC has low voltage protection function (UVLO : Under Voltage Lock Out). And protect from the illegal operation of IC by a low power supply voltage.
The detection voltage is 2.4V (TYP), so it does not influence 3.3V of recommended operation voltage. UVLO controls the whole of IC, and does both the negative power supply charge pump and the headphone amplifier in power down.

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Audio amplifier block timing chart

(Usually Operation)

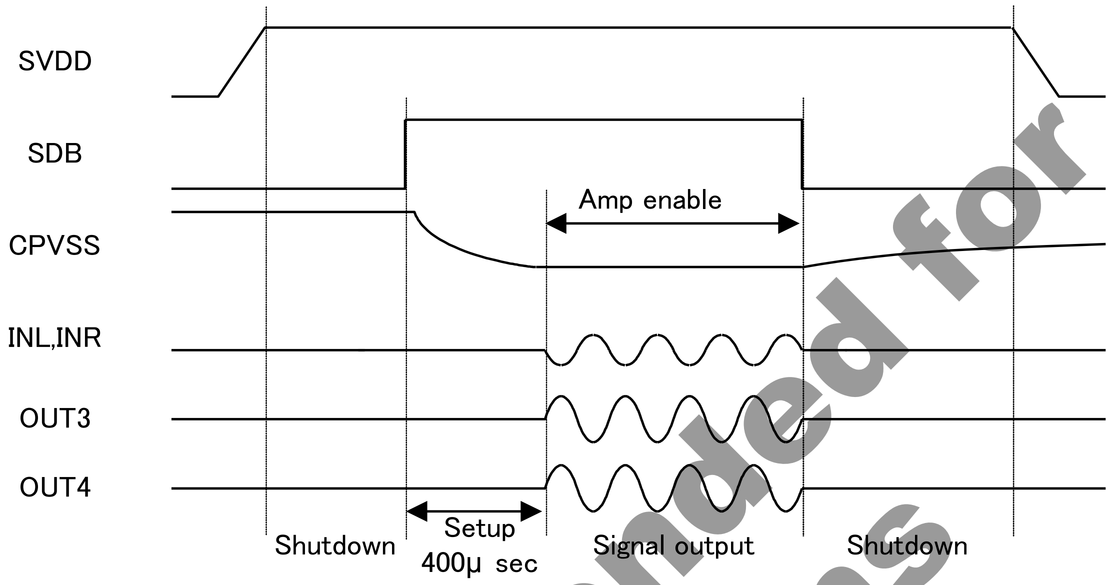

Figure 111. Usually Operation

(UVLO Operation)

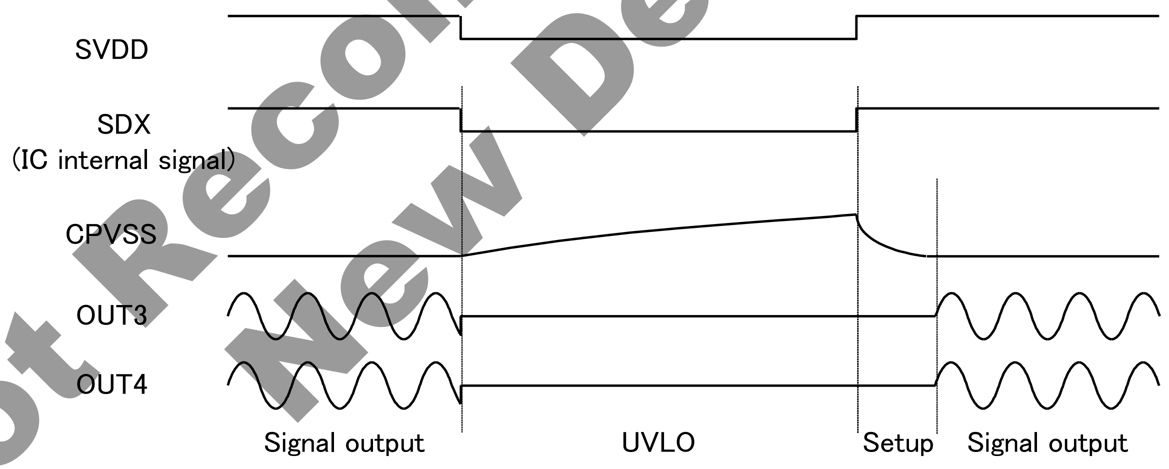

Figure 112. UVLO Operation

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Application Circuit Example (Stereo BTL output, RL1=8Ω)

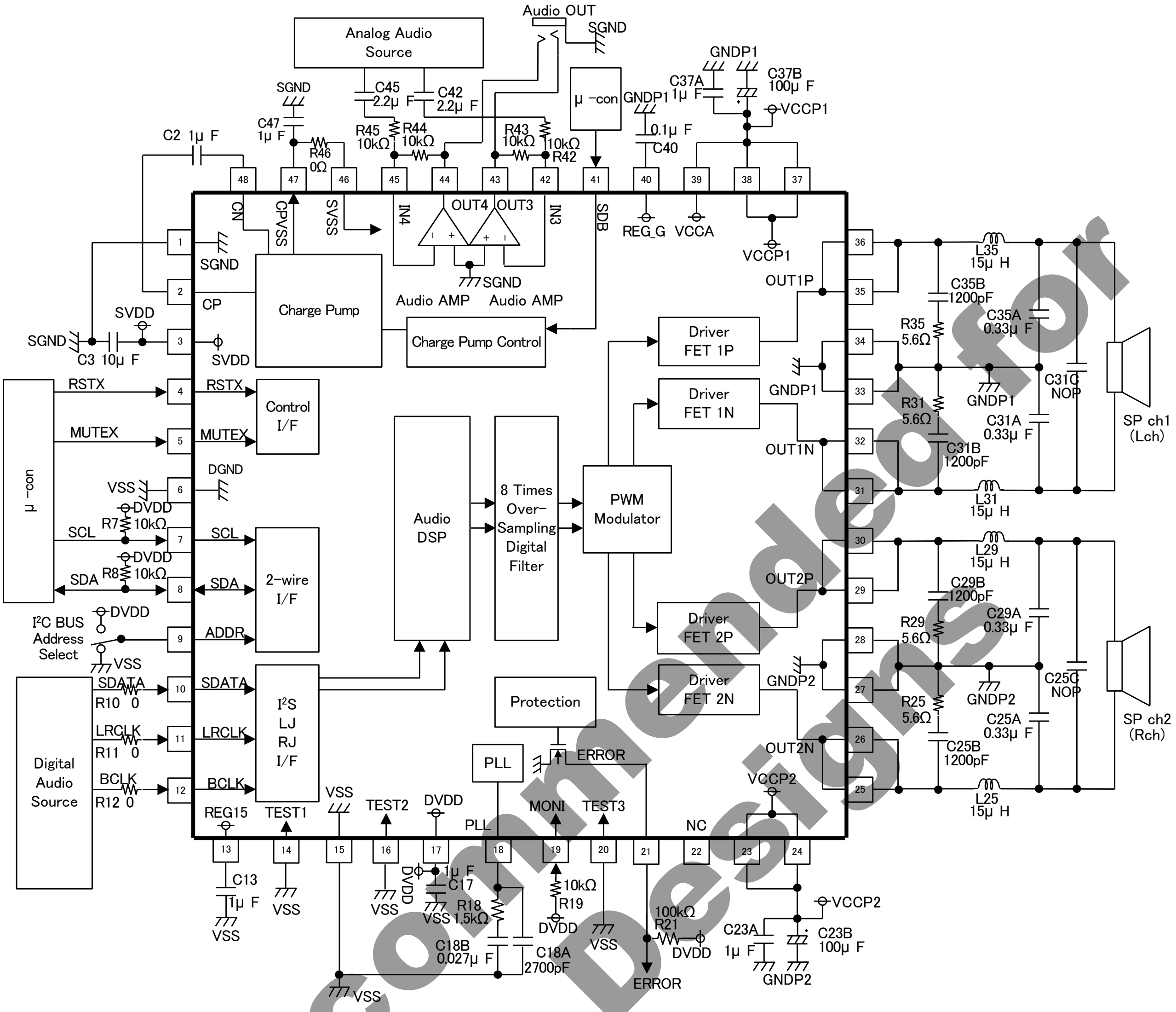

Figure 113

BOM list(Stereo BTL output, R_{L1}=8Ω)

Parts	Parts No.	Value	Company	Product No.	Rated Voltage	Tolerance	Size
Inductor	L25, L29, L31, L35	15uH	TOKO	B1047AS-150M	–	(±20%)	7.6mm×7.6mm
Resister	R25, R29 R31, R35	5.6Ω	ROHM	MCR03EZPJ5R6	1/10W	J(±5%)	1.6mm×0.8mm
	R18	1.5kΩ		MCR01MZPF1501	1/16W	F(±1%)	1.0mm×0.5mm
	R7, R8, R19, R42, R43 R44, R45	10kΩ		MCR01MZPJ1002	1/16W	J(±5%)	1.0mm×0.5mm
	R46	0Ω		MCR03EZPJ000	1/10W	J(±5%)	1.6mm×0.8mm
	R21	100kΩ		MCR01MZPJ1003	1/16W	J(±5%)	1.0mm×0.5mm
Capacitor	C25B, C29B C31B, C35B	1200pF	MURATA	GRM188B11H122KA01	50V	B(±10%)	1.6mm×0.8mm
	C18A	2700pF		GRM033B10J272KA01	6.3V	B(±10%)	0.6mm×0.3mm
	C18B	0.027uF		GRM033B10J273KE01	6.3V	B(±10%)	0.6mm×0.3mm
	C25A, C29A, C31A, C35A,	0.33uF		GRM219B31H34KA87	50V	B(±10%)	2.0mm×1.25mm
	C23A, C37A ※	1uF		GRM21BB31H105KA12	50V	B(±10%)	2.0mm×1.25mm
	C42, C45	2.2uF		GRM185B31C225KE43	16V	B(±10%)	1.6mm×0.8mm
	C47, C2	1uF		GRM185B31C105KE43	16V	B(±10%)	1.6mm×0.8mm
	C13, C17	1uF		GRM185B31A105KE43	10V	B(±10%)	1.6mm×0.8mm
	C3	10uF		GRM21BB31C106KE15	16V	B(±10%)	2.0mm×1.25mm
	C40	0.1uF		GRM188B11A104KA92D	10V	B(±10%)	1.6mm×0.8mm
	C23B, C37B	100uF	PANASONIC	ECA1VMH101	35V	±20%	φ8mm×11.5mm

※Please put the C23A and C37A near the VCCP1 and VCCP2 pins on the board.

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Application Circuit Example (Monaural BTL output, RL1=8Ω)

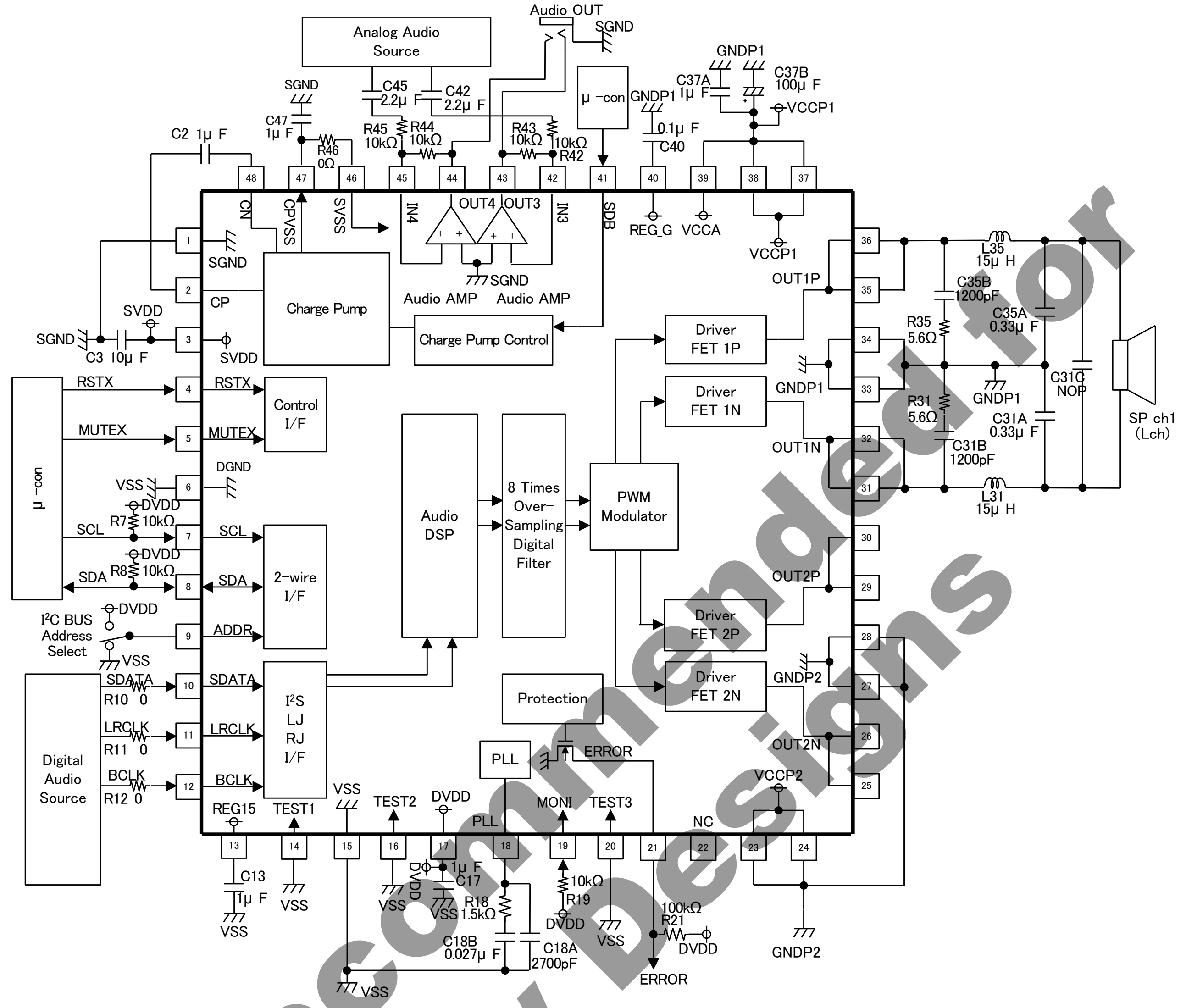

Figure 114

BOM list(Monaural BTL output, R_{L1}=8Ω)

Parts	Parts No.	Value	Company	Product No.	Rated Voltage	Tolerance	Size
Inductor	L31, L35	15uH	TOKO	B1047AS-150M	–	(±20%)	7.6mm×7.6mm
Resister	R31, R35	5.6Ω	ROHM	MCR03EZPJ5R6	1/10W	J(±5%)	1.6mm× 0.8mm
	R18	1.5kΩ		MCR01MZPF1501	1/16W	F(±1%)	1.0mm×0.5mm
	R7, R8, R19, R42, R43 R44, R45	10kΩ		MCR01MZPJ1002	1/16W	J(±5%)	1.0mm×0.5mm
	R46	0Ω		MCR03EZPJ000	1/10W	J(±5%)	1.6mm×0.8mm
	R21	100kΩ		MCR01MZPJ1003	1/16W	J(±5%)	1.0mm×0.5mm
Capacitor	C31B, C35B	1200pF	MURATA	GRM188B11H122KA01	50V	B(±10%)	1.6mm×0.8mm
	C18A	2700pF		GRM033B10J272KA01	6.3V	B(±10%)	0.6mm×0.3mm
	C18B	0.027uF		GRM033B10J273KE01	6.3V	B(±10%)	0.6mm×0.3mm
	C31A, C35A,	0.33uF		GRM219B31H34KA87	50V	B(±10%)	2.0mm×1.25mm
	C37A ※	1uF		GRM21BB31H105KA12	50V	B(±10%)	2.0mm×1.25mm
	C42, C45	2.2uF		GRM185B31C225KE43	16V	B(±10%)	1.6mm×0.8mm
	C47, C2	1uF		GRM185B31C105KE43	16V	B(±10%)	1.6mm×0.8mm
	C13, C17	1uF		GRM185B31A105KE43	10V	B(±10%)	1.6mm×0.8mm
	C3	10uF		GRM21BB31C106KE15	16V	B(±10%)	2.0mm×1.25mm
	C40	0.1uF		GRM188B11A104KA92D	10V	B(±10%)	1.6mm×0.8mm
	C37B	100uF	PANASONIC	ECA1VMH101	35V	±20%	φ8mm×11.5mm

※Please put the C37A near the VCCP1 pins on the board.

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Selection of Components Externally Connected

1) Output LC Filter Circuit

An output filter is required to eliminate radio-frequency components exceeding the audio-frequency region supplied to a load (speaker). Because this IC uses sampling clock frequencies from 256kHz(fs=32kHz) to 384kHz(fs=48kHz) in the output PWM signals, the high-frequency components must be appropriately removed.

This section takes an example of an LC type LPF shown below, in which coil L and capacitor C compose a differential filter with an attenuation property of -12dB/oct. A large part of switching currents flow to capacitor C, and only a small part of the currents flow to speaker R_{L1}. This filter reduces unwanted emission this way. In addition, coil L and capacitor Cg composes a filter against in-phase components, reducing unwanted emission further.

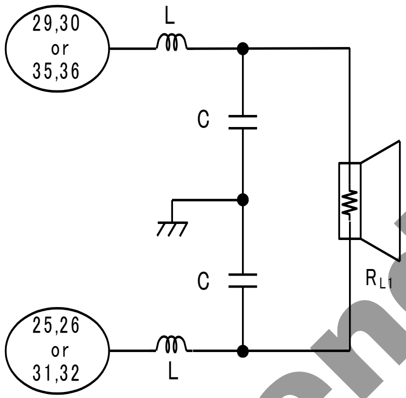


Figure 115

Following presents output LC filter constants with typical load impedances.

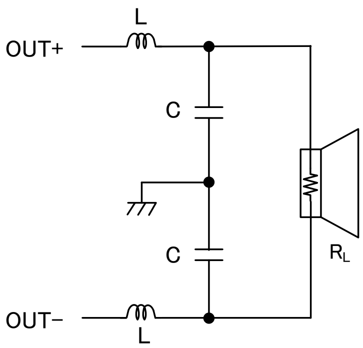
R_L	L	C
4Ω	10μH	1μF
6Ω	10μH	0.33μF
8Ω	15μH	0.33μF

Use coils with a low direct-current resistance and with a sufficient margin of allowable currents. A high direct-current resistance causes power losses. In addition, select a closed magnetic circuit type product in normal cases to prevent unwanted emission.

Use capacitors with a low equivalent series resistance, and good impedance characteristics at high frequency ranges (100kHz or higher). Also, select an item with sufficient withstand voltage because flowing massive amount of high-frequency currents is expected.

2) The value of the LC filter circuit computed equation

The output LC filter circuit of BD5452AMUV is as it is shown in Figure 116. The LC filter circuit of Figure 116 is thought to substitute it like Figure 117 on the occasion of the computation of the value of the LC filter circuit.



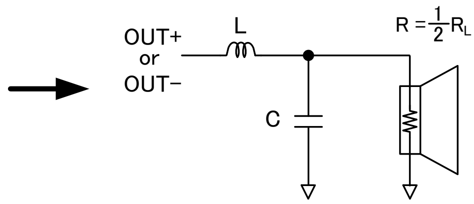


Figure 116. Output LCfilter 1

Figure 117. Output LCfilter 2

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The transfer function H(s) of the LC filter circuit of Figure 117 becomes the following.

$$H(s)=\frac{\frac{1}{LC}}{s^2+\frac{1}{CR}s+\frac{1}{LC}}=\frac{\omega^2}{s^2+\frac{\omega}{Q}s+\omega^2}$$

The ω and Q become the followings here.

$$\omega^2=\frac{1}{LC} \qquad \omega=2\pi f_{CL} \qquad f_{CL}=\frac{1}{2\pi\sqrt{LC}}$$

$$Q=R\sqrt{\frac{C}{L}}=\frac{1}{2}R_L\sqrt{\frac{C}{L}}$$

Therefore, L and C become the followings.

$$L=\frac{1}{\omega^2 C}=\frac{R_L}{4\pi f_{CL}Q} \qquad C=\frac{Q}{\omega R}=\frac{Q}{\pi f_{CL}R_L}$$

The R_L and L should be made known, and fCL is set up, and C is decided.

3) The settlement of the L value of the coil

A standard for selection of the L value of a coil to use is to take the following back anti-matter into consideration except for the factor such as a low cost-ization, miniaturization, pale pattern.

①When L value was made small.
(1) Circuit electric currents increase without a signal. And, efficiency in the low output gets bad.
(2) Direct current resistance value is restrained small when the coil of other L value and size are made the same. Therefore, maximum output is easy to take out. And, it can be used in the low power supply voltage because DC electric current (allowable electric current) value can be taken greatly.

②When L value was made large.
(1) Circuit electric current is restrained low without a signal. Efficiency in the low output improves.
(2) Direct current resistance value grows big when the coil of other L value and size are made the same. Therefore, maximum output is hard to take out. And, because it becomes small, use becomes difficult 【 the DC electric current (allowable electric current) value 】 in the low power supply voltage, too.

4) The settlement of the f_{CL}

As for the settlement of the fixed number of the LC filter circuit, it is taken into consideration about two points of the following, and set up.

①The PWM sampling frequency fPWM (=8fS) of BM5481MUV is set up in 384kHz (@fS=48kHz).
It is set up with fC < fPWM to restrain career frequency omission after the LC filter circuit.
②When fc is lowered too much, the voltage profit of the voice obi stage (especially, the neighborhood of 20kHz) declines in the speaker output frequency character of the difference movement mode.
And, the speaker output frequency character of the difference movement mode becomes the following.

RL=8Ω				RL=6Ω				RL=4Ω			
L[uH]	C[uF]	fc[kHz]	Q	L[uH]	C[uF]	fc[kHz]	Q	L[uH]	C[uF]	fc[kHz]	Q
10	0.1	75.32	0.40	10	0.1	51.01	0.30	10	0.1	32.19	0.20
	0.15	80.85	0.49		0.15	54.76	0.37		0.15	33.35	0.24
	0.22	86.79	0.59		0.22	56.73	0.44		0.22	34.55	0.30
	0.33	89.92	0.73		0.33	63.1	0.54		0.33	35.8	0.36
	0.47	86.79	0.87		0.47	66.68	0.65		0.47	38.37	0.43
	1.0	69.01	1.26		1.0	62.29	0.95		1.0	44.1	0.63
15	0.1	46.99	0.33	15	0.1	33.11	0.24	15	0.1	21.68	0.16
	0.15	49.66	0.40		0.15	34.36	0.30		0.15	22.08	0.20
	0.22	53.46	0.48		0.22	35.65	0.36		0.22	22.49	0.24
	0.33	57.54	0.59		0.33	38.37	0.44		0.33	22.91	0.30
	0.47	59.7	0.71		0.47	41.3	0.53		0.47	23.77	0.35
	1.0	52.75	1.03		1.0	44.67	0.77		1.0	27.47	0.52
22	0.1	30.76	0.27	22	0.1	22.49	0.20	22	0.1	14.72	0.13
	0.15	31.92	0.33		0.15	22.91	0.25		0.15	14.72	0.17
	0.22	33.73	0.40		0.22	23.77	0.30		0.22	15	0.20
	0.33	36.31	0.49		0.33	24.66	0.37		0.33	15.28	0.24
	0.47	39.08	0.58		0.47	26.06	0.44		0.47	15.56	0.29
	1.0	39.30	0.85		1.0	30.05	0.64		1.0	17.33	0.43

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5) About the EMI countermeasure

As a part EMI countermeasure except for the output LC filter recommended with P.93/106 to P.94/106, It can be confirmed with following;

・Chip Common Mode Choke Coil(DLY5ATN401) manufactured by Murata +1000pF(50V,Tolerance:B,1608),

・Chip inductor LCC3225T2R2MR manufactured by TAIYOYUDEN +1000pF(50V,Tolerance:B,1608)

6) The settlement of the snubber

The Snubber circuit must be optimized for application circuit to reduce the overshoot and undershoot of output PWM.

① Measure the spike resonance frequency f1 of the PWM output wave shape (When it stands up.) by using FET probe in the OUT terminal. (Figure 68) The FET probe is to monitor very near pin and shorten ground lead at the time of that.

② Measure resonance frequency f2 of the spike as a snubber circuit fixed number R=0Ω(Only with the condenser C, to connect GND) At this time, the value of the condenser C is adjusted until it becomes half of the frequency (2f2=f1) of the resonance frequency f1 of ①. The value of C which it could get here is three times of the parasitic capacity Cp that a spike is formed. (C=3Cp)

③ Parasitic inductance Lp is looked for at the next formula.

$$L_p = \frac{1}{(2\pi f_1)^2 C_p}$$

④The character impedance Z of resonance is looked for from the parasitic capacity Cp and the parasitism inductance Lp at the next formula.

$$Z = \sqrt{\frac{L_p}{C_p}}$$

⑤ A snubber circuit fixed number R is set up in the value which is the same as the character impedance Z. A snubber circuit fixed number C is set up in the value of 4-10 times of the parasitic capacity Cp. (C=4Cp to 10Cp) Decide it with trade-off with the character because switching electric currents increase when the value of C is enlarged too much.

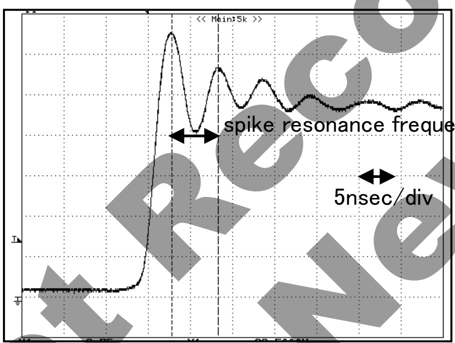

Figure 118. PWM Output waveform (measure of spike resonance frequency

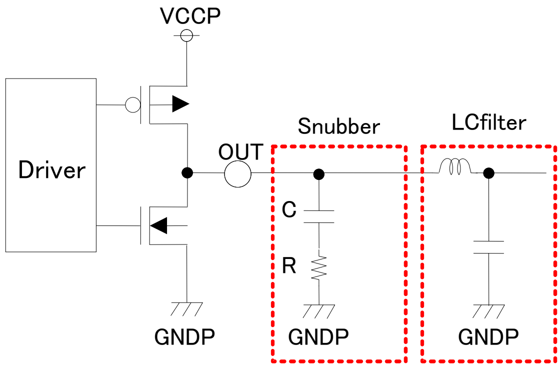

Figure 119. snubber schematic

Following presents Snubber filter constants with the recommendation value at ROHM 4 layer board.

R_L	*C25B,C29B, C31B,C35B*	*R25,R29, R31,R35*
4Ω	3300pF	5.6Ω
6Ω	3300pF	5.6Ω
8Ω	1200pF	5.6Ω

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Level Diagram of Audio Signal

Level diagram of audio signal is shown the below figure. Speaker output level is depended on I2S digital audio input level, DSP gain, PWM gain, BTL gain and Loss of power stage and low pass filter.
I2S input level is full-scale signal, the supply voltage of the block is DVDD, therefore, 0dBFS is equal to DVDD voltage [Vpp]. DSP gain is set by 2 wire control variably, and -0.5dB is set at PWM Modulator block usually. At the Power stage, the PWM Modulator output is shifted PWM signal level from DVDD to VCC, and added loss of the output transistor resistance rDS and DC resistance of coil rDC.

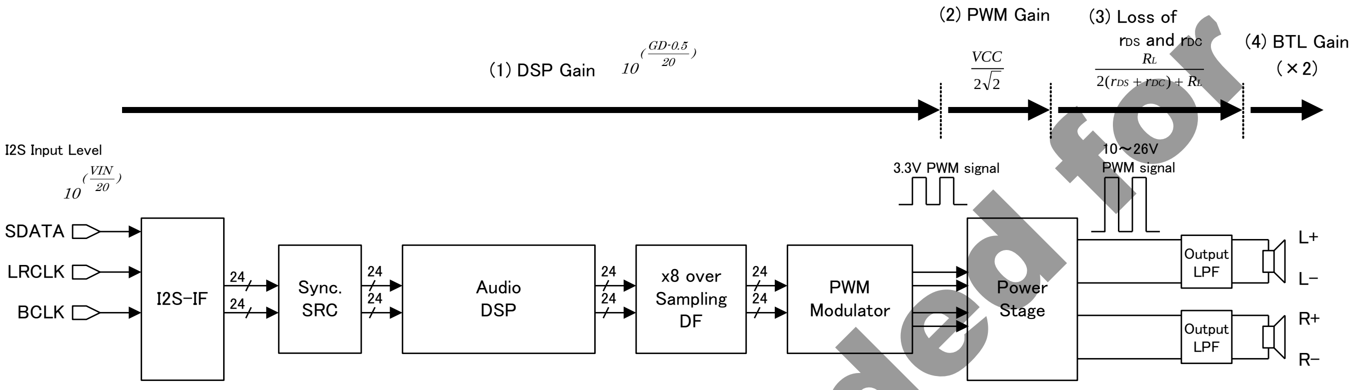

Figure 120. Level Diagram of Audio Signal

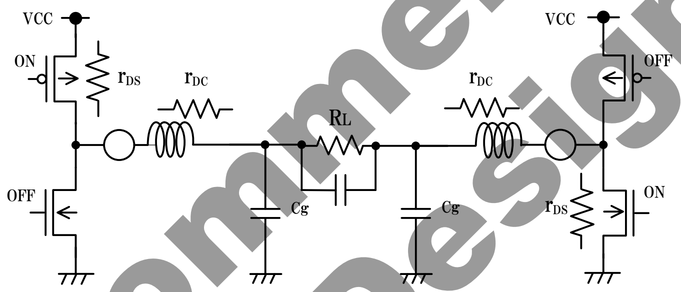

Figure 121. Output LPF circuit

In Bridge-Tied-Load (BTL) connection, the following formula gives an approximate value of output power *Po at non*-clipping output waveform:

$$P_o = \frac{\left(\overbrace{10^{VIN/20}}^{\text{I2S Input Level}} \times \overbrace{10^{(GD-0.5)/20}}^{\text{DSP Gain}} \times \overbrace{\frac{VCC}{2\sqrt{2}}}^{\text{PWM Gain}} \times \overbrace{2}^{\text{BTL Gain}} \times \overbrace{\frac{R_L}{2\times(r_{DS}+r_{DC})+R_L}}^{\text{Loss of } r_{DS} \text{ and } r_{DC}}\right)^2}{R_L}$$

VIN : I2S Input level [dBFS]
GD : DSP gain [dB]
VCC : Power supply voltage of Power stage [V]
DVDD : Power supply voltage of DSP block [V]
RL : Load impedance [Ω]
rDS : Turn-on resistance of output MOS Tr. [Ω]
(Typ=180m Ω)
rDC : DC resistance of output LPF coil [Ω]

If the circuit is driven further until an output waveform is clipped, an output power higher than that without distortion is obtained. In general a clipped output is quantified where “THD+N = 1% and 10%,” and a maximum output power under that status is calculated by the following formula:

$$P_{O(1\%)} = \frac{\left(10^{(-0.5/20)} \times \frac{VCC}{\sqrt{2}} \times \frac{R_L}{2(r_{DS}+r_{DC})+R_L}\right)^2}{R_L}\ [W]$$

$$P_{O(10\%)} = P_{O(1\%)} \times 1.25\ [W]$$

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Power Dissipation (VQFN048V7070)

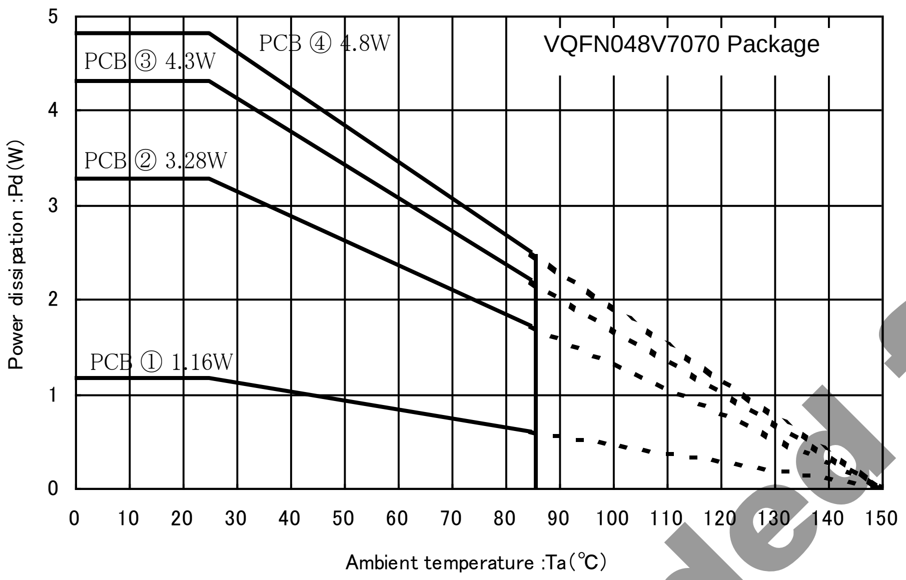

Figure 122

Measuring instrument: TH-156 (Shibukawa Kuwano Electrical Instruments Co., Ltd.)
Measuring conditions: Installation on ROHM's board
Board size: 114.3mm × 76.2mm × 1.6mm (with thermal via on board)
Material: FR4
・The board and exposed heat sink on the back of package are connected by soldering.

PCB (1): 1- layer board (back copper foil size: 34.09mm2), θja = 107.8°C/W
PCB (2): 2- layer board (back copper foil size: 5505mm2), θja = 38.1°C/W
PCB (3): 4- layer board (Top and bottom layer back copper foil size: 34.09mm2, 2nd and 3rd layer back copper foil size: 5505mm2), θja = 29.1°C/W
PCB (4): 4- layer board (back copper foil size: 5505mm2), θja = 25.9°C/W

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions. This IC exposes its frame of the backside of package. Note that this part is assumed to use after providing heat dissipation treatment to improve heat dissipation efficiency. Try to occupy as wide as possible with heat dissipation pattern not only on the board surface but also the backside.
Full Digital speaker amplifier is high efficiency and low heat generation by comparison with conventional Analog power amplifier. However, In case it is operated continuously by maximum output power, Power dissipation (Pdiss) might exceed package dissipation. Please consider about heat design that Power dissipation (Pdiss) does not exceed Package dissipation (Pd) in average power (Poav). (Tjmax : Maximum junction temperature=150°C, Ta : Peripheral temperature[°C], θja : Thermal resistance of package[°C/W], Poav : Average power[W], η : Efficiency)

Package dissipation : Pd (W) =(Tjmax – Ta) / θja
Power dissipation : Pdiss (W) = Poav x (1/η – 1)

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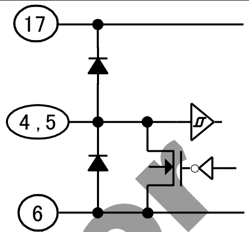
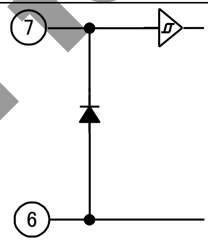
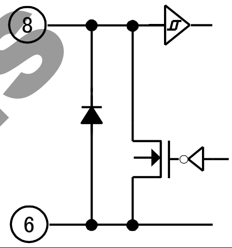
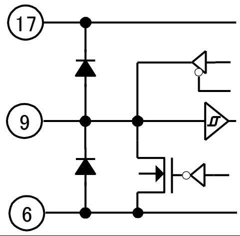
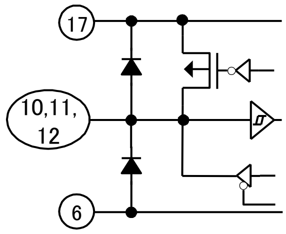
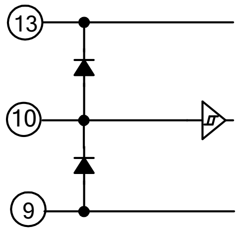
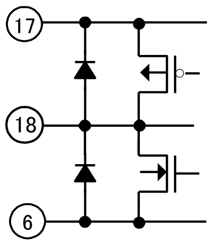
I/O equivalence circuit (Provided pin voltages are typ Values)

Pin No.	Pin name	Pin voltage	Pin explanation	Internal equivalence circuit
4 5	RSTX MUTEX	0V 0V	Reset pin for Digital circuit H:Reset OFF L:Reset ON Speaker output mute control pin H:Mute OFF L:Mute ON	
6	DGND	0V	GND pin for Digital I/O	—
7	SCL	—	2 wire transmit clock input pin ・Please notice. Absolute Maximum Voltage is 4.5V.	
8	SDA	—	2 wire data input/output pin ・Please notice. Absolute Maximum Voltage is 4.5V.	
9	ADDR	0V	2 wire Slave address select pin	
10 11 12	SDATA LRCLK BCLK	3.3V	Digital sound signal input pin	
19	MONI	3.3V	TEST pin. Please pull up to DVDD.	
15	VSS	0V	GND pin for Digital block	—
18	PLL	1V	PLL's filter pin	

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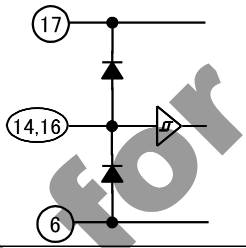
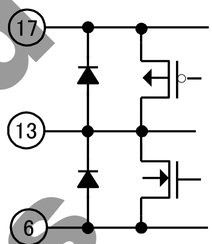
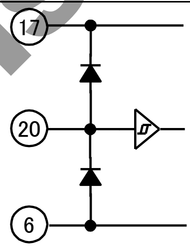
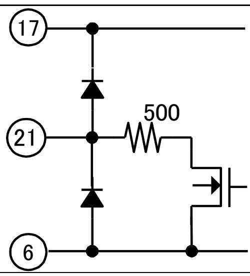
I/O equivalence circuit (Provided pin voltages are typ Values)

Pin No.	Pin name	Pin voltage	Pin explanation	Internal equivalence circuit
17	DVDD	3.3V	Power supply pin for Digital I/O.	—
14 16	TEST1 TEST2	— —	Test pin Please connect to VSS.	
13	REG15	1.5V	Internal power supply pin for Digital circuit	
20	TEST3	—	Test pin Please connect to VSS.	
21	ERROR	3.3V	Error flag pin H: While Normal L: While Error	
22	NC	—	Non Connection Pin	—

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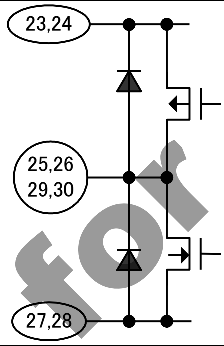
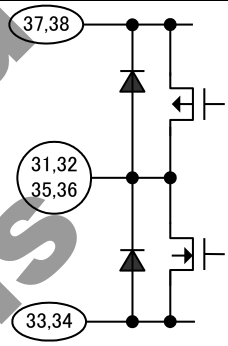
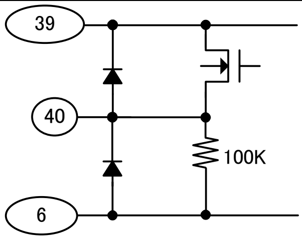
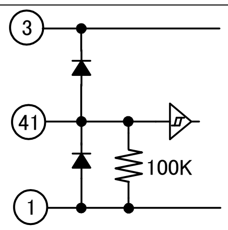
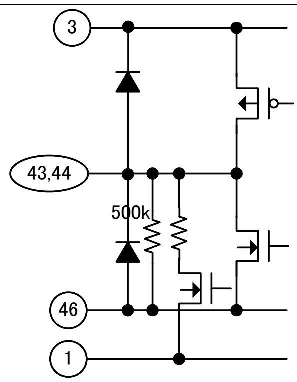
I/O equivalence circuit (Provided pin voltages are typ Values)

Pin No.	Pin name	Pin voltage	Pin explanation	Internal equivalence circuit
23 24	VCCP2	VCC	Power supply pin for ch2 PWM signal	
25 26	OUT2N	VCC ~ 0V	Output pin of ch2 positive PWM Please connect to Output LPF.	
27 28	GNDP2	0V	GND pin for ch2 PWM signal	
29 30	OUT2P	VCC ~ 0V	Output pin of ch2 negative PWM Please connect to Output LPF.	
31 32	OUT1N	VCC ~ 0V	Output pin of ch1 negative PWM Please connect to Output LPF.	
33 34	GNDP1	0V	GND pin for ch1 PWM signal	
35 36	OUT1P	VCC ~ 0V	Output pin of ch1 positive PWM Please connect to Output LPF.	
37 38	VCCP1	VCC	Power supply pin for ch1 PWM signal	
39	VCCA	VCC	Power supply pin for Analog signal	—
40	REG_G	5.5V	Internal power supply pin for gate driver Please connect the capacitor.	
41	SDB	0V	Audio amplifier control pin H: Shut down OFF L: Shut down ON	
43 44	OUT3 OUT4	0V 0V	Audio amplifier output pin	

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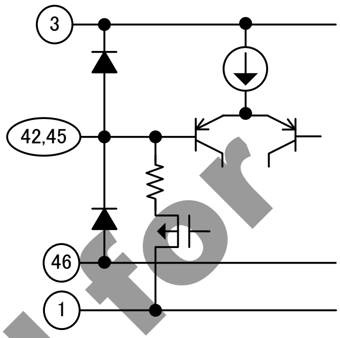
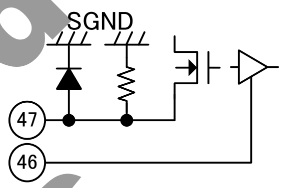
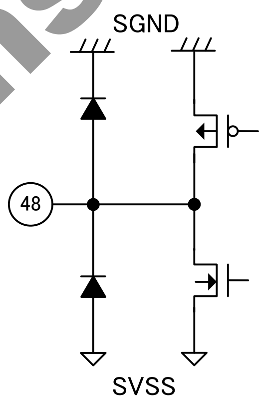
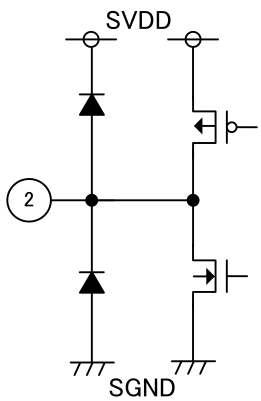
I/O equivalence circuit (Provided pin voltages are typ Values)

Pin No.	Pin name	Pin voltage	Pin explanation	Internal equivalence circuit
42 45	IN3 IN4	0V 0V	Audio amplifier input pin	
46 47	SVSS CPVSS	–	Charge pump output pin	
48	CN	–	Flying capacitor negative pin	
1	SGND	0V	GND pin for Audio amplifier	–
2	CP	–	Flying capacitor positive pin	
3	SVDD	3.3V	Power supply for Audio amplifier	–

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned OFF completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – continued

12. Regarding the Input Pin of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

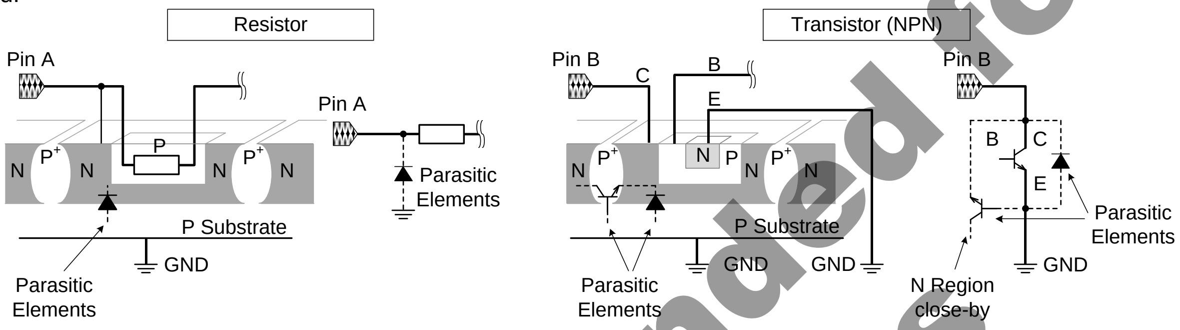

Figure 78. Example of Monolithic IC Structure

13. Ceramic Capacitor
When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)
Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over-Current Protection Circuit (OCP)
This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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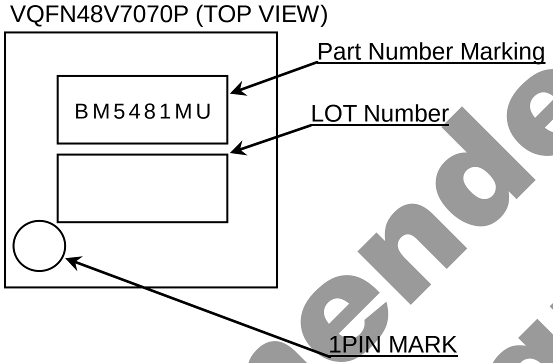
Ordering Information

B M 5 4 8 1 M U V - E 2

- Part Number
- Package
  MUV: VQFN48V7070P
- Packaging and forming specification
  E2: Embossed tape and reel

Marking Diagram



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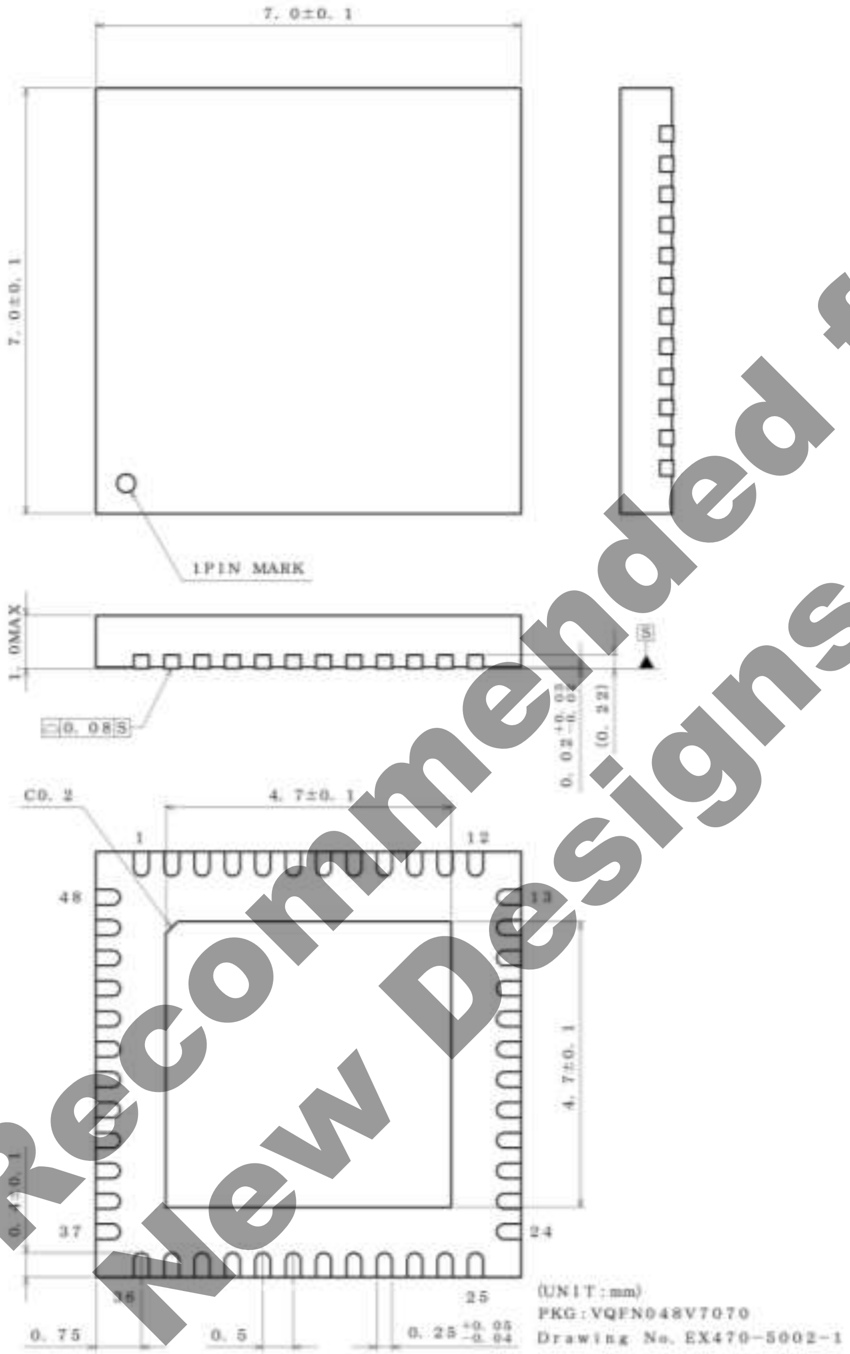
Physical Dimension, Tape and Reel Information

Package Name	VQFN048V7070P



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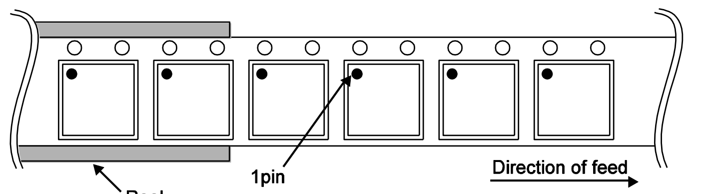
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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