ESD150-B1-W0201

Bi-directional ESD protection device, 3.3 V, 0.15 pF, 0201

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Product description

This Infineon ESD (electrostatic discharge) protection device has a bi-directional and symmetric *I*/*V* characteristic and excellent clamping performance.

Feature list

- ESD / transient protection according to:
  - IEC61000-4-2 (ESD): ±12 kV (contact) / ±12 kV (air)
  - IEC61000-4-4 (EFT): ±2.5 kV / ±50 A (5/50 ns)
  - IEC61000-4-5 (Surge): ±3 A (8/20 µs)
- Bi-directional maximum working voltage: V_{WM} = ±3.3 V
- Line capacitance: C_L = 0.15 pF at f = 10 GHz
- Clamping voltage: V_{cl} = 5.4 V at I_{TLP} = 16 A with R_{dyn} = 0.16 Ω
- Very low leakage current: I_L = 0.1 nA
- Small form factor SMD size 0201, low profile (0.58 x 0.28 x 0.15 mm^3)

Potential applications

- USB4 Gen 2/Gen 3, USB 3.x Gen 1/Gen 2, USB 2.0, Thunderbolt 3
- HDMI 2.1, DisplayPort 1.4

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Device information

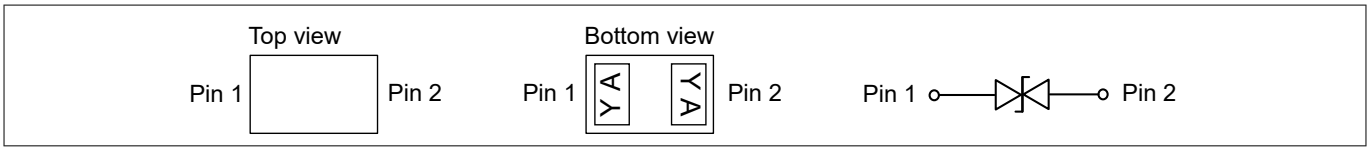

Figure 1 Pin configuration and schematic diagram

Table 1 Part information

Product name / Ordering code	Package	Pin configuration	Marking	Pieces / Reel
ESD150-B1-W0201 / ESD150B1W0201E6327XTSA1	WLL-2-3	1 line, bi-directional	YA	15 k

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1 Absolute maximum ratings

Table 2 Absolute maximum ratings at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Values		Unit	Note or test condition
		Min.	Max.		
Working voltage [1]	V_{WM}	-3.3	+3.3	V	
ESD discharge voltage	V_{ESD} (contact)	-12	+12	kV	Discharge network: R = 330 Ω, C = 150 pF [2]
	V_{ESD} (air)	-12	+12		
Peak pulse power	P_{PK}	–	12	W	Stress pulse: 8/20 µs current waveform [3]
Peak pulse current	I_{PP}	-3	+3	A	
Operating temperature	T_{op}	-55	+125	°C	
Storage temperature	T_{stg}	-65	+150		

Attention**: **Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings. Exceeding only one of these values may cause irreversible damage to the component.

1 Device snaps back to a low holding voltage, refer to application note AN525 for latch-up prevention.
2 Based on IEC61000-4-2.
3 Based on IEC61000-4-5.

2 Electrical characteristics

Note: *T_A = 25°C, unless otherwise specified. Device is electrically symmetrical.*

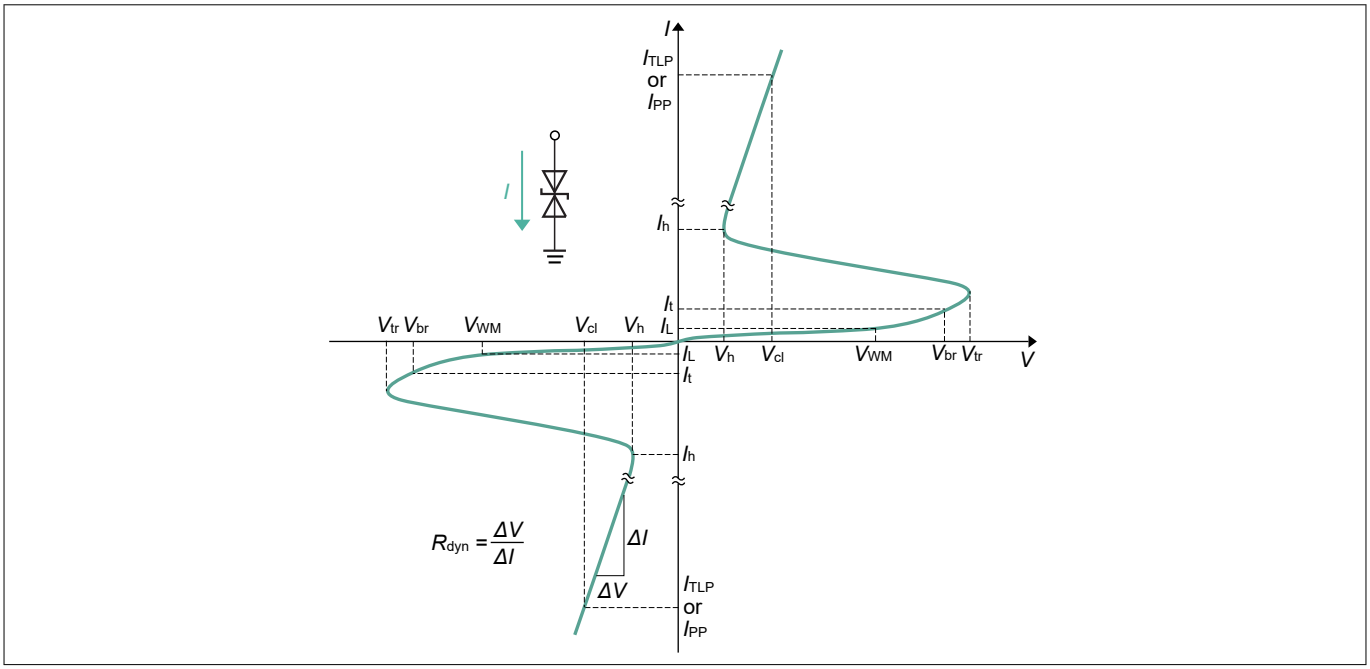

Figure 2 ***I/V* characteristic curve**

Table 3 ***I/V* characteristic parameters**

Symbol	Parameter
I_h	Holding current
I_L	Leakage current
I_{PP}	Peak pulse current, based on IEC61000-4-5
I_t	Test current
I_{TLP}	TLP current
R_{dyn}	Dynamic resistance
V_{br}	Breakdown voltage
V_{cl}	Clamping voltage
V_h	Holding voltage
V_t	Test voltage
V_{tr}	Trigger voltage
V_{WM}	Maximum working voltage

Note: *For more detailed explanation of electrical parameters refer to [1]*

2 Electrical characteristics

Table 4 DC characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Breakdown voltage	V_{br}	5.9	8.4	9.6	V	I_t = 1 mA
Holding voltage	V_h	–	2.5	–		$I = I_h$
Holding current	I_h	–	30	–	mA	$V = V_h$
Leakage current	I_L	–	0.1	10	nA	V_{WM} = 3.3 V

Table 5 AC characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	0.24	0.35	pF	V = 0 V, f = 1 MHz
		–	0.17	–		V = 0 V, f = 1 GHz
		–	0.16	–		V = 0 V, f =5 GHz
		–	0.15	–		V = 0 V, f = 10 GHz
Series inductance	L_S	–	<0.1	–	nH	Extracted from S-parameters

Table 6 Protection characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Clamping voltage (TLP) [4] [5]	V_{cl}	–	3.5	–	V	I_{TLP} = 4 A
		–	4.2	–		I_{TLP} = 8 A
		–	5.4	–		I_{TLP} = 16 A
		–	8	–		I_{TLP} = 30 A
Clamping voltage (8/20 µs) [6]		–	3.4	–		I_{PP} = 1 A
		–	3.6	–		I_{PP} = 2 A
		–	3.8	–		I_{PP} = 3 A
Dynamic resistance [4]	R_{dyn}	–	0.16	–	Ω	

4 TLP parameters: Z_0 = 50 Ω, t_p = 100 ns, t_r = 0.6 ns, averaging window 30-60 ns.
5 Refer to application note AN210 [2]
6 t_p = 8/20 µs. Stress pulse based on IEC61000-4-5.

3 Typical characteristic diagrams

Note: $T_A = 25$ °C, *unless otherwise specified.*

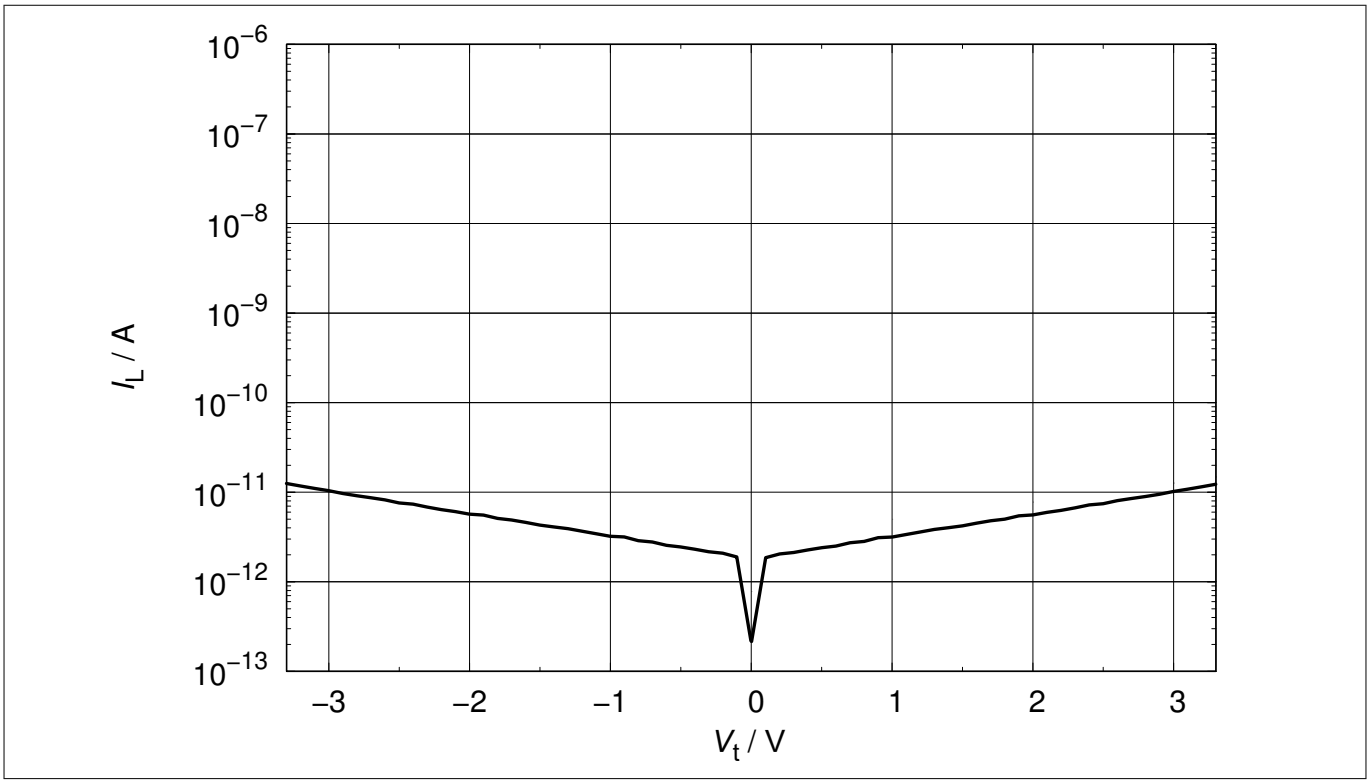

Figure 3 **Leakage current: $I_L = f(V_t)$**

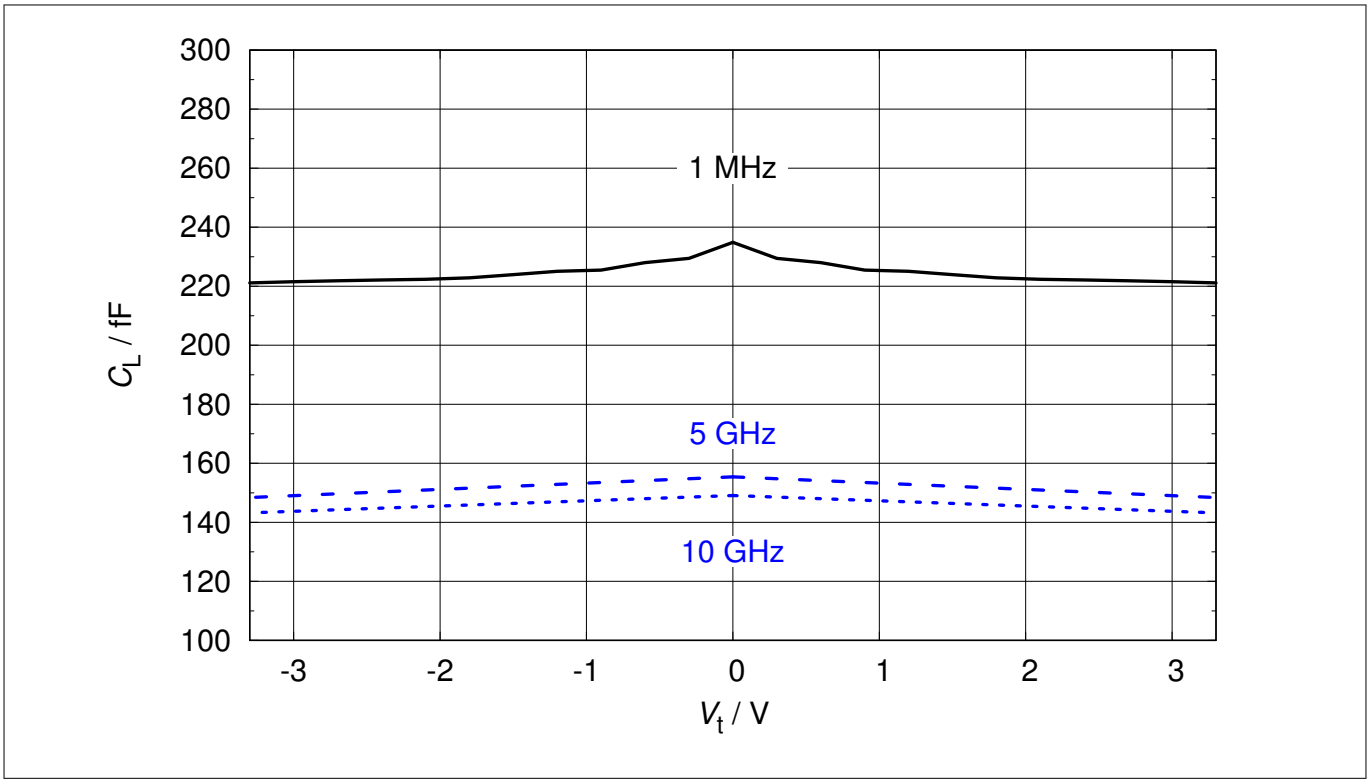

Figure 4 **Line capacitance: $C_L = f(V_t)$, f = 1 MHz, 5 GHz, 10 GHz**

3 Typical characteristic diagrams

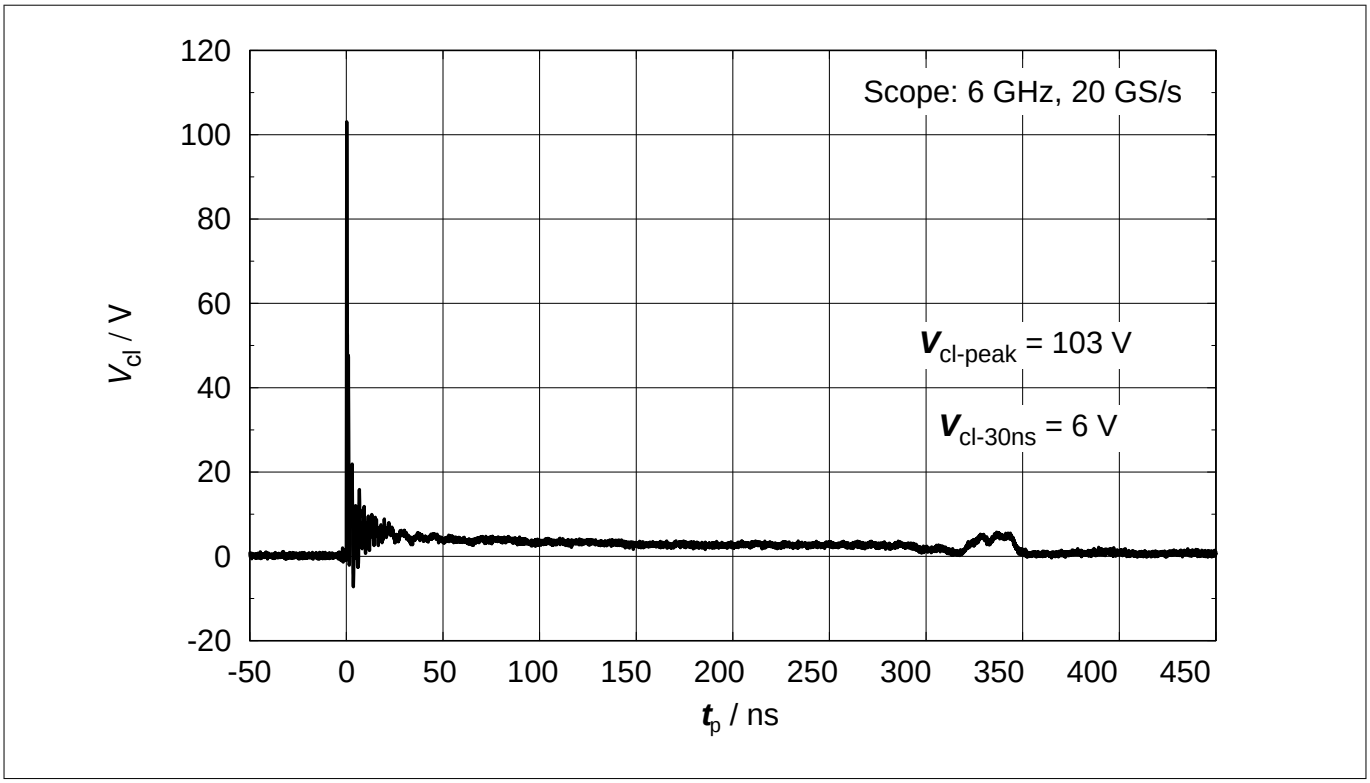

Figure 5 **Clamping voltage (ESD): $V_{cl} = f(t_p)$, 8 kV positive pulse based on IEC61000-4-2**

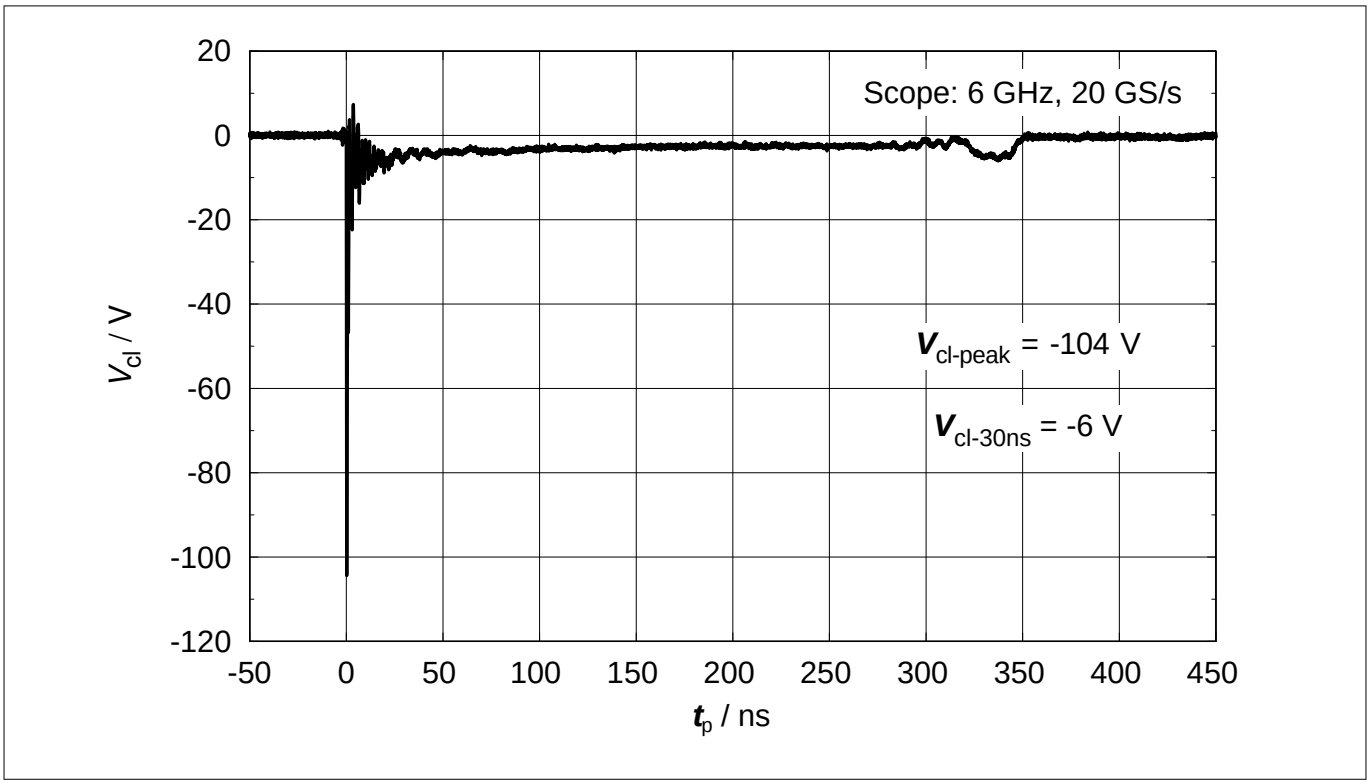

Figure 6 **Clamping voltage (ESD): $V_{cl} = f(t_p)$, 8 kV negative pulse based on IEC61000-4-2**

3 Typical characteristic diagrams

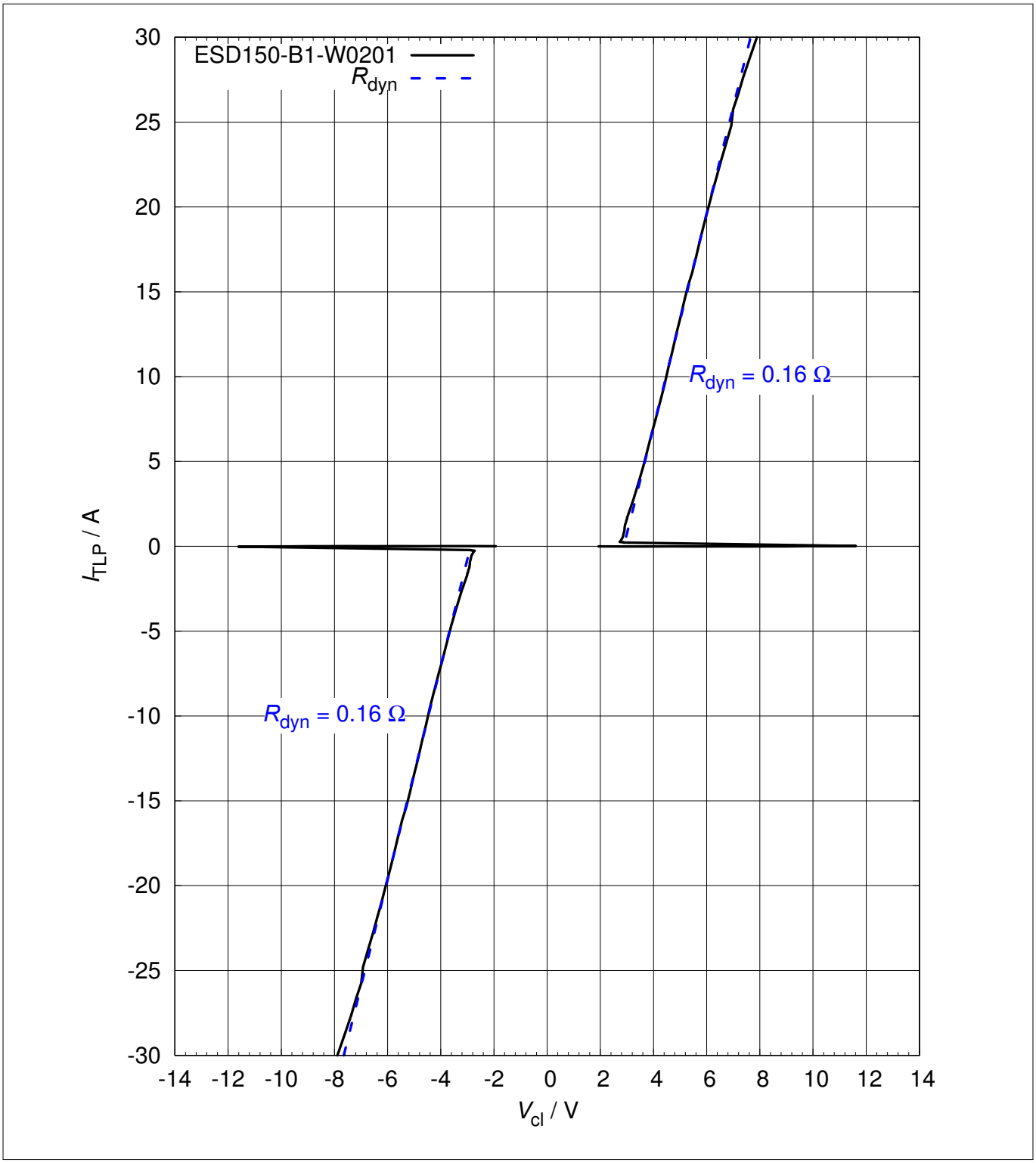

Figure 7 **Clamping voltage (TLP): I_{TLP} = f(V_{cl})**

3 Typical characteristic diagrams

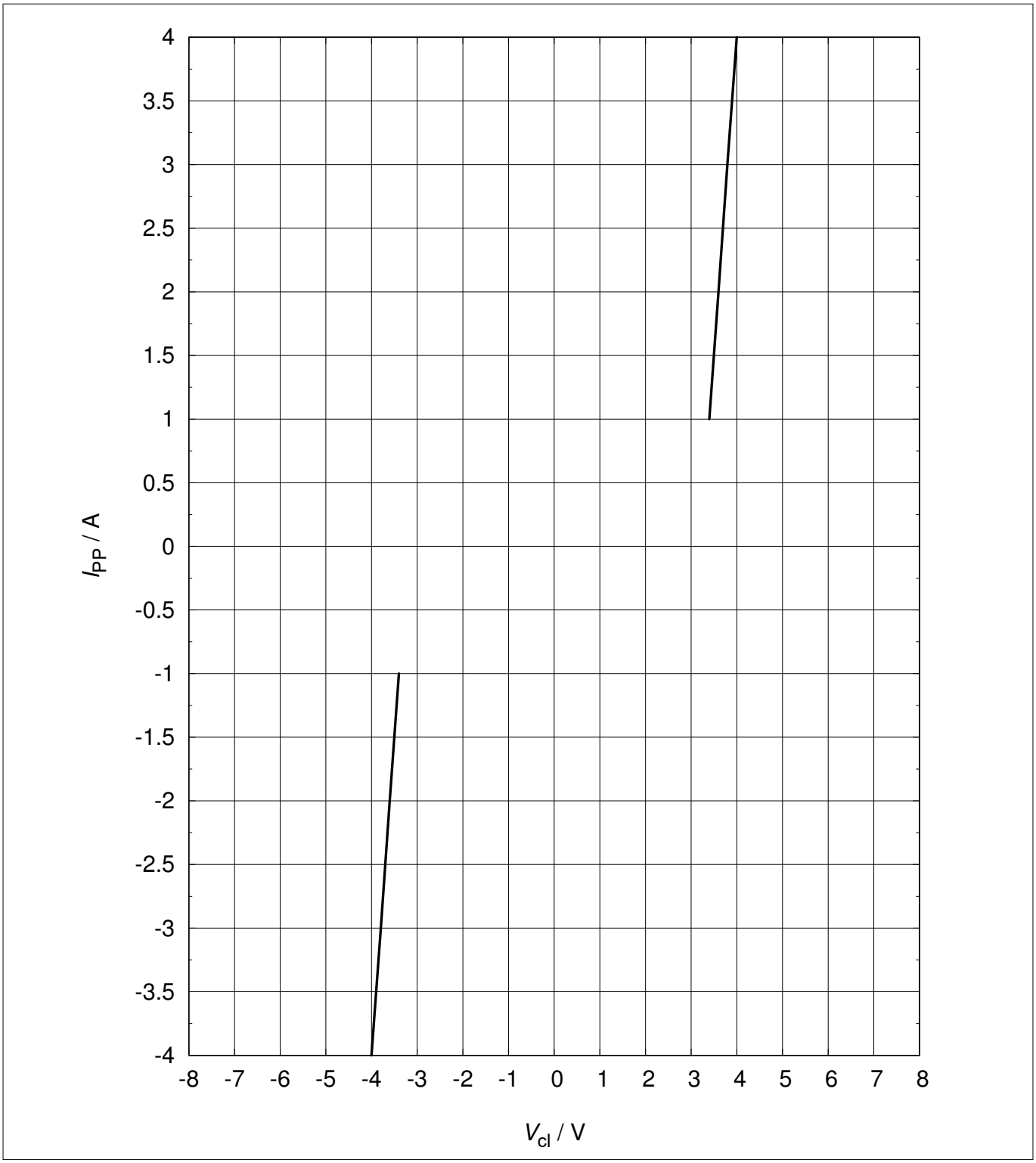

Figure 8 Clamping voltage (Surge): I_{PP} = f(V_{cl}), based on IEC61000-4-5

3 Typical characteristic diagrams

Figure 9 **Insertion loss *IL* = f(*f*), measured in a 50 Ω system**

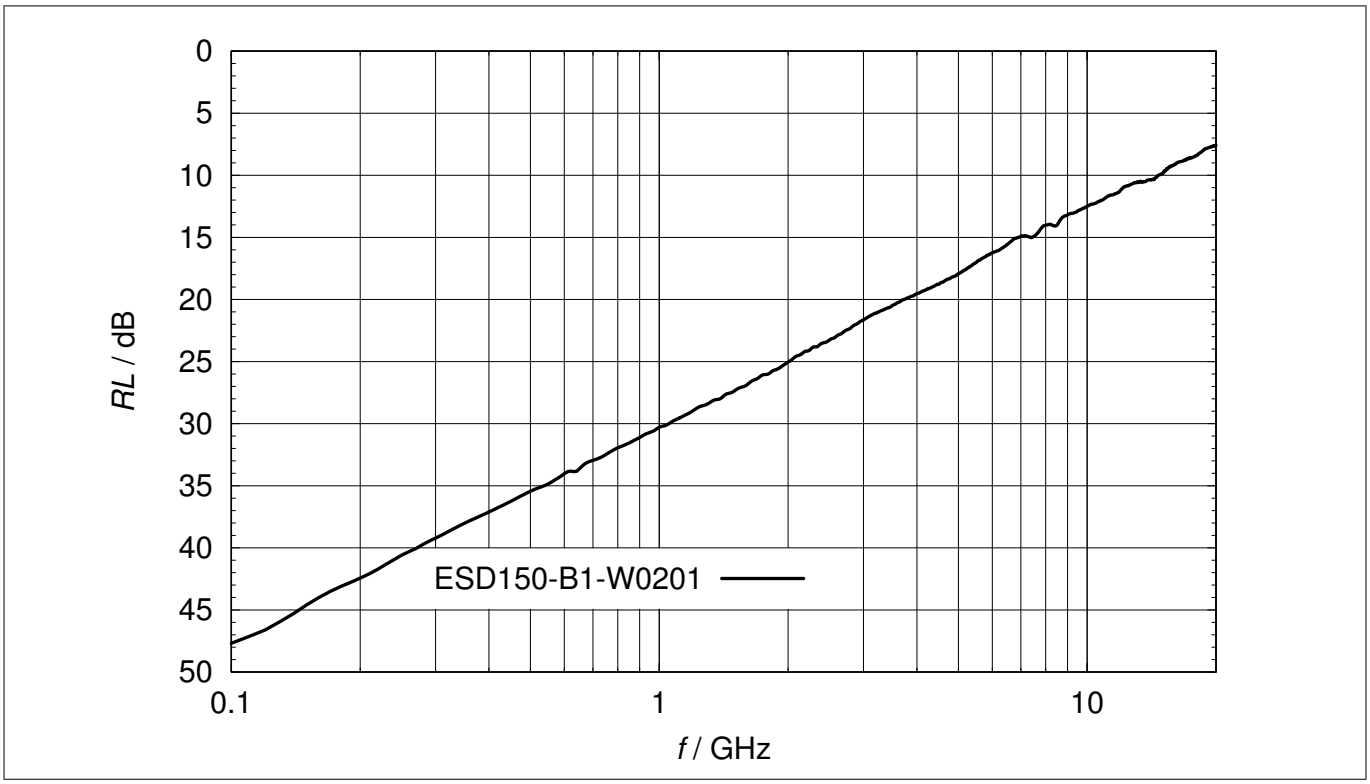

Figure 10 **Return loss *RL* = f(*f*), measured in a 50 Ω system**

4 Package information WLL-2-3

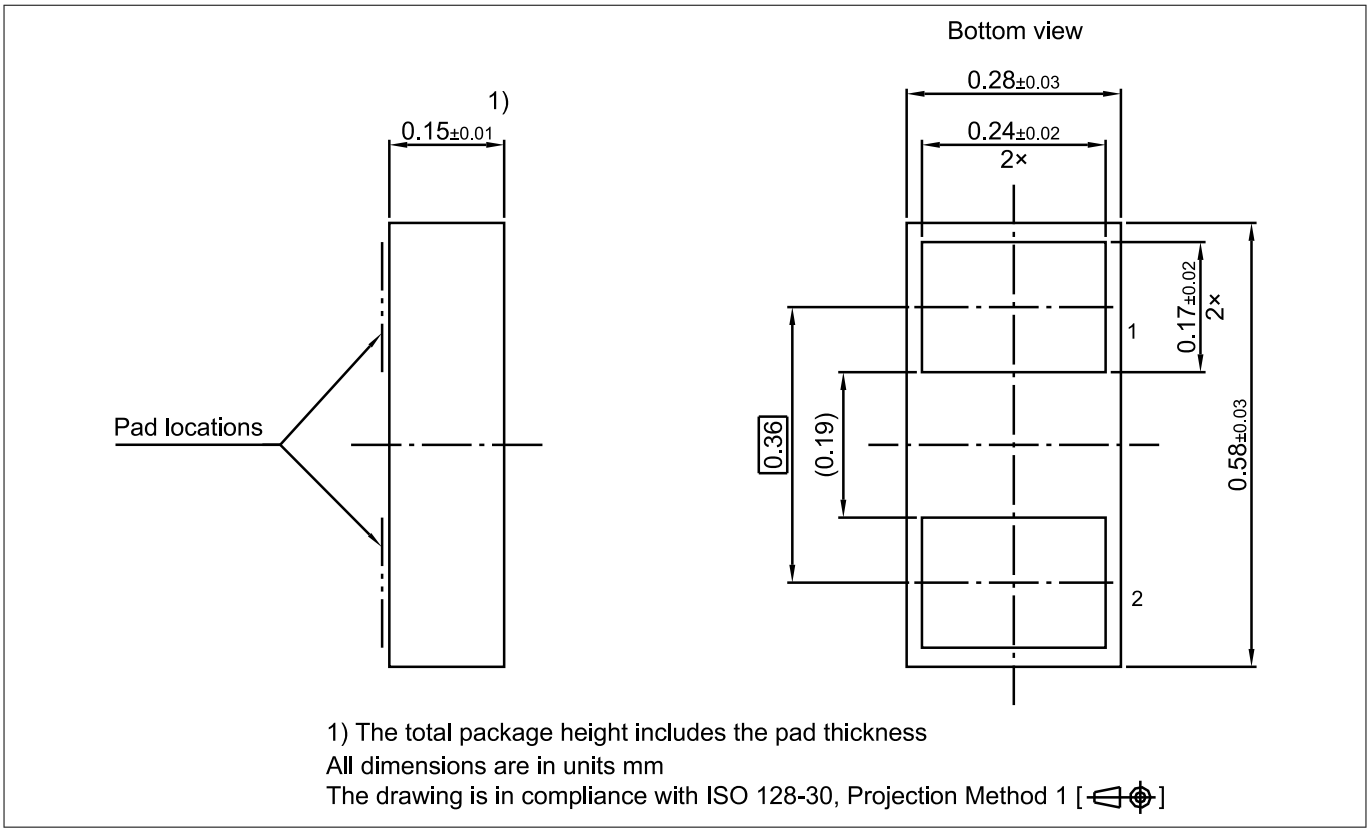

Figure 11 WLL-2-3 package

Note: For package information including footprint, packing and assembly recommendation refer to:

https://www.infineon.com/cms/en/product/packages/SG-WLL/SG-WLL-2-3/

5 References

[1]	Infineon AG - Understanding ESD protection device characteristics
[2]	Infineon AG - **Application note AN210**: Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology

6 Revision history

Document version	Date of release	Description of changes
v1.0	2020-10-23	• First final datasheet version
v2.0	2022-04-26	• Potential applications updated
v2.1	2022-09-27	• Editorial change

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Edition 2022-09-27

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
IFX-wyr1587022064650

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