RW610

Wireless MCU with Integrated Wi-Fi 6 and Bluetooth Low Energy 5.4

Rev. 8 — 2 July 2024 Product data sheet

1 Product overview

The RW610 is a highly integrated, low-power Wireless MCU with an integrated MCU and Wi-Fi 6 + Bluetooth Low Energy (LE) radios designed for a broad array of applications. Applications include connected smart home and appliances, enterprise and industrial automation and smart energy.

The RW610 MCU subsystem includes a 260 MHz Arm® Cortex®-M33 core with TrustZone™-M, 1.2 MB on-chip SRAM. The RW610 also includes a Quad SPI interface with high bandwidth, and an on-the-fly decryption engine for securely accessing off-chip XIP flash and PSRAM.

The RW610 includes a full-featured 1x1 dual-band (2.4 GHz / 5 GHz) 20 MHz Wi-Fi 6 (802.11ax) subsystem bringing higher throughput, better network efficiency, lower latency, and improved range over previous generation Wi-Fi standards. The Bluetooth LE radio supports 2 Mbit/s high-speed data rate, and long range and extended advertising.

The RW610 is an ideal device for Matter applications running over Wi-Fi or Ethernet. This capability enables Matter functionality for local and cloud-based control, and for monitoring of IoT products seamlessly across major ecosystems.

EdgeLock™ security technology of NXP is incorporated, offering secure boot, secure debug, secure firmware updates, and secure life cycle management as well as hardware cryptography and Physically Unclonable Function (PUF) for secure key management.

The advanced design of the RW610 delivers tight integration, low power, and highly secure operation in a space- and cost-efficient wireless MCU requiring only a single 3.3 V power supply.

Figure 1 shows RW610 overall block diagram for the dual-antenna configuration.

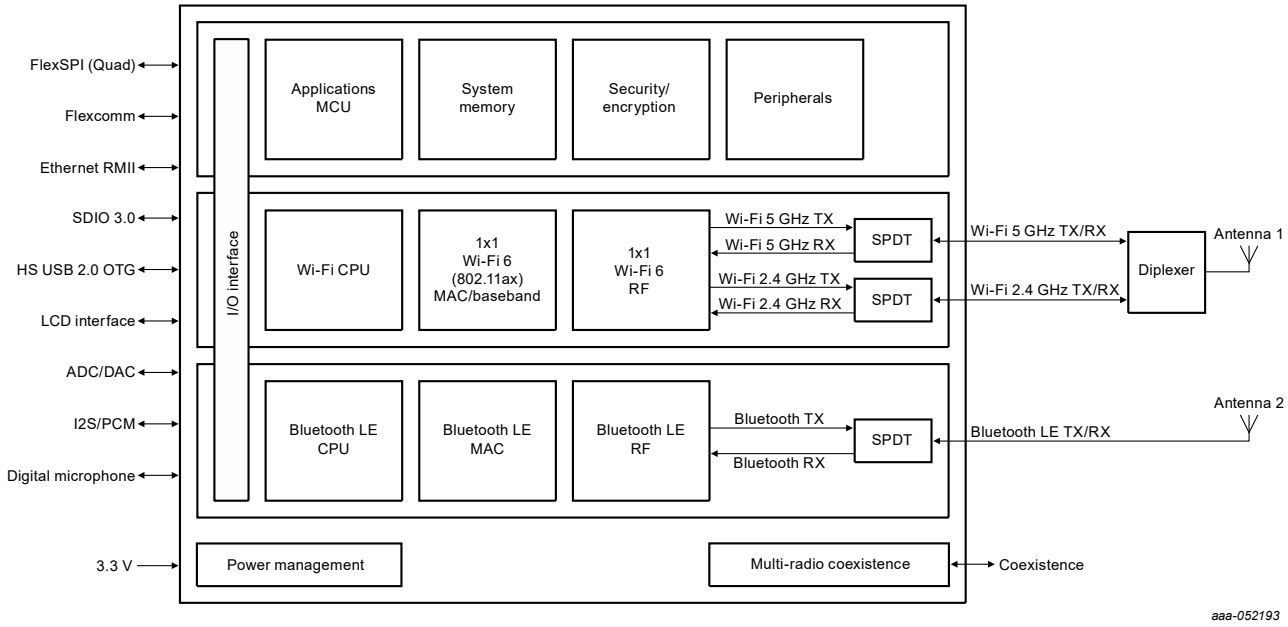


Figure 1. RW610 block diagram (two antennas)

Figure 2 shows RW610 overall block diagram for the single-antenna configuration.

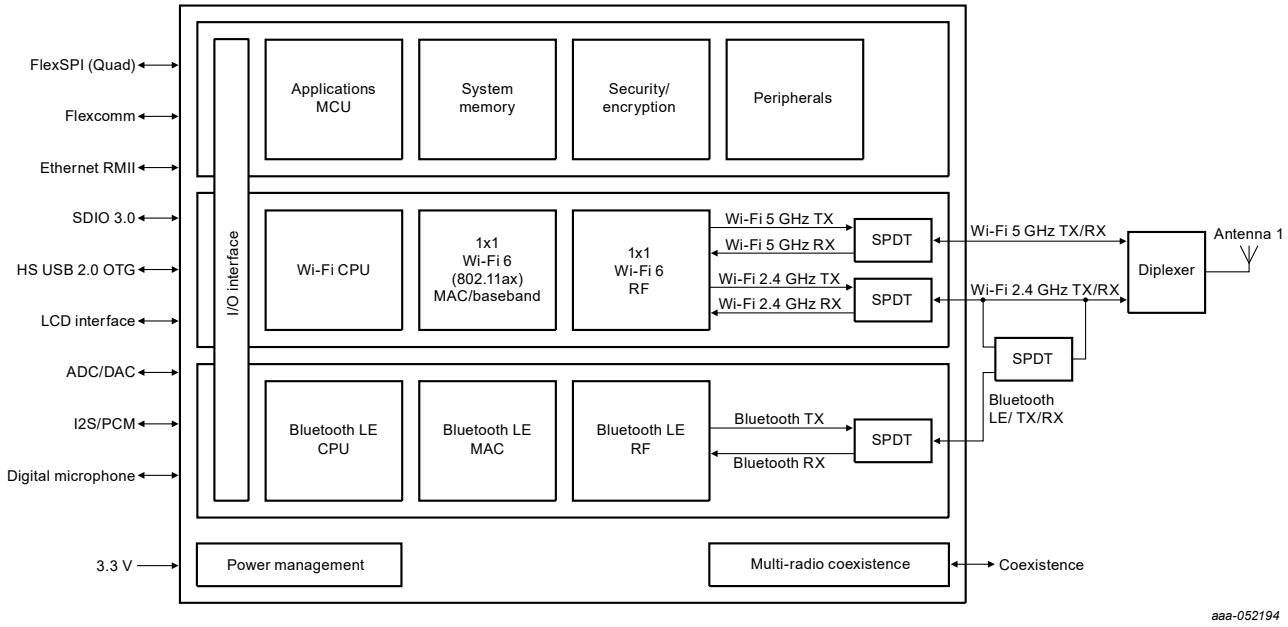


Figure 2. RW610 block diagram (one antenna)

1.1 Applications

- **Smart home**: smart outlet, light switch, security camera, thermostat, sprinkler controller, door lock, doorbell, garage door, security system, and smart display
- **Industrial**: building automation, smart lighting, security / physical access, Point of Sale (POS) terminals
- **Smart devices**—air purifier, pet monitor, weighing scale, glucometer, blood pressure monitor, fitness equipment
- **Smart appliances**—refrigerator, washer, dryer, oven range, microwave, dishwasher, water heater, air conditioner, robotic vacuum cleaner
- **Smart accessories**—smart speakers, headset, alarm clock, gaming accessory, remote control
- **Gateways**—Multi-radio hub/smart device gateway to/for Internet/IP connectivity

1.2 RW610 architecture

Figure 3 shows RW610 main subsystems.

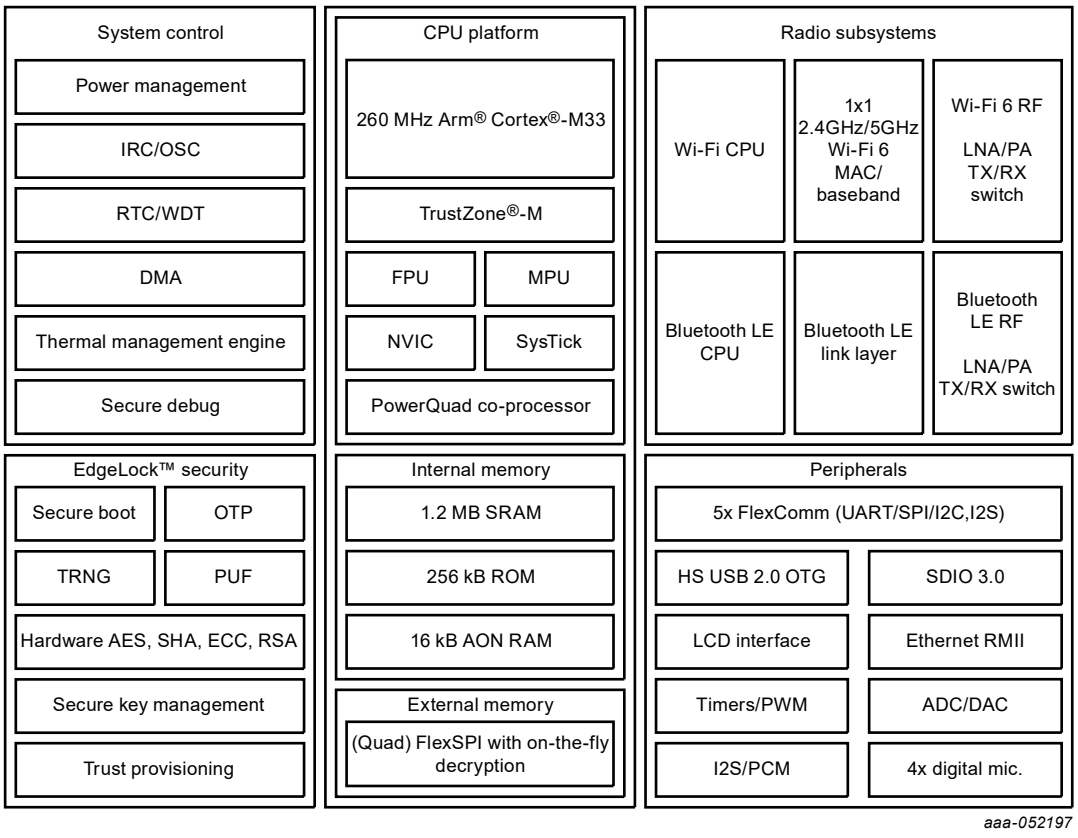


Figure 3. RW610 main subsystems

1.2.1 MCU and system memory

- 260 MHz Arm Cortex-M33 with TrustZone-M
- CoreMark® score: 1,033; 3.97 CoreMark/MHz
- 1.2 MB integrated SRAM
- FlexSPI external flash interface supports eXecute-In-Place (XIP) and on-the-fly firmware encryption/decryption and authentication
- FlexSPI external flash interface supports up to 128 MB.
- FlexSPI external PSRAM interface for system memory expansion supports up to 128 MB.
- The combined external memory interfaces support up to 128 MB in total (flash + PSRAM).

1.2.2 System interfaces and connectivity

- Up to five configurable universal serial interface modules (FlexComm interfaces). Configurable as SPI/I2C/I2S/UART
- SDIO 3.0
- High Speed USB 2.0 On-The-Go (OTG) with integrated PHY
- IEEE 1588 RMII/Fast Ethernet interface
- QVGA (320 x 240) LCD interface supporting SPI and 8080 interfaces
- 16-bit ADC and 10-bit DAC
- 32-bit general purpose timers/PWM
- 4 x digital microphone support

1.2.3 Platform security

- NXP EdgeLock™ Assurance
- NXP EdgeLock 2GO Trust Provisioning
- Trusted execution environment (TEE) based on Arm TrustZone-M
- Hardware root of trust
- Hardware cryptography accelerators (symmetric, asymmetric, secure hash, KDF, etc.)
- True Random Number Generator (TRNG)
- Physically Unclonable Function (PUF)
- OTP-based device configuration and life cycle management
- Secure boot, software update and debug
- On-chip tamper detection for voltage level and glitch, temperature and reset
- SESIP Assurance Level 3 (SESIP3)
- PSA Certified Level 3

1.2.4 System control and debugging

- Integrated system PLLs
- System DMA
- RTC and watchdog timers
- Integrated thermal management engine
- Secure JTAG/SWD

1.3 Wi-Fi 6 (802.11ax) key features

- 1x1 dual-band 2.4 GHz/5 GHz Wi-Fi 6 radio
- Integrated Wi-Fi PA, LNA, and T/R switch, up to +21 dBm Tx power
- 20 MHz channel operation
- Wi-Fi 6 Target Wake Time (TWT) support
- Wi-Fi 6 Extended Range (ER) and Dual Carrier Modulation (DCM)
- Low-power Wi-Fi idle, standby, and sleep modes
- WPA2/WPA3 security
- Support for Matter over Wi-Fi

1.4 Bluetooth LE 5.4 radio key features

- Bluetooth Low Energy 5.4 certified
- Supports Bluetooth Low Energy 5.2 features
- Bluetooth LE 2 Mbps high speed mode and Long Range operation (125 / 500 kbps)
- Integrated PA / LNA / Switch with up to +15 dBm Tx output
- I2S and PCM audio interface

1.5 Power management

- Integrated Buck switching regulators and LDOs to supply internal power domains
- Independent power modes across applications and radio subsystems
- Individual subsystem wake-up through dedicated GPIO, IRQ, and RTC
- Low-leakage always-on power domain enabling fast wakeup while minimizing sleep/deep-sleep mode power consumption
- Ability to power the entire RW610 using a single 3.3 V external voltage supply with optional 1.8 V external power supply input to VIO

1.6 SDK, tool-kits and middleware

- MCUXpresso SDK
- FreeRTOS open-source kernel and libraries
- lwIP and mbedTLS security middleware
- Trusted Firmware (TF-M) support

1.7 Packaging and operating characteristics

- Package
  - TFBGA145 - 8 x 8 x 1.07 mm, with 0.5 mm ball pitch
  - WLCSP151 - 4.680 x 5.165 x 0.455 mm, with 0.3 mm ball pitch
  - HVQFN116 - 9 x 9 x 0.85 mm, with 0.5 mm pitch
- Operating temperature
  - Industrial: -40°C to 85°C

2 Ordering information

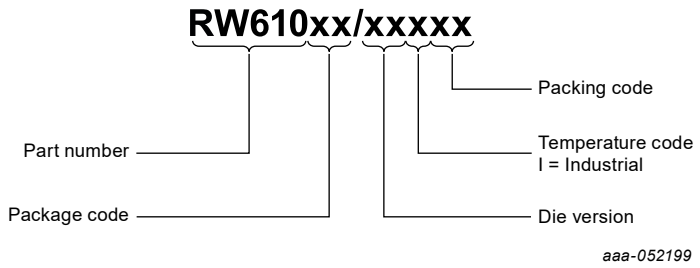


Figure 4. Part numbering scheme

Table 1. Part order codes

Part order code	Package type	Operating temperature range	Packing
RW610HN/A2IK	HVQFN116 - 9 x 9 x 0.85 mm, with 0.5 mm pitch	Industrial	Tray
RW610HN/A2IMP	HVQFN116 - 9 x 9 x 0.85 mm, with 0.5 mm pitch	Industrial	Tape and Reel
RW610ET/A2IK	TFBGA145 - 8 x 8 x 1.07 mm, with 0.5 mm ball pitch	Industrial	Tray
RW610ET/A2IY	TFBGA145 - 8 x 8 x 1.07 mm, with 0.5 mm ball pitch	Industrial	Tape and Reel
RW610UK/A2IZ	WLCSP151 - 4.680 x 5.165 x 0.455 mm with 0.3 mm ball pitch	Industrial	Tape and Reel

3 Microcontroller (MCU)

3.1 Architectural overview

The Arm Cortex-M33 includes two AHB-Lite interfaces, the system bus and the C-code bus. If concurrent operations target different devices, the two core buses are used for simultaneous operations.

A multi-layer AHB matrix connects the CPU and other bus masters to peripherals in a flexible manner that optimizes performance. With AHB matrix, different bus masters can access the peripherals which are on different client ports. Find more information on the multilayer matrix in Section 3.11.1. Connections in the multilayer matrix are shown in Table 3. While the AHB itself supports word, halfword, and byte accesses, not all AHB peripherals need or provide that support.

3.2 Arm Cortex-M33 processor

The Cortex-M33 is a general-purpose 32-bit microprocessor, which offers high performance and very low power consumption.

The Cortex-M33 offers:

- An instruction set based on Thumb®-2
- Low interrupt latency
- Interruptible/continuable multiple load and store instructions
- Automatic states save and restore for interrupts
- A tightly integrated interrupt controller
- Multiple core buses capable of simultaneous accesses
- A floating point unit

The RW610 includes the Armv8-M TrustZone Security Extension that adds security through code and data protection features.

Read more about Cortex-M33 configuration options in the user manual [1].

3.3 Arm Cortex-M33-integrated floating point unit (FPU)

The FPU fully supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between fixed-point and floating-point data formats, and floating-point constant instructions.

The FPU provides a floating-point computation functionality. This functionality is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic, referred to as the IEEE 754 standard.

3.4 Memory protection unit (MPU)

The Cortex-M33 processor has a memory protection unit (MPU) that defines the memory attributes for different memory regions (fine grain memory control). The MPU enables applications to implement security privilege levels by separating code, data, and stack on a task-by-task basis. Such requirements are critical in many embedded applications.

The MPU allows separating processing tasks by:

- Disallowing access to the data of each other
- Disabling access to memory regions
- Allowing memory regions to be defined as read-only
- Detecting unexpected memory accesses that could potentially break the system

The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to eight regions each of which can be divided into eight sub regions.

The Memory Management Fault exception occurs when accesses to memory locations are not defined in the MPU regions, or not permitted by the region setting.

3.5 Nested vectored interrupt controller (NVIC) for Cortex-M33

The NVIC is a part of the Cortex-M33. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

3.5.1 Features

- Controls system exceptions and peripheral interrupts
- Supports up to 129 vectored interrupts
- Eight programmable interrupt priority levels, with hardware priority level masking
- Relocatable vector table
- Non-maskable interrupt (NMI)
- Software interrupt generation

3.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

Table 2. List of interrupts

Number	Name	Interrupt description
0	WDT0	Windowed watchdog timer 0 (WDT0) (Cortex-M33 watchdog)
1	DMA0	Direct memory access (DMA) controller 0 (secure or Cortex-M33 DMA)
2	GPIO_INTA	GPIO interrupt A
3	GPIO_INTB	GPIO interrupt B
4	PIN_INT0	Pin interrupt 0 or pattern match engine slice 0
5	PIN_INT1	Pin interrupt 1 or pattern match engine slice 1
6	PIN_INT2	Pin interrupt 2 or pattern match engine slice 2
7	PIN_INT3	Pin interrupt 3 or pattern match engine slice 3
8	UTICK	Micro-tick timer (UTICK)
9	MRT	Multi-rate timer (MRT). Global MRT interrupts

Table 2. List of interrupts*...continued*

Number	Name	Interrupt description
10	CTIMER0	Standard counter/timer CTIMER0
11	CTIMER1	Standard counter/timer CTIMER1
12	SCT0	SCTimer/PWM
13	CTIMER3	Standard counter/timer CTIMER3
14	Flexcomm0	Flexcomm Interface 0
15	Flexcomm1	Flexcomm Interface 1
16	Flexcomm2	Flexcomm Interface 2
17	Flexcomm3	Flexcomm Interface 3
18	—	—
19	—	—
20	Flexcomm14[1]	Flexcomm Interface 14
21	—	—
22	—	—
23	GFMRT	Free multi-rate timer (MRT). Global MRT interrupts
24	—	—
25	DMIC	Digital microphone (DMIC) and DMIC subsystem
26	WKDEEPSLEEP	Wake-up from deep sleep
27	HYPERVISOR	Hypervisor service software interrupt
28	SECUREVIOLATION	Secure violation
29	HWVAD	Hardware voice activity detector (HWVAD)
30	—	—
31	—	—
32	RTC	Real time clock (RTC) alarm and wake-up
33	—	—
34	—	—
35	PIN_INT4	Pin interrupt 4 or pattern match engine slice 4
36	PIN_INT5	Pin interrupt 5 or pattern match engine slice 5
37	PIN_INT6	Pin interrupt 6 or pattern match engine slice 6
38	PIN_INT7	Pin interrupt 7 or pattern match engine slice 7
39	CTIMER2	Standard counter/timer CTIMER2
40	CTIMER4	Standard counter/timer CTIMER4
41	OS_EVENT_TIMER	OS event timer 0
42	FlexSPI	FlexSPI interface
43	—	—
44	—	—
45	—	—

Table 2. List of interrupts*...continued*

Number	Name	Interrupt description
46	SDIO	The secure digital interface
47	SGPIO_INTA	Secure GPIO (SGPIO) interrupt A
48	SGPIO_INTB	Secure GPIO interrupt B
49	—	—
50	USB	USB
51	—	—
52	—	—
53	—	—
54	DMA1	DMA controller 1 (non-secure)
55	PUF	Physical unclonable function (PUF)
56	POWERQUAD	PowerQuad math coprocessor
57	—	—
58	—	—
59	—	—
60	—	—
61	LCD	LCD interface controller (LCDIC)
62	CAPTIMER	Capture pin input signal timer
63	—	—
64	W2MWKUP_DONE0	Wi-Fi to MCU, wakeup done 0
65	W2MWKUP_DONE1	Wi-Fi to MCU, wakeup done 1
66	W2MWKUP_DONE2	Wi-Fi to MCU, wakeup done 2
67	W2MWKUP_DONE3	Wi-Fi to MCU, wakeup done 3
68	W2MWKUP_DONE4	Wi-Fi to MCU, wakeup done 4
69	W2MWKUP_DONE5	Wi-Fi to MCU, wakeup done 5
70	W2MWKUP_DONE6	Wi-Fi to MCU, wakeup done 6
71	W2MWKUP_DONE7	Wi-Fi to MCU, wakeup done 7
72	W2MWKUP0	Wi-Fi to MCU, wakeup signal 0
73	W2MWKUP1	Wi-Fi to MCU, Wakeup signal 1
74	WL_MCI_INT0	Wi-Fi to MCU interrupt 0
75	WL_MCI_INT1	Reserved for Wi-Fi to MCU
76	WL_MCI_INT2	Reserved for Wi-Fi to MCU
77	WL_MCI_INT3	Reserved for Wi-Fi to MCU
78	WL_MCI_INT4	Reserved for Wi-Fi to MCU
79	WL_MCI_INT5	Reserved for Wi-Fi to MCU
80	WL_MCI_INT6	Reserved for Wi-Fi to MCU
81	WL_MCI_INT7	Reserved for Wi-Fi to MCU

Table 2. List of interrupts*...continued*

Number	Name	Interrupt description
82	B2MWKUP_DONE0	Bluetooth LE to MCU, wakeup done 0
83	B2MWKUP_DONE1	Bluetooth LE to MCU, wakeup done 1
84	B2MWKUP_DONE2	Bluetooth LE to MCU, wakeup done 2
85	B2MWKUP_DONE3	Bluetooth LE to MCU, wakeup done 3
86	B2MWKUP_DONE4	Bluetooth LE to MCU, wakeup done 4
87	B2MWKUP_DONE5	Bluetooth LE to MCU, wakeup done 5
88	B2MWKUP_DONE6	Bluetooth LE to MCU, wakeup done 6
89	B2MWKUP_DONE7	Bluetooth LE to MCU, wakeup done 7
90	B2MWKUP0 ble_mci_irq0	Bluetooth LE to MCU wakeup signal0
91	B2MWKUP1 ble_mci_irq1	Bluetooth LE to MCU wakeup signal 1
92	BLE_MCI_INT0	Bluetooth to MCU interrupt 0
93	BLE_MCI_INT1	Reserved for Bluetooth LE to MCU
94	BLE_MCI_INT2	Reserved for Bluetooth LE to MCU
95	BLE_MCI_INT3	Reserved for Bluetooth LE to MCU
96	BLE_MCI_INT4	Reserved for Bluetooth LE to MCU
97	BLE_MCI_INT5	Reserved for Bluetooth LE to MCU
98	BLE_MCI_INT6	Reserved for Bluetooth LE to MCU
99	BLE_MCI_INT7	Reserved for Bluetooth LE to MCU
100	PIN0_INT	From AON GPIO
101	PIN1_INT	From AON GPIO
102	ELS	EdgeLock subsystem (ELS)
103	ELS_GDET	ELS IRQ line for GDET error
104	ELS_GDET_UM	ELS un-gated latched error (irq line without enable conditioning)
105	PKC_INT	Public key crypto-processor (PKC) interrupt
106	PKC_ERR	PKC error
107	CDOG_INT	Code watchdog timer interrupt
108	GAU_DAC	General analog unit (GAU) digital to analog converter (DAC)
109	GAU_ACOMP_WKUP	GAU analog comparator (ACOMP) wake-up
110	GAU_ACOMP	GAU analog comparator
111	GAU_ADC1	GAU analog to digital converter 1(ADC1)
112	GAU_ADC0	GAU analog to digital converter 0 (ADC0)
113	USIM	Universal subscriber identity module (USIM) interface
114	OTP	One time programmable (OTP) memory interrupt
115	ENET	Ethernet interrupt
116	ENETTIMER	Ethernet timer interrupt
117	PMIP	Power management IP (PMIP) (from PMIP, Vbat brown detector output: 1 for vbat<1.85V)

Table 2. List of interrupts*...continued*

Number	Name	Interrupt description
118	PMIPChange	PMIP change from 1 to 0
119	ITRC	Intrusion and tamper response controller (ITRC) interrupt request
120	—	—
121	—	—
122	—	—
123	TRNG	TRNG interrupt request
124	ACC_C_INT	Advanced high-performance bus (AHB) memory access checker - Cortex-M33 code bus
125	ACC_S_INT	AHB memory access checker - Cortex-M33 sys bus
126	WACC	Wi-Fi is accessed during Wi-Fi 1. power off - 2. under reset - 3. clock off - 4. sleep
127	BACC	Bluetooth LE is accessed during Bluetooth LE 1. power off - 2. under reset - 3. clock off - 4. sleep
128	GDMA	General purpose direct memory access (GDMA) interrupt

[1] Flexcomm 14 is available through GPIO on BGA and WLCSP packages, not on HVQFN package.

3.6 System tick timer (SysTick)

The Arm Cortex-M33 includes a system tick timer (SysTick) that is intended to generate a dedicated SYSTICK interrupt. The clock source for the SysTick can be the free running oscillator (FRO) or the Cortex-M33 core clock.

3.7 PowerQuad coprocessor

The PowerQuad is a hardware accelerator targeting common calculations in DSP applications. With the assistance of the PowerQuad coprocessor, the Cortex-M33 can be freed to perform other tasks. While the PowerQuad is executing the assigned computation task, the Cortex-M33 can prepare the next PowerQuad task, resulting in a pipeline of PowerQuad tasks.

The PowerQuad-enabled low-level math functions are included in the NXP MCUXpresso SDK which supports easy porting of DSP software APIs such as the Arm CMSIS-DSP.

3.8 On-chip static RAM

The RW610 supports 1.2 MB SRAM with separate bus master access for higher throughput and individual power control for low-power operation.

3.9 On-chip ROM

The 256 kB on-chip ROM contains the secure bootloader and the following application programming interfaces (API):

- In-application programming (IAP) and in-system programming (ISP)
- Supports secure booting from UART/I2C/SPI/USB
- OTP API to program the OTP memory
- Random Number Generator (RNG) API

3.10 OTP

The RW610 MCU contains up to 2 kilobyte of one-time-programmable memory used for part configuration, security parameters, and other uses. The OTP contains pre-programmed factory configuration data such as on-chip oscillator calibration values. Customer applications can use the OTP to configure:

- Details of the device operation
- Code signature values
- Aspects of device security
- Debug options
- Boot options

3.11 Memory mapping

The RW610 incorporates several distinct memory regions. The APB peripheral area is 512 kB in size and is divided to allow for up to 64 peripherals. Each peripheral is allocated 4 kB of space simplifying the address decoding. The CPU registers such as NVIC, SysTick, and sleep mode control are in the private peripheral bus.

The Arm Cortex-M33 processor has a single 4 GB address space.

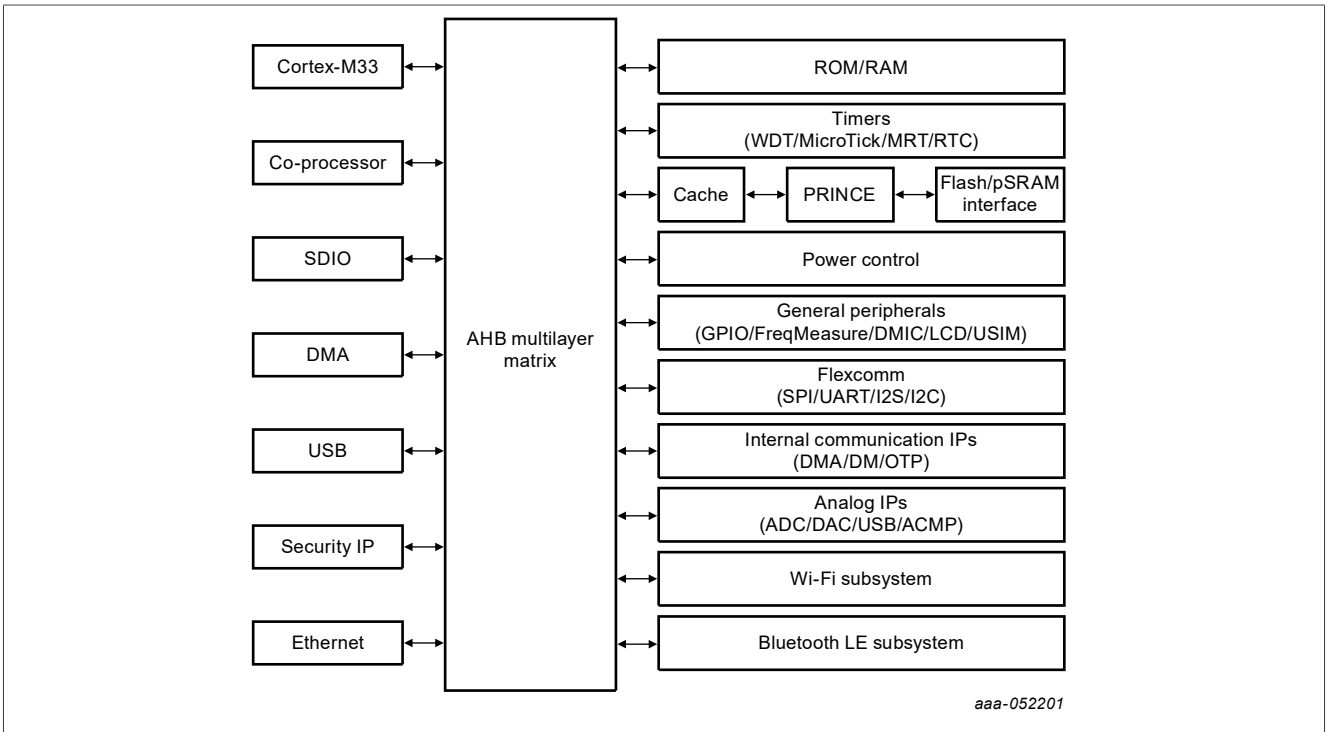


Figure 5. RW610 MCU block diagram

3.11.1 AHB multilayer matrix

The RW610 uses a multi-layer advanced high-performance bus (AHB) matrix to connect the CPU buses and other bus masters to peripherals in a flexible manner that optimizes performance. That is, the RW610 allows different bus masters to access peripherals that are on different client ports of the matrix. Table 3 shows details of the available matrix connections. These are fixed and cannot be turned on or off by software.

Note: *An exception generally occurs when the Cortex-M33 attempts to access unused spaces between the assigned memory and the peripheral spaces.*

Table 3. AHB multilayer matrix

Subsystem	Cortex-M33 C-code bus	Cortex-M33 system bus	PowerQuad	DMA	ELS	USB	PKC	SDIO	Ethernet	GDMA
ROM	√	—	—	—	√	—	√	√	—	—
Cache + PRINCE + FlexSPI flash	√	—	—	—	—	—	—	—	—	—
Cache + PRINCE + FlexSPI pSRAM	—	√	—	√	√	—	—	—	—	√
non-cache + PRINCE + FlexSPI flash	—	√	√	√	√	√	√	√	√	√
SRAM	—	—	√	√	√	√	√	√	√	√
APB peripherals	—	√	—	√	—	—	—	—	—	—
AHB peripherals	—	√	—	√	—	—	—	—	—	—
Wi-Fi subsystem	—	√	—	√	√	√	√	√	√	√
Narrow band subsystem	—	√	—	√	√	√	√	√	√	√
SOC_TOP peripherals	—	√	—	—	—	—	—	—	—	—

3.11.2 TrustZone and Cortex-M33 busing on this device

The implementation of Arm TrustZone on this device involves using the address bit 28 to divide the address space into potential secure and non-secure regions. The address bit 28 is not decoded in the memory access hardware. So each physical location appears in two places on whichever bus they are. Other hardware determines which types of accesses (including non-secure callable) are allowed for any particular address.

In addition, the shared RAM is commonly used for code and data, with different ratios depending on the applications. Some applications may require much code and little data, others may require most of the shared RAM to be used for data. For this reason, the entire shared RAM appears on both the code bus and the data bus of the Cortex-M33. The code can be stored at addresses that are on the code bus. And data can be stored at addresses that are on the data bus. The shared RAM is connected on different AHB matrix client ports. So the code and data contained in the shared RAM can each be accessed simultaneously on the appropriate bus.

Table 4 shows the overall mapping of the code and data buses for secure and non-secure accesses to various device resources.

The “checker” hardware present on all AHB matrix ports confirms the types of access allowed for each peripheral or memory range. The granularity for each port is 32 memory ranges.

Table 4. TrustZone and Cortex-M33 general mapping [1]

Start address	End address	TrustZone [2]	CM-33 bus	CM-33 usage
0x0000 0000	0x0FFF FFFF	Non-secure	Code	Shared RAM, Boot ROM, FlexSPI memory mapped region.
0x1000 0000	0x1FFF FFFF	Secure	Code	Same as above
0x2000 0000	0x2012 FFFF	Non-secure	Data	Shared RAM.
0x3000 0000	0x3012 FFFF	Secure	Data	Same as above
0x4000 0000	0x4500 FFFF	Non-secure	Data	AHB and APB peripherals.
0x5000 0000	0x5500 FFFF	Secure	Data	Same as above

[1] The size shown for peripherals spaces indicates the space allocated in the memory map, not the actual space used by the peripheral.
[2] Selected areas of secure regions may be marked as non-secure callable.

3.11.3 Cortex-M33 memory overview

Table 5 gives a more detailed memory map as seen by the Cortex-M33. The purpose of the four address spaces for the shared RAMs is outlined at the beginning of this chapter. The details of which shared RAM regions are on which AHB matrix client ports can be seen here.

Table 5. Cortex-M33 memory map overview

AHB port	Non-secure start address	Non-secure end address	Secure start address	Secure end address	Function [1]
4	0x0000 0000	0x0001 FFFF	0x1000 0000	0x1001 FFFF	Shared RAM on Cortex-M33 code bus, partitions 0 to 1.
5	0x0002 0000	0x0003 FFFF	0x1002 0000	0x1003 FFFF	Shared RAM on Cortex-M33 code bus, partitions 2 to 3.
6	0x0004 0000	0x0005 FFFF	0x1004 0000	0x1005 FFFF	Shared RAM on Cortex-M33 code bus, partitions 4 to 7.
7	0x0006 0000	0x0007 FFFF	0x1006 0000	0x1007 FFFF	Shared RAM on Cortex-M33 code bus, partitions 8 to 11.
8	0x0008 0000	0x000B FFFF	0x1008 0000	0x100B FFFF	Shared RAM on Cortex-M33 code bus, partitions 12 to 15.
9	0x000C 0000	0x000F FFFF	0x100C 0000	0x100F FFFF	Shared RAM on Cortex-M33 code bus, partitions 16 to 19.
10	0x0010 0000	0x0012 FFFF	0x1010 0000	0x1012 FFFF	Shared RAM on Cortex-M33 code bus, partitions 20 to 23.
0	0x0300 0000	0x0303 FFFF	0x1300 0000	0x1303 FFFF	Boot ROM
1	0x0800 0000	0x0FFF FFFF	0x1800 0000	0x1FFF FFFF	FlexSPI space with cache 0
2	0x2800 0000	0x2FFF FFFF	0x3800 0000	0x3FFF FFFF	FlexSPI mapped space with cache1
3	0x4800 0000	0x4FFF FFFF	0x5800 0000	0x5FFF FFFF	FlexSPI mapped space with non-cache
4	0x2000 0000	0x2001 FFFF	0x3000 0000	0x3001 FFFF	Shared RAM on Cortex-M33 data bus, partitions 0 to 1.
5	0x2002 0000	0x2003 FFFF	0x3002 0000	0x3003 FFFF	Shared RAM on Cortex-M33 data bus, partitions 2 to 3.
6	0x2004 0000	0x2005 FFFF	0x3004 0000	0x3005 FFFF	Shared RAM on Cortex-M33 data bus, partitions 4 to 7.
7	0x2006 0000	0x2007 FFFF	0x3006 0000	0x3007 FFFF	Shared RAM on Cortex-M33 data bus, partitions 8 to 11.
8	0x2008 0000	0x200B FFFF	0x3008 0000	0x300B FFFF	Shared RAM on Cortex-M33 data bus, partitions 12 to 15.
9	0x200C 0000	0x200F FFFF	0x300C 0000	0x300F FFFF	Shared RAM on Cortex-M33 data bus, partitions 16 to 19.
10	0x2010 0000	0x2012 FFFF	0x3010 0000	0x3012 FFFF	Shared RAM on Cortex-M33 data bus, partitions 20 to 23.
11	0x4000 0000	0x4001 FFFF	0x5000 0000	0x5001 FFFF	AHB to APB bridge 0
	0x4002 0000	0x4003 FFFF	0x5002 0000	0x5003 FFFF	AHB to APB bridge 1
12	0x4011 0000	0x4011 FFFF	0x5011 0000	0x5011 FFFF	AHB peripherals
13	0x4012 0000	0x4012 FFFF	0x5012 0000	0x5012 FFFF	AHB peripherals

Table 5. Cortex-M33 memory map overview*...continued*

AHB port	Non-secure start address	Non-secure end address	Secure start address	Secure end address	Function [1]
14	0x4013 0000	0x4013 FFFF	0x5013 0000	0x5013 FFFF	AHB peripherals
15	0x4014 0000	0x4014 FFFF	0x5014 0000	0x5014 FFFF	AHB peripherals
16	0x4015 0000	0x4015 FFFF	0x5015 0000	0x5015 FFFF	AHB peripherals
17	0x4100 0000	0x413F FFFF	0x5100 0000	0x513F FFFF	Wi-Fi peripherals
18	0x4400 0000	0x443F FFFF	0x5400 0000	0x543F FFFF	Bluetooth LE peripherals
19	0x4500 0000	0x4500 FFFF	0x5500 0000	0x5500 FFFF	SOC_TOP peripherals

3.11.4 Shared SRAM detail

Table 6 shows further details of the shared SRAM partitions, address ranges, and corresponding AHB client ports. The Cortex-M33 accesses the shared SRAM through two separate buses: C-AHB and S-AHB. The AHB client ports are only relevant for other bus masters than C-AHB and S-AHB. The other AHB bus masters access the SRAM via the AHB matrix.

An SRAM interface (ICM) is associated with each SRAM partition. ICM arbitrates between C-AHB, S-AHB, and AHB buses with a fixed-priority scheme where:

- Cortex-M33 C-AHB is the highest priority.
- Cortex-M33 S-AHB is the next priority.
- The AHB matrix is the lowest priority.

The partitions shown in Table 6 are mirrored in all four shared SRAM address regions for the Cortex-M33. The purpose of those regions is outlined in Section 3.11.2.

The difference sizes of the shared SRAM partitions provide flexibility when assigning the usage of those spaces. Yet, assigning the code and data to different partitions during the software compilation is strongly recommended. For example, if the code with a size of 132 KB is placed in partitions 0, 1, and 2, do not place the data in these same three partitions.

For each application, the shared SRAM usage should be planned to minimize collision of accesses. Access collisions can occur between Cortex-M33 two buses and other bus masters, including DMA controllers. A best case would be if only one master accesses each shared SRAM partition at any particular time, “ownership” being passed to another master. For instance, when a buffer is filled from a peripheral, an algorithm processes a block of data. To summarize, access collisions can occur under the following conditions:

- On the AHB matrix: when two AHB masters access a resource on the same client port at the same time
- Cortex-M33 accessing the shared SRAM: when the Cortex-M33 and a Matrix master access the same shared SRAM partition at the same time. In this case, the access collision happens at the partition, not at the client port. Since there are multiple partitions for each client port, these partitions are even more opportunities to avoid collisions.

Table 6. Shared SRAM memory map: offsets for all types of shared memory accesses

AHB port	Partition	Start offset	End offset	Size
4	0	0x00 0000	0x00 FFFF	64 kB
	1	0x01 0000	0x01 FFFF	64 kB
5	2	0x02 0000	0x02 FFFF	64 kB
	3	0x03 0000	0x03 FFFF	64 kB
6	4	0x04 0000	0x04 FFFF	64 kB
	5	0x05 0000	0x05 FFFF	64 kB
7	8	0x06 0000	0x06 FFFF	64 kB
	9	0x07 0000	0x07 FFFF	64 kB
8	12	0x08 0000	0x08 FFFF	64 kB
	13	0x09 0000	0x09 FFFF	64 kB
	14	0x0A 0000	0x0A FFFF	64 kB
	15	0x0B 0000	0x0B FFFF	64 kB
9	16	0x0C 0000	0x0C FFFF	64 kB
	17	0x0D 0000	0x0D FFFF	64 kB

Table 6. Shared SRAM memory map: offsets for all types of shared memory accesses*...continued*

AHB port	Partition	Start offset	End offset	Size
	18	0x0E 0000	0x0E FFFF	64 kB
	19	0x0F 0000	0x0F FFFF	64 kB
10	20	0x10 0000	0x10 FFFF	64 kB
	21	0x11 0000	0x11 FFFF	64 kB
	22	0x12 0000	0x12 FFFF	64 kB

3.11.5 APB peripherals

Table 7 provides details of the addresses for the advanced peripheral bus (APB) peripherals. APB peripherals have both secure and non-secure access possibilities.

Table 7. APB peripheral memory map

AHB port	APB bridge	Non-secure base address	Secure base address	Peripheral
11	0	0x4000 0000	0x5000 0000	RSTCTL0: reset control group 0 [1]
	0	0x4000 1000	0x5000 1000	CLKCTL0: clock control group 0[1]
	0	0x4000 2000	0x5000 2000	SYSCTL0: system control group 0[1]
	0	0x4000 3000	0x5000 3000	SYSCTL2: system control group 2
	0	0x4000 4000	0x5000 4000	IOCON: pin function selection and pin control setup
	0	0x4000 6000	0x5000 6000	PUF: physical unclonable function cryptographic key generation
	0	0x4000 7000	0x5000 7000	ELS: EdgeLock subsystem
	0	0x4000 8000	0x5000 8000	USIM: universal subscriber identity module
	0	0x4000 9000	0x5000 9000	PKC: public key crypto-processor
	0	0x4000 A000	0x5000 A000	OTP controller (OCOTP)
	0	0x4000 B000	0x5000 B000	OTP adapter
	0	0x4000 E000	0x5000 E000	Windowed watchdog timer (WWDT)
	0	0x4000 F000	0x5000 F000	Micro-tick timer (UTICK)
	0	0x4001 4000	0x5001 4000	True random number generator (TRNG)

Table 7. APB peripheral memory map*...continued*

AHB port	APB bridge	Non-secure base address	Secure base address	Peripheral
11	1	0x4002 0000	0x5002 0000	Reset control group 1 (RSTCTL1)[1]
	1	0x4002 1000	0x5002 1000	Clock control group 1 (CLKCTL1)[1]
	1	0x4002 2000	0x5002 2000	System control group 1 (SYSCTL1)[1]
	1	0x4002 4000	0x5002 4000	Intrusion and tamper response controller (ITRC)
	1	0x4002 5000	0x5002 5000	GPIO pin interrupts (PINT)
	1	0x4002 6000	0x5002 6000	Input multiplexing controls
	1	0x4002 8000	0x5002 8000	Standard counter/timer 0 (CT32B0)
	1	0x4002 9000	0x5002 9000	Standard counter/timer 1 (CT32B1)
	1	0x4002 A000	0x5002 A000	Standard counter/timer 2 (CT32B2)
	1	0x4002 B000	0x5002 B000	Standard counter/timer 3 (CT32B3)
	1	0x4002 D000	0x5002 D000	Multi-rate timer (MRT)
11	1	0x4002 F000	0x5002 F000	Frequency measure unit.
	1	0x4003 0000	0x5003 0000	Real time clock (RTC) and wake-up timer
	1	0x4003 1000	0x5003 1000	Power management unit (PMU)
	1	0x4003 3000	0x5003 3000	Flexspi_cache0
	1	0x4003 4000	0x5003 4000	Flexspi_cache1
	1	0x4003 8000	0x5003 8000	General analog unit (GAU)
	1	0x4003 B000	0x5003 B000	Secure system configuration
	1	0x4003 F000	0x5003 F000	Multi-rate timer 1 (MRT1)

[1] Reset, clock, and system control functions are separated into 2 groups to allow the possibility of securing group 0 while leaving group 1 unsecured.

3.11.6 AHB peripherals

Table 8 provides details of the addresses for AHB peripherals. AHB peripherals have both secure and non-secure access possibilities.

Table 8. AHB peripheral memory map

AHB port	Non-secure base address	Secure base address	Peripheral
12	0x4010 0000	0x5010 0000	High Speed GPIO (general purpose I/O for port pins that are not selected for some other function by IOCON)
	0x4010 4000	0x5010 4000	DMA0 registers
	0x4010 5000	0x5010 5000	DMA1 registers
	0x4010 6000	0x5010 6000	Flexcomm Interface 0
	0x4010 7000	0x5010 7000	Flexcomm Interface 1
	0x4010 8000	0x5010 8000	Flexcomm Interface 2
	0x4010 9000	0x5010 9000	Flexcomm Interface 3
	0x4010 F000	0x5010 F000	Debug mailbox
13	0x4012 0000	0x5012 0000	CRC Engine
	0x4012 1000	0x5012 1000	DMIC (8-channel PDM digital microphone interface)
	0x4012 6000	0x5012 6000	Flexcomm Interface 14
	0x4012 8000	0x5012 8000	LCD
14	0x4013 4000	0x5013 4000	FlexSPI
	0x4013 8000	0x5013 8000	Ethernet
	0x4013 B000	0x5013 B000	OS Event Timer 0 (for access by Cortex-M33).
	0x4013 C000	0x5013 C000	ROM controller with patch (ROMCP)
15	0x4014 5000	0x5014 5000	USB_OTG
	0x4014 6000	0x5014 6000	SCTimer/PWM
	0x4014 8000	0x5014 8000	Security Control registers (AHB_SECURE_CTRL)
	0x4014 C000	0x5014 C000	Code watchdog timer
	0x4014 E000	0x5014 E000	GDMA
16	0x4015 0000	0x5015 0000	PowerQuad coprocessor
	0x4015 4000	0x5015 4000	Secure GPIO (S_GPIO)
	0x4015 8000	0x5015 8000	SDIO
	0x4015 A000	0x5015 A000	PKC memory interface
	0x4015 C000	0x5015 C000	Always-on memory (aon mem)

3.11.7 SOC_TOP peripherals

Table 9 provides the addresses for SOC_TOP peripherals.

Table 9. SOC_TOP peripherals

AHB port	Non-secure base address	Secure base address	Peripheral
19	0x45000000	0x450003FF	Soc Top AHB arbiter configuration
	0x45000400	0x45000FFF	Reserved
	0x45001000	0x45001FFF	Always-on SoC control (SOC CIU pad control)
	0x45002000	0x45002FFF	Common analog unit (CAU)
	0x45003000	0x450031FF	Reserved
	0x45003400	0x450037FF	SoC OTP
	0x45003800	0x450038FF	SoC test mux
	0x45003900	0x45003FFF	Reserved
	0x45004000	0x450040FF	SoC security sensor control
	0x45004100	0x45004FFF	Reserved
	0x45004400	0x4500FFFF	Reserved

3.11.8 Memory checker

Table 10 lists the mem_rules for client port and the sector definitions.

Table 10. Memory checker

port	client	mem_ rules	address	space	address space msb	sector	each
P0	s0 (boot rom)	Y	0300_0000 0303_FFFF	256KB	17	32	8KB
p1	s0	Y	0800_0000 083F_FFFF	4MB	21	32	128KB
	s1	Y	0840_0000 087F_FFFF	4MB	21	8	512KB
	s2	Y	0880_0000 08FF_FFFF	8MB	22	8	1MB
	s3	Y	0900_0000 09FF_FFFF	16MB	23	8	2MB
	s4	Y	0A00_0000 0BFF_FFFF	32MB	24	8	4MB
	s5	Y	0C00_0000 0C3F_FFFF	4MB	21	32	128KB
	s6	Y	0C40_0000 0C7F_FFFF	4MB	21	8	512KB
	s7	Y	0C80_0000 0CFF_FFFF	8MB	22	8	1MB
	s8	Y	0D00_0000 0DFF_FFFF	16MB	23	8	2MB
	s9	Y	0E00_0000 0FFF_FFFF	32MB	24	8	4MB
p2	s0	Y	2800_0000 283F_FFFF	4MB	21	32	128KB
	s1	Y	2840_0000 287F_FFFF	4MB	21	8	512KB
	s2	Y	2880_0000 28FF_FFFF	8MB	22	8	1MB
	s3	Y	2900_0000 29FF_FFFF	16MB	23	8	2MB
	s4	Y	2A00_0000 2BFF_FFFF	32MB	24	8	4MB
	s5	Y	2C00_0000 2C3F_FFFF	4MB	21	32	128KB
	s6	Y	2C40_0000 2C7F_FFFF	4MB	21	8	512KB
	s7	Y	2C80_0000 2CFF_FFFF	8MB	22	8	1MB
	s8	Y	2D00_0000 2DFF_FFFF	16MB	23	8	2MB
	s9	Y	2E00_0000 2FFF_FFFF	32MB	24	8	4MB
p3	s0	Y	4800_0000 483F_FFFF	4MB	21	32	128KB
	s1	Y	4840_0000 487F_FFFF	4MB	21	8	512KB
	s2	Y	4880_0000 48FF_FFFF	8MB	22	8	1MB
	s3	Y	4900_0000 49FF_FFFF	16MB	23	8	2MB
	s4	Y	4A00_0000 4BFF_FFFF	32MB	24	8	4MB
	s5	Y	4C00_0000 4C3F_FFFF	4MB	21	32	128KB
	s6	Y	4C40_0000 4C7F_FFFF	4MB	21	8	512KB
	s7	Y	4C80_0000 4CFF_FFFF	8MB	22	8	1MB
	s8	Y	4D00_0000 4DFF_FFFF	16MB	23	8	2MB
	s9	Y	4E00_0000 4FFF_FFFF	32MB	24	8	4MB

Table 10. Memory checker*...continued*

port	client	mem_ rules	address	space	address space msb	sector	each
p4	s0	Y	2000_0000 2000_FFFF	64KB	15	32	2KB
	s1	Y	2001_0000 2001_FFFF	64KB	15	32	2KB
p5	s0	Y	2002_0000 2002_FFFF	64KB	15	32	2KB
	s1	Y	2003_0000 2003_FFFF	64KB	15	32	2KB
p6	s0	Y	2004_0000 2004_FFFF	64KB	15	32	2KB
	s1	Y	2005_0000 2005_FFFF	64KB	15	32	2KB
p7	s0	Y	2006_0000 2006_FFFF	64KB	15	32	2KB
	s1	Y	2007_0000 2007_FFFF	64KB	15	32	2KB
p8	s0	Y	2008_0000 2008_FFFF	64KB	15	32	2KB
	s1	Y	2009_0000 2009_FFFF	64KB	15	32	2KB
	s2	Y	200A_0000 200A_FFFF	64KB	15	32	2KB
	s3	Y	200B_0000 200B_FFFF	64KB	15	32	2KB
p9	s0	Y	200C_0000 200C_FFFF	64KB	15	32	2KB
	s1	Y	200D_0000 200D_FFFF	64KB	15	32	2KB
	s2	Y	200E_0000 200E_FFFF	64KB	15	32	2KB
	s3	Y	200F_0000 200F_FFFF	64KB	15	32	2KB
p10	s0	Y	2010_0000 2010_FFFF	64KB	15	32	2KB
	s1	Y	2011_0000 2011_FFFF	64KB	15	32	2KB
	s2	Y	2012_0000 2012_FFFF	64KB	15	32	2KB
P14	s0 (aips)	Y	4013_0000 4013_FFFF	64KB	15	16	4KB
P15	s3 (security)	Y	4014_8000 4014_BFFF	16KB	13	4	4KB
P16	s6 (aon_mem)	Y	4015_A000 4015_DFFF	16KB	13	4	4KB
P17	s1 (wlan_s1)	Y	4138_0000 413F_FFFF	512KB	18	32	16KB
P18	s1 (BLE_s1)	Y	443C_0000 443F_FFFF	256KB	17	32	8KB
P19	s0 (soc_top_s0)	Y	4500_0000 4500_FFFF	64KB	15	32	2KB

3.12 System control

3.12.1 Clock sources

The RW610 supports three internal clock sources and one external clock source:

- Crystal oscillator 40 MHz or 38.4 MHz
- 32 kHz crystal oscillator
- RC 32 kHz internal oscillator
- External clock input pin

3.12.1.1 Crystal oscillator

The main crystal oscillator on the RW610 can be used with crystal frequencies of 40 MHz or 38.4 MHz. The crystal oscillator can be used to drive a PLL to achieve higher clock rates.

One aspect of the oscillator high-gain mode is that a larger voltage swing is used at the crystal pin. This voltage swing gives a higher noise immunity within the oscillator and less edge to edge jitter of the internal clock. When high-gain mode is not required, the power used by the crystal oscillator can be reduced by using low-power mode.

3.12.1.2 32 kHz crystal oscillator

The 32 kHz oscillator resides in the “always-on” domain (AON) and is used to drive the real-time clock (RTC). The crystal oscillator can also be used for other purposes, such as:

- Low-power UART operation
- Main system clock for very low frequency operation

The 32 kHz crystal oscillator has very high accuracy and can be selected as *clk_32k* option after AON_domain reset release, as illustrated in Figure 10.

3.12.1.3 RC 32 kHz internal oscillator

The RC 32 kHz internal oscillator resides in the “always-on” domain and is used as *clk_32k* default option to drive the real-time clock. The RC internal oscillator can also be used for other purposes, such as:

- Low-power UART operation
- Main system clock for very low frequency operation with ± 50% accuracy

3.12.1.4 Internal sleep clock CAU_SOC_SLP_REF_GEN_CLK

The internal sleep clock CAU_SOC_SLP_REF_GEN_CLK(3.84/4M) is generated from CAU and available for use in PM2 stand-by mode. The clock is followed by a divider to create a 32 kHz clock with ±200 ppm accuracy.

3.12.2 System PLLs

The system includes:

- T3 - The PLL provides the 60 MHz, 213.3 MHz, and 256 MHz system clock and 365 MHz clock to FlexSPI.
- TCPU - The PLL provides the 260 MHz clock to Cortex-M33, and the 312 MHz clock to FlexSPI.
- TDDR - The PLL provides the 50 MHz clock to Ethernet and the 400 MHz clock to FlexSPI.

The T3, TCPU and TDDR PLLs can be enabled or disabled individually by software.

3.12.3 PHY PLL

The PLL can be enabled or disabled by software.

3.12.4 Audio PLL

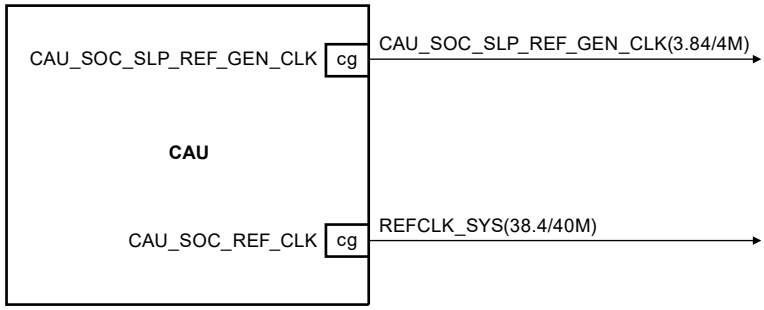
The audio clock generator (AVPLL) consists of a core PLL. The PLL generates clock outputs covering a frequency range of 1.5 GHz to 2.97 GHz. In addition, the AVPLL includes three programmable interpolators (PIs):

- One PI is used inside the PLL
- The remaining two PIs are used for the two output clock channels (C1 and C2). C1 and C2 single-ended output clocks can be programmed as audio clocks.

The PLL can be enabled or disabled by software.

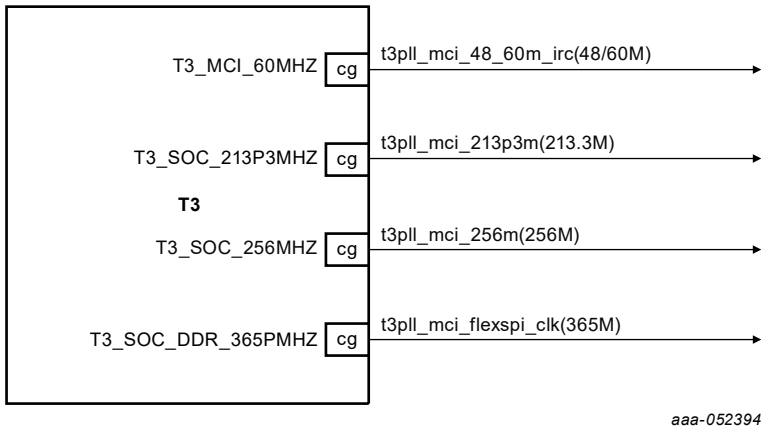
3.12.5 Clock generation

- Figure 6 "Clock generation - CAU"
- Figure 7 "Clock generation - T3 PLL"
- Figure 8 "Clock generation - TCPU PLL"
- Figure 9 "Clock generation - TDDR PLL"
- Figure 10 "Clock generation - AON domain"
- Figure 11 "Clock generation - System PLLs"
- Figure 12 "Clock generation - Ethernet"
- Figure 13 "Clock generation - Flexcomm"
- Figure 14 "Clock generation - Timers"
- Figure 15 "Clock generation - DMIC, FlexSPI, SDU, LCD, USIM, and GAU"
- Figure 16 "Clock generation - Output to pad"



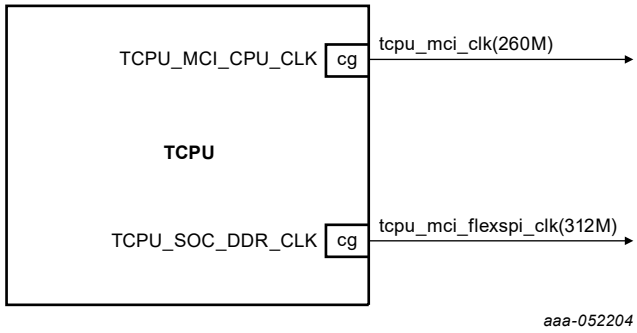
cg means enable the clock or gate/stop the clock

Figure 6. Clock generation - CAU



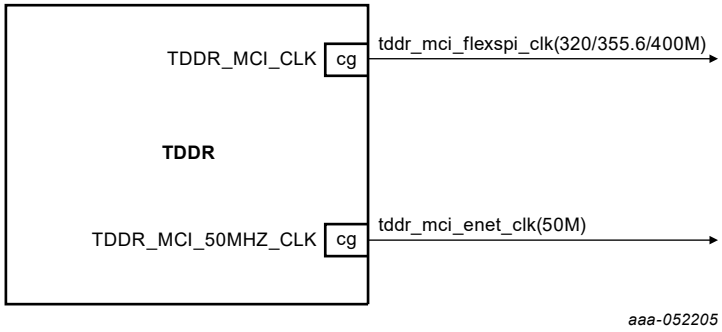
cg means enable the clock or gate/stop the clock

Figure 7. Clock generation - T3 PLL



cg means enable the clock or gate/stop the clock

Figure 8. Clock generation - TCPU PLL



cg means enable the clock or gate/stop the clock

Figure 9. Clock generation - TDDR PLL

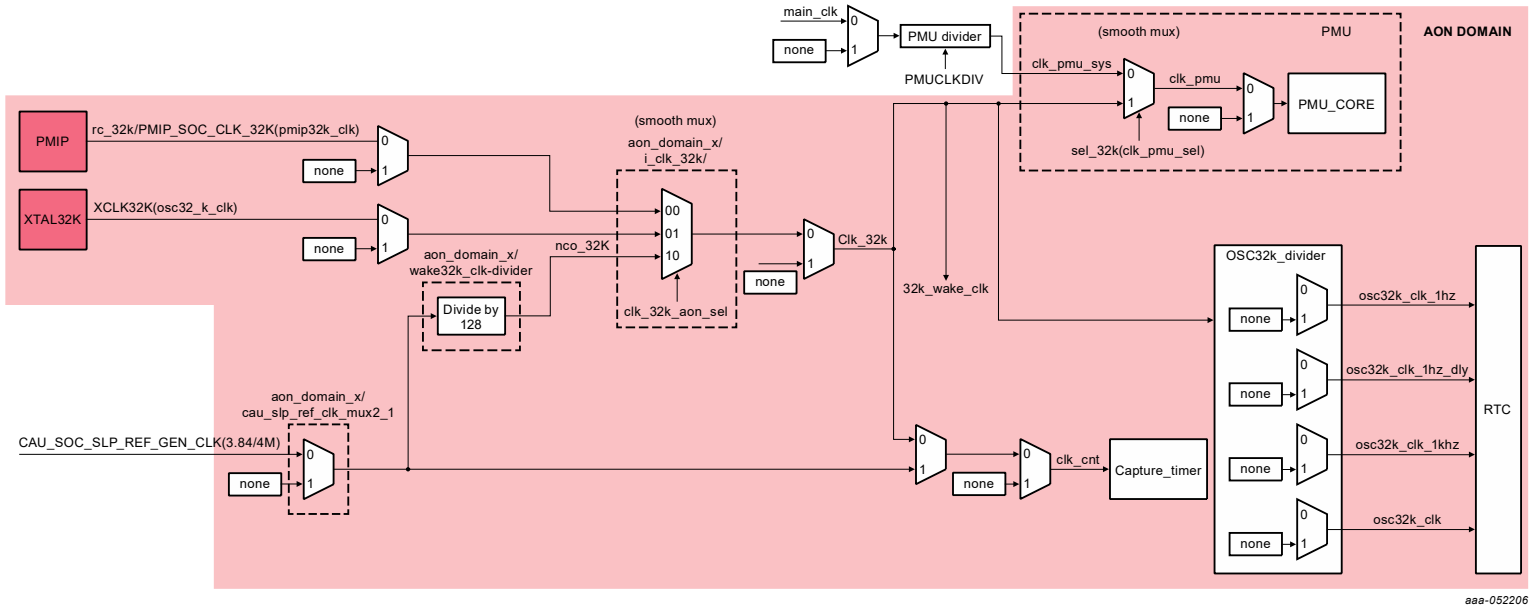


Figure 10. Clock generation - AON domain

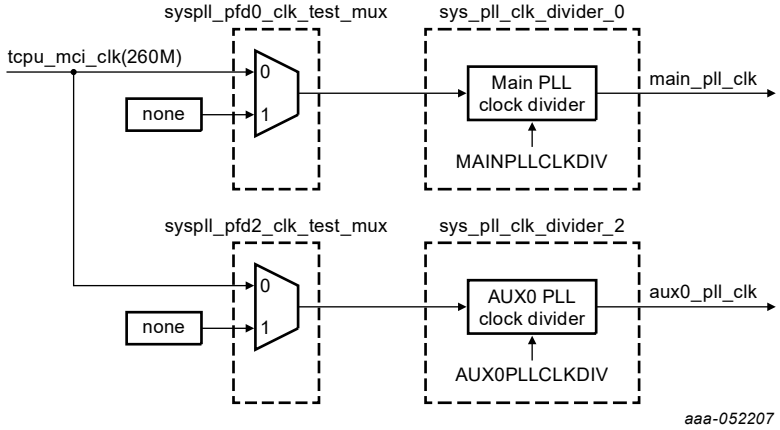
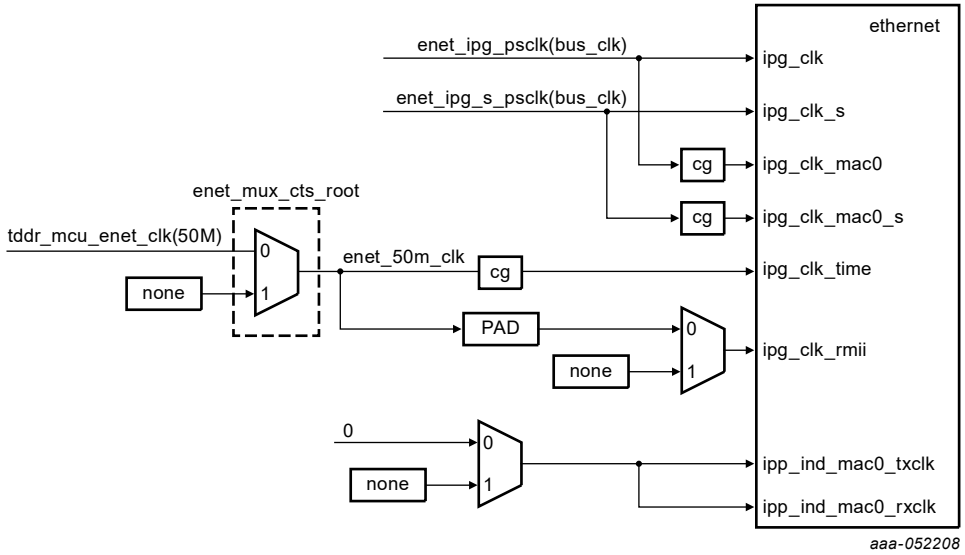


Figure 11. Clock generation - System PLLs



cg means enable the clock or gate/stop the clock

Figure 12. Clock generation - Ethernet

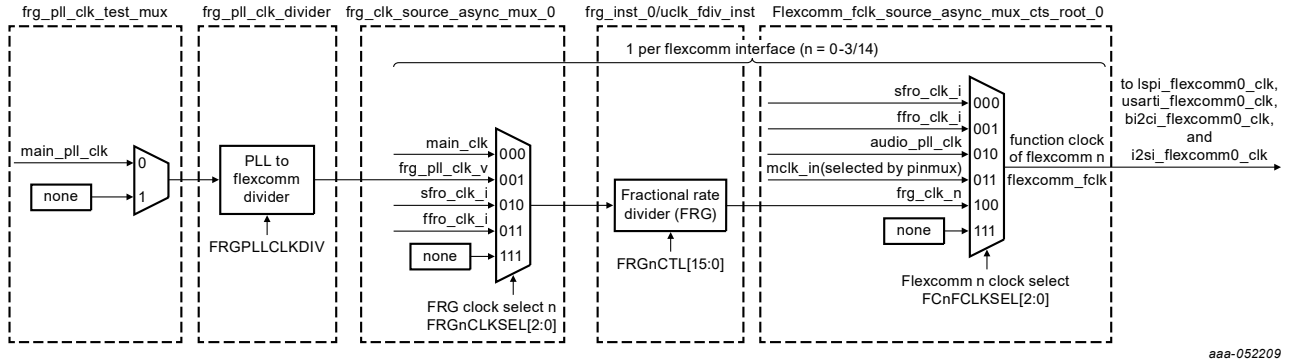


Figure 13. Clock generation - Flexcomm

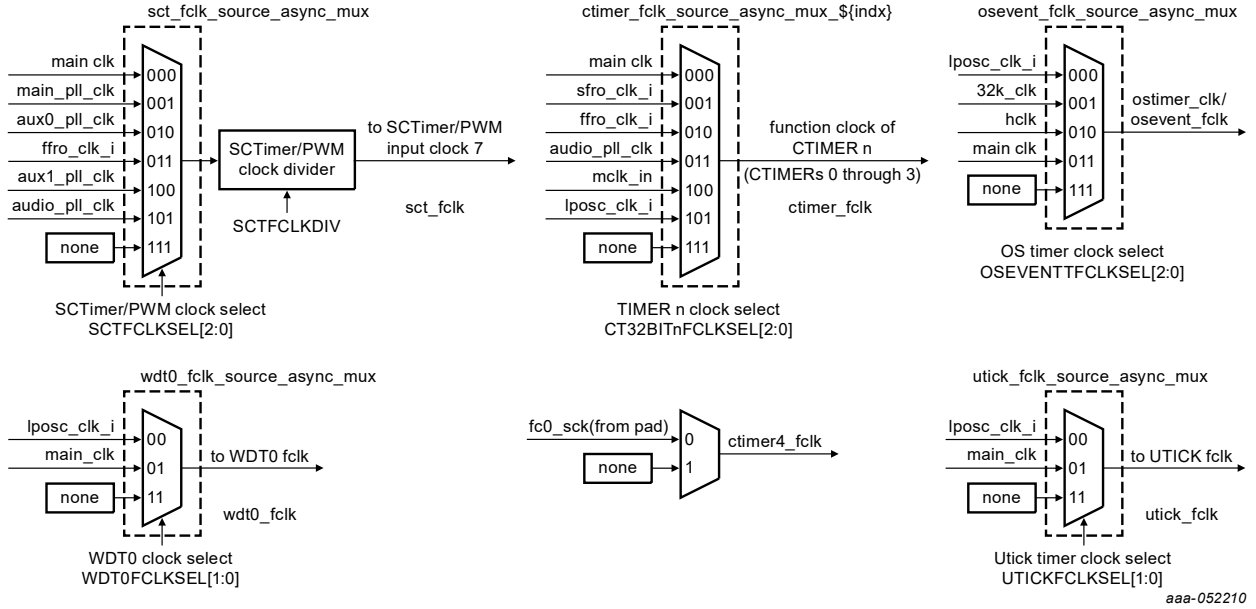


Figure 14. Clock generation - Timers

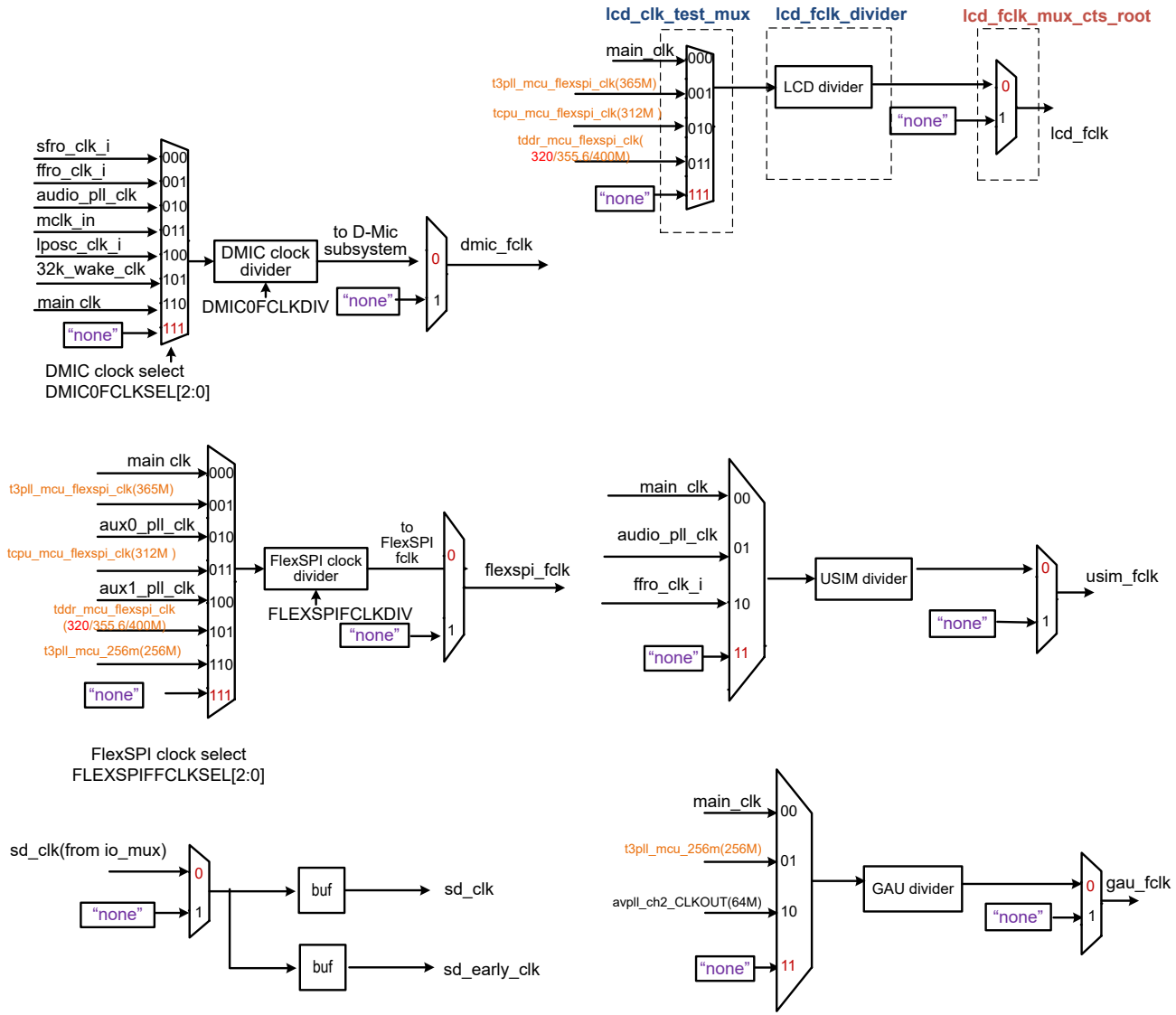


Figure 15. Clock generation - DMIC, FlexSPI, SDU, LCD, USIM, and GAU

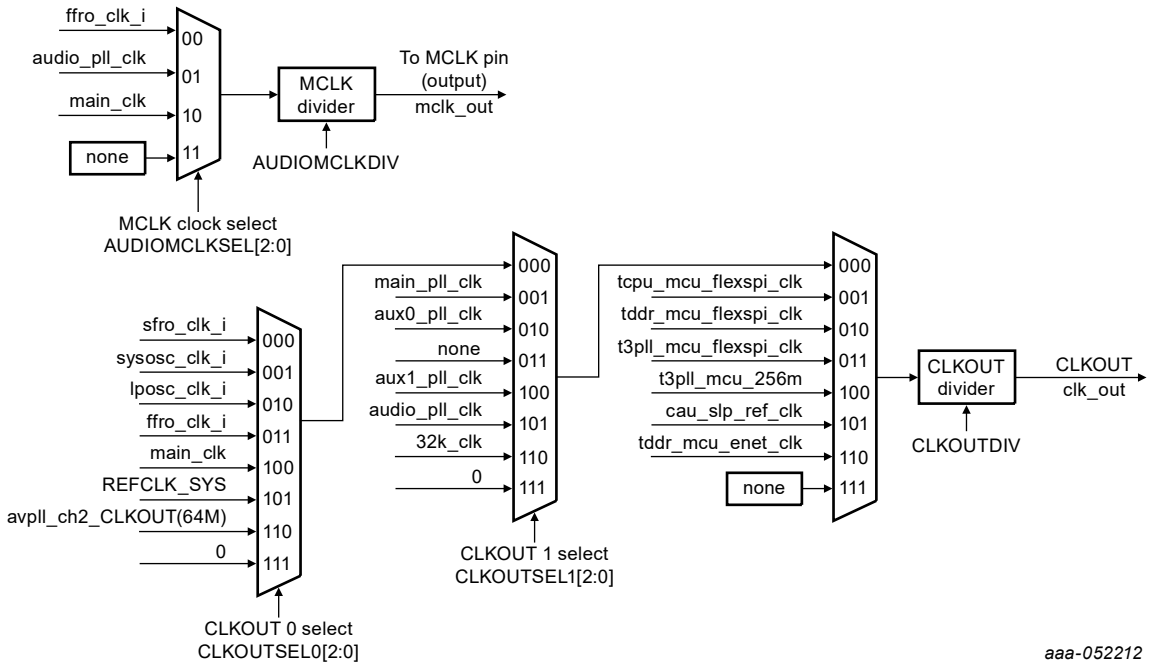


Figure 16. Clock generation - Output to pad

3.12.6 Safety

The RW610 includes a windowed watchdog timer (WWDT), which can be enabled by software after reset. Once enabled, the WWDT remains locked and cannot be modified in any way until a reset occurs.

3.13 Power control

The RW610 supports various power control features. In active mode, when the device is running, power and clocks to selected peripherals can be adjusted for power consumption. In addition, there are individual power-down controls for many (analog) peripherals. Finally, any set of individual shared RAM partitions may be placed in retain/standby mode or powered-off entirely. This selection can be made on a partition-by-partition basis.

In addition, there are three special modes of processor power reduction with different peripherals running: standby mode, sleep mode, and deep-sleep mode that can be activated using the power API library from the SDK software package.

3.13.1 Power structure

Figure 17 illustrates the power structure.

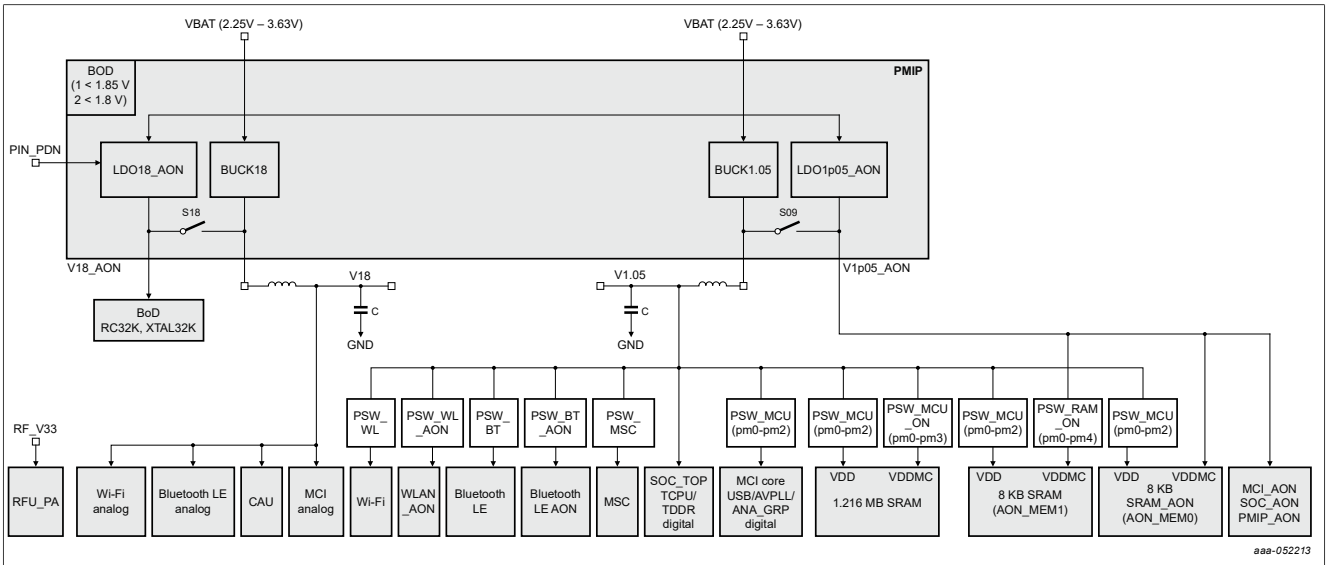


Figure 17. RW610 power structure

3.13.2 PM0 – Active mode

In active mode:

- The MCU is actively running
- The MCU clocks are active and can be scaled to various frequencies depending on application requirement
- SRAM is in active state
- All peripherals are available. The peripheral function clocks can be gated by user via programming
- PLL is running and is the source clock for most of the peripherals
- The analog modules are available and can be powered up by the user via programming

3.13.3 PM1 – Idle mode

The device is powered on. Cortex-M33 is in sleep mode and waits for the interrupt instructions (WFI).

3.13.4 PM2 – Standby mode

In standby mode:

- Cortex-M33 is in sleep with state retained, the clock is gated
- SRAM is in standby state by default
- All peripherals are in retention state except AON domain which is active
- The analog modules are in power-down mode by default
- REFCLK_SYS is gated
- CAU_SOC_SLP_REF_GEN_CLK(3.84/4M) is running (Figure 10. The DMA can use the 1M clock (3.84/4M divided by 4) to transfer data between some peripherals and the memory in PM2 mode.
- T3 PLL clock is gated
- AUD/USB/TCPU PLL power down
- TDDR PLL by default is ON. Can be powered down by software programming if tddr_mci_enet_clk(50M) is gated.
- tddr_mci_enet_clk(50M) exists by default and can be gated by software programming

3.13.5 PM3 – Sleep mode

In sleep mode:

- Cortex-M33 power is removed
- 1.2 MB SRAM is in programmable retention state
- All peripherals are power removed except PMU/RTC/capture pulse which is active
- The on-chip SDIO IP is shut down. SDIO in-band wake-up is not supported in PM3 mode. Out-of-band wake-up of SDIO and other hosts can go through GPIO[24]/GPIO[25].
- AON SRAM is in retention state
- XTAL32K power is programmable, and RC32K is always running
- The analog modules are in power-down mode
- BUCK11 is in sleep mode, (if Wi-Fi and Bluetooth LE are both in sleep/off mode) V11 can be reduced to 0.8 V to retain the state

3.13.6 PM4 – Deep sleep mode

Deep sleep mode is the same as sleep mode (PM3), except that the 1.2 MB SRAM are powered off.

In deep sleep mode:

- 8KB AON SRAM0 is in retention state, and 8KB AON SRAM1 is in Programmable retention state
- BUCK11 is off (if Wi-Fi/ Bluetooth LE are both off), and MCU analog module power is removed
- The on-chip SDIO IP is shut down. SDIO in-band wake-up is not supported in PM4 mode. Out-of-band wake-up of SDIO and other hosts can go through GPIO[24]/GPIO[25].

3.13.7 MCU memory power partition

In sleep mode (PM3), the MCU provides programmable memory retention options.

Table 11. MCU memory power partition

Mem option	AON mem		Static OFF Mem					
Unit	(KB)	(KB)	(KB)	(KB)	(KB)	(KB)	(KB)	(KB)
Power mode	8	8	384	64	64	128	256	320
PM0 PM1	ON	ON	ON	ON	ON	ON	ON	ON
PM2	ON/standby	ON/standby	ON/standby	ON/standby	ON/standby	ON/standby	ON/standby	ON/standby
PM3	RETAIN	RETAIN	RETAIN/ OFF	RETAIN/ OFF	RETAIN/ OFF	RETAIN/ OFF	RETAIN/ OFF	RETAIN/ OFF
PM4	RETAIN	RETAIN/ OFF	OFF	OFF	OFF	OFF	OFF	OFF

3.13.8 Wi-Fi power modes

Wi-Fi has three power modes:

- WPM0 – Active mode
- WPM1 – Sleep/deep-sleep mode
- WPM2 – Power off

Table 12 lists the power mode transitions.

Table 12. Power mode transitions

Mode transition		Management unit
Active to sleep mode	WPM0 to WPM1	Advance power management unit (APU)
Active or sleep/deep-sleep mode to power off	WPM0/WPM1 to WPM2	APU and power management unit (PMU)
Wake up from Sleep/deep-sleep mode	WPM1 to WPM0	APU and PMU
Wake up from power-off mode	WPM2 to WPM0	PMU

3.13.9 Bluetooth LE power modes

Bluetooth LE has three power modes:

- BPM0 – Active mode
- BPM1 – Sleep/deep-sleep mode
- BPM2 – Power off

Go to sleep

BPM0->BPM1 --- APU

Go to power off

BPM0/BPM1->BPM2 --- PMU

Wake up

BPM1->BPM0 --- APU and PMU

BPM2->BPM0 --- PMU

3.14 General-purpose I/O (GPIO)

The RW610 provides GPIO ports with a total of up to 64 GPIO pins (Table 13).

The GPIO registers control the device pins that are not connected to a specific peripheral function. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The current level of a port pin can be read back no matter what peripheral is selected for that pin.

Features

- Accelerated GPIO functions:
  - GPIO registers are in the AHB so that the fastest possible I/O timing can be achieved
  - Mask registers allow treating sets of port bits as a group, leaving other bits unchanged
  - All GPIO registers are byte and halfword addressable
  - An entire port value can be written in one instruction
- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port
- Direction control of individual bits
- All I/O default to inputs after reset
- All GPIO pins can be selected to create an edge or level-sensitive GPIO interrupt request
- A combination of any pin or pins can trigger one GPIO group interrupt

Table 13 lists the number of GPIOs for the three packages.

Table 13. Number of GPIOs for each package

Package	Number of GPIOs	Number of secure GPIOs
TFBGA	64	32
WLCSP	56	24
HVQFN	41	12

3.15 Pin interrupt/pattern engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC. The pattern match engine can be used with the software to create complex state machines based on pin inputs. Any digital pin can be configured through the SYSCON block as an input to the pin interrupt or pattern match engine. And the digital pin configuration is independent of the function selected through the switch matrix. The registers that control the pin interrupt or pattern match engine are in the I/O+ bus for fast single-cycle access.

Features

- Pin interrupts:
  - Up to eight pins can be selected from all GPIO pins on ports 0 and 1 as edge-sensitive or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH-active or LOW-active.
  - Pin interrupts can wake up the device from idle mode and standby mode.
- Pattern match engine:
  - Up to eight pins can be selected from all digital pins on ports 0 and 1 to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each bit slice comprising the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can also be programmed to generate an RXEV notification to the CPU. The RXEV signal can be connected to a pin.
  - Pattern match can be used with the software to create complex state machines based on pin inputs.
  - Pattern match engine facilities wake up only from idle and standby modes.

3.16 Communications peripherals

3.16.1 High-speed USB host/device interface (USB)

The 16-bit USB 2.0 UTMI+ level 3 PHY handles the low-level USB 2.0 protocol and signaling, with functions including:

- Data serialization and de-serialization (provides simple low-frequency parallel system interface)
- Bit-stuffing and unstuffing
- NRZI encoding and decoding
- Clock recovery and synchronization from the received serial bit stream
- Generation of the SYNC and EOP packet fields
- Multi-port and single-port hard macros are supported; multi-port implementations share PLL and reference circuitry to minimize die area
- Optional circuit blocks to support On-The-Go (OTG) and/or Battery Charging detection
- Integrated signal and power pads with ESD protection and protection for DP/DM short to VBUS or GND
- Standard 16-bit/8-bit UTMI+ level 3 transceiver interface enables multiple choices for USB 2.0 controllers; also supports Full-Speed/Low-Speed serial interface mode for legacy controllers
- UTMI interface signals are synchronized to transceiver clock CLK_OUT domain (30 MHz for 16-bit mode, 60 MHz for 8-bit mode)
- Supports 480 Mbps High Speed (HS)/12 Mbps Full Speed (FS)/1.5 Mbps Low Speed (LS), FS only, and LS only serial data transmission rates
- High Speed and Full Speed operation to support the development of dual-mode devices
- Low-power suspend mode supported
- Elastic buffer for receive data to accommodate bit rate differences between connection partners
- Logic to facilitate suspend/resume signaling and remote wake-up detection
- Supports USB 2.0 Test Modes
- Integrated terminations (Full-Speed/Low-Speed/High-Speed, Host/Peripheral)
- Integrated low-jitter PLL to generate higher speed serial data clocks
- Swap DP/DM pads with a register bit
- 480 MHz and 160 MHz clock outputs for other system uses
- Automatic VCO calibration, SQ amplitude calibration, and TX impedance calibration
- Built-in Self-Test loopback modes for basic functional testing at all speeds
- Digital logic portion of PHY supports scan test and extensive digital debug capabilities
- Flexible performance optimization through extensive programmable analog parameters

3.16.1.1 USB controller

The RW610 USB interface includes one USB OTG-capable dual-role host/device controller that is compliant with the USB 2.0 specification. The USB OTG controller integrates one OTG transceiver.

Features

- Full USB OTG functionality with integrated transceiver, allowing support for an Enhanced Host Controller Interface (EHCI) host or a device
- High-Speed/Full-Speed/Low-Speed USB 2.0 Host/Device/OTG mode support
- Up to 8 configurable bidirectional endpoints for device mode. The endpoints can be configured as IN/OUT for control, Interrupt, Bulk, or Isochronous; except endpoint 0 which is always configured for control.
- Control signals for external power supply and detection of voltages for OTG signaling
- Capability to respond as self or bus powered device and control to allow charging from bus
- 2 kB TXFIFO for each endpoint, which can hold the largest USB 2.0 packet.
- 2 kB shared Receive buffer for all incoming data

3.16.2 FlexSPI interface

The flexible serial peripheral interface (FlexSPI) host controller supports up to two SPI channels and up to two external devices. Each channel supports single/dual/quad mode data transfer (1/2/4 bidirectional data lines).

FlexSPI flash interface with 32 kB cache and dynamic decryption for execute-in-place and supports DMA.

FlexSPI pSRAM interface with 32 kB cache and dynamic decryption for execute-in-place and supports DMA.

Features

- FlexSPI is compliant to JEDEC JESD251C for xSPI standard specification
- Flexible sequence engine (LUT table) to support various vendor devices:
  - Serial NOR Flash: all SPI/dual SPI/quad SPI flash devices
  - Serial pSRAM: all SPI/dual SPI/quad SPI flash devices
- Flash access mode:
  - Single/dual/quad
  - SDR/DDR mode
  - Individual mode
- Support sampling clock mode:
  - Internal dummy read strobe looped back internally
  - Internal dummy read strobe looped back from pad
  - Flash provided read strobe
- Automatic data learning to select the correct sample clock phase
- Memory mapped read/write access by AHB
  - AHB RX buffer implemented to reduce read latency. Total AHB RX Buffer size: 128 * 64 bits
  - 16 AHB masters supported with priority for read access
  - Eight flexible and configurable buffers in AHB RX buffer
  - AHB TX buffer implemented to buffer all write data from one AHB burst. AHB TX buffer size: 8 * 64 bits
  - All AHB masters share this AHB TX Buffer. No AHB master number limitation for Write Access.
- Software triggered Flash read/write access by IP bus
  - IP RX FIFO implemented to buffer all read data from External device. FIFO size: 64 * 64 bits
  - IP TX FIFO implemented to buffer all Write data to External device. FIFO size: 128 * 64 bits
  - DMA support to fill IP TX FIFO
  - DMA support to read IP RX FIFO
  - SCLK stopped when reading flash data and IP RX FIFO is full
  - SCLK stopped when writing flash data and IP TX FIFO is empty

3.16.3 SDIO 3.0 interface

SDIO device interface conforms to the industry standard full-speed and UHS-I card specification. The host controller uses the SDIO bus protocol to access RW610 device.

3.16.4 Ethernet interfaces

The MAC-NET core, with a 10/100 MAC, implements layer 3 network acceleration functions. MAC-NET core accelerates the processing of common networking protocols, such as IP, TCP, UDP, and ICMP. Thus, providing wire speed services to client applications.

Features

- Supports all IEEE 1588 features
- Implements the full 802.3 specification with preamble/SFD generation, frame padding generation, CRC generation, and checking
- Supports zero-length preamble
- Dynamically configurable to support 10/100 Mbit/s operation
- Supports configurable half-duplex operation
- Compliant with the AMD magic packet detection with interrupt for node remote power management
- Seamless interface to commercial Ethernet PHY devices via a 2-bit Reduced MII (RMII) operating at 50 MHz
- Simple 64-bit FIFO user-application interface
- CRC-32 checking at full speed with optional forwarding of the frame check sequence (FCS) field to the client
- CRC-32 generation and append on transmit or forwarding of user application provided FCS selectable on a per-frame basis
- In half-duplex mode: provides full collision support, including jamming, back-off, and automatic retransmission
- Supports VLAN-tagged frames according to IEEE 802.1Q
- Programmable MAC address: Insertion on transmit; discards frames with mismatching destination address on receive (except broadcast and pause frames)
- Programmable promiscuous mode support to omit MAC destination address checking on receive
- Multicast and unicast address filtering on receive based on 64-entry hash table, reducing higher layer processing load
- Programmable frame maximum length (support for any standard or proprietary frame length)
- Statistics indicators for frame traffic and errors (alignment, CRC, length) and pause frames. These indicators provide for IEEE 802.3 basic and mandatory management information database (MIB) package and remote network monitoring (RFC 2819)
- Simple handshake user application FIFO interface with fully programmable depth and threshold levels
- Provides a separate status word for each received frame on the user interface providing information such as frame length, frame type, VLAN tag, and error information
- MDIO master interface for PHY device configuration and management with two programmable MDIO base addresses
- Supports legacy FEC buffer descriptors
- Interrupt coalescing reduces the number of interrupts generated by the MAC, reducing CPU loading
- Software-programmable precise time-stamping of ingress and egress frames
- Timer monitoring capabilities for system calibration and timing accuracy management
- Precise time-stamping of external events with programmable interrupt generation
- Programmable event and interrupt generation for external system control
- Supports hardware- and software-controllable timer synchronization.
- Provides a 4-channel IEEE 1588 timer — each channel supports input capture and output compare using the 1588 counter.

3.16.4.1 RMII interface

In RMII receive mode, for normal reception following assertion of CRS_DV, RXD[1:0] is 00 until the receiver determines that the receive event has a proper start-of-stream delimiter (SSD).

The preamble appears (RXD[1:0]=01) and the MACs begin capturing data following detection of SFD.

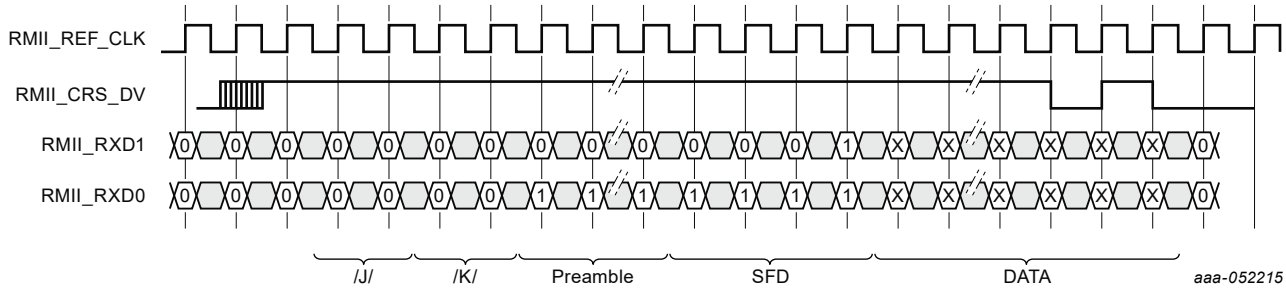


Figure 18. RMII receiver operation

If a false carrier is detected (bad SSD), then RXD[1:0] is 10 until the end of the receive event. This is a unique pattern since a false carrier can only occur at the beginning of a packet where the preamble is decoded (RXD[1:0] = 01).

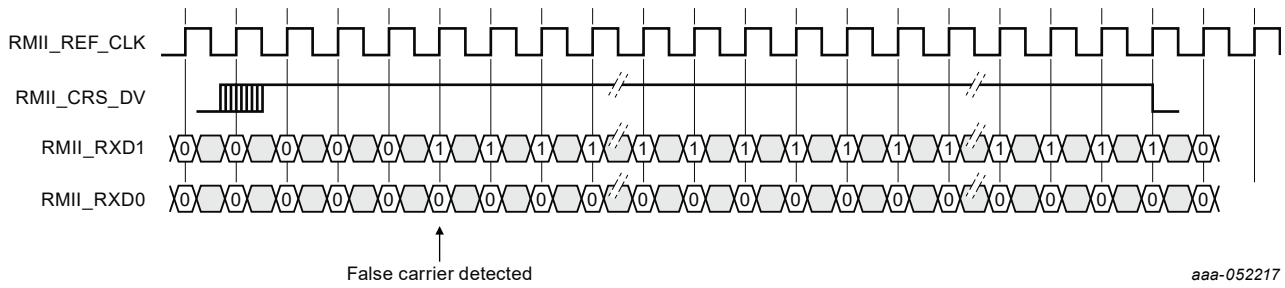


Figure 19. RMII receive operation with false carrier

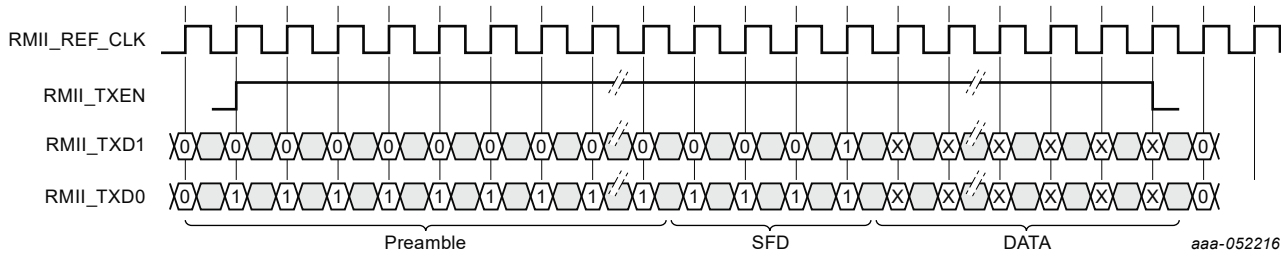


Figure 20. RMII transmit operation

3.16.5 Flexcomm interface serial communication

Features

- USART with asynchronous operation, or synchronous master or client operation
- SPI controller or target, with up to four target selects
- I2C, including separate controller, target, and monitor functions
- I2S functions using Flexcomm
- Data for USART, SPI, and I2S traffic uses the Flexcomm interface FIFO. The I2C function does not use the FIFO.

3.16.5.1 SPI serial I/O controller (Flexcomm interfaces 0 - 3 and 14)

- Maximum supported bit rate for SPI controller mode (transmit/receive) of 30 Mbit/s (excluding delays introduced by external device and PCB)
- Maximum supported bit rate for SPI target mode (transmit/receive) of 30 Mbit/s (excluding delays introduced by external device and PCB)
- Data frames of 1 to 16 bits supported directly. Larger frames supported by software or DMA set-up
- Controller and target operation
- Data can be transmitted to a target without the need to read incoming data - useful while setting up an SPI memory.
- Control information can optionally be written along with data - allows very versatile operation, including “any length” frames.
- Four target-select input/outputs with selectable polarity and flexible usage.
- Activity on the SPI in target mode allows wake-up from deep-sleep mode on any enabled interrupt.

Note: *Texas Instruments SSI and National Microwire modes are not supported.*

3.16.5.2 I2C-bus interface

The I2C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device has a unique address and can operate as either a receiver-only device (for example, an LCD driver) or a transmitter. Devices such as memories can both receive and send information. Transmitters and/or receivers can operate in either controller or target mode. The mode depends on whether the device has to initiate a data transfer or is only addressed. The I2C is a multi-controller bus. That is, more than one bus controller connected to the I2C can control the I2C.

Features

- All I2Cs support standard, Fast-mode, and Fast-mode Plus with data rates of up to 1 Mbit/s
- All I2Cs support high-speed target mode with data rates of up to 3.4 Mbit/s
- Independent controller, target, and monitor functions
- Supports both multi-controller and multi-controller with target functions
- Multiple I2C target addresses supported in hardware
- One target address can be selectively qualified with a bit mask or an address range in order to respond to multiple I2C-bus addresses
- 10-bit addressing supported with software assist
- Supports SMBus.
- Activity on the I2C in target mode allows wake-up from deep-sleep mode on any enabled interrupt

3.16.5.3 USART

Features

- Maximum bit rates in asynchronous mode of 6.25 Mbit/s (excluding delays introduced by external device and PCB)
- Maximum supported bit rate for USART master synchronous mode of 20 Mbit/s (excluding delays introduced by external device and PCB)
- Maximum supported bit rate for USART client synchronous mode of 20.0 Mbit/s (excluding delays introduced by external device and PCB)
- 7, 8, or 9 data bits and 1 or 2 stop bits
- Synchronous mode with master or client operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address comparison
- RS-485 transceiver output enable
- Autobaud mode for automatic baud rate detection
- Parity generation and checking: odd, even, or none
- Software selectable oversampling from 5 to 16 clocks in asynchronous mode
- One transmit and one receive data buffer
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator with auto-baud function
- One fractional rate divider is shared among all USARTs
- Interrupts available for:
  - Receiver Ready
  - Transmitter Ready
  - Receiver Idle
  - Change in receiver break detect
  - Framing error
  - Parity error
  - Overrun
  - Under-run
  - Delta CTS detect
  - Receiver sample noise detected
- Loop-back mode for testing of data and flow control
- In synchronous client mode, wakes up the part from deep-sleep mode
- Special operating mode allows operation at up to 9600 baud using the 32.768 kHz RTC oscillator as the UART clock. This mode can be used while the device is in deep-sleep mode and can wake up the device when a character is received.
- USART transmit and receive functions work with the system DMA controller.

3.16.5.4 I2S-bus interface

The I2S bus provides a standard communication interface for streaming data transfer applications such as digital audio or data collection. The I2S bus specification defines a 3-wire serial bus with one data signal, one clock signal, and one word select/frame trigger signal. The three signals are used for single or dual (mono or stereo) audio data transfer as well as other configurations.

The I2S interface within one Flexcomm Interface provides at least one channel pair that can be configured as a central or a peripheral. Other channel pairs, if present, always operate as peripherals. All of the channel pairs within one Flexcomm Interface share one set of I2S signals. And the channel pairs are configured together for either transmit or receive operation, using the same mode, same data configuration, and frame configuration. All such channel pairs can participate in a time division multiplexing (TDM) arrangement. The cases requiring an MCLK input and/or output are handled outside the I2S block in the system level clocking scheme.

Features

- One Flexcomm interface may implement one or more I2S channel pairs. The first pair could be a central or a peripheral, and the rest of the channel pairs would be peripherals. All channel pairs are configured together for either transmit or receive and other shared attributes. The number of channel pairs is defined for each Flexcomm interface, and may be from 0 to 4.
- Configurable data size for all channels within one Flexcomm interface, from 4 bits to 32 bits. Each channel pair can also be configured independently to act as a single channel (mono as opposed to stereo operation).
- All channel pairs within one Flexcomm interface share a single bit clock (SCK) and word select/frame trigger (WS), and data line (SDA).
- Data for all I2S traffic within one Flexcomm interface uses the Flexcomm interface FIFO. The FIFO depth is 8 entries.
- Left-justified and right-justified data modes.
- DMA support using FIFO level triggering.
- Time division multiplexing (TDM) with several stereo slots and/or mono slots is supported. Each channel pair can act as any data slot. Multiple channel pairs can participate as different slots on one TDM data line.
- The bit clock and WS can be selectively inverted.
- Supported sampling frequencies depend on the specific device configuration and applications constraints such as system clock frequency and PLL availability. But standard audio data rates are supported. See the data rates section in I2S chapter in the RT6xx user manual for clock and sample rate calculations.

3.17 Counter/timer peripherals

3.17.1 General-purpose 32-bit timers/external event counter

The RW610 includes five general-purpose 32-bit timer/counters.

The timer/counter is designed to count cycles of the system derived clock or of an externally supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

Features

- A 32-bit timer/counter with a programmable 32-bit pre scaler
- Counter or timer operation
- Up to four 32-bit captures can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt. The number of capture inputs for each timer that are available on device pins may vary by device
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match
  - Stop timer on match with optional interrupt generation
  - Reset timer on match with optional interrupt generation
  - Shadow registers are added for glitch-free PWM output
- Each timer has up to four external outputs that relate to the match registers, with the following capabilities:
  - Set LOW on match
  - Set HIGH on match
  - Toggle on match
  - Do nothing on match
- Up to two match registers can be used to generate timed DMA requests
- The timer and pre scaler can be configured so they are cleared on a designated capture event. This feature permits easy pulse width measurement:
  - The timer is cleared on the leading edge of an input pulse.
  - The timer value is captured on the trailing edge.
- Up to four match registers can be configured for PWM operation, allowing up to three single edged controlled PWM outputs.

3.17.2 Windowed watchdog timer (WWDT)

If the software fails to service the controller periodically within a programmable window, the watchdog resets the controller.

Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled
- If enabled, incorrect feed sequence causes reset or interrupt
- Flag to indicate watchdog reset
- Programmable 24-bit timer with internal pre scaler
- Selectable time period from ($T_{cy(WDCLK)}$ × 256 × 4) to ($T_{cy(WDCLK)}$ × 2^24 × 4) in multiples of $T_{cy(WDCLK)}$ × 4.
- The watchdog clock (WDCLK) runs at 1 MHz

3.17.3 SCTimer/PWM

The SCTimer/PWM allows a wide variety of timing, counting, output modulation, and input capture operations. The inputs and outputs of the SCTimer/PWM are shared with the capture and match inputs/outputs of the 32-bit general-purpose counter/timers.

The SCTimer/PWM can be configured as two 16-bit counters or a unified 32-bit counter. In the two-counter case, in addition to the counter value the following operational elements are independent for each half:

- State variable
- Limit, halt, stop, and start conditions
- Values of match/capture registers, plus reload or capture control values

In the two-counter case, the following operational elements are global to the SCTimer/PWM, but the last three can use match conditions from either counter:

- Clock selection
- Inputs
- Events
- Outputs
- Interrupts

Features

- Two 16-bit counters or one 32-bit counter
- Counter clocked by bus clock or selected input
- Up counter or up-down counter
- State variable allows sequencing across multiple counter cycles
- Event combines input or output condition and/or counter match in a specified state
- Events control outputs, interrupts, and the SCTimer/PWM states
  - Match register 0 can be used as an automatic limit.
  - In bidirectional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- Selected events can limit, halt, start, or stop a counter
- Supports:
  - 8 inputs
  - 10 outputs
  - 16 match/capture registers
  - 16 events
  - 32 states
- PWM capabilities including dead time and emergency abort functions

3.17.4 Real-time clock (RTC) timer

The RTC timer is a 32-bit timer which counts down from a preset value to zero. At zero, the preset value is reloaded and the counter continues. The RTC timer uses the 32.768 kHz clock input to create a 1 Hz or 1 kHz clock.

3.17.5 Multi-rate timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

Features

- 24-bit interrupt timer
- Four channels independently counting down from individually set values
- Repeat and one-shot interrupt modes

3.17.6 OS/EVENT timer

An OS/EVENT timer module provides a common timebase for event synchronization and time-stamping.

The OS/EVENT timer includes:

- A shared, free-running counter
- Match and capture registers

The shared and local counters in OS/EVENT timer module are implemented using Gray code. With this implementation, the processing domains can read the counters asynchronously.

The main counter in the OS/EVENT timer module begins counting immediately following power-up. And it continues counting through any subsequent system resets (except those resets caused by a new POR).

Features

- 64-bit Gray code counter. Using Gray code means that the timer can run at a frequency unrelated to the CPU clock. Gray code is a reflected binary code that changes in a single bit position for each increment.
- Functions:
  - A capture register can copy the main counter value when triggered by a CPU request
  - A match register can be compared to the main counter and can optionally generate an interrupt or wake-up event

3.17.7 MicroTick timer

A 32-bit MicroTick timer that runs at 1 MHz. This timer can wake up the device from reduced power modes up to deep-sleep, with extremely low power consumption. The MicroTick timer has an added timestamp feature in the form of four capture registers.

Features

- Ultra simple, ultra-low power timer that can run and wake up the device in reduced power modes other than deep power-down
- Write once to start
- Interrupt or software polling
- External pin transitions can trigger the four capture registers

3.18 Other digital peripherals

3.18.1 SDMA controller

The DMA controller allows peripheral-to memory, memory-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional DMA transfers for a single source and destination.

Two identical DMA controllers are provided on the RW610. The user may elect, for example, to dedicate one DMA controller for secure processing and the other DMA controller for non-secure applications.

Features

- One channel per on-chip peripheral direction: typically one for input and one for output for most peripherals
- On-chip or off-chip events can optionally trigger DMA operations
- Priority is user selectable for each channel
- Continuous priority arbitration
- Address cache
- Efficient use of data bus
- Supports single transfers up to 1,024 words
- Address increment options allow packing and/or unpacking data

3.18.2 GDMA controller

RW610 has a dedicated four-channel GDMA controller that supports memory-to-memory transactions. Each DMA stream provides unidirectional DMA transfers for a single source and destination.

There are two FIFOs in GDMA: FIFO_01 and FIFO_23. Burst transfer is supported.

- Flash channel 0 --- share FIFO_01
- PSRAM channel 1 --- share FIFO_01
- Wi-fi TX channel 2 --- share FIFO_23
- Wi-fi RX channel 3 --- share FIFO_23

3.18.3 DMIC subsystem

Features

- Pulse-density modulation (PDM) data input for left and/or right channels on one or two buses
- Flexible decimation
- 16-entry FIFO for each channel
- DC blocking or unaltered DC bias can be selected.
- Data can be transferred using DMA from deep-sleep mode without waking up the CPU, then automatically returning to deep-sleep mode
- Data can be streamed directly to I2S on Flexcomm interfaces 0 to 3 and 14

3.18.4 CRC engine

The cyclic redundancy check (CRC) generator with programmable polynomial settings supports several CRC standards commonly used. To save system power and bus bandwidth, the CRC engine supports DMA transfers.

Features

- Supports three common polynomials CRC-CCITT, CRC-16, and CRC-32
  - CRC-CCITT: x16 + x12 + x5 + 1
  - CRC-16: x16 + x15 + x2 + 1
  - CRC-32: x32 + x26 + x23 + x22 + x16 + x12 + x11 + x10 + x8 + x7 + x5 + x4 + x2 + x + 1
- Bit order reverse and one's complement programmable setting for input data and CRC sum
- Programmable seed number setting
- Supports CPU PIO or DMA back-to-back transfer
- Accept any size of data width per write: 8, 16 or 32-bit
  - 8-bit write: 1-cycle operation.
  - 16-bit write: 2-cycle operation (8-bit x 2-cycle).
  - 32-bit write: 4-cycle operation (8-bit x 4-cycle).

3.18.5 LCD

The LCD controller supports:

- Tearing Effect Signal to eliminate tearing effect
- DMA transmission
- Intel 8080 interface with a maximum clock frequency of 16 MHz (WR), and 8 MHz (RD)
- Three- or four-wire SPI interface with a maximum clock frequency of 32 MHz[1]

1 FPS is calculated as:

$$FPS = \frac{(clock\ \ frequency \times data\_pin\_numbers)}{(\text{image\_resolution} \times \text{bit\_per\_pixel})}$$

Example of FPS calculation when the image resolution is 320 * 240 and RGB565: $FPS = \frac{(32M \times 1)}{(320 \times 240 \times 16)} = 26$

Refer to Figure 15 for the clock source and LCD clock divider (N).

3.18.6 USIM

The Universal Subscriber Identity Module Interface, USIM _IF, is a primary device and communication interface for a GSM mobile handset. The USIM interface supports communication with smart cards as specified in:

- The standard ISO 7816-3
- The technical specification 3G TS 31.101 of the Third-Generation Partnership Project

Smart cards are used in many applications and the GSM network USIM card is only one of many applications. Smart cards usually consist of a CPU, Flash memory, and a serial-communication interface device similar to the one described in this chapter. More sophisticated cards contain PLL for frequency enhancement. Encryption accelerators can also exist in a smart card since many of their applications are security-oriented. In all smart card applications, the physical layer and data link layer are identical, so this module may serve them as well.

Software controls the session between the USIM_ IF and the card by updating the USIM_ IF registers. For example, read/write operations to the USIM_IF registers accomplish the following:

- Choosing protocol type and parameters
- Receiving or sending a byte to/from the card
- Activating/deactivating the card
- Setting transmitter/receiver baud rates

Transforming byte convention (inverse to direct and vice versa, according to the session convention) is performed within the USIM_IF. Hence, software does not have to perform format inversion before character receipt. The USIM_IF provides the functionality to support the above standards but the software must ensure that the standards are met.

3.18.7 ITRC

The intrusion and tamper response controller (ITRC) is used to configure the response action for an intrusion event. The on-chip security sensors detect the intrusion event. A device performs an intrusion response to prevent:

- The misuse of the device, or
- The disclosure of critical assets

Critical assets such as cryptographic keys, and/or personal data are generated or stored within the device.

Either a signal from an on-chip sensor—designed to detect that the device is in a threat condition—, or a software command trigger the response mechanism.

The intrusion response erases (zeroizes) all the memory locations that contain cryptographic keys, passwords, or other critical assets. So, any critical asset is protected from disclosure to hostile entities. The response must also prevent the device from being misused while in the threat condition. It does so by inhibiting authentication, key management, and cryptographic services from being initiated. The response action must be completed quickly enough to prevent the threat from compromising the integrity of the device. Hence a configurable hardware module must be defined on secure MCUs.

3.18.8 Peripheral input multiplex

The following peripherals feature an input multiplex, so they can select more input sources:

- SCTimer
- GPIO
- DMA0
- DMA1
- Timer0/1/2/3
- Frequency measurement

3.19 Analog peripherals

3.19.1 Analog digital converter (ADC)

The RW610 ADC is a 2-step converter with up to 16-bit resolution. The ADC includes an analog multiplexer (AMUX) and a programmable gain amplifier (PGA) with as many as eight individually configurable channels, and a reference voltage regulator. The conversion results can be written to the memory through the DMA. Several modes of operation are available.

Features

- Selectable throughput rates and resolution (12 to 16 bits)
- Throughput rate as fast as 2 MHz
- Single-ended and differential conversions from 8 external and 6 internal sources
- ADC gain setting support: 1x, 2x
- Additional PGA setting support: 4x, 8x, 16x, 32x
- Selectable reference voltage (Vref)
  - Internal reference 1.2V (Vref_12)
  - Vref_18
  - External reference (do not exceed 1.8V)
- Input voltage ranges (differential)
  - Vref/PGA to + Vref/PGA
  - Do not exceed VDDIO_6 voltage level
- Offset and gain auto calibration
- Embedded temperature sensor with internal or external diode options
- DAC dual inputs
- Sequences with scan length up to 16
- Sequential conversion composed of any channel in any order
- 1-shot or continuous mode
- Scan average of 1, 2, 4, 8, 16
- Interrupt generation and/or DMA request
- Internal GPT trigger on ADC conversion
- Battery measurement capability
- 2-bit conversion rate of 5.0 Msamples/s. Options for reduced resolution at higher conversion rates.
- Burst conversion mode for single or multiple inputs.
- Synchronous or asynchronous operation. Asynchronous operation maximizes flexibility in choosing the ADC clock frequency, Synchronous mode minimizes trigger latency and can eliminate uncertainty and jitter in response to a trigger.

3.19.2 Digital analog converter (DAC)

The RW610 integrates a register string-based DAC with true 10-bit resolution. The DAC includes two channels. Each channel can output a single-ended signal or combine both channels to output a differential signal.

- 10-bit resolution
- Throughput rate as fast as 2 µs (500 kHz)
- Capable of directly driving a piezo speaker with 5 kΩ load
- Flexible waveform generator (sinusoidal, triangle, noise, and so forth) at various frequency ranges
- Selectable output mode: single-ended or differential
- Internal or external reference voltage
- Interrupt generation and/or DMA request
- Three selectable output ranges
- Supports event trigger from GPT or GPIO

3.19.3 Analog comparator

The RW610 has two analog identical comparators, ACOMP0 and ACOMP1. The comparators are designed to have true rail-to-rail inputs and operate over the full voltage range of the power supply IO voltage. The comparator outputs are latched and can be used as interrupts.

3.20 Security features

The security system on RW610 uses hardware blocks and ROM code to implement the security features of the device.

Features

- Arm TrustZone-M
- EdgeLock subsystem (ELS)
- Public-key cryptocoprocessor (PKC)
- Physically unclonable function (PUF)
- Code watchdog
- PRINCE-GCM based memory encryption and authentication for external Flash and PSRAM

The processor or the DMA engine can access all the components of the system to encrypt or decrypt data and for hashing.

The ROM is used for secure boot in addition to supporting various security functions.

3.20.1 EdgeLock subsystem (ELS)

The EdgeLock subsystem (ELS) is a hardware module that supports a range of security functions such as cryptographic operations, key management, and random number generation.

Features

- AES 128/192/256 ECB, CBC, CTR data encryption
- GCM 128/192/256
- SHA-2 224/256/384/512 secure hash
- CMAC 128/256
- HMAC 256
- ECC P-256 operations (ECDSA, ECDH)
- SP800-90 compliant TRNG and DRBG (using AES CTR 128)
- AES keywrap (RFC3394)
- Key management functions including generation, derivation, storage, and protection

3.20.2 Public-key cryptocoprocessor (PKC)

The public-key cryptocoprocessor (PKC) is a hardware accelerator that provides hardware acceleration for a wide range of RSA and ECC asymmetric cryptographic operations.

The supported operations are:

- EdDSA
- ECDSA 192-521 secp521r1
- ECDSA 192-256 secp256k1
- ECDSA 160-512 brainpool
- RSA 2048-4096 PSS

3.20.3 Physically unclonable function (PUF)

A physically unclonable function (PUF) is a digital fingerprint that serves as a unique identity for a semiconductor device. The RW610 includes a ring-oscillator-based PUF design that provides a unique identity for each device while highly resistant to cloning and reverse engineering.

3.20.4 Code watchdog

The Code watchdog provides two main mechanisms for detecting fault attacks, or execution of unexpected instruction sequences.

- Secure counter (SEC_CNT): Detects altered software execution flow.
  - The software loads the initial value to this counter, then issues ADD and SUB commands to increment/decrement the counter.
  - Periodically, the software requests a secure counter value check by passing the expected value to the CW-DOG using the STOP and RESTART commands.
  - A mismatch between the internal secure counter, and the value passed by the software, indicates that side channel attacks have altered the expected execution flow.
- Instruction timer (INST_TIMER): Places a hard upper-limit on the interval between checks of the secure counter.
  - The START command loads the internal decrementing secure counter. Before the counter underflows (reaches 0), a STOP or RESTART command must be executed, which forces the secure counter check.

3.20.5 PRINCE-based memory encryption for external Flash and PSRAM

The Prince GCM function is integrated into the FlexSPI interface on RW610. The GCM function uses the Prince encryption algorithm to provide both encryption and authentication for up to sixteen independently configurable areas in the external flash memory and PSRAM memory.

4 Wi-Fi subsystem

4.1 IEEE 802.11 standards

- 802.11ax 1x1 SU OFDMA and MU-MIMO
- 802.11ac Wave 1/2
- 802.11n/a/g/b
- 802.11e quality of service
- 802.11i enhanced security
- 802.11k radio resource measurement
- 802.11v Basic Service Set (BSS) Transition Management (BTM) for frame transmission and/or reception
- 802.11w protected management frames
- Fully supports clients (stations) implementing IEEE Power Save mode
- 802.1X Wi-Fi security and authentication

4.2 Wi-Fi MAC

- 802.11ax 1x1 MU-MIMO MAC
- Trigger frame formats
  - Basic trigger frame
  - MU-BAR, MU-RTS, Beamforming Report Poll (BFRP), BSR Poll (BSRP) trigger variant
  - Trigger frame MAC padding
- HE Variants of HT Control
  - Basic format
  - UL Power Headroom
  - Receive Operation Mode control sub-field
- HE MU Frame Exchange Sequences
- MU Acknowledgment (ACK)
- M-BA and C-BA Variants in BA Frames
- Target Wake Time Scheduling
- HE Dual-NAV
- UL Carrier Sensing
- Buffer Status Reports in response to BSRP trigger frame
- Operating Mode Indication (OMI)
- Multiple-BSS/Station
- A-MPDU Rx (de-aggregation) and Tx (aggregation) (supports single-MPDU A-MPDU)
- Management information base counters

4.3 Wi-Fi baseband

- 802.11ax 1x1 baseband, backward compatible with 802.11ac/n/a/g/b technology
- Bandwidth support
  - 20 MHz
- Modulation and coding schemes (MCS)
  - 802.11ax—MCS0~9
  - 802.11ac—MCS0~8
  - 802.11n—MCS0~7
  - Dual sub-carrier modulation (DCM)
    - MCS0
  - BCC coding
- Frame formats
  - 802.11ax HE_SU (Tx/Rx)
  - 802.11ax HE_MU (Rx)
  - 802.11ax HE_ER_SU (Tx/Rx)
  - 802.11ax HE_TB (Tx)
  - 802.11ac VHT
  - 802.11n HT
  - 802.11a
  - 802.11g
  - 802.11b
  - Channel state information (CSI)
- Uplink MU-MIMO and OFDMA Tx as STA
- Downlink MU-MIMO and OFDMA Rx as STA
- Aggressive packet extension
- Extended range (ER)
- Target wake time (TWT)
- Dual carrier modulation (DCM)
- Receiver beam change
- Guard interval (GI) modes
  - 1x HE-LTF with 0.8 us GI
  - 1x HE-LTF with 1.6 us GI (for UL TB PPDU)
  - 2x HE-LTF with 0.8 us GI
  - 2x HE-LTF with 1.6 us GI
  - 4x HE-LTF with 3.2 us GI
- Optional 802.11ac and 802.11n MIMO features:
  - 20 MHz coexistence with middle-packet detection (GI detection) for enhanced clear channel assessment (CCA)
  - Short guard interval (0.4 us)
  - RIFS on receive path for 802.11n packets
  - VHT MU-PPDU (receive)
- Spectral intelligence
  - Spectrum monitoring
  - Interference identification/classification
- Power save features

4.4 Wi-Fi radio

- 5 GHz and 2.4 GHz Wi-Fi band operation
- 802.11ax 1x1 on-chip RF radio
- Integrated PA, LNA and T/R switch

4.5 Wi-Fi encryption

- Data Frame Encryption/Decryption
  - WPA2/WPA3 personal and enterprise
  - AES/CCMP
  - AES/GCMP
- Management Frame Encryption/Decryption for broadcast/multicast packets
  - AES/CMAC
- Management Frame Encryption/Decryption for unicast packets
  - AES/CCMP
  - AES/GCMP

4.6 Transmit beamforming (TxBF)

- 802.11ax/ac/n Explicit Beamformee
  - Supports sounding feedback for up to 4x4 Beamformer

4.7 RF channels

Table 14 shows the list of supported 2.4 GHz and 5 GHz channels.

Table 14. Wi-Fi channel list

Channel number	Frequency	Channel number	Frequency	Channel number	Frequency
2.4 GHz channel					
1	2412 MHz	2	2417 MHz	3	2422 MHz
4	2427 MHz	5	2432 MHz	6	2437 MHz
7	2442 MHz	8	2447 MHz	9	2452 MHz
10	2457 MHz	11	2462 MHz	12	2467 MHz
13	2472 MHz	—	—	—	—
5 GHz channel					
36	5180 MHz	40	5200 MHz	44	5220 MHz
48	5240 MHz	52	5260 MHz	56	5280 MHz
60	5300 MHz	64	5320 MHz	100	5500 MHz
104	5520 MHz	108	5540 MHz	112	5560 MHz
116	5580 MHz	120	5600 MHz	124	5620 MHz
128	5640 MHz	132	5660 MHz	136	5680 MHz
140	5700 MHz	144	5720 MHz	149	5745 MHz
153	5765 MHz	157	5785 MHz	161	5805 MHz
165	5825 MHz	169	5845 MHz	173	5865 MHz
177	5885 MHz	—	—	—	—

5 Narrow band radio subsystem

5.1 Bluetooth LE features

- Bluetooth LE 5.4 certified
- Bluetooth LE 5.2 features supported
- Supports up to 16 simultaneous central/peripheral connections
- Wi-Fi/Bluetooth coexistence protocol support
- Encryption (AES) support
- Intelligent Adaptive Frequency Hopping (AFH)
- Bluetooth LE Privacy 1.2
- Bluetooth LE Secure Connection
- Bluetooth LE Data Length Extension
- Bluetooth LE Advertising Extension
- Bluetooth LE Long Range
- Bluetooth LE Power Control
- Bluetooth LE 2 Mbps
- Bluetooth LE Isochronous Channels

6 Coexistence

6.1 Antenna configurations

The RW610 supports two antenna configurations: single-antenna and dual-antenna configurations.

6.1.1 Dual-antenna configuration

The two separate antennas allow simultaneous independent operation of the Wi-Fi and Bluetooth LE radios.

Table 15. Supported TX and or RX operations for Wi-Fi and Bluetooth LE radios in dual-antenna configuration

Bluetooth LE	Wi-Fi 2.4 GHz	Wi-Fi 5 GHz
TX/RX	TX/RX	—
TX/RX	—	TX/RX

6.1.2 Single-antenna configuration

In single-antenna configuration, simultaneous 5 GHz Wi-Fi and Bluetooth is supported. In the 2.4 GHz band, the single-antenna configuration allows arbitrated transmit and receive operation of Wi-Fi and Bluetooth.

Table 16 shows the supported TX and/or RX operations with the RW610 single-antenna configuration.

Table 16. Wi-Fi and Bluetooth LE supported TX and or RX operations - Single-antenna configuration

Row #	Bluetooth LE	Wi-Fi 2.4 GHz	Wi-Fi 5 GHz
1	TX	—	TX/RX
2	—	TX	—
3	RX	—	TX/RX
4	—	RX	—

In single-antenna configuration:

- Wi-Fi 2.4 GHz TX and Bluetooth LE TX operations are arbitrated (rows 1 and 2)
- Wi-Fi 2.4 GHz RX and Bluetooth LE RX operations are arbitrated (rows 3 and 4)
- Wi-Fi 5 GHz TX/RX and Bluetooth LE RX or TX operations are simultaneous (rows 1 and 3)

6.2 Central hardware packet traffic arbiter

The central hardware packet traffic arbiter arbitrates the transmit and/or receive operations between the on-chip Wi-Fi and Bluetooth LE radios as per the supported hardware configuration. See Section 6.1.

In addition to the on-chip radios, the central hardware packet traffic arbiter arbitrates one external radio. Refer to Section 6.3.

6.3 Coexistence with an external radio

WCI-2 and PTA external coexistence interfaces are used for the coexistence with an external radio.

WCI-2 external coexistence interface

WCI-2 is the two-wire wireless coexistence interface 2 protocol defined in the Bluetooth Core Specification (Vol 7 Part C).

Figure 21 illustrates the hardware coexistence interface between the central hardware packet traffic arbiter and the external radio. In the figure, Wireless SoC is RW610.

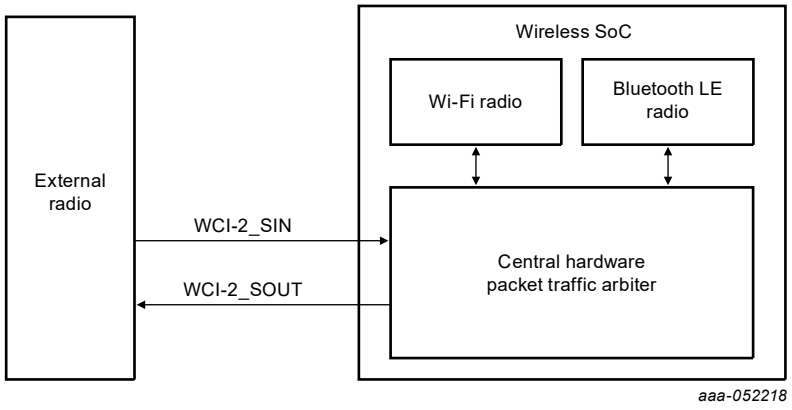


Figure 21. Hardware coexistence interface - WCI-2 coexistence interface

Note: *Refer to Section 7.6.15 for the description of WCI-2 coexistence interface signals.*

PTA external coexistence interface

Figure 22 illustrates the hardware coexistence interface between the central hardware packet traffic arbiter and the external radio. In the figure, Wireless SoC is RW610.

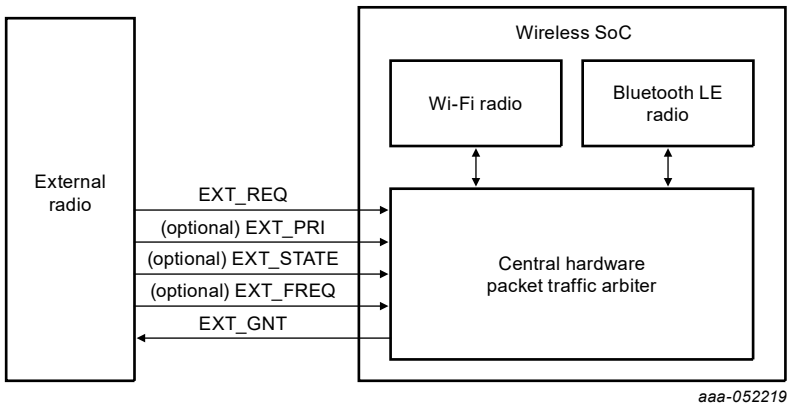


Figure 22. Hardware coexistence interface - PTA external coexistence interface

Note: *Refer to Section 7.6.16 for the description of PTA external coexistence interface signals.*

7 Pin information

7.1 Signal diagrams

Note: *Signals are muxed on dedicated pins. See Section 7.6 "Pin description" for the dedicated pin/muxed signal descriptions.*

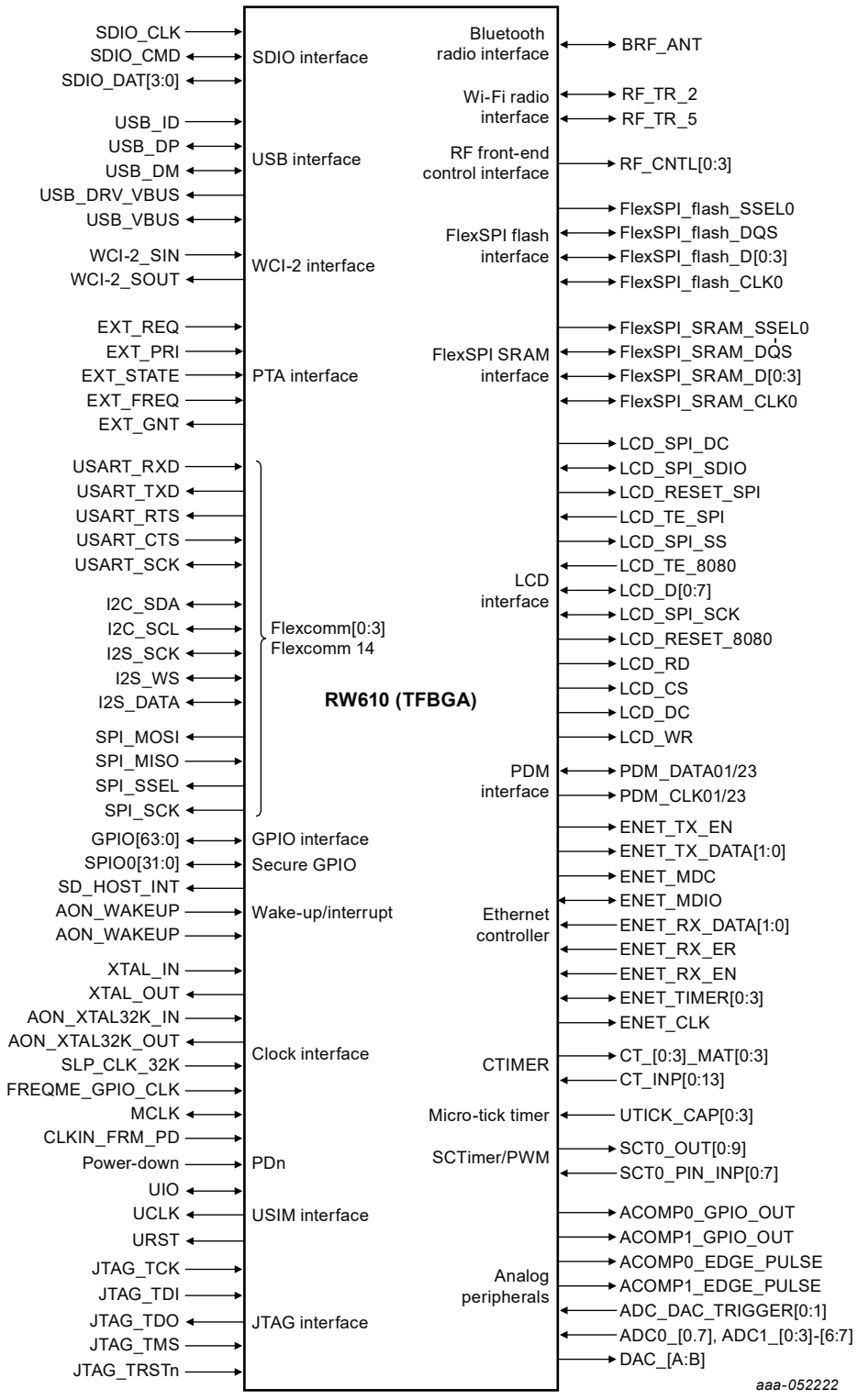


Figure 23. Signal diagram for TFBGA package

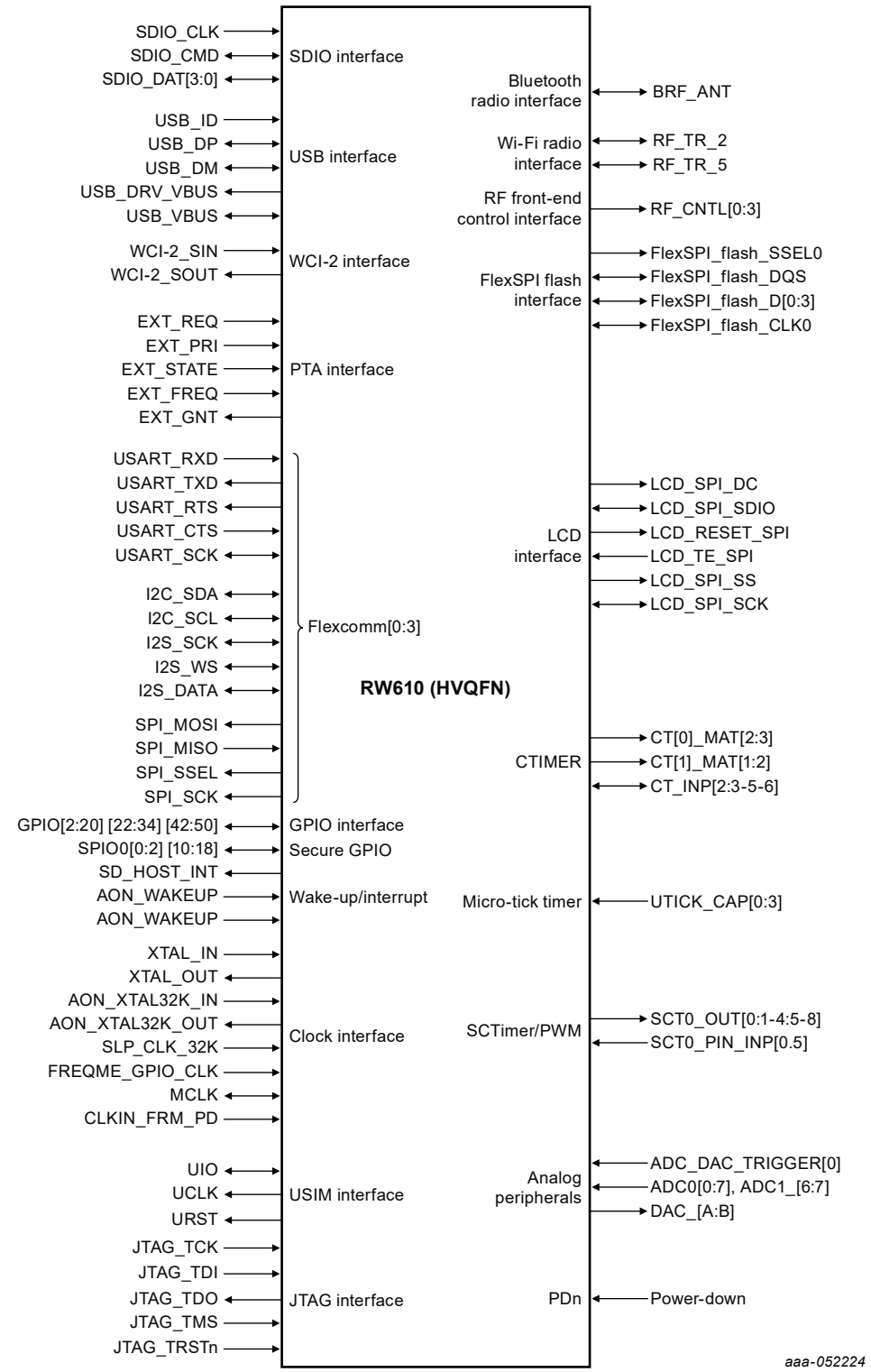


Figure 24. Signal diagram for HVQFN package

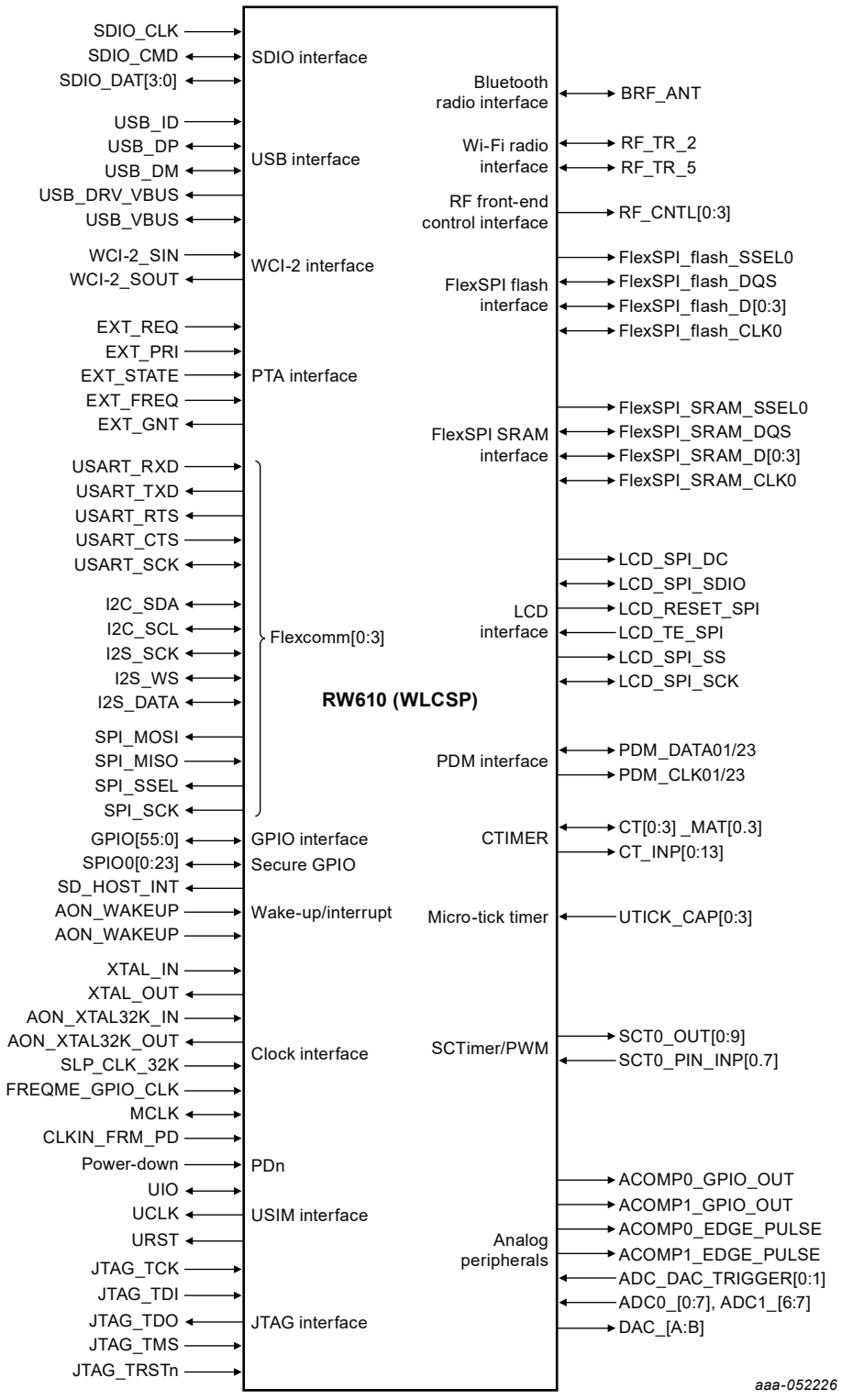


Figure 25. Signal diagram for WLCSP package

7.2 Pin assignment

7.2.1 Bump assignment - TFBGA145 package

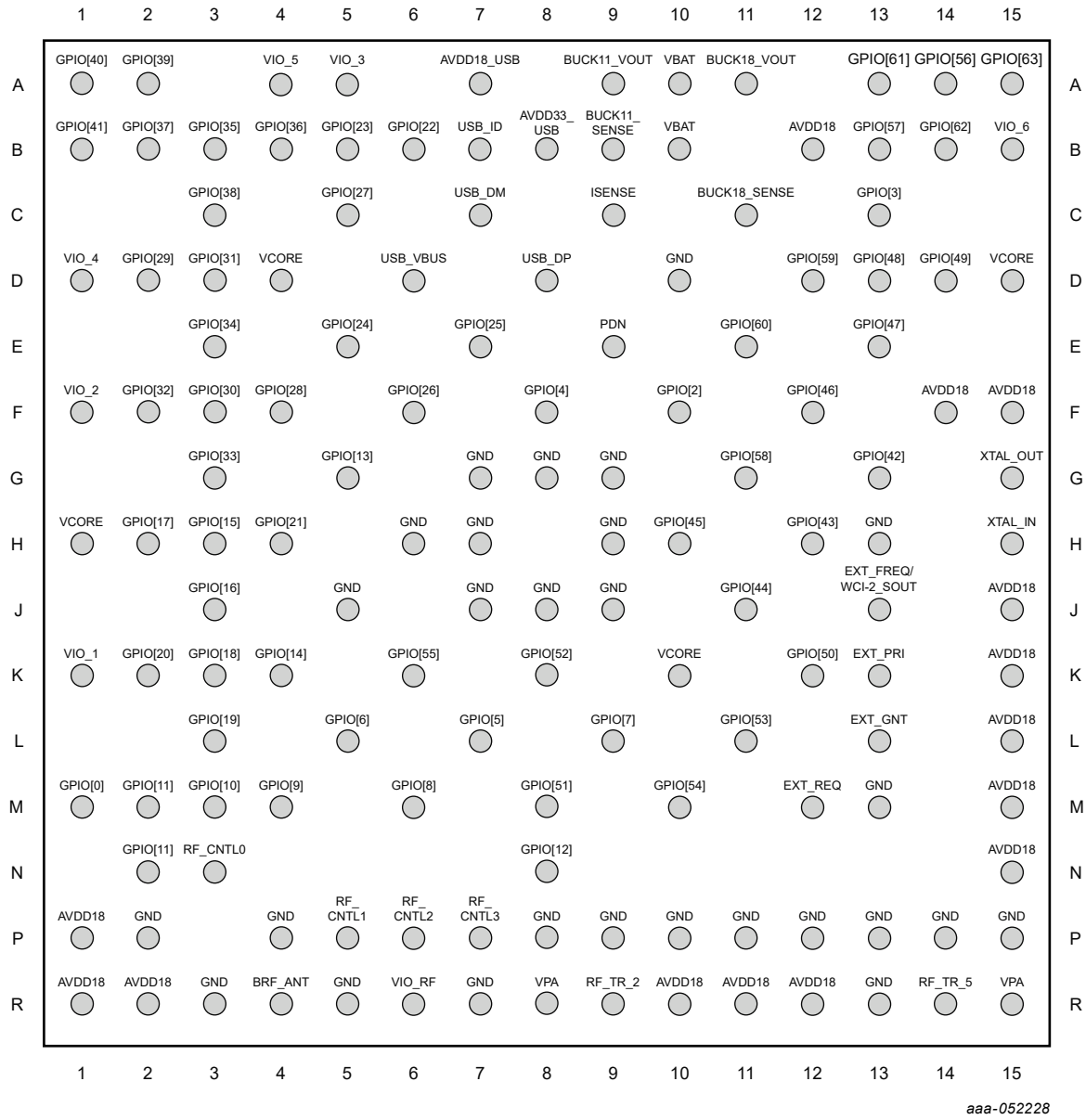


Figure 26. Bump assignment - TFBGA145 package (bump-side view)

7.2.2 Pin assignment - HVQFN116 package

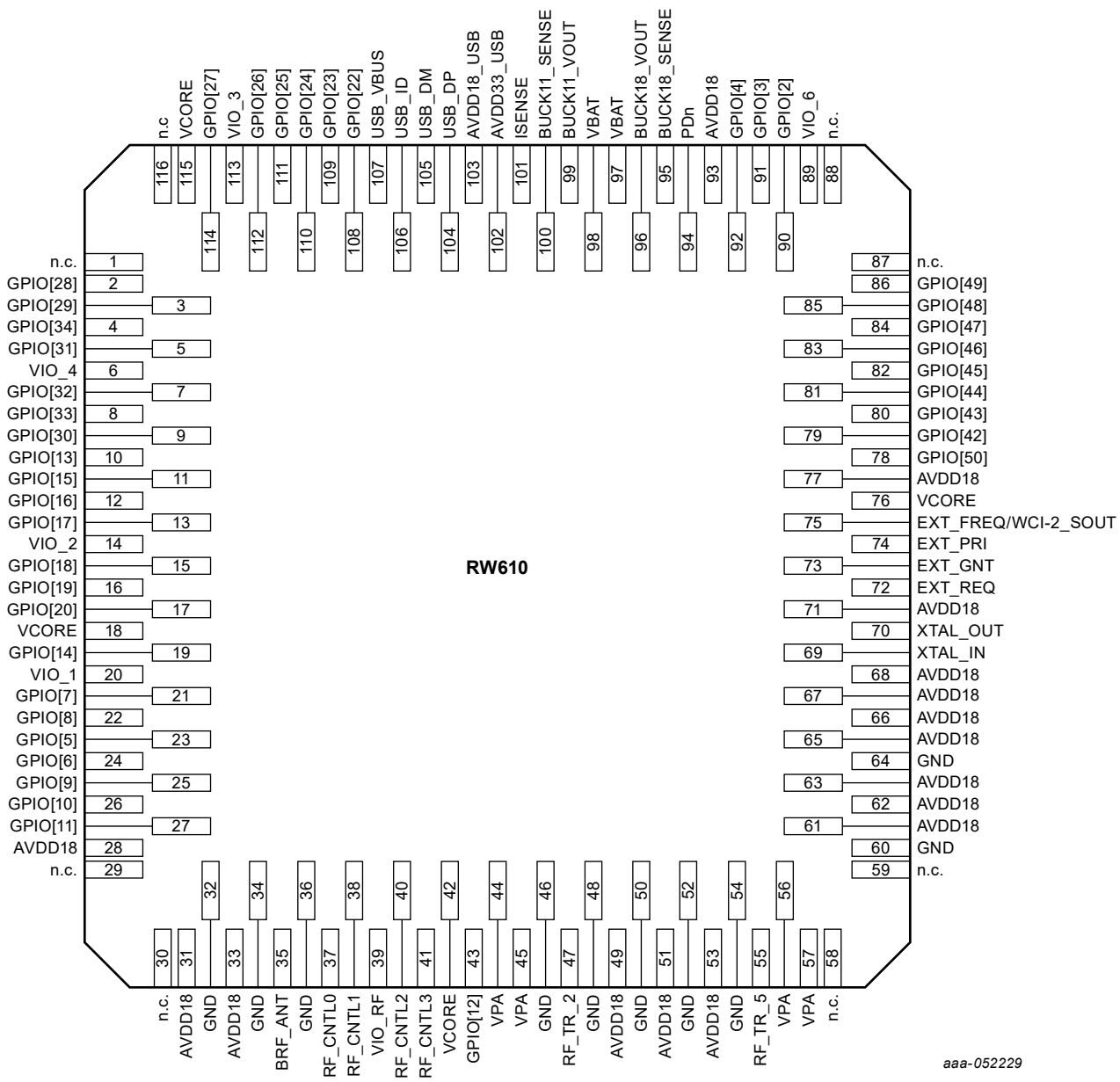


Figure 27. Pin assignment - HVQN116 package (top view)

7.2.3 Bump assignment - WLCSP151 package

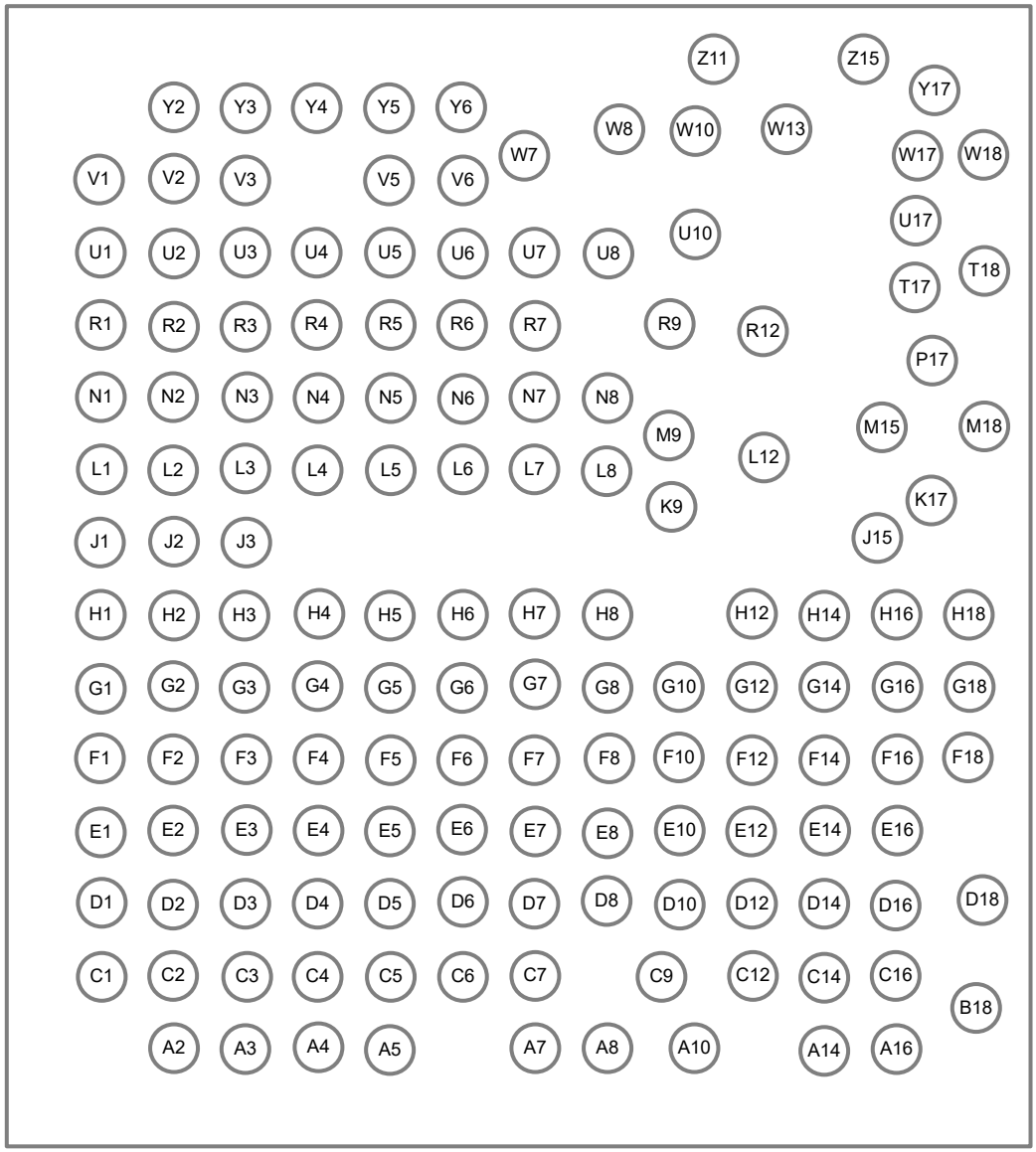


Figure 28. Bump assignment - WLCSP151 package (bottom view)

7.3 Pin types

Table 17. Pin types

Pin type	Description
I/O	Digital input/output
I	Digital input
O	Digital output
A, I	Analog input
A, O	Analog output
A, I/O	Analog input/output
NC	Not connected
Power	Power
Ground	Ground

7.4 Pin states

Table 18. Pin power down states (PDn = 0)

Pin	Power down state (PDn = 0)
RF_CNTL0	Drive low
RF_CNTL1	Drive high
RF_CNTL2	Drive low
RF_CNTL3	Drive high
GPIO[63:0]	Tristate

7.5 Pin lists

7.5.1 List by number for TFBGA145 package

Table 19. Bump list by number - TFBGA145 package

Number	TFBGA	Bump name	Power supply	Bump type
1	A1	GPIO[40]	VIO_5	I/O
2	A2	GPIO[39]	VIO_5	I/O
3	A4	VIO_5	—	Power
4	A5	VIO_3	—	Power
5	A7	AVDD18_USB	—	Power
6	A9	BUCK11_VOUT	—	Power
7	A10	VBAT	—	Power
8	A11	BUCK18_VOUT	—	Power
9	A13	GPIO[61]	VIO_6	I/O
10	A14	GPIO[56]	VIO_6	I/O
11	A15	GPIO[63]	VIO_6	I/O
12	B1	GPIO[41]	VIO_5	I/O
13	B2	GPIO[37]	VIO_5	I/O
14	B3	GPIO[35]	VIO_5	I/O
15	B4	GPIO[36]	VIO_5	I/O
16	B5	GPIO[23]	VIO_3	I/O
17	B6	GPIO[22]	VIO_3	I/O
18	B7	USB_ID	AVDD33_USB	A, I
19	B8	AVDD33_USB	—	Power
20	B9	BUCK11_SENSE	—	Power
21	B10	VBAT	—	Power
22	B12	AVDD18	—	Power
23	B13	GPIO[57]	VIO_6	I/O
24	B14	GPIO[62]	VIO_6	I/O
25	B15	VIO_6	—	Power
26	C3	GPIO[38]	VIO_5	I/O
27	C5	GPIO[27]	VIO_3	I/O
28	C7	USB_DM	AVDD33_USB	A, I/O
29	C9	ISENSE	AVDD18	I
30	C11	BUCK18_SENSE	—	Power
31	C13	GPIO[3]	VIO_6	I/O
32	D1	VIO_4	—	Power
33	D2	GPIO[29]	VIO_4	I/O

Table 19. Bump list by number - TFBGA145 package*...continued*

Number	TFBGA	Bump name	Power supply	Bump type
34	D3	GPIO[31]	VIO_4	I/O
35	D4	VCORE	—	Power
36	D6	USB_VBUS	—	A, I/O
37	D8	USB_DP	AVDD33_USB	A, I/O
38	D10	GND	—	Power
39	D12	GPIO[59]	VIO_6	I/O
40	D13	GPIO[48]	VIO_6	I/O
41	D14	GPIO[49]	VIO_6	I/O
42	D15	VCORE	—	Power
43	E3	GPIO[34]	VIO_4	I/O
44	E5	GPIO[24]	VIO_3	I/O
45	E7	GPIO[25]	VIO_3	I/O
46	E9	PDn	VBAT	I
47	E11	GPIO[60]	VIO_6	I/O
48	E13	GPIO[47]	VIO_6	I/O
49	F1	VIO_2	—	Power
50	F2	GPIO[32]	VIO_4	I/O
51	F3	GPIO[30]	VIO_4	I/O
52	F4	GPIO[28]	VIO_4	I/O
53	F6	GPIO[26]	VIO_3	I/O
54	F8	GPIO[4]	VIO_6	I/O
55	F10	GPIO[2]	VIO_6	I/O
56	F12	GPIO[46]	VIO_6	I/O
57	F14	AVDD18	—	Power
58	F15	AVDD18	—	Power
59	G3	GPIO[33]	VIO_4	I/O
60	G5	GPIO[13]	VIO_2	I/O
61	G7	GND	—	Power
62	G8	GND	—	Power
63	G9	GND	—	Power
64	G11	GPIO[58]	VIO_6	I/O
65	G13	GPIO[42]	VIO_6	I/O
66	G15	XTAL_OUT	AVDD18	A, O
67	H1	VCORE	—	Power
68	H2	GPIO[17]	VIO_2	I/O
69	H3	GPIO[15]	VIO_2	I/O

Table 19. Bump list by number - TFBGA145 package*...continued*

Number	TFBGA	Bump name	Power supply	Bump type
70	H4	GPIO[21]	VIO_2	I/O
71	H6	GND	—	Power
72	H7	GND	—	Power
73	H9	GND	—	Power
74	H10	GPIO[45]	VIO_6	I/O
75	H12	GPIO[43]	VIO_6	I/O
76	H13	GND	—	Power
77	H15	XTAL_IN	AVDD18	A, I
78	J3	GPIO[16]	VIO_2	I/O
79	J5	GND	—	Power
80	J7	GND	—	Power
81	J8	GND	—	Power
82	J9	GND	—	Power
83	J11	GPIO[44]	VIO_6	I/O
84	J13	EXT_FREQ/WCI-2_SOUT	AVDD18	I/O
85	J15	AVDD18	—	Power
86	K1	VIO_1	—	Power
87	K2	GPIO[20]	VIO_2	I/O
88	K3	GPIO[18]	VIO_2	I/O
89	K4	GPIO[14]	VIO_2	I/O
90	K6	GPIO[55]	VIO_1	I/O
91	K8	GPIO[52]	VIO_1	I/O
92	K10	VCORE	—	Power
93	K12	GPIO[50]	VIO_6	I/O
94	K13	EXT_PRI	AVDD18	I
95	K15	AVDD18	—	Power
96	L3	GPIO[19]	VIO_2	I/O
97	L5	GPIO[6]	VIO_1	I/O
98	L7	GPIO[5]	VIO_1	I/O
99	L9	GPIO[7]	VIO_1	I/O
100	L11	GPIO[53]	VIO_1	I/O
101	L13	EXT_GNT	AVDD18	O
102	L15	AVDD18	—	Power
103	M1	GPIO[0]	VIO_1	I/O
104	M2	GPIO[11]	VIO_1	I/O
105	M3	GPIO[10]	VIO_1	I/O

Table 19. Bump list by number - TFBGA145 package*...continued*

Number	TFBGA	Bump name	Power supply	Bump type
106	M4	GPIO[9]	VIO_1	I/O
107	M6	GPIO[8]	VIO_1	I/O
108	M8	GPIO[51]	VIO_1	I/O
109	M10	GPIO[54]	VIO_1	I/O
110	M12	EXT_REQ	AVDD18	I
111	M13	GND	—	Power
112	M15	AVDD18	—	Power
113	N2	GPIO[1]	VIO_1	I/O
114	N3	RF_CNTL0	VIO_RF	O
115	N8	GPIO[12]	VIO_RF	I/O
116	N15	AVDD18	—	Power
117	P1	AVDD18	—	Power
118	P2	GND	—	Power
119	P4	GND	—	Power
120	P5	RF_CNTL1	VIO_RF	O
121	P6	RF_CNTL2	VIO_RF	O
122	P7	RF_CNTL3	VIO_RF	O
123	P8	GND	—	Power
124	P9	GND	—	Power
125	P10	GND	—	Power
126	P11	GND	—	Power
127	P12	GND	—	Power
128	P13	GND	—	Power
129	P14	GND	—	Power
130	P15	GND	—	Power
131	R1	AVDD18	—	Power
132	R2	AVDD18	—	Power
133	R3	GND	—	Power
134	R4	BRF_ANT	AVDD18	A, I/O
135	R5	GND	—	Power
136	R6	VIO_RF	—	Power
137	R7	GND	—	Power
138	R8	VPA	—	Power
139	R9	RF_TR_2	AVDD18	A, I/O
140	R10	AVDD18	—	Power
141	R11	AVDD18	—	Power

Table 19. Bump list by number - TFBGA145 package*...continued*

Number	TFBGA	Bump name	Power supply	Bump type
142	R12	AVDD18	—	Power
143	R13	GND	—	Power
144	R14	RF_TR_5	AVDD18	A, I/O
145	R15	VPA	—	Power

7.5.2 List by number for HVQFN116 package

Table 20. Pin list by number - HVQFN116 package

Pin number	Pin name	Power supply	Pin type
1	NC	—	Not connected
2	GPIO[28]	VIO_4	I/O
3	GPIO[29]	VIO_4	I/O
4	GPIO[34]	VIO_4	I/O
5	GPIO[31]	VIO_4	I/O
6	VIO_4	—	Power
7	GPIO[32]	VIO_4	I/O
8	GPIO[33]	VIO_4	I/O
9	GPIO[30]	VIO_4	I/O
10	GPIO[13]	VIO_2	I/O
11	GPIO[15]	VIO_2	I/O
12	GPIO[16]	VIO_2	I/O
13	GPIO[17]	VIO_2	I/O
14	VIO_2	—	Power
15	GPIO[18]	VIO_2	I/O
16	GPIO[19]	VIO_2	I/O
17	GPIO[20]	VIO_2	I/O
18	VCORE	—	Power
19	GPIO[14]	VIO_2	I/O
20	VIO_1	—	Power
21	GPIO[7]	VIO_1	I/O
22	GPIO[8]	VIO_1	I/O
23	GPIO[5]	VIO_1	I/O
24	GPIO[6]	VIO_1	I/O
25	GPIO[9]	VIO_1	I/O
26	GPIO[10]	VIO_1	I/O
27	GPIO[11]	VIO_1	I/O
28	AVDD18	—	Power
29	NC	—	Not connected
30	NC	—	Not connected
31	AVDD18	—	Power
32	GND	—	Power
33	AVDD18	—	Power
34	GND	—	Power
35	BRF_ANT	AVDD18	A, I/O

Table 20. Pin list by number - HVQFN116 package*...continued*

Pin number	Pin name	Power supply	Pin type
36	GND	—	Power
37	RF_CNTL0	VIO_RF	O
38	RF_CNTL1	VIO_RF	O
39	VIO_RF	—	Power
40	RF_CNTL2	VIO_RF	O
41	RF_CNTL3	VIO_RF	O
42	VCORE	—	Power
43	GPIO[12]	VIO_RF	I/O
44	VPA	—	Power
45	VPA	—	Power
46	GND	—	Power
47	RF_TR_2	AVDD18	A, I/O
48	GND	—	Power
49	AVDD18	—	Power
50	GND	—	Power
51	AVDD18	—	Power
52	GND	—	Power
53	AVDD18	—	Power
54	GND	—	Power
55	RF_TR_5	AVDD18	A, I/O
56	VPA	—	Power
57	VPA	—	Power
58	NC	—	Not connected
59	NC	—	Not connected
60	GND	—	Power
61	AVDD18	—	Power
62	AVDD18	—	Power
63	AVDD18	—	Power
64	GND	—	Power
65	AVDD18	—	Power
66	AVDD18	—	Power
67	AVDD18	—	Power
68	AVDD18	—	Power
69	XTAL_IN	AVDD18	A, I
70	XTAL_OUT	AVDD18	A, O
71	AVDD18	—	Power

Table 20. Pin list by number - HVQFN116 package*...continued*

Pin number	Pin name	Power supply	Pin type
72	EXT_REQ	AVDD18	I
73	EXT_GNT	AVDD18	O
74	EXT_PRI	AVDD18	I
75	EXT_FREQ/WCI-2_SOUT	AVDD18	I/O
76	VCORE	—	Power
77	AVDD18	—	Power
78	GPIO[50]	VIO_6	I/O
79	GPIO[42]	VIO_6	I/O
80	GPIO[43]	VIO_6	I/O
81	GPIO[44]	VIO_6	I/O
82	GPIO[45]	VIO_6	I/O
83	GPIO[46]	VIO_6	I/O
84	GPIO[47]	VIO_6	I/O
85	GPIO[48]	VIO_6	I/O
86	GPIO[49]	VIO_6	I/O
87	NC	—	Not connected
88	NC	—	Not connected
89	VIO_6	—	Power
90	GPIO[2]	VIO_6	I/O
91	GPIO[3]	VIO_6	I/O
92	GPIO[4]	VIO_6	I/O
93	AVDD18	—	Power
94	PDn	VBAT	I
95	BUCK18_SENSE	—	Power
96	BUCK18_VOUT	—	Power
97	VBAT	—	Power
98	VBAT	—	Power
99	BUCK11_VOUT	—	Power
100	BUCK11_SENSE	—	Power
101	ISENSE	AVDD18	I
102	AVDD33_USB	—	Power
103	AVDD18_USB	—	Power
104	USB_DP	AVDD33_USB	A, I/O
105	USB_DM	AVDD33_USB	A, I/O
106	USB_ID	AVDD33_USB	A, I
107	USB_VBUS	—	A, I/O

Table 20. Pin list by number - HVQFN116 package*...continued*

Pin number	Pin name	Power supply	Pin type
108	GPIO[22]	VIO_3	I/O
109	GPIO[23]	VIO_3	I/O
110	GPIO[24]	VIO_3	I/O
111	GPIO[25]	VIO_3	I/O
112	GPIO[26]	VIO_3	I/O
113	VIO_3	—	Power
114	GPIO[27]	VIO_3	I/O
115	VCORE	—	Power
116	NC	—	Not connected

7.5.3 List by number for WLCSP151 package

Table 21. Bump list by number - WLCSP151 package

WLCSP151	Bump name	X (µm)	Y (µm)
A10	GND	798.6	-2159
A14	AVDD18	1387	-2159
A16	AVDD18	1717	-2159
A2	GND	-1583	-2159
A3	VIO_4	-1253	-2159
A4	GPIO[30]	-923	-2159
A5	VIO_2	-593	-2159
A7	GND	67	-2159
A8	GPIO[54]	397	-2159
B18	GND	2071.6	-1973.7
C1	VIO_5	-1913	-1829
C12	GPIO[1]	1057	-1829
C14	GND	1387	-1829
C16	GND	1717	-1829
C2	GPIO[39]	-1583	-1829
C3	GPIO[41]	-1253	-1829
C4	GPIO[32]	-923	-1829
C5	GPIO[33]	-593	-1829
C6	GPIO[16]	-263	-1829
C7	GPIO[20]	67	-1829
C9	VIO_1	644.5	-1829
D1	VIO_3	-1913	-1499
D10	GPIO[5]	727	-1499
D12	GPIO[0]	1057	-1499
D14	GND	1387	-1499
D16	AVDD18	1717	-1499
D18	BRF_ANT	2111.8	-1484.9
D2	GPIO[36]	-1583	-1499
D3	GPIO[40]	-1253	-1499
D4	GPIO[29]	-923	-1499
D5	GPIO[31]	-593	-1499
D6	GPIO[15]	-263	-1499
D7	GPIO[19]	67	-1499
D8	GPIO[51]	397	-1499
E1	GPIO[23]	-1913	-1169

Table 21. Bump list by number - WLCSP151 package*...continued*

WLCSP151	Bump name	X (µm)	Y (µm)
E10	GPIO[8]	727	-1169
E12	GPIO[10]	1057	-1169
E14	GPIO[11]	1387	-1169
E16	GND	1717	-1169
E2	GPIO[22]	-1583	-1169
E3	GPIO[35]	-1253	-1169
E4	GPIO[38]	-923	-1169
E5	GPIO[34]	-593	-1169
E6	GPIO[18]	-263	-1169
E7	GPIO[17]	67	-1169
E8	GPIO[52]	397	-1169
F1	USB_DM	-1913	-839
F10	GPIO[7]	727	-839
F12	GPIO[6]	1057	-839
F14	GND	1387	-839
F16	GND	1717	-839
F18	VIO_RF	2047	-839
F2	USB_DP	-1583	-839
F3	GPIO[24]	-1253	-839
F4	GPIO[37]	-923	-839
F5	GPIO[28]	-593	-839
F6	GPIO[13]	-263	-839
F7	GPIO[14]	67	-839
F8	GPIO[53]	397	-839
G1	AVDD18_USB	-1913	-509
G10	GPIO[9]	727	-509
G12	GND	1057	-509
G14	GND	1387	-509
G16	RF_CNTL0	1717	-509
G18	GND	2047	-509
G2	AVDD33_USB	-1583	-509
G3	GPIO[25]	-1253	-509
G4	GPIO[27]	-923	-509
G5	VCORE	-593	-509
G6	GPIO[21]	-263	-509
G7	GND	67	-509

Table 21. Bump list by number - WLCSP151 package*...continued*

WLCSP151	Bump name	X (µm)	Y (µm)
G8	GPIO[55]	397	-509
H1	GND	-1913	-179
H12	RF_CNTL2	1057	-179
H14	RF_CNTL3	1387	-179
H16	RF_CNTL1	1717	-179
H18	GPIO[12]	2047	-179
H2	ISENSE	-1583	-179
H3	USB_VBUS	-1253	-179
H4	GPIO[26]	-923	-179
H5	VCORE	-593	-179
H6	GND	-263	-179
H7	VCORE	67	-179
H8	VCORE	397	-179
J1	BUCK11_VOUT	-1913	151
J15	VPA	1628.7	177.1
J2	BUCK11_VSENSE	-1583	151
J3	USB_ID	-1253	151
K17	GND	1880.4	343.4
K9	GND	685.8	311.5
L1	VBAT	-1913	481
L12	GND	1110.9	539.9
L2	VBAT	-1583	481
L3	GND	-1253	481
L4	GPIO[3]	-923	481
L5	VCORE	-593	481
L6	GND	-263	481
L7	VCORE	67	481
L8	VCORE	397	481
M15	GND	1649.6	676.9
M18	RF_TR_2	2111.8	676.9
M9	GND	685.8	641.5
N1	BUCK18_VOUT	-1913	811
N2	BUCK18_VSENSE	-1583	811
N3	GPIO[4]	-1253	811
N4	GPIO[47]	-923	811
N5	GPIO[49]	-593	811

Table 21. Bump list by number - WLCSP151 package*...continued*

WLCSP151	Bump name	X (µm)	Y (µm)
N6	EXT_PRI	-263	811
N7	GND	67	811
N8	GND	397	811
P17	AVDD18	1880.4	979.1
R1	GND	-1913	1141
R12	GND	1110.9	1111.2
R2	PDn	-1583	1141
R3	GPIO[46]	-1253	1141
R4	GPIO[43]	-923	1141
R5	GPIO[50]	-593	1141
R6	EXT_FREQ	-263	1141
R7	EXT_GNT	67	1141
R9	GND	685.8	1141
T17	GND	1803.8	1313.1
T18	AVDD18	2111.8	1390.8
U1	VDD18_OTP	-1913	1471
U10	GND	798.6	1553.9
U17	GND	1803.8	1614.2
U2	GPIO[2]	-1583	1471
U3	GPIO[45]	-1253	1471
U4	GPIO[42]	-923	1471
U5	AVDD18	-593	1471
U6	GND	-263	1471
U7	EXT_REQ	67	1471
U8	GND	397	1471
V1	GND	-1913	1801
V2	VIO_6	-1583	1801
V3	GPIO[44]	-1253	1801
V5	XTAL_OUT	-593	1801
V6	GND	-263	1801
W10	GND	798.6	2027.9
W13	GND	1210.1	2027.9
W17	GND	1803.8	1914.5
W18	RF_TR_5	2111.8	1914.5
W7	GND	24.7	1914.5
W8	AVDD18	455.7	2027.9

Table 21. Bump list by number - WLCSP151 package*...continued*

WLCSP151	Bump name	X (µm)	Y (µm)
Y17	VPA	1880.4	2211.4
Y2	GPIO[48]	-1583	2131
Y3	VDD18	-1253	2131
Y4	GND	-923	2131
Y5	XTAL_IN	-593	2131
Y6	AVDD18_XTAL	-263	2131
Z11	AVDD18	884.7	2354.3
Z15	AVDD18	1562.1	2354.3

7.6 Pin description

7.6.1 General purpose I/O (GPIO)

Table 22. GPIO interface pins and other function pins

TFBGA145	HVQFN116	WLCSP151	Symbol	Supply	Type	Description
M1	—	D12	GPIO[0]	VIO_1	I/O	**GPIO mode**: General purpose I/O 0
					I	**CT_INP0**: pin input 0 to CTIMER
					O	**CT0_MAT0**: CTIMER 0 match output 0
					I	**FC0_CTS_SDA_SSELN0_USART**: Flexcomm 0 USART clear-to-send
					I/O	**FC0_CTS_SDA_SSELN0_SPI**: Flexcomm 0 SPI chip select
N2	—	C12	GPIO[1]	VIO_1	I/O	**GPIO mode**: General purpose I/O 1
					I	**CT_INP1**: pin input 1 to CTIMER
					O	**CT0_MAT1**: CTIMER 0 match output 1
F10	90	U2	GPIO[2]	VIO_6	I/O	**GPIO mode**: General purpose I/O 2
					I	**FC0_RXD_SDA_MOSI_DATA_USART**: Flexcomm0 USART receiver
					I/O	**FC0_RXD_SDA_MOSI_DATA_I2C**: Flexcomm 0 I2C data in/out
					I/O	**FC0_RXD_SDA_MOSI_DATA_I2S**: Flexcomm 0 I2S receiver/transmitter
					I/O	**FC0_RXD_SDA_MOSI_DATA_SPI**: Flexcomm 0 SPI controller out/target in
C13	91	L4	GPIO[3]	VIO_6	I/O	**GPIO mode**: General purpose I/O 3
					O	**SCT0_OUT0**: SCTimer 0/PWM output 0
					I	**SCT0_PIN_INP0**: Input pin 0 to SCTimer 0/ PWM
					O	**FC0_TXD_SCL_MISO_WS_USART**: Flexcomm 0 USART transmitter
					I/O	**FC0_TXD_SCL_MISO_WS_I2C**: Flexcomm 0 I2C clock
					I/O	**FC0_TXD_SCL_MISO_WS_I2S**: Flexcomm 0 I2S word select
					I/O	**FC0_TXD_SCL_MISO_WS_SPI**: Flexcomm 0 SPI controller in/target out

Table 22. GPIO interface pins and other function pins*...continued*

TFBGA145	HVQFN116	WLCSP151	Symbol	Supply	Type	Description
F8	92	N3	GPIO[4]	VIO_6	I/O	**GPIO mode**: General purpose I/O 4
					I	**Coexistence mode**: Ext_STATE/WCI-2_SIN
					O	**SCT0_OUT1**: SCTimer 0/PWM output 1
					I	**SCT0_PIN_INP1**: Input pin 1 to SCTimer 0/ PWM
					I	**CLKIN_FRM_PD**: Clock from pad which can replace the internal clock for debug purpose
					I/O	**FC0_SCK_USART**: Flexcomm 0 USART clock
					I/O	**FC0_SCK_I2S**: Flexcomm 0 I2S clock
					I/O	**FC0_SCK_SPI**: Flexcomm 0 SPI clock
L7	23	D10	GPIO[5]	VIO_1	I/O	**GPIO mode**: General purpose I/O 5
					I/O	**MCLK**: MCLK input or output for I2S and/or digital microphone
					O	**FC0_RTS_SCL_SSELN1_USART**: Flexcomm 0 USART request-to-send
L5	24	F12	GPIO[6]	VIO_1	I/O	**GPIO mode**: General purpose I/O 6
					I	**JTAG_TCK**: JTAG test clock input signal
					I	**FC1_CTS_SDA_SSELN0_USART**: Flexcomm 1 USART clear-to-send
					I/O	**FC1_CTS_SDA_SSELN0_SPI**: Flexcomm 1 SPI chip select
L9	21	F10	GPIO[7]	VIO_1	I/O	**GPIO mode**: General purpose I/O 7
					I	**JTAG_TMS**: JTAG test mode select input signal
					I/O	**FC1_SCK_USART**: Flexcomm 1 USART clock
					I/O	**FC1_SCK_I2S**: Flexcomm 1 I2S clock
					I/O	**FC1_SCK_SPI**: Flexcomm 1 SPI clock
M6	22	E10	GPIO[8]	VIO_1	I/O	**GPIO mode**: General purpose I/O 8
					I	**JTAG_TDI**: JTAG test data input signal
					O	**FC1_TXD_SCL_MISO_WS_USART**: Flexcomm 1 USART transmitter
					I/O	**FC1_TXD_SCL_MISO_WS_I2C**: Flexcomm 1 I2C clock
					I/O	**FC1_TXD_SCL_MISO_WS_I2S**: Flexcomm 1 I2S word select
					I/O	**FC1_TXD_SCL_MISO_WS_SPI**: Flexcomm 1 SPI controller in/target out

Table 22. GPIO interface pins and other function pins*...continued*

TFBGA145	HVQFN116	WLCSP151	Symbol	Supply	Type	Description
M4	25	G10	GPIO[9]	VIO_1	I/O	**GPIO mode**: General purpose I/O 9
					O	**JTAG_TDO**: JTAG test data output signal
					I	**FC1_RXD_SDA_MOSI_DATA_USART**: Flexcomm 1 USART receiver
					I/O	**FC1_RXD_SDA_MOSI_DATA_I2C**: Flexcomm 1 I2C data in/out
					I/O	**FC1_RXD_SDA_MOSI_DATA_I2S**: Flexcomm 1 I2S receiver/transmitter
					I/O	**FC1_RXD_SDA_MOSI_DATA_SPI**: Flexcomm 1 SPI controller out/target in
M3	26	E12	GPIO[10]	VIO_1	I/O	**GPIO mode**: General purpose I/O 10
					I	**JTAG_TRSTN**: JTAG test reset signal
					O	**FC1_RTS_SCL_SSELN1_USART**: Flexcomm 1 USART request-to-send
M2	27	E14	GPIO[11]	VIO_1	I/O	**GPIO mode**: General purpose I/O 11
					O	**SCT0_OUT8**: SCTimer 0/PWM output 8
N8	43	H18	GPIO[12]	VIO_RF	I/O	**GPIO mode**: General purpose I/O 12
					O	**USB_DRV_VBUS** : enables + 5 V voltage supply to USB OTG
					O	**CT0_MAT2**: CTIMER 0 match output 2
					I	**CT_INP2**: Pin input 2 to CTIMER
					O	**SD_HOST_INT**: SD host interrupt output signal
G5	10	F6	GPIO[13]	VIO_2	I/O	**GPIO mode**: General purpose I/O 13
					I	**CT_INP3**: pin input 3 to CTIMER
					O	**CT0_MAT3**: CTIMER 0 match output 3
					I	**SWCLK**: Serial wire clock input signal
					I	**FC2_RXD_SDA_MOSI_DATA_USART**: Flexcomm 2 USART receiver
					I/O	**FC2_RXD_SDA_MOSI_DATA_I2C**: Flexcomm 2 I2C data in/out
					I/O	**FC2_RXD_SDA_MOSI_DATA_I2S**: Flexcomm 2 I2S receiver/transmitter
					I/O	**FC2_RXD_SDA_MOSI_DATA_SPI**: Flexcomm 2 SPI controller out/target in

Table 22. GPIO interface pins and other function pins*...continued*

TFBGA145	HVQFN116	WLCSP151	Symbol	Supply	Type	Description
K4	19	F7	GPIO[14]	VIO_2	I/O	**GPIO mode**: General purpose I/O 14
					I	**CT_INP4**: Pin input 4 to CTIMER
					O	**CT1_MAT0**: CTIMER 1 match output 0
					I/O	**SWDIO**: Serial wire debug data input/output signal
					O	**FC2_TXD_SCL_MISO_WS_USART**: Flexcomm 2 USART transmitter
					I/O	**FC2_TXD_SCL_MISO_WS_I2C**: Flexcomm 2 I2C clock
					I/O	**FC2_TXD_SCL_MISO_WS_I2S**: Flexcomm 2 I2S word select
					I/O	**FC2_TXD_SCL_MISO_WS_SPI**: Flexcomm 2 SPI controller in/target out
H3	11	D6	GPIO[15]	VIO_2	I/O	**GPIO mode**: General purpose I/O 15
					I	**SDIO mode**: SD_CLK SDIO clock input
					I	**UTICK_CAP0**: Micro-tick timer capture input 0
					O	**UCLK**: USIM clock
					I/O	**FC2_SCK_USART**: Flexcomm 2 USART clock
					I/O	**FC2_SCK_I2S**: Flexcomm 2 I2S clock
					I/O	**FC2_SCK_SPI**: Flexcomm 2 SPI clock
J3	12	C6	GPIO[16]	VIO_2	I/O	**GPIO mode**: General purpose I/O 16
					I/O	**SDIO mode**: (SD_D3) SDIO_DAT3 SDIO data input/output 3
					I	**UTICK_CAP1**: Micro-tick timer capture input 1
					O	**URST**: USIM reset signal
					I	**FC2_CTS_SDA_SSELN0_USART**: Flexcomm 2 USART clear-to-send
					I/O	**FC2_CTS_SDA_SSELN0_SPI**: Flexcomm 2 SPI chip select
					I/O	**FC2_CTS_SDA_SSELN0_I2C_COPY**: (I2C_SDA) Flexcomm 2 backup-I2C data in/out
H2	13	E7	GPIO[17]	VIO_2	I/O	**GPIO mode**: General purpose I/O 17
					I/O	**SDIO mode**: SDIO_CMD SDIO command line
					I	**UTICK_CAP2**: Micro-tick timer capture input 2
					I/O	**UIO**: USIM transmit receive signal
					O	**FC2_RTS_SCL_SSELN1_USART**: Flexcomm 2 USART request-to-send
					I/O	**FC2_RTS_SCL_SSELN1_I2C_COPY** (I2C_SCL) Flexcomm 2 backup-I2C clock

Table 22. GPIO interface pins and other function pins*...continued*

TFBGA145	HVQFN116	WLCSP151	Symbol	Supply	Type	Description
K3	15	E6	GPIO[18]	VIO_2	I/O	**GPIO mode**: General purpose I/O 18
					I/O	**SDIO mode**: SDIO_DAT2 SDIO data input/ output 2
					I	**UTICK_CAP3**: Micro-tick timer capture input 3
					O	**UVS**: USIM mode selection
					O	**GPIO_INT_BMAT**: Output of the interrupt pattern match engine
L3	16	D7	GPIO[19]	VIO_2	I/O	**GPIO mode**: General purpose I/O 19
					I/O	**SDIO mode**: SDIO_DAT0 SDIO data input/ output 0
					O	**FC3_RTS_SCL_SSELN1_USART**: Flexcomm 3 USART request-to-send
					I/O	**FC3_RTS_SCL_SSELN1_I2C_COPY**: (I2C_ SCL) Flexcomm 3 backup-I2C clock
K2	17	C7	GPIO[20]	VIO_2	I/O	**GPIO mode**: General purpose I/O 20
					I/O	**SDIO mode**: SDIO_DAT1 SDIO data input/ output 1
					I	**FC3_CTS_SDA_SSELN0_USART**: Flexcomm 3 USART clear-to-send
					I/O	**FC3_CTS_SDA_SSELN0_SPI**: Flexcomm 3 SPI chip select
					I/O	**FC3_CTS_SDA_SSELN0_I2C_COPY**: (I2C_ SDA) Flexcomm 3 backup-I2C data in/out
H4	—	G6	GPIO[21]	VIO_2	I/O	**GPIO mode**: General purpose I/O 21
					O	**CT1_MAT1**: CTIMER 1 match output 1
					I	**CT_INP5**: Pin input 5 to CTIMER
B6	108	E2	GPIO[22]	VIO_3	I/O	**GPIO mode**: General purpose I/O 22
					A,I	**AON_XTAL32K_IN**: Always-on 32K crystal input signal
					I	**SLP_CLK_32K**: External sleep clock input signal
					I	**SCT0_PIN_INP2**: Pin input 2 to SCTimer 0/ PWM
					I	**ENET_RX_DATA0**: ipp_ind_mac0_rxdata0 (I)
B5	109	E1	GPIO[23]	VIO_3	I/O	**GPIO mode**: General purpose I/O 23
					A,O	**AON_XTAL32K_OUT**: Always-on 32K crystal output signal
					I	**SCT0_PIN_INP3**: Pin input 3 to SCTimer 0/ PWM
					I	**ENET_RX_DATA1**: ipp_ind_mac0_rxdata1(I)

Table 22. GPIO interface pins and other function pins*...continued*

TFBGA145	HVQFN116	WLCSP151	Symbol	Supply	Type	Description
E5	110	F3	GPIO[24]	VIO_3	I/O	**GPIO mode**: General purpose I/O 24
					I	**AON_WAKEUP**: Always on out-of-band wake-up input signal
					O	**CT1_MAT2**: 32-bit CTIMER 1 match output 2
					I	**CT_INP6**: Pin input 6 to CTIMER
					I/O	**ENET_TIMER2**: Bit 2 of Ethernet controller timer
					I	**FC3_RXD_SDA_MOSI_DATA_USART**: Flexcomm 3 USART receiver
					I/O	**FC3_RXD_SDA_MOSI_DATA_I2C**: Flexcomm 3 I2C data in/out
					I/O	**FC3_RXD_SDA_MOSI_DATA_I2S**: Flexcomm 3 I2S receiver/transmitter
					I/O	**FC3_RXD_SDA_MOSI_DATA_SPI**: Flexcomm 3 SPI controller out/target in
E7	111	G3	GPIO[25]	VIO_3	I/O	**GPIO mode**: General purpose I/O 25
					I	**AON_WAKEUP**: Always on out-of-band wake-up input signal
					O	**CT1_MAT3**: 32-bit CTIMER 1 match output 3
					I	**CT_INP7**: Pin input 7 to CTIMER
					O	**ENET_CLK**: Ethernet controller reference clock
					I/O	**FC3_SCK_USART**: Flexcomm 3 USART clock
					I/O	**FC3_SCK_I2S**: Flexcomm 3 I2S clock
					I/O	**FC3_SCK_SPI**: Flexcomm 3 SPI clock
F6	112	H4	GPIO[26]	VIO_3	I/O	**GPIO mode**: General purpose I/O 26
					I	**AON_CAPT**: Capture timer input signal
					O	**SCT0_OUT4**: SCTimer 0/PWM output 4
					I	**SCT0_PIN_INP4**: Pin input 4 to SCTimer 0/PWM
					I/O	**ENET_TIMER3**: Bit 3 of Ethernet controller timer
					O	**FC3_TXD_SCL_MISO_WS_USART**: Flexcomm 3 USART transmitter
					I/O	**FC3_TXD_SCL_MISO_WS_I2C**: Flexcomm 3 I2C clock
					I/O	**FC3_TXD_SCL_MISO_WS_I2S**: Flexcomm 3 I2S word select
					I/O	**FC3_TXD_SCL_MISO_WS_SPI**: Flexcomm 3 SPI controller in/target out

Table 22. GPIO interface pins and other function pins*...continued*

TFBGA145	HVQFN116	WLCSP151	Symbol	Supply	Type	Description
C5	114	G4	GPIO[27]	VIO_3	I/O	**GPIO mode**: General purpose I/O 27
					O	**AON_OUT**: Always-on GPIO output signal
					O	**SCT0_OUT5**: SCTimer 0/PWM output 5
					I	**SCT0_PIN_INP5**: Pin input 5 to SCTimer 0/PWM
					I/O	**ENET_TIMER0**: Bit 0 of Ethernet controller timer
F4	2	F5	GPIO[28]	VIO_4	I/O	**GPIO mode**: General purpose I/O 28
					O	**FlexSPI_flash_SSEL0**: FlexSPI flash client select 0
D2	3	D4	GPIO[29]	VIO_4	I/O	**GPIO mode**: General purpose I/O 29
					I/O	**FlexSPI_flash_DQS**: Data strobe input/output for the FlexSPI Flash interface
F3	9	A4	GPIO[30]	VIO_4	I/O	**GPIO mode**: General purpose I/O 30
					I/O	**FlexSPI_flash_D0**: Data bit 0 for FlexSPI flash interface
D3	5	D5	GPIO[31]	VIO_4	I/O	**GPIO mode**: General purpose I/O 31
					I/O	**FlexSPI_flash_D1**: Data bit 1 for FlexSPI flash interface
F2	7	C4	GPIO[32]	VIO_4	I/O	**GPIO mode**: General purpose I/O 32
					I/O	**FlexSPI_flash_D2**: Data bit 2 for FlexSPI flash interface
					I/O	**Secure GPIO mode**: SPIO0[0]
G3	8	C5	GPIO[33]	VIO_4	I/O	**GPIO mode**: General purpose I/O 33
					I/O	**FlexSPI_flash_D3**: Data bit 3 for FlexSPI flash interface
					I/O	**Secure GPIO mode**: SPIO0[1]
E3	4	E5	GPIO[34]	VIO_4	I/O	**GPIO mode**: General purpose I/O 34
					O	**FlexSPI_flash_CLK0**: FlexSPI flash interface clock 0
					I/O	**Secure GPIO mode**: SPIO0[2]
B3	—	E3	GPIO[35]	VIO_5	I/O	**GPIO mode**: General purpose I/O 35
					O	**FlexSPI_SRAM_CLK0**: FlexSPI SRAM interface clock 0
					O	**SCT0_OUT6**: SCTimer 0/PWM output 6
					I	**SCT0_PIN_IN6**: Pin input 6 to SCTimer 0/PWM
					I/O	**Secure GPIO mode**: SPIO0[3]

Table 22. GPIO interface pins and other function pins*...continued*

TFBGA145	HVQFN116	WLCSP151	Symbol	Supply	Type	Description
B4	—	D2	GPIO[36]	VIO_5	I/O	**GPIO mode**: General purpose I/O 36
					O	**FlexSPI_SRAM_SSL0**: FlexSPI SRAM interface client select 0
					O	**SCT0_OUT7**: SCTimer 0/PWM output 7
					I	**SCT0_PIN_IN7**: Pin input 7 to SCTimer 0/PWM
					I/O	**Secure GPIO mode**: SPIO0[4]
B2	—	F4	GPIO[37]	VIO_5	I/O	**GPIO mode**: General purpose I/O 37
					I/O	**FlexSPI_SRAM_DQS**: Data strobe input/output for FlexSPI SRAM interface
					O	**CT2_MAT0**: CTimer 2 match output 0
					I	**CT_INP8**: Pin input 8 to CTIMER
					I/O	**Secure GPIO mode**: SPIO0[5]
C3	—	E4	GPIO[38]	VIO_5	I/O	**GPIO mode**: General purpose I/O 38
					I/O	**FlexSPI_SRAM_D0**: Data bit 0 for FlexSPI SRAM interface
					O	**CT2_MAT1**: CTIMER 2 match output 1
					I	**CT_INP9**: Pin input 9 to CTIMER
					I/O	**Secure GPIO mode**: SPIO0[6]
A2	—	C2	GPIO[39]	VIO_5	I/O	**GPIO mode**: General purpose I/O 39
					I/O	**FlexSPI_SRAM_D1**: Data bit 1 for FlexSPI SRAM interface
					O	**CT2_MAT2**: CTIMER 2 match output 2
					I	**CT_INP10**: Pin input 10 to CTIMER
					I/O	**Secure GPIO mode**: SPIO0[7]
A1	—	D3	GPIO[40]	VIO_5	I/O	**GPIO mode**: General purpose I/O 40
					I/O	**FlexSPI_SRAM_D2**: Data bit 2 for FlexSPI SRAM interface
					I/O	**Secure GPIO mode**: SPIO0[8]
B1	—	C3	GPIO[41]	VIO_5	I/O	**GPIO mode**: General purpose I/O 41
					I/O	**FlexSPI_SRAM_D3**: Data bit 3 for FlexSPI SRAM interface
					I/O	**Secure GPIO mode**: SPIO0[9]
G13	79	U4	GPIO[42]	VIO_6	I/O	**GPIO mode**: General purpose I/O 42
					A,I	**ADC0_0**: ADC0 channel 0
					A,I	**ACOMP0**: ACOMP channel 0
					I/O	**LCD 8080 mode**: LCD_D0 - Data line 0 for LCD [1]
					I/O	**Secure GPIO mode**: SPIO0[10]

Table 22. GPIO interface pins and other function pins*...continued*

TFBGA145	HVQFN116	WLCSP151	Symbol	Supply	Type	Description
H12	80	R4	GPIO[43]	VIO_6	I/O	**GPIO mode**: General purpose I/O 43
					I/O	**LCD 8080 mode**: LCD_D1 - Data line 1 for LCD[1]
					A,I	**ADC0_1**: ADC0 channel 1
					A,I	**ACOMP1**: ACOMP channel 1
					A,O	**DAC_B**: DAC channel B
					I/O	**Secure GPIO mode**: SPIO0[11]
J11	81	V3	GPIO[44]	VIO_6	I/O	**GPIO mode**: General purpose I/O 44
					A,O	**DAC_A**: DAC channel A
					A,I	**ADC0_2**: ADC0 channel 2
					A,I	**ACOMP2**: ACOMP channel 2
					O	**LCD SPI mode**: output signal to reset the device
					O	**LCD 8080 mode**: output signal to reset the device[1]
					I/O	**Secure GPIO mode**: SPIO0[12]
H10	82	U3	GPIO[45]	VIO_6	I/O	**GPIO mode**: General purpose I/O 45
					I	**LCD 8080 mode**: LCD tearing effect input signal used to synchronize MCU frame writing[1]
					I	**LCD SPI mode**: LCD tearing effect input signal used to synchronize MCU frame writing
					A,I	**ADC0_3**: ADC0 channel 3
					A,I	**ACOMP3**: ACOMP channel 3
					A,I	**EXT_VREF_ADC0_DAC**: ADC0 or DAC external voltage reference input
					I/O	**Secure GPIO mode**: SPIO0[13]
F12	83	R3	GPIO[46]	VIO_6	I/O	**GPIO mode**: General purpose I/O 46
					I/O	**LCD 8080 mode**: LCD_D2 - Data bit 2 for LCD[1]
					I/O	**LCD SPI mode**: LCD SPI interface data input/ output
					A,I	**ADC0_4**: ADC0 channel 4
					A,I	**ACOMP4**: ACOMP channel 4
					I/O	**Secure GPIO mode**: SPIO0[14]

Table 22. GPIO interface pins and other function pins*...continued*

TFBGA145	HVQFN116	WLCSP151	Symbol	Supply	Type	Description
E13	84	N4	GPIO[47]	VIO_6	I/O	**GPIO mode**: General purpose I/O 47
					I/O	**LCD 8080 mode**: LCD_D3 - Data bit 3 for LCD[1]
					O	**LCD SPI mode**: LCD SPI interface data/ command output
					A,I	**ADC0_5**: ADC0 channel 5
					A,I	**ACOMP5**: ACOMP channel 5
					I/O	**Secure GPIO mode**: SPIO0[15]
D13	85	Y2	GPIO[48]	VIO_6	I/O	**GPIO mode**: General purpose I/O 48
					O	**LCD 8080 mode**: LCD 8080 interface read control[1]
					O	**LCD SPI mode**: LCD SPI interface clock
					A,I	**ADC0_6**: ADC0 channel 6
					A,I	**ADC1_6**: ADC1 channel 6
					A,I	**ACOMP6**: ACOMP channel 6
					I/O	**Secure GPIO mode**: SPIO0[16]
D14	86	N5	GPIO[49]	VIO_6	I/O	**GPIO mode**: General purpose I/O 49
					I/O	**LCD 8080 mode**: LCD_D4 - Data bit 4 for LCD[1]
					O	**LCD SPI mode**: LCD SPI interface chip select
					A,I	**ADC0_7**: ADC0 channel 7
					A,I	**ADC1_7**: ADC1 channel 7
					A,I	**ACOMP7**: ACOMP channel 7
					I/O	**Secure GPIO mode**: SPIO0[17]
K12	78	R5	GPIO[50]	VIO_6	I/O	**GPIO mode**: General purpose I/O 50
					I	**FREQME_GPIO_CLK**: Frequency measure pin clock input
					I	**ADC_DAC_TRIGGER0**: Bit 2 of ADC/DAC external trigger
					I/O	**Secure GPIO mode**: SPIO0[18]

Table 22. GPIO interface pins and other function pins*...continued*

TFBGA145	HVQFN116	WLCSP151	Symbol	Supply	Type	Description
M8	—	D8	GPIO[51]	VIO_1	I/O	**GPIO mode**: General purpose I/O 51
					I	**PDM_DATA01**: PDM data input for DMIC channels 0 and 1
					I/O	**LCD 8080 mode**: LCD_D5 - Data bit 5 for LCD[1]
					O	**CT2_MAT3**: CTIMER 2 match output 3
					I	**CT_INP11**: Pin input 11 to CTIMER
					O	**ACOMP0_GPIO_OUT**: Analog comparator 0 level output
					I/O	**Secure GPIO mode**: SPIO0[19]
K8	—	E8	GPIO[52]	VIO_1	I/O	**GPIO mode**: General purpose I/O 52
					I	**PDM_DATA23**: PDM data input for DMIC channels 2 and 3
					O	**CT3_MAT0**: CTIMER 3 match output 0
					I	**CT_INP12**: Pin input 12 to CTIMER
					O	**ACOMP0_EDGE_PULSE**: Analog comparator 0 edge pulse
					I/O	**LCD 8080 mode**: LCD_D6 - Data bit 6 for LCD[1]
					I/O	**Secure GPIO mode**: SPIO0[20]
L11	—	F8	GPIO[53]	VIO_1	I/O	**GPIO mode**: General purpose I/O 53
					O	**PDM_CLK01**: PDM clock output for DMIC channels 0 and 1
					O	**CT3_MAT1**: CTIMER 3 match output 1
					I	**CT_INP13**: Pin input 13 to CTIMER
					O	**ACOMP1_GPIO_OUT**: Analog comparator 1 level output
					I/O	**LCD 8080 mode**: LCD_D7 - Data bit 7 for LCD[1]
					I/O	**Secure GPIO mode**: SPIO0[21]
					I	**FC14_CTS_SDA_SSELN0_USART**: Flexcomm 14 USART clear-to-send[2]
					I/O	**FC14_CTS_SDA_SSELN0_SPI**: Flexcomm 14 SPI chip select[2]

Table 22. GPIO interface pins and other function pins*...continued*

TFBGA145	HVQFN116	WLCSP151	Symbol	Supply	Type	Description
M10	—	A8	GPIO[54]	VIO_1	I/O	**GPIO mode**: General purpose I/O 54
					O	**ACOMP1_EDGE_PULSE**: Analog comparator 1 edge pulse
					O	**PDM_CLK23**: PDM clock output for DMIC channels 2 and 3
					O	**CT3_MAT2**: CTIMER 3 match output 2
					I	**CT_INP14**: Pin input 14 to CTIMER
					O	**LCD 8080 mode**: LCD 8080 interface write control signal [1]
					I/O	**Secure GPIO mode**: SPIO0[22]
					I/O	**FC14_SCK_USART**: Flexcomm 14 USART clock[2]
					I/O	**FC14_SCK_I2S**: Flexcomm 14 I2S clock[2]
					I/O	**FC14_SCK_SPI**: Flexcomm 14 SPI clock[2]
K6	—	G8	GPIO[55]	VIO_1	I/O	**GPIO mode**: General purpose I/O 55
					O	**SCT0_OUT9**: SCTimer 0/PWM output 9
					I	**ADC_DAC_TRIGGER1**: Bit 3 of ADC/DAC external trigger
					I/O	**Secure GPIO mode**: SPIO0[23]
					O	**FC14_RTS_SCL_SSELN1_USART**: Flexcomm 14 USART request-to-send [2]
A14	—	—	GPIO[56]	VIO_6	I/O	**GPIO mode**: General purpose I/O 56
					O	**LCD 8080 mode**: LCD 8080 interface chip select
					O	**ENET_MDC**: Ethernet controller data clock
					I/O	**Secure GPIO mode**: SPIO0[24]
					O	**FC14_TXD_SCL_MISO_WS_USART**: Flexcomm 14 USART transmitter
					I/O	**FC14_TXD_SCL_MISO_WS_I2C**: Flexcomm 14 I2C clock
					I/O	**FC14_TXD_SCL_MISO_WS_I2S**: Flexcomm 14 I2S word select
					I/O	**FC14_TXD_SCL_MISO_WS_SPI**: Flexcomm 14 SPI controller in/target out

Table 22. GPIO interface pins and other function pins*...continued*

TFBGA145	HVQFN116	WLCSP151	Symbol	Supply	Type	Description
B13	—	—	GPIO[57]	VIO_6	I/O	**GPIO mode**: General purpose I/O 57
					O	**LCD 8080 mode**: LCD 8080 interface data/ command signal
					I/O	**ENET_MDIO**: Ethernet data input/output management
					I/O	**Secure GPIO mode**: SPIO0[25]
					I	**FC14_RXD_SDA_MOSI_DATA_USART**: Flexcomm 14 USART receiver
					I/O	**FC14_RXD_SDA_MOSI_DATA_I2C**: Flexcomm 14 I2C data in/out
					I/O	**FC14_RXD_SDA_MOSI_DATA_I2S**: Flexcomm 14 I2S receiver/transmitter
					I/O	**FC14_RXD_SDA_MOSI_DATA_SPI**: Flexcomm 14 SPI controller out/target in
G11	—	—	GPIO[58]	VIO_6	I/O	**GPIO mode**: General purpose I/O 58
					O	**ENET_TX_DATA0**: Bit 0 of Ethernet transmit data
					A,I	**ADC1_3**: ADC1 channel 3
					A,I	**EXT_VREF_ADC1**: ADC1 external voltage reference input
					I/O	**Secure GPIO mode**: SPIO0[26]
D12	—	—	GPIO[59]	VIO_6	I/O	**GPIO mode**: General purpose I/O 59
					O	**ENET_TX_DATA1**: Bit 1 of Ethernet transmit data
					A,I	**ADC1_2**: ADC1 channel 2
					I/O	**Secure GPIO mode**: SPIO0[27]
E11	—	—	GPIO[60]	VIO_6	I/O	**GPIO mode**: General purpose I/O 60
					O	**ENET_TX_EN**: Ethernet transmit mode enable
					A,I	**ADC1_1**: ADC1 channel 1
					I/O	**Secure GPIO mode**: SPIO0[28]
A13	—	—	GPIO[61]	VIO_6	I/O	**GPIO mode**: General purpose I/O 61
					I/O	**ENET_TIMER1**: Bit 1 of Ethernet controller timer
					A,I	**ADC1_0**: ADC1 channel 0
					I/O	**Secure GPIO mode**: SPIO0[29]
B14	—	—	GPIO[62]	VIO_6	I/O	**GPIO mode**: General purpose I/O 62
					I	**ENET_RX_EN**: Ethernet controller receive mode enable
					I/O	**Secure GPIO mode**: SPIO0[30]

Table 22. GPIO interface pins and other function pins*...continued*

TFBGA145	HVQFN116	WLCSP151	Symbol	Supply	Type	Description
A15	—	—	GPIO[63]	VIO_6	I/O	**GPIO mode**: General purpose I/O 63
					I	**ENET_RX_ER**: Ethernet controller receive error
					I/O	**Secure GPIO mode**: SPIO0[31]

[1] WLCSP151 and HVQFN116 packages do not support LCD 8080
[2] WLCSP151 and HVQFN116 packages do not support Flexcomm14

7.6.2 Wi-Fi RF front-end interface

Table 23. Wi-Fi RF front-end interface

TFBGA145	HVQFN116	WLCSP151	Pin name	Type	Supply	Description
N3	37	G16	RF_CNTL0	O	VIO_RF	Wi-Fi RF front-end control line 0
P5	38	H16	RF_CNTL1	O	VIO_RF	Wi-Fi RF front-end control line 1
P6	40	H12	RF_CNTL2	O	VIO_RF	Wi-Fi RF front-end control line 2
P7	41	H14	RF_CNTL3	O	VIO_RF	Wi-Fi RF front-end control line 3

7.6.3 Wi-Fi radio interface

Table 24. Wi-Fi radio interface

TFBGA145	HVQFN116	WLCSP151	Pin name	Type	Supply	Description
R9	47	M18	RF_TR_2	A, I/O	AVDD18	Wi-Fi transmit/receive (2.4 GHz)
R14	55	W18	RF_TR_5	A, I/O	AVDD18	Wi-Fi transmit/receive (5 GHz)

7.6.4 Bluetooth radio interface

Table 25. Bluetooth radio interface

TFBGA145	HVQFN116	WLCSP151	Pin name	Type	Supply	Description
R4	35	D18	BRF_ANT	A, I/O	AVDD18	Bluetooth radio transmit/receive

7.6.5 High-speed USB host/device interface

Table 26. High-speed USB host/device interface

TFBGA145	HVQFN116	WLCSP151	Pin name	Type	Supply	Description
A7	103	G1	AVDD18_USB	Power	—	USB 1.8 V analog power supply. See Section 7.6.19 "Power supply and ground pins".
B8	102	G2	AVDD33_USB	Power	—	USB 3.3 V analog power supply. See Section 7.6.19 "Power supply and ground pins".
D8	104	F2	USB_DP	A, I/O	AVDD33_USB	USB bus data+
C7	105	F1	USB_DM	A, I/O	AVDD33_USB	USB bus data-
B7	106	J3	USB_ID	A, I	AVDD33_USB	USB OTG ID pin
D6	107	H3	USB_VBUS	A, I/O	—	VBUS selection, 5 V analog power supply

7.6.6 FlexSPI flash interface

Table 27. FlexSPI Flash interface

Symbol	TFBGA145	HVQFN116	WLCSP151	Pin name	Type	Supply	Description
GPIO[28]	F4	2	F5	FlexSPI_flash_SSEL0	O	VIO_4	FlexSPI flash client select 0
GPIO[29]	D2	3	D4	FlexSPI_flash_DQS	I/O	VIO_4	FlexSPI flash data strobe input/output
GPIO[30]	F3	9	A4	FlexSPI_flash_D0	I/O	VIO_4	Data bit 0 for FlexSPI flash
GPIO[31]	D3	5	D5	FlexSPI_flash_D1	I/O	VIO_4	Data bit 1 for FlexSPI flash
GPIO[32]	F2	7	C4	FlexSPI_flash_D2	I/O	VIO_4	Data bit 2 for FlexSPI flash
GPIO[33]	G3	8	C5	FlexSPI_flash_D3	I/O	VIO_4	Data bit 3 for FlexSPI flash
GPIO[34]	E3	4	E5	FlexSPI_flash_CLK0	O	VIO_4	Clock 0 signal for FlexSPI flash interface

7.6.7 FlexSPI SRAM interface

Table 28. FlexSPI SRAM interface

Symbol	TFBGA145	HVQFN116	WLCSP151	Pin name	Type	Supply	Description
GPIO[35]	B3	—	E3	FlexSPI_SRAM_CLK0	O	VIO_5	Clock 0 signal for FlexSPI SRAM interface
GPIO[36]	B4	—	D2	FlexSPI_SRAM_SSEL0	O	VIO_5	FlexSPI SRAM client select 0
GPIO[37]	B2	—	F4	FlexSPI_SRAM_DQS	I/O	VIO_5	Data strobe input/output for FlexSPI SRAM interface
GPIO[38]	C3	—	E4	FlexSPI_SRAM_D0	I/O	VIO_5	Data bit 0 for FlexSPI SRAM
GPIO[39]	A2	—	C2	FlexSPI_SRAM_D1	I/O	VIO_5	Data bit 1 for FlexSPI SRAM interface
GPIO[40]	A1	—	D3	FlexSPI_SRAM_D2	I/O	VIO_5	Data bit 2 for FlexSPI SRAM interface
GPIO[41]	B1	—	C3	FlexSPI_SRAM_D3	I/O	VIO_5	Data bit 3 for FlexSPI SRAM interface

7.6.8 USART interface

Table 29. USART interface

Symbol	TFBGA145	HVQFN116	WLCSP151	Supply	Type	Pin name and description
GPIO[0]	M1	—	D12	VIO_1	I	**FC0_CTS_SDA_SSELN0_USART**: USART clear-to-send input signal (Flexcomm 0)
GPIO[2]	F10	90	U2	VIO_6	I	**FC0_RXD_SDA_MOSI_DATA_USART**: USART receive input signal (Flexcomm 0)
GPIO[3]	C13	91	L4	VIO_6	O	**FC0_TXD_SCL_MISO_WS_USART** USART transmit output signal (Flexcomm 0)
GPIO[4]	F8	92	N3	VIO_6	I/O	**FC0_SCK_USART**: USART clock (Flexcomm 0)
GPIO[5]	L7	23	D10	VIO_1	O	**FC0_RTS_SCL_SSELN1_USART**: USART request-to-send output signal (Flexcomm 0)
GPIO[6]	L4	24	F12	VIO_1	I	**FC1_CTS_SDA_SSELN0_USART**: USART clear-to-send input signal (Flexcomm 1)
GPIO[7]	L9	21	F10	VIO_1	I/O	**FC1_SCK_USART**: USART clock (Flexcomm 1)
GPIO[8]	M6	22	E10	VIO_1	O	**FC1_TXD_SCL_MISO_WS_USART**: USART transmit output signal (Flexcomm 1)
GPIO[9]	M4	25	G10	VIO_1	I	**FC1_RXD_SDA_MOSI_DATA_USART**: USART receive input signal (Flexcomm 1)
GPIO[10]	M3	26	E12	VIO_1	O	**FC1_RTS_SCL_SSELN1_USART**: USART request-to-send output signal (Flexcomm 1)
GPIO[13]	G5	10	F6	VIO_2	I	**FC2_RXD_SDA_MOSI_DATA_USART**: USART receive input signal (Flexcomm 2)
GPIO[14]	K4	19	F7	VIO_2	O	**FC2_TXD_SCL_MISO_WS_USART**: USART transmit output signal (Flexcomm 2)
GPIO[15]	H3	11	D6	VIO_2	I/O	**FC2_SCK_USART**: USART clock (Flexcomm 2)
GPIO[16]	J3	12	C6	VIO_2	I	**FC2_CTS_SDA_SSELN0_USART**: USART clear-to-send input signal (Flexcomm 2)
GPIO[17]	H2	13	E7	VIO_2	O	**FC2_RTS_SCL_SSELN1_USART**: USART request-to-send output signal (Flexcomm 2)
GPIO[19]	L3	16	D7	VIO_2	O	**FC3_RTS_SCL_SSELN1_USART**: USART request-to-send output signal (Flexcomm 3)
GPIO[20]	K2	17	C7	VIO_2	I	**FC3_CTS_SDA_SSELN0_USART**: USART clear-to-send input signal (Flexcomm 3)
GPIO[24]	E5	110	F3	VIO_3	I	**FC3_RXD_SDA_MOSI_DATA_USART**: USART receive input signal (Flexcomm 3)
GPIO[25]	E7	111	G3	VIO_3	I/O	**FC3_SCK_USART**: USART clock (Flexcomm 3)
GPIO[26]	F6	112	H4	VIO_3	O	**FC3_TXD_SCL_MISO_WS_USART**: USART transmit output signal (Flexcomm 3)
GPIO[53]	L11	—	—	VIO_1	I	**FC14_CTS_SDA_SSELN0_USART**: USART clear-to-send input signal (Flexcomm 14)
GPIO[54]	M10	—	—	VIO_1	I/0	**FC14_SCK_USART**: USART clock (Flexcomm 14)
GPIO[55]	K6	—	—	VIO_1	0	**FC14_RTS_SCL_SSELN1_USART**: USART request-to-send output signal (Flexcomm 14)

Table 29. USART interface*...continued*

Symbol	TFBGA145	HVQFN116	WLCSP151	Supply	Type	Pin name and description
GPIO[56]	A14	—	—	VIO_6	0	**FC14_TXD_SCL_MISO_WS_USART**: USART transmit output signal (Flexcomm 14)
GPIO[57]	B13	—	—	VIO_6	I	**FC14_RXD_SDA_MOSI_DATA_USART**: USART receive input signal (Flexcomm 14)

7.6.9 I2C bus interface

Table 30. I2C bus interface

Symbol	TFBGA145	HVQFN116	WLCSP151	Supply	Type	Pin name and description
GPIO[2]	F10	90	U2	VIO_6	I/O	**FC0_RXD_SDA_MOSI_DATA_I2C**: I2C data in/data out (Flexcomm 0)
GPIO[3]	C13	91	L4	VIO_6	I/O	**FC0_TXD_SCL_MISO_WS_I2C**: I2C clock (Flexcomm 0)
GPIO[8]	M6	22	E10	VIO_1	I/O	**FC1_TXD_SCL_MISO_WS_I2C**: I2C clock (Flexcomm 1)
GPIO[9]	M4	25	G10	VIO_1	I/O	**FC1_RXD_SDA_MOSI_DATA_I2C**: I2C data in/data out (Flexcomm 1)
GPIO[13]	G5	10	F6	VIO_2	I/O	**FC2_RXD_SDA_MOSI_DATA_I2C**: I2C data in/data out (Flexcomm 2)
GPIO[14]	K4	19	F7	VIO_2	I/O	**FC2_TXD_SCL_MISO_WS_I2C**: I2C clock (Flexcomm 2)
GPIO[16]	J3	12	C6	VIO_2	I/O	**FC2_CTS_SDA_SSELN0_I2C_COPY**: (I2C_SDA) Flexcomm 2 backup-I2C data in/out
GPIO[17]	H2	13	E7	VIO_2	I/O	**FC2_RTS_SCL_SSELN1_I2C_COPY** (I2C_SCL) Flexcomm 2 backup-I2C clock
GPIO[19]	L3	16	D7	VIO_2	I/O	**FC3_RTS_SCL_SSELN1_I2C_COPY**: (I2C_SCL) Flexcomm 3 backup-I2C clock
GPIO[20]	K2	17	C7	VIO_2	I/O	**FC3_CTS_SDA_SSELN0_I2C_COPY**: (I2C_SDA) Flexcomm 3 backup-I2C data in/out
GPIO[24]	E5	110	F3	VIO_3	I/O	**FC3_RXD_SDA_MOSI_DATA_I2C**: I2C data in/data out (Flexcomm 3)
GPIO[26]	F6	112	H4	VIO_3	I/O	**FC3_TXD_SCL_MISO_WS_I2C**: I2C clock (Flexcomm 3)
GPIO[56]	A14	—	—	VIO_6	I/O	**FC14_TXD_SCL_MISO_WS_I2C**: I2C clock (Flexcomm 14)
GPIO[57]	B13	—	—	VIO_6	I/O	**FC14_RXD_SDA_MOSI_DATA_I2C**: I2C data in/ data out (Flexcomm 14)

7.6.10 I2S bus interface

Table 31. I2S bus interface (Flexcomm interfaces 0 to 3 and 14)

Symbol	TFBGA145	HVQFN116	WLCSP151	Supply	Type	Pin name and description
GPIO[2]	F10	90	U2	VIO_6	I/O	**FC0_RXD_SDA_MOSI_DATA_I2S**: I2S receiver/ transmitter (Flexcomm 0)
GPIO[3]	C13	91	L4	VIO_6	I/O	**FC0_TXD_SCL_MISO_WS_I2S**: I2S word select (Flexcomm 0)
GPIO[4]	F8	92	N3	VIO_6	I/O	**FC0_SCK_I2S**: I2S clock (Flexcomm 0)
GPIO[7]	L9	21	F10	VIO_1	I/O	**FC1_SCK_I2S**: I2S clock (Flexcomm 1)
GPIO[8]	M6	22	E10	VIO_1	I/O	**FC1_TXD_SCL_MISO_WS_I2S**: I2S word select (Flexcomm 1)
GPIO[9]	M4	25	G10	VIO_1	I/O	**FC1_RXD_SDA_MOSI_DATA_I2S**: I2S receiver/ transmitter (Flexcomm 1)
GPIO[13]	G5	10	F6	VIO_2	I/O	**FC2_RXD_SDA_MOSI_DATA_I2S**: I2S receiver/ transmitter (Flexcomm 2)
GPIO[14]	K4	19	F7	VIO_2	I/O	**FC2_TXD_SCL_MISO_WS_I2S**: I2S word select (Flexcomm 2)
GPIO[15]	H3	11	D6	VIO_2	I/O	**FC2_SCK_I2S**: I2S clock (Flexcomm 2)
GPIO[24]	E5	110	F3	VIO_3	I/O	**FC3_RXD_SDA_MOSI_DATA_I2S**: I2S receiver/ transmitter (Flexcomm 3)
GPIO[25]	E7	111	G3	VIO_3	I/O	**FC3_SCK_I2S**: I2S clock (Flexcomm 3)
GPIO[26]	F6	112	H4	VIO_3	I/O	**FC3_TXD_SCL_MISO_WS_I2S**: I2S word select (Flexcomm 3)
GPIO[54]	M10	—	—	VIO_1	I/O	**FC14_SCK_I2S**: I2S clock (Flexcomm 14)
GPIO[56]	A14	—	—	VIO_6	I/O	**FC14_TXD_SCL_MISO_WS_I2S**: I2S word select (Flexcomm 14)
GPIO[57]	B13	—	—	VIO_6	I/O	**FC14_RXD_SDA_MOSI_DATA_I2S**: I2S transmitter/ receiver (Flexcomm 14)

7.6.11 SPI interface

Table 32. SPI interface

Symbol	TFBGA145	HVQFN116	WLCSP151	Supply	Type	Pin name and description
GPIO[0]	M1	—	D12	VIO_1	I/O	**FC0_CTS_SDA_SSELN0_SPI**: SPI chip select (Flexcomm 0)
GPIO[2]	F10	90	U2	VIO_6	I/O	**FC0_RXD_SDA_MOSI_DATA_SPI**: SPI controller out/target in (Flexcomm 0)
GPIO[3]	C13	91	L4	VIO_6	I/O	**FC0_TXD_SCL_MISO_WS_SPI**: SPI controller in/ target out (Flexcomm 0)
GPIO[4]	F8	92	N3	VIO_6	I/O	**FC0_SCK_SPI**: SPI clock (Flexcomm 0)
GPIO[6]	L5	24	F12	VIO_1	I/O	**FC1_CTS_SDA_SSELN0_SPI**: SPI chip select (Flexcomm 1)
GPIO[7]	L9	21	F10	VIO_1	I/O	**FC1_SCK_SPI**: SPI clock (Flexcomm 1)
GPIO[8]	M6	22	E10	VIO_1	I/O	**FC1_TXD_SCL_MISO_WS_SPI**: SPI controller in/ target out (Flexcomm 1)
GPIO[9]	M4	25	G10	VIO_1	I/O	**FC1_RXD_SDA_MOSI_DATA_SPI**: SPI controller out/target in (Flexcomm 1)
GPIO[13]	G5	10	F6	VIO_2	I/O	**FC2_RXD_SDA_MOSI_DATA_SPI**: SPI controller out/target in (Flexcomm 2)
GPIO[14]	K4	19	F7	VIO_2	I/O	**FC2_TXD_SCL_MISO_WS_SPI**: SPI controller in/ target out (Flexcomm 2)
GPIO[15]	H3	11	D6	VIO_2	I/O	**FC2_SCK_SPI**: SPI clock (Flexcomm 2)
GPIO[16]	J3	12	C6	VIO_2	I/O	**FC2_CTS_SDA_SSELN0_SPI**: SPI chip select (Flexcomm 2)
GPIO[20]	K2	17	C7	VIO_2	I/O	**FC3_CTS_SDA_SSELN0_SPI**: SPI chip select (Flexcomm 3)
GPIO[24]	E5	110	F3	VIO_3	I/O	**FC3_RXD_SDA_MOSI_DATA_SPI**: SPI controller out/target in (Flexcomm 3)
GPIO[25]	E7	111	G3	VIO_3	I/O	**FC3_SCK_SPI**: SPI clock (Flexcomm 3)
GPIO[26]	F6	112	H4	VIO_3	I/O	**FC3_TXD_SCL_MISO_WS_SPI**: SPI controller in/ target out (Flexcomm 3)
GPIO[53]	L11	—	—	VIO_1	I/O	**FC14_CTS_SDA_SSELN0_SPI**: SPI chip select (Flexcomm 14)
GPIO[54]	M10	—	—	VIO_1	I/O	**FC14_SCK_SPI**: SPI clock (Flexcomm 14)
GPIO[56]	A14	—	—	VIO_6	I/O	**FC14_TXD_SCL_MISO_WS_SPI**: SPI controller in/ target out (Flexcomm 14)
GPIO[57]	B13	—	—	VIO_6	I/O	**FC14_RXD_SDA_MOSI_DATA_SPI**: SPI controller out/target in (Flexcomm 14)

7.6.12 SDIO interface

Table 33. SDIO interface

Symbol	TFBGA145	HVQFN116	WLCSP151	Pin name	Type	Supply	Description
GPIO[15]	H3	11	D6	SDIO_CLK	I	VIO_2	SDIO clock input
GPIO[16]	J3	12	C6	SDIO_DAT3	I/O	VIO_2	SDIO data input/output 3
GPIO[17]	H2	13	E7	SDIO_CMD	I/O	VIO_2	SDIO command line
GPIO[18]	K3	15	E6	SDIO_DAT2	I/O	VIO_2	SDIO data input/output 2
GPIO[19]	L3	16	D7	SDIO_DAT0	I/O	VIO_2	SDIO data input/output 0
GPIO[20]	K2	17	C7	SDIO_DAT1	I/O	VIO_2	SDIO data input/output 1

7.6.13 Ethernet interface

Table 34. Ethernet interface

Symbol	TFBGA145	HVQFN116	WLCSP151	Pin name	Type	Supply	Description
GPIO[22]	B6	108	E2	ENET_RX_DATA0	I	VIO_3	Ethernet input data transferred from the PHY to the media-access controller when ENET_RX_EN is asserted.
GPIO[23]	B7	109	E1	ENET_RX_DATA1	I	VIO_3	
GPIO[56]	A1	—	—	ENET_MDC	O	VIO_6	Output clock: provides a timing reference to the PHY for data transfers on ENET_MDIO signal.
GPIO[57]	B13	—	—	ENET_MDIO	I/O	VIO_6	Transfers control information between the external PHY and the media-access controller. Data is synchronous to ENET_MDC. This signal is an input after reset.
GPIO[58]	G11	—	—	ENET_TX_DATA0	O	VIO_6	Serial output Ethernet data. Only valid during ENET_TX_EN assertion.
GPIO[59]	D12	—	—	ENET_TX_DATA1	O	VIO_6	
GPIO[60]	E11	—	—	ENET_TX_EN	O	VIO_6	Indicates when valid nibbles are present on the MII.
GPIO[62]	B14	—	—	ENET_RX_EN	I	VIO_6	Asserting this input indicates that the PHY has valid nibbles present on the MII. Must remain asserted from the first recovered nibble of the frame through to the last nibble.
GPIO[63]	A15	—	—	ENET_RX_ER	I	VIO_6	When asserted with ENET_RX_EN, indicates that the PHY has detected an error in the current frame.
GPIO[24]	E5	110	F3	ENET_TIMER2	I/O	VIO_3	Captures and compares the block input/output event bus.[1]
GPIO[26]	F6	112	H4	ENET_TIMER3	I/O	VIO_3	
GPIO[27]	C5	114	G4	ENET_TIMER0	I/O	VIO_3	
GPIO[61]	A13	—	—	ENET_TIMER1	I/O	VIO_6	

[1] When configured for capture and a rising edge is detected, the current timer value is latched and transferred into the corresponding ENET_TCCRn register for inspection by software.
When configured for compare, the corresponding signal ENET_TIMER is asserted for one cycle when the timer reaches the compare value programmed in register ENET_TCCRn. An interrupt or DMA request can be triggered if the corresponding bit in ENET_TCSRn[TIE] or ENET_TCSRn[TDRE] is set.

7.6.14 LCD interface

Table 35. LCD SPI interface signals

Symbol	TFBGA145	HVQFN116	WLCSP151	Pin name	Type	Supply	Description
GPIO[44]	J11	81	V3	LCD_RESETN	O	VIO_6	LCD output signal to reset the device
GPIO[45]	H10	82	U3	LCD_TE	I	VIO_6	LCD tearing effect input signal used to synchronize MCU frame writing
GPIO[46]	F12	83	R3	LCD_SPI_DATA	I/O	VIO_6	LCD SPI interface data input/output
GPIO[47]	E13	84	N4	LCD_SPI_DC	O	VIO_6	LCD SPI interface data/ command select
GPIO[48]	D13	85	Y2	LCD_SPI_SCK	O	VIO_6	LCD SPI interface clock
GPIO[49]	D14	86	N5	LCD_SPI_SS	O	VIO_6	LCD SPI interface chip select

Table 36. LCD 8080 interface signals

Symbol	TFBGA145	HVQFN116	WLCSP151	Pin name	Type	Supply	Description
GPIO[42]	G13	79	U4	LCD_8080_DATA0	I/O	VIO_6	LCD 8080 interface data line 0
GPIO[43]	H12	80	R4	LCD_8080_DATA1	I/O	VIO_6	LCD 8080 interface data line 1
GPIO[44]	J11	81	V3	LCD_RESETN	O	VIO_6	LCD output signal to reset the device
GPIO[45]	H10	82	U3	LCD_TE	I	VIO_6	LCD tearing effect input signal used to synchronize MCU frame writing
GPIO[46]	F12	83	R3	LCD_8080_DATA2	I/O	VIO_6	LCD 8080 interface data line 2
GPIO[47]	E13	84	N4	LCD_8080_DATA3	I/O	VIO_6	LCD 8080 interface data line 3
GPIO[48]	D13	85	Y2	LCD_8080_RD	O	VIO_6	LCD 8080 interface read control signal
GPIO[49]	D14	86	N5	LCD_8080_DATA4	I/O	VIO_6	LCD 8080 interface data line 4
GPIO[51]	M8	—	D8	LCD_8080_DATA5	I/O	VIO_1	LCD 8080 interface data line 5
GPIO[52]	K8	—	E8	LCD_8080_DATA6	I/O	VIO_1	LCD 8080 interface data line 6
GPIO[53]	L11	—	F8	LCD_8080_DATA7	I/O	VIO_1	LCD 8080 interface data line 7
GPIO[54]	M10	—	A8	LCD_8080_WR	O	VIO_1	LCD 8080 interface write control signal
GPIO[56]	A14	—	—	LCD_8080_CS	O	VIO_6	LCD 8080 interface chip select
GPIO[57]	B13	—	—	LCD_8080_DC	O	VIO_6	LCD 8080 interface data/command select

7.6.15 WCI-2 coexistence interface

Table 37. WCI-2 coexistence interface

Pins may be Multi-Functional Pins (MFP).

Symbol	TFBGA145	HVQFN116	WLCSP151	Pin name	Type	Supply	Description
GPIO[4]	F8	92	N3	WCI-2_SIN	I	VIO_6	Input signal from external radio. Multi-functional pin: GPIO[4] input/output. Muxed with EXT_STATE signal of PTA interface.
—	J13	75	R6	WCI-2_SOUT	O	AVDD18	Output signal to external radio. Muxed with EXT_FREQ signal of PTA interface.

7.6.16 PTA coexistence interface

Table 38. PTA coexistence interface

Pins may be Multi-Functional Pins (MFP).

Symbol	TFBGA145	HVQFN116	WLCSP151	Pin name	Type	Supply	Description
GPIO[4]	F8	92	N3	EXT_STATE	I	VIO_6	External radio state input signal (optional) - muxed with GPIO[4] and WCI-2_SIN signal of WCI-2 interface. External radio traffic direction (Tx/Rx): • 1: Tx • 0: Rx
—	J13	75	R6	EXT_FREQ	I	AVDD18	External radio frequency input signal (optional) - muxed with WCI-2_SOUT signal of WCI-2 interface. Frequency overlap between external radio and Wi-Fi: • 1: overlap • 0: non-overlap This signal is useful when the external radio is a frequency hopping device.
—	K12	74	N6	EXT_PRI	I	AVDD18	External radio input priority signal (optional) Priority of the request from the external radio. Can support 1 bit priority (sample once). Can also have Tx/Rx info following the priority info if EXT_STATE is not used.
—	K13	73	R7	EXT_GNT	O	AVDD18	External radio grant output signal (mandatory).
—	M12	72	U7	EXT_REQ	I	AVDD18	Request from external radio (mandatory).

7.6.17 Clock control interface

Table 39. Clock control interface

Symbol	TFBGA145	HVQFN116	WLCSP151	Pin name	Type	Supply	Description
—	H15	69	Y5	XTAL_IN	A,I	AVDD18	Crystal oscillator input
—	G15	70	V5	XTAL_OUT	A,O	AVDD18	Crystal oscillator output
GPIO[4]	F8	92	N3	CLKIN_FRM_PD	I	VIO_6	Clock from pad which can replace the internal clock
GPIO[5]	L7	23	D10	MCLK	I/O	VIO_1	Input or output for I2S and/or digital microphone
GPIO[15]	H3	11	D6	UCLK (USIM mode)	O	VIO_2	USIM clock
GPIO[22]	B6	108	E2	AON_XTAL32K_IN	A,I	VIO_3	Always-on 32K crystal input signal
GPIO[22]	B6	108	E2	SLP_CLK_32K	I	VIO_3	External sleep clock input signal
GPIO[23]	B5	109	E1	AON_XTAL32K_OUT	A,O	VIO_3	Always-on 32K crystal output signal
GPIO[50]	K12	78	R5	FREQME_GPIO_CLK	I	VIO_6	Frequency measure pin clock input
GPIO[53]	L11	—	F8	PDM_CLK01	O	VIO_1	PDM clock output for DMIC channels 0 and 1
GPIO[54]	M10	—	A8	PDM_CLK23	O	VIO_1	PDM clock output for DMIC channels 2 and 3

7.6.18 Power down pin

Table 40. Power down pin

TFBGA145	HVQFN116	WLCSP151	Pin name	Type	Supply	Description
E9	94	R2	PDn	I	VBAT	Full Power-down (input) (active low) 0 = full power-down mode 1 = normal mode • PDn can accept an input of 1.75 V to 3.63 V • PDn may be driven by the host • PDn must be high for normal operation No internal pull-up on this pin. This pin has an always-on internal weak pull-down.

7.6.19 Power supply and ground pins

Note: *See Section 10 "Recommended operating conditions" for ratings.*

Table 41. Power supply and ground pins

TFBGA145	HVQFN116	WLCSP151	Pin name	Type	Description
D4 D15 H1 K10	18 42 76 115	G5 H5 H7 H8 L5 L7 L8	VCORE	Power	Nominal 1.05 V core power supply input
K1	20	C9	VIO_1	Power	1.8 V/3.3 V digital I/O power supply
F1	14	A5	VIO_2	Power	1.8 V/3.3 V digital I/O power supply
A5	113	D1	VIO_3	Power	1.8 V/3.3 V digital I/O power supply
D1	6	A3	VIO_4	Power	1.8 V/3.3 V digital I/O power supply
A4	—	C1	VIO_5	Power	1.8 V/3.3 V digital I/O power supply
B15	89	V2	VIO_6	Power	1.8 V/3.3 V digital I/O power supply
R6	39	F18	VIO_RF	Power	1.8 V/3.3 V digital I/O power supply
B8	102	G2	AVDD33_USB	Power	3.3 V USB analog power supply
A7	103	G1	AVDD18_USB	Power	1.8 V USB analog power supply
B12 F14 F15 J15 K15 L15 M15 N15 P1 R1 R2 R10 R11 R12	28 31 33 49 51 53 61 62 63 65 66 67 68 71 77 93	A14 A16 D16 P17 T18 U5 W8 Y6 Z11 Z15	AVDD18	Power	1.8 V analog power supply
C9	101	H2	ISENSE	Power	USB current source Connect pin to ground with resistance of 6.04 kΩ
C11	95	N2	BUCK18_SENSE	Power	Internal buck BUCK18 voltage sense. This pin senses the output of BUCK18_VOUT
A11	96	N1	BUCK18_VOUT	Power	Internal buck BUCK18 voltage output

Table 41. Power supply and ground pins*...continued*

TFBGA145	HVQFN116	WLCSP151	Pin name	Type	Description
B9	100	J2	BUCK11_SENSE	Power	Internal buck BUCK11 voltage sense. This pin senses the output of BUCK11_VOUT
A9	99	J1	BUCK11_VOUT	Power	Internal buck BUCK11 voltage output
R8 R15	44 45 56 57	J15 Y17	VPA	Power	3.3 V analog power supply
A10 B10	97 98	L1 L2	VBAT	Power	Input power supply to internal buck regulators

7.6.20 Reset and wake-up

Table 42. Reset and wake-up

Symbol	TFBGA145	HVQFN116	WLCSP151	Pin name	Type	Supply	Description
GPIO[12]	N8	43	H18	SD_HOST_INT	O	VIO_RF	SD host interrupt output signal
GPIO[24]	E5	110	F3	AON_WAKEUP	I	VIO_3	Always-on wake-up input signal
GPIO[25]	E7	111	G3	AON_WAKEUP	I	VIO_3	Always-on wake-up input signal

7.6.21 Analog peripheral interface

Table 43. Analog peripheral interface

Symbol	TFBGA145	HVQFN116	WLCSP151	Pin name	Type	Supply	Description
DAC							
GPIO[43]	H12	80	R4	DAC_B	A,O	VIO_6	DAC channel B
GPIO[44]	J11	81	V3	DAC_A	A,O	VIO_6	DAC channel A
GPIO[45]	H10	82	U3	EXT_VREF_ADC0_ DAC	A,I	VIO_6	ADC0 or DAC external voltage reference input
GPIO[50]	K12	78	R5	ADC_DAC_TRIGGER0	I	VIO_6	Bit 2 of ADC/DAC external trigger
GPIO[55]	K6	—	G8	ADC_DAC_TRIGGER1	I	VIO_1	Bit 3 of ADC/DAC external trigger
ADC							
GPIO[42]	G13	79	U4	ADC0_0	A,I	VIO_6	ADC0 channel 0
GPIO[43]	H12	80	R4	ADC0_1	A,I	VIO_6	ADC0 channel 1
GPIO[44]	J11	81	V3	ADC0_2	A,I	VIO_6	ADC0 channel 2
GPIO[45]	H12	82	U3	ADC0_3	A,I	VIO_6	ADC0 channel 3
GPIO[46]	F12	83	R3	ADC0_4	A,I	VIO_6	ADC0 channel 4
GPIO[47]	E13	84	N4	ADC0_5	A,I	VIO_6	ADC0 channel 5
GPIO[48]	D13	85	Y2	ADC0_6	A,I	VIO_6	ADC0 channel 6
GPIO[48]	D13	85	Y2	ADC1_6	A,I	VIO_6	ADC1 channel 6
GPIO[49]	D14	86	N5	ADC0_7	A,I	VIO_6	ADC0 channel 7
GPIO[49]	D14	86	N5	ADC1_7	A,I	VIO_6	ADC1 channel 7
GPIO[50]	K12	78	R5	ADC_DAC_TRIGGER0	I	VIO_6	Bit 2 of ADC/DAC external trigger
GPIO[55]	K6	—	G8	ADC_DAC_TRIGGER1	I	VIO_1	Bit 3 of ADC/DAC external trigger
GPIO[58]	G11	—	—	ADC1_3	A,I	VIO_6	ADC1 channel 3
GPIO[58]	G11	—	—	EXT_VREF_ADC1	A,I	VIO_6	ADC1 external voltage reference input
GPIO[45]	H12	82	U3	EXT_VREF_ADC0_ DAC	A,I	VIO_6	ADC0 or DAC external voltage reference input
GPIO[59]	D12	—	—	ADC1_2	A,I	VIO_6	ADC1 channel 2
GPIO[60]	E11	—	—	ADC1_1	A,I	VIO_6	ADC1 channel 1
GPIO[61]	A13	—	—	ADC1_0	A,I	VIO_6	ADC1 channel 0

Table 43. Analog peripheral interface*...continued*

Symbol	TFBGA145	HVQFN116	WLCSP151	Pin name	Type	Supply	Description
ACOMP							
GPIO[42]	G13	79	U4	ACOMP0	A,I	VIO_6	ACOMP channel 0
GPIO[43]	H12	80	R4	ACOMP1	A,I	VIO_6	ACOMP channel 1
GPIO[44]	J11	81	V3	ACOMP2	A,I	VIO_6	ACOMP channel 2
GPIO[45]	H12	82	U3	ACOMP3	A,I	VIO_6	ACOMP channel 3
GPIO[46]	F12	83	R3	ACOMP4	A,I	VIO_6	ACOMP channel 4
GPIO[47]	E13	84	N4	ACOMP5	A,I	VIO_6	ACOMP channel 5
GPIO[48]	D13	85	Y2	ACOMP6	A,I	VIO_6	ACOMP channel 6
GPIO[49]	D14	86	N5	ACOMP7	A,I	VIO_6	ACOMP channel 7
GPIO[51]	M8	—	D8	ACOMP0_GPIO_OUT	O	VIO_1	Analog comparator 0 level output
GPIO[52]	K8	—	E8	ACOMP0_EDGE_ PULSE	O	VIO_1	Analog comparator 0 edge pulse
GPIO[53]	L11	—	F8	ACOMP1_GPIO_OUT	O	VIO_1	Analog comparator 1 level output
GPIO[54]	M10	—	A8	ACOMP1_EDGE_ PULSE	O	VIO_1	Analog comparator 1 edge pulse

7.6.22 JTAG interface

Table 44. JTAG interface

Symbol	TFBGA145	HVQFN116	WLCSP151	Pin name	Type	Supply	Description
GPIO[6]	L5	24	F12	JTAG_TCK	I	VIO_1	JTAG test clock input signal
GPIO[7]	L9	21	F10	JTAG_TMS	I	VIO_1	JTAG test mode select input signal
GPIO[8]	M6	22	E10	JTAG_TDI	I	VIO_1	JTAG test data input signal
GPIO[9]	M4	25	G10	JTAG_TDO	O	VIO_1	JTAG test data output signal
GPIO[10]	M3	26	E12	JTAG_TRSTN	I	VIO_1	JTAG test reset signal

7.7 Configuration pins

Table 45 shows the pins used as configuration inputs to set parameters following a reset. The definition of these pins changes immediately after reset to their usual function. To set a configuration bit to 0, attach a resistor value of 51 kΩ or less from the pin to ground. No external circuitry is required to set a configuration bit to 1.

Table 45. Configuration pins

Configura bits	Pin name	Configuration function
CON[11]	RF_CNTL2 CONFIG_DAP_USE_JTAG	0 = DAP uses SWD 1 = DAP uses JTAG (default)
CON[5]	RF_CNTL0/ CONFIG_XOSC_SEL	Reference clock frequency selection 0 = 38.4 MHz 1 = 40 MHz (default)
CON[3:0]	CONFIG_HOST_BOOT[3:0] EXT_FREQ/WCI-2_SOUT, EXT_PRI, EXT_GNT, EXT_REQ	Host configuration options. Selects the host interface. See the table below.

Table 46. Host configuration options

CONFIG_HOST[3:0]	Boot
1111	Boot from FlexSPI Flash (default)
1110	ISP boot (UART/I2C/SPI/USB)
1101	Serial boot (UART/I2C/SPI/USB)
1100	ISP boot (SDIO)
1011	Serial boot (SDIO)
1010	Reserved

8 Power information

8.1 Power modes

See Section 3.13 "Power control".

8.2 Power-up sequence

The RW610 does not have power-up sequence requirements other than VBAT and VPA to be powered up no later than the other external supply rails. The power-down pin (PDn) must be held low (asserted) until all external clock and power supply rails are stable. See Figure 29.

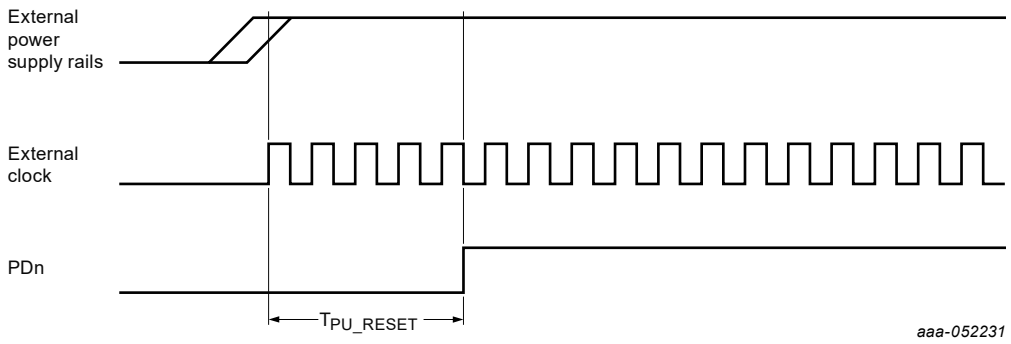


Figure 29. PDn held low (asserted)[1]

[1] T_{PU_RESET} is defined in Section 12.6.1.

8.3 Internal buck regulators

VCORE and AVDD18 pins must be supplied by the internal Buck regulators. Figure 30, Figure 31, and Figure 32 show the application circuit for VCORE and AVDD18 supply using the internal Buck regulators. The power inductor in the application is chosen to maximize the internal Buck efficiency.

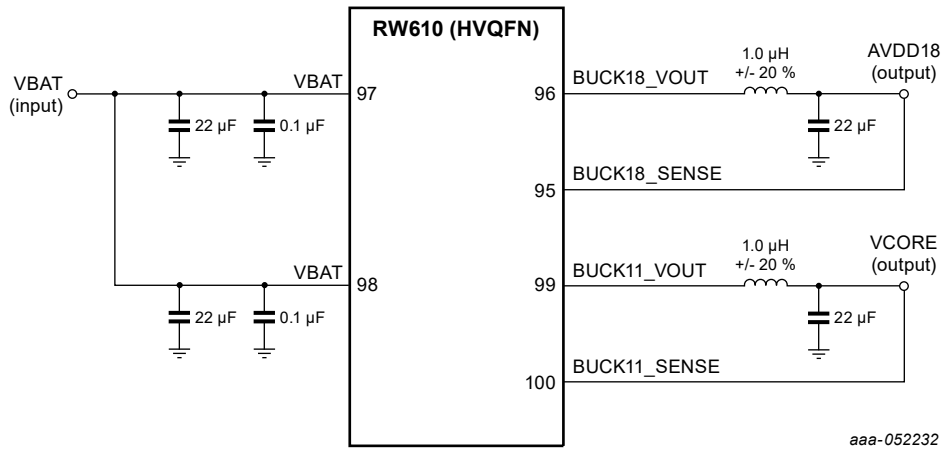


Figure 30. Internal buck regulators - HVQFN package

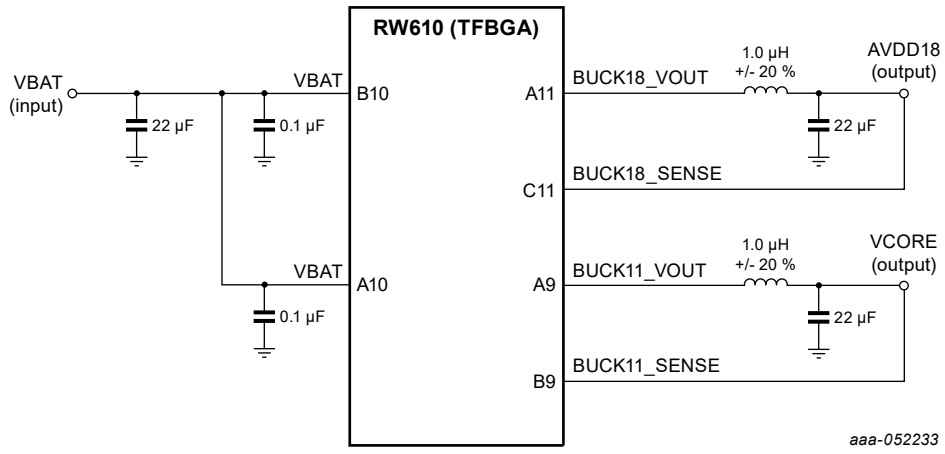


Figure 31. Internal buck regulators - TFBGA package

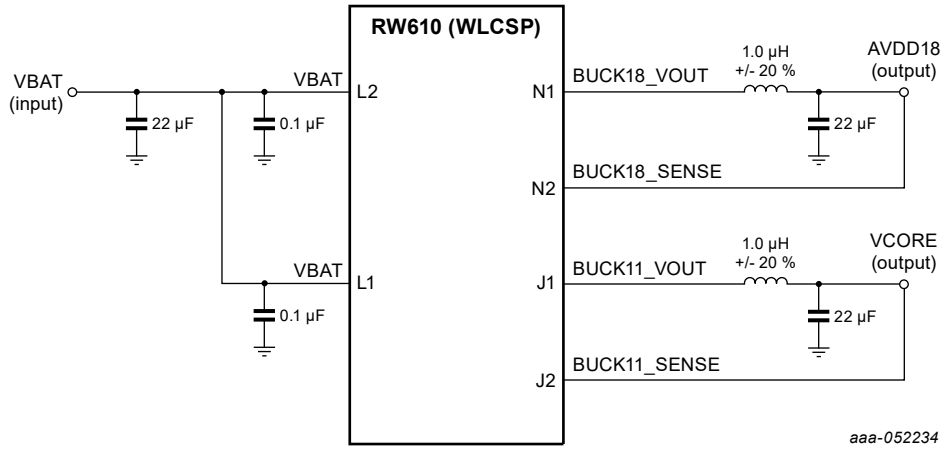


Figure 32. Internal buck regulators - WLCSP package

9 Absolute maximum ratings

CAUTION: The absolute maximum ratings table defines the limitations for electrical and thermal stresses. These limits prevent permanent damage to the device. Exposure to conditions at or beyond these ratings is not guaranteed and can damage the device.

Table 47. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
VCORE[1]	Nominal 1.05 V Vcore power supply	—	1.155	V
VIO[2]	1.8 V/3.3 V digital I/O power supply	—	2.16	V
		—	3.96	V
VIO_RF	1.8 V/3.3 V digital I/O power supply	—	2.16	V
		—	3.96	V
AVDD18[3]	1.8 V analog power supply	—	2.16	V
VPA	3.3 V analog power supply	—	3.96	V
VBAT	Input power supply to internal buck regulators	—	3.96	V
USB_VBUS	USB VBUS detection	—	5.25	V
$T_{STORAGE}$	Storage Temperature	-55	+125	°C

[1] VCORE must be powered from the internal buck as illustrated in Section 8.3 "Internal buck regulators"
[2] Applies to VIO_1, VIO_2, VIO_3, VIO_4, VIO_5, and VIO_6
[3] Applies to AVDD18 and AVDD18_USB

Table 48. Limiting values

Symbol	Parameter	Condition	Min	Max	Unit
V_{ESD}	Electrostatic discharge	human body model (HBM)[1]	-2	+2	kV
		charged device model (CDM)[2]	-500	+500	V

[1] According to ANSI/ESDA/JEDEC JS-001.
[2] According to ANSI/ESDA/JEDEC JS-002

10 Recommended operating conditions

Note: *Operation beyond the recommended operating conditions is neither recommended nor guaranteed.*

Table 49. Recommended operating conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCORE [1]	Nominal 1.05 V Vcore power supply[2]	—	1.010	—	1.155	V
VIO[3]	1.8 V digital I/O power supply	—	1.71	1.8	1.89	V
	3.3 V digital I/O power supply	—	2.97	3.3	3.46	V
VIO_RF	1.8 V digital I/O power supply	—	1.71	1.8	1.89	V
	3.3 V digital I/O power supply	—	3.14	3.3	3.46	V
AVDD18[4]	1.8 V analog power supply	—	1.71	1.8	1.89	V
	1.8 V analog supply ripple	Peak-to-peak	—	—	10	mV
AVDD33_USB	3.3 V analog power supply	—	3.14	3.3	3.46	V
VBAT	Input power supply to internal buck regulators	—	2.25	3.3	3.63	V
USB_VBUS[5]	USB VBUS detection	—	4.75	—	5.25	V
VPA	3.3 V analog power supply	—	3.14	3.3	3.46	V
T_A	Ambient operating temperature	Industrial	-40	—	85	°C
T_J	Maximum junction temperature	--	—	--	125	°C

[1] VCORE must be powered by the internal Buck as illustrated in Section 8.3 "Internal buck regulators".
[2] Operating voltage set by firmware
[3] Applies to VIO_1, VIO_2, VIO_3, VIO_4, VIO_5, and VIO_6
[4] Applies to AVDD18 and AVDD18_USB
[5] USB_VBUS pin can be left unconnected in applications that do not require USB VBUS detection with register override.

11 Radio specifications

11.1 Wi-Fi radio specifications

11.1.1 Wi-Fi radio performance measurement

The Wi-Fi transmit/receive performance is measured either at the antenna port or at the chip port with Wi-Fi radio interface pins. In Figure 33, the Wireless SoC is RW610.

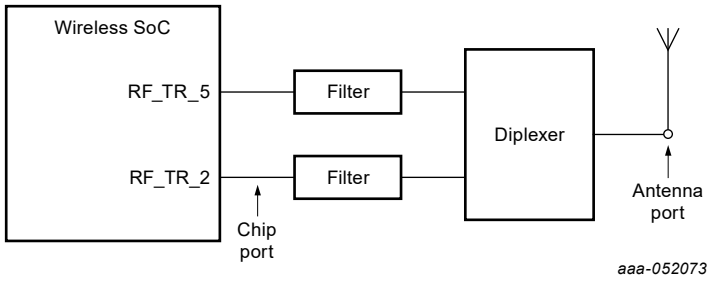


Figure 33. RF performance measurement points

11.1.2 2.4 GHz Wi-Fi receiver performance

Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at RF_TR_2 pin.

Table 50. 2.4 GHz Wi-Fi receiver performance

Parameter	Condition	Min	Typ	Max	Unit
RF frequency range	—	2400	—	2483.5	MHz
RF signal bandwidth	—	20	—	20	MHz
S11	—	—	-10	—	dB
Image rejection	After calibration	—	—	-48	dBc
Receiver sensitivity[1]					
Receiver sensitivity 802.11b	20 MHz 1 Mbps	—	-99.25	—	dBm
Receiver sensitivity 802.11b	20 MHz 11 Mbps	--	-91	--	dBm
Receiver sensitivity 802.11g	20 MHz 6 Mbps	—	-94.5	—	dBm
Receiver sensitivity 802.11g	20 MHz 54 Mbps	—	-77.25	—	dBm
Receiver sensitivity 802.11n	20 MHz MCS0 Nss1 BCC	—	-93.75	—	dBm
Receiver sensitivity 802.11n	20 MHz MCS7 Nss1 BCC	—	-75	—	dBm
Receiver sensitivity 802.11ax	4x3.2 20 MHz MCS0 Nss1 BCC	—	-93.5	—	dBm
Receiver sensitivity 802.11ax	4x3.2 20 MHz MCS9 Nss1 BCC	—	-68.75	—	dBm
Receiver maximum input level (MIL)					
Receiver maximum input level DSSS[2]	802.11b DSSS MIL	—	-0.2	—	dBm
Receiver maximum input level DSSS[2]	802.11b CCK MIL	—	-0.2	—	dBm
Receiver maximum input level OFDM	OFDM MIL	—	-5	—	dBm
Receiver adjacent channel interference (ACI)					
Receiver ACI 802.11b	20 MHz 1 Mbps	—	53	—	dB
Receiver ACI 802.11b	20 MHz 11 Mbps	—	45	—	dB
Receiver ACI 802.11g	20 MHz 6 Mbps	—	30	—	dB
Receiver ACI 802.11g	20 MHz 54 Mbps	—	22	—	dB
Receiver ACI 802.11n	20 MHz MCS0 Nss1 BCC	—	42	—	dB
Receiver ACI 802.11n	20 MHz MCS7 Nss1 BCC	—	25	—	dB
Receiver ACI 802.11ax	4x3.2 20 MHz MCS0 Nss1 BCC	—	29	—	dB
Receiver ACI 802.11ax	4x3.2 20 MHz MCS9 Nss1 BCC	—	8	—	dB

Table 50. 2.4 GHz Wi-Fi receiver performance*...continued*

Parameter	Condition	Min	Typ	Max	Unit
Receiver alternate adjacent channel interference (AACI)					
Receiver AACI 802.11b	20 MHz 1 Mbps	—	53	—	dB
Receiver AACI 802.11b	20 MHz 11 Mbps	—	49	—	dB
Receiver AACI 802.11g	20 MHz 6 Mbps	—	48	—	dB
Receiver AACI 802.11g	20 MHz 54 Mbps	—	32	—	dB
Receiver AACI 802.11n	20 MHz MCS0 Nss1 BCC	—	50	—	dB
Receiver AACI 802.11n	20 MHz MCS7 Nss1 BCC	—	31	—	dB
Receiver AACI 802.11ax	4x3.2 20 MHz MCS0 Nss1 BCC	—	47	—	dB
Receiver AACI 802.11ax	4x3.2 20 MHz MCS9 Nss1 BCC	—	25	—	dB

[1] The sensitivity values are 0.5 dB better for WLCSP as compared to QFN and TFBGA packages.
[2] Measurements for 2.4 GHz IEEE 802.11b DSSS/CCK MIL are limited by the test setup capability.

11.1.3 5 GHz Wi-Fi receiver performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at RF_TR_5 pin.*

Table 51. 5 GHz Wi-Fi receiver performance

Parameter	Condition	Min	Typ	Max	Unit
RF frequency range	—	5170	—	5895	MHz
RF signal bandwidth	—	20	—	20	MHz
S11	—	—	-10	—	dB
Receiver sensitivity[1]					
Receiver sensitivity 802.11a	20 MHz 6 Mbps	—	-93.5	—	dBm
Receiver sensitivity 802.11a	20 MHz 54 Mbps	---	-76.5	--	dBm
Receiver sensitivity 802.11n	20 MHz MCS0 Nss1 BCC	—	-92.75	—	dBm
Receiver sensitivity 802.11n	20 MHz MCS7 Nss1 BCC	—	-74	—	dBm
Receiver sensitivity 802.11ac	20 MHz MCS0 Nss1 BCC	—	-92.75	—	dBm
Receiver sensitivity 802.11ac	20 MHz MCS8 Nss1 BCC	—	-70	—	dBm
Receiver sensitivity 802.11ax	4x3.2 20 MHz MCS0 Nss1 BCC	—	-92.5	—	dBm
Receiver sensitivity 802.11ax	4x3.2 20 MHz MCS9 Nss1 BCC	—	-67.75	—	dBm
Receiver maximum input level (MIL)					
Receiver maximum input level OFDM	OFDM MIL	—	-7	—	dBm
Receiver adjacent channel interference (ACI)					
Receiver ACI 802.11a	20 MHz 6 Mbps	—	23	—	dB
Receiver ACI 802.11a	20 MHz 54 Mbps	—	16	—	dB
Receiver ACI 802.11n	20 MHz MCS0 Nss1 BCC	—	32	—	dB
Receiver ACI 802.11n	20 MHz MCS7 Nss1 BCC	—	12	—	dB
Receiver ACI 802.11ac	20 MHz MCS0 Nss1 BCC	—	28	—	dB
Receiver ACI 802.11ac	20 MHz MCS8 Nss1 BCC	—	8	—	dB
Receiver ACI 802.11ax	4x3.2 20 MHz MCS0 Nss1 BCC	—	29	—	dB
Receiver ACI 802.11ax	4x3.2 20 MHz MCS9 Nss1 BCC	—	8	—	dB
Receiver alternate adjacent channel interference (AACI)					
Receiver AACI 802.11a	20 MHz 6 Mbps	—	47	—	dB
Receiver AACI 802.11a	20 MHz 54 Mbps	—	27	—	dB
Receiver AACI 802.11n	20 MHz MCS0 Nss1 BCC	—	47	—	dB
Receiver AACI 802.11n	20 MHz MCS7 Nss1 BCC	—	29	—	dB
Receiver AACI 802.11ac	20 MHz MCS0 Nss1 BCC	—	47	—	dB
Receiver AACI 802.11ac	20 MHz MCS8 Nss1 BCC	—	24	—	dB
Receiver AACI 802.11ax	4x3.2 20 MHz MCS0 Nss1 BCC	—	47	—	dB
Receiver AACI 802.11ax	4x3.2 20 MHz MCS9 Nss1 BCC	—	24	—	dB

[1] The sensitivity values are 1 dB better for WLCSP as compared to QFN and TFBGA packages.

11.1.4 2.4 GHz Wi-Fi transmitter performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at RF_TR_2 pin.*

Table 52. 2.4 GHz Wi-Fi transmitter performance

Parameter	Condition	Min	Typ	Max	Units
RF frequency range	2.4 GHz	2400	—	2483.5	MHz
Maximum linear output power with 20 MHz bandwidth	802.11b 1 Mbps	—	22	—	dBm
	802.11b 11 Mbps	—	22	—	dBm
	802.11g 6 Mbps	—	22	—	dBm
	802.11g 54 Mbps	—	19	—	dBm
	802.11n MCS7	—	19	—	dBm
	802.11ax MCS9	—	18	—	dBm
Transmit I/Q suppression with IQ calibration	After calibration	—	—	-48	dBc
Second harmonic (HD2)	At 21 dBm, CW	—	-45	—	dBr
Third harmonic (HD3)	At 21 dBm, CW	—	-35	—	dBr
Transmit power accuracy	With manufacturing-time calibration per board	-2	—	2	dB
Out-of-band noise floor at different operation standard frequency range Transmit 1 Mbps at 18 dBm with 100% duty cycle	—	—	-150	—	dBm/Hz
Transmit carrier suppression		—	-40	—	dBc
Transmit frequency error	—	-5	—	5	PPM
Transmit output power control step	—	—	1	—	dB
Transmit output power level control range	—	-10	—	22	dBm
Transmit general spurs, harmonics and sub-harmonics[1] 6 Mbps Tx at 18 dBm with 100% duty cycle	< 1 GHz	—	-96	—	dBm/100 kHz
	1 GHz to 18 GHz	—	-96	—	dBm/100 kHz
	Second harmonic	—	-65	—	dBm/1 MHz
	Third harmonic	—	-56	—	dBm/1 MHz
	LO leakage	—	-65	—	dBm

[1] Spurious and harmonics are measured with the front-end configuration of the reference design.

11.1.5 5 GHz Wi-Fi transmitter performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at RF_TR_5 pin.*

Table 53. 5 GHz Wi-Fi transmitter performance

Parameter	Condition	Min	Typ	Max	Units
RF frequency range	5 GHz	5170	—	5895	MHz
Maximum linear output power with 20 MHz bandwidth	802.11a 6 Mbps	—	23	—	dBm
	802.11a 54 Mbps	—	20	—	dBm
	802.11n MCS0	—	22	—	dBm
	802.11n MCS7	—	20	—	dBm
	802.11ac MCS0	—	22	—	dBm
	802.11ac MCS8	—	19	—	dBm
	802.11ax MCS0	—	22	—	dBm
	802.11ax MCS9	—	19	—	dBm
Transmit I/Q suppression with IQ calibration	After calibration	—	—	-48	dBc
Second harmonic (HD2)	At 20 dBm, CW	—	—	-25	dBr
Third harmonic (HD3)	At 20 dBm, CW	—	—	-55	dBr
Transmit power accuracy	—	-2	—	2	dB
Transmit power control resolution	—	—	0.0625	—	dB
Out-of-band noise floor at different operation standard frequency range Transmit 1 Mbps at 18 dBm with 100% duty cycle	—	—	-147	—	dBm/Hz
Transmit carrier suppression	—	—	-34	—	dBc
Transmit frequency error	—	-5	—	5	PPM
Transmit output power control step	—	—	1	—	dB
Transmit output power level control range	—	-10	—	22	dBm
Transmit general spurs, harmonics and sub-harmonics[1] 6 Mbps Tx at 18 dBm with 100% duty cycle	< 1 GHz	—	-97	—	dBm/100 kHz
	1 GHz to 18 GHz	—	-97	—	dBm/100 kHz
	Second harmonic	—	-68	—	dBm/1 MHz
	Third harmonic	—	-65	—	dBm/1 MHz
	LO leakage	—	-58	—	dBm

[1] Spurious and harmonics are measured with the front-end configuration of the reference design.

11.2 Bluetooth LE radio specifications

11.2.1 Bluetooth LE receiver performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at BRF_ANT pin.*

Table 54. Bluetooth LE receiver performance [1]

Parameter	Conditions	Min	Typ.	Max	Unit
RF frequency range	—	2400	—	2483.5	MHz
S11	—	—	-10	—	dB
Receiver sensitivity					
Bluetooth LE 1 Mbps	—	—	-100.2	—	dBm
Bluetooth LE 2 Mbps	—	—	-97.9	—	dBm
Bluetooth LR 125 Kbps	—	—	-108.1	—	dBm
Bluetooth LR 500 Kbps	—	—	-101.1	—	dBm
Receiver maximum input level (MIL)[2]					
Bluetooth LE 1 Mbps	—	—	-3	—	dBm
Bluetooth LE 2 Mbps	—	—	-3	—	dBm
Bluetooth LR 125 Kbps	—	—	-3	—	dBm
Bluetooth LR 500 Kbps	—	—	-3	—	dBm
Receiver interference/selectivity performance[3]					
Bluetooth LE 1 Mbps					
Receiver selectivity @ -5 MHz (image -1)	Bluetooth LE 1 Mbps selectivity	—	44	—	dB
Receiver AACS @ -4 MHz (image)	Bluetooth LE 1 Mbps alternate adjacent channel selectivity	—	38	—	dB
Receiver selectivity @ -3 MHz (image +1)	Bluetooth LE 1 Mbps selectivity	—	34	—	dB
Receiver ACS @ -2 MHz	Bluetooth LE 1 Mbps adjacent channel selectivity	—	41	—	dB
Receiver selectivity @ -1 MHz	Bluetooth LE 1 Mbps selectivity	—	4	—	dB
Receiver CCS	Bluetooth LE 1 Mbps co-channel selectivity	—	-8	—	dB
Receiver selectivity @ +1 MHz	Bluetooth LE 1 Mbps selectivity	—	8	—	dB
Receiver ACS @ +2 MHz	Bluetooth LE 1 Mbps adjacent channel selectivity	—	42	—	dB
Receiver selectivity @ +3 MHz	Bluetooth LE 1 Mbps selectivity	—	49	—	dB

Table 54. Bluetooth LE receiver performance [1]*...continued*

Parameter	Conditions	Min	Typ.	Max	Unit
Bluetooth LE 2 Mbps					
Receiver selectivity @ -6 MHz (image -2)	Bluetooth LE 2 Mbps 3rd adjacent channel selectivity	—	53	—	dB
Receiver AACS @ -4 MHz (image)	Bluetooth LE 2 Mbps alternate adjacent channel selectivity	—	32	—	dB
Receiver ACS @ -2 MHz (image +2)	Bluetooth LE 2 Mbps adjacent channel selectivity	—	22	—	dB
Receiver CCS	Bluetooth LE 2 Mbps co-channel selectivity	—	-8	—	dB
Receiver ACS @ +2 MHz	Bluetooth LE 2 Mbps adjacent channel selectivity	—	28	—	dB
Receiver AACS @ +4 MHz	Bluetooth LE 2 Mbps alternate adjacent channel selectivity	—	51	—	dB
Receiver selectivity @ +6 MHz	Bluetooth LE 2 Mbps 3rd adjacent channel selectivity	—	54	—	dB
Bluetooth LR 125 Kbps					
Receiver selectivity @ -5 MHz (image -1)	Bluetooth LR 125 kbps selectivity	—	49	—	dB
Receiver AACS @ -4 MHz (image)	Bluetooth LR 125 kbps alternate adjacent channel selectivity	—	32	—	dB
Receiver selectivity @ -3 MHz (image +1)	Bluetooth LR 125 kbps selectivity	—	38	—	dB
Receiver ACS @ -2 MHz	Bluetooth LR 125 kbps adjacent channel selectivity	—	50	—	dB
Receiver selectivity @ -1 MHz	Bluetooth LR 125 kbps selectivity	—	8	—	dB
Receiver CCS	Bluetooth LR 125 kbps co-channel selectivity	—	-7	—	dB
Receiver selectivity @ +1 MHz	Bluetooth LR 125 kbps selectivity	—	11	—	dB
Receiver ACS @ +2 MHz	Bluetooth LR 125 kbps adjacent channel selectivity	—	52	—	dB
Receiver selectivity @ +3 MHz	Bluetooth LR 125 kbps selectivity	—	59	—	dB

Table 54. Bluetooth LE receiver performance [1]*...continued*

Parameter	Conditions	Min	Typ.	Max	Unit
Bluetooth LR 500 Kbps					
Receiver selectivity @ -5 MHz (image -1)	Bluetooth LR 500 kbps selectivity	—	48	—	dB
Receiver AACS @ -4 MHz (image)	Bluetooth LR 500 kbps alternate adjacent channel selectivity	—	31	—	dB
Receiver selectivity @ -3 MHz (image +1)	Bluetooth LR 500 kbps selectivity	—	38	—	dB
Receiver ACS @ -2 MHz	Bluetooth LR 500 kbps adjacent channel selectivity	—	50	—	dB
Receiver selectivity @ -1 MHz	Bluetooth LR 500 kbps selectivity	—	7	—	dB
Receiver CCS	Bluetooth LR 500 kbps co-channel selectivity	—	-9	—	dB
Receiver selectivity @ +1 MHz	Bluetooth LR 500 kbps selectivity	—	9	—	dB
Receiver ACS @ +2 MHz	Bluetooth LR 500 kbps adjacent channel selectivity	—	55	—	dB
Receiver selectivity @ +3 MHz	Bluetooth LR 500 kbps selectivity	—	58	—	dB

[1] Bluetooth/Bluetooth LE receiver performance is measured with Dirty Tx. That is, the transmitter has impairments as specified by the Bluetooth SIG standard. The Packet length is 255 bytes.
[2] The true MIL numbers are higher than -3 dBm. The measurements are limited by the setup capability.
[3] The selectivity numbers indicate the I/C ratio [in dB].

11.2.2 Bluetooth LE transmitter performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at BRF_ANT pin.*

Table 55. Bluetooth LE transmitter performance

Parameter	Conditions	Min	Typ.	Max	Unit
RF frequency range	—	2400	—	2483.5	MHz
Bluetooth LE maximum transmit power	—	—	15	—	dBm
Out-of band noise floor at different operation standard frequency range Transmit at 15 dBm with 100% duty cycle	—	—	-140	-130	dBm/Hz
Transmit frequency error	Includes XTAL error	-15	—	15	kHz
Transmit output power accuracy	—	-2	—	2	dB
Transmit output power control step	—	—	0.5	—	dB
Transmit output power level control range	—	-20	—	15	dBm
Transmit general spurs, harmonics and sub-harmonics[1] Transmit at 15 dBm with 100% duty cycle	< 1 GHz	—	-84	—	dBm/100 kHz
	1 GHz to 18 GHz	—	-78	—	dBm/100 kHz
	Second harmonic	—	-56	—	dBm/1 MHz
	Third harmonic	—	-60	—	dBm/1 MHz
	LO leakage	—	-57	—	dBm

[1] Spurious and harmonics are measured with the front-end configuration of the reference design.

11.3 External coexistence interface specifications

11.3.1 WCI-2 coexistence interface specifications

11.3.1.1 WCI-2 interface

WCI-2 is a simplified 2-wire UART interface defined in Bluetooth Core Spec Vol 7 Part C.

Figure 34 shows UART waveform.

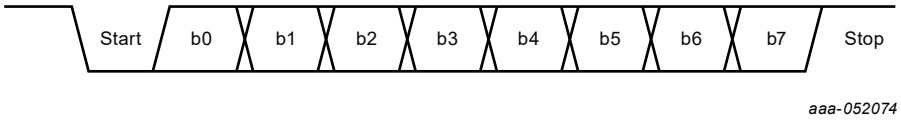


Figure 34. UART waveform

Figure 35 illustrates WCI-2 hardware coexistence interface between RW610 (Wireless SoC) and the external radio.

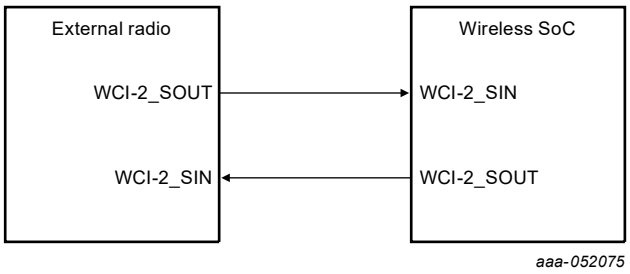


Figure 35. WCI-2 coexistence interface

11.3.1.2 WCI-2 messages

WCI-2 coexistence interface supports the messages defined in Bluetooth Core Specification Vol 7 Part C for request and grant, where:

- The real time message from the external radio to RW610 indicates the request to operate (Figure 36)
  - MWS_Rx=1 indicates an external radio request to Rx
  - MWS_Tx=1 indicates an external radio request to Tx

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
0	0	0	FRAME_SYNC	MWS_RX	MWS_TX	MWS_PATTERN[0]	MWS_PATTERN[1]

aaa-052076

Figure 36. Type 0: Real time signaling message - external radio to RW610

- The external radio can send an optional second message following the real time message to indicate the traffic priority using the vendor specific message (Figure 37). Otherwise, the priority is set via a BCA register.

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
1	1	1	0	MWS_TX_PRI[0]	MWS_TX_PRI[1]	MWS_RX_PRI[0]	MWS_RX_PRI[1]

aaa-052077

Figure 37. Type 7: Vendor specific message - external radio to RW610

- The real time message from RW610 to the external radio indicates the arbitration results (Figure 38):
  - BT_Rx_Pri = 1: the Bluetooth radio Rx wins the arbitration and is in operation
  - BT_Tx_On = 1: the Bluetooth radio Tx wins the arbitration and is in operation
  - 802_Rx_Pri = 1: Wi-Fi Rx wins the arbitration and is in operation
  - 802_Tx_On = 1: Wi-Fi Tx wins the arbitration and is in operation
  - Otherwise, the external radio is granted

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
0	0	0	NB_RX_PRI	NB_TX_ON	802_RX_PRI	802_TX_ON	RFU

aaa-052078

Figure 38. Type 0: Real time signaling message - RW610 to external radio

WCI-2 coexistence interface supports the messages defined in Bluetooth Core Specification Vol 7 Part C for other purposes, such as:

- Transport control message from RW610 to the external radio to request real time message upon wake up (Figure 39)

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
0	0	1	Resend_real_time	RFU	RFU	RFU	RFU

aaa-052079

Figure 39. Type 1: Transport control message time signaling message - RW610 to external radio

- MWS inactivity duration message from the external radio to RW610 indicates the inactivity duration to RW610 before going to sleep (Figure 40)

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
0	1	1	Duration[0]	Duration[1]	Duration[2]	Duration[3]	Duration[4]

aaa-052081

Figure 40. MWS inactivity duration message

- MWS scan frequency message from the external radio to RW610 indicates the external radio scan frequency to RW610 (Figure 41)

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
1	0	0	Freq[0]	Freq[1]	Freq[2]	Freq[3]	Freq[4]

aaa-052080

Figure 41. Type 5: MWS scan frequency message

11.3.1.3 WCI-2 signal waveform format

The messaging is based on a standard UART format.

Figure 42 shows the waveform for the transmit signal (UART_SOUT to UART_SIN).

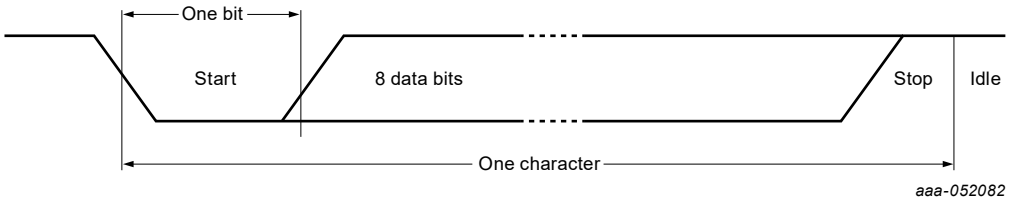


Figure 42. WCI-2 transmit signal waveform

Table 56. WCI-2 interface transport settings

Parameter	Range	Note
Baud rate	921600 ~ 4000000	Baud
Data bits	8	LSB first
Parity bits	0	No parity
Stop bit	1	One stop bit
Flow control	No	No flow control

11.3.2 PTA interface coexistence specifications

This section illustrates how the central hardware packet traffic arbiter samples the interface signals. The sampling is based on which interface signals are being used.

Figure 43 shows PTA coexistence interface signal timing diagram for the example where:

- Input: request, 1-bit priority
  - Priority ready at Request signal assertion
- Output: grant

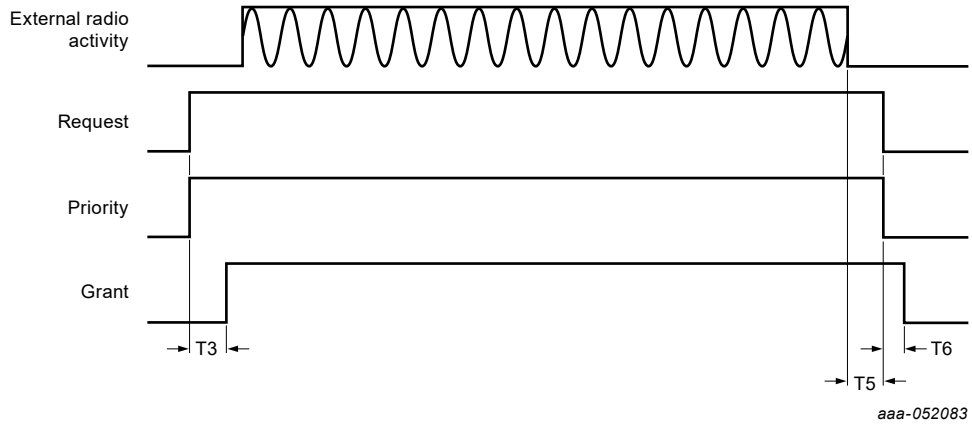


Figure 43. PTA coexistence interface timing diagram - Example 1

Figure 44 shows PTA coexistence interface timing diagram for the example where:

- Input: request, 1-bit priority, state
  - Priority signal and State signal are ready at Request signal assertion
- Output: grant

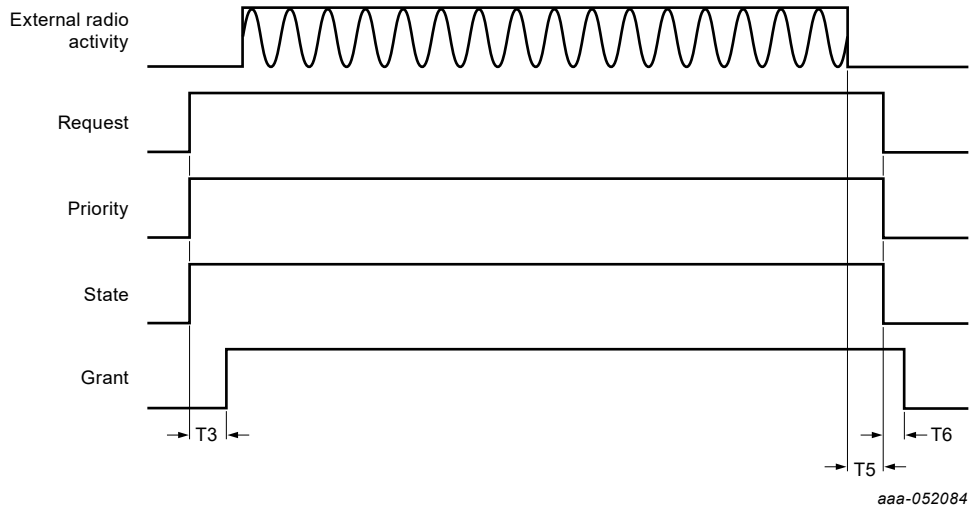


Figure 44. PTA coexistence interface timing diagram - Example 2

Figure 45 shows PTA coexistence interface timing diagram for the example where:

- Input: request, 1-bit priority, frequency, state
  - Priority, State, and Frequency ready at Request assertion
- Output: grant

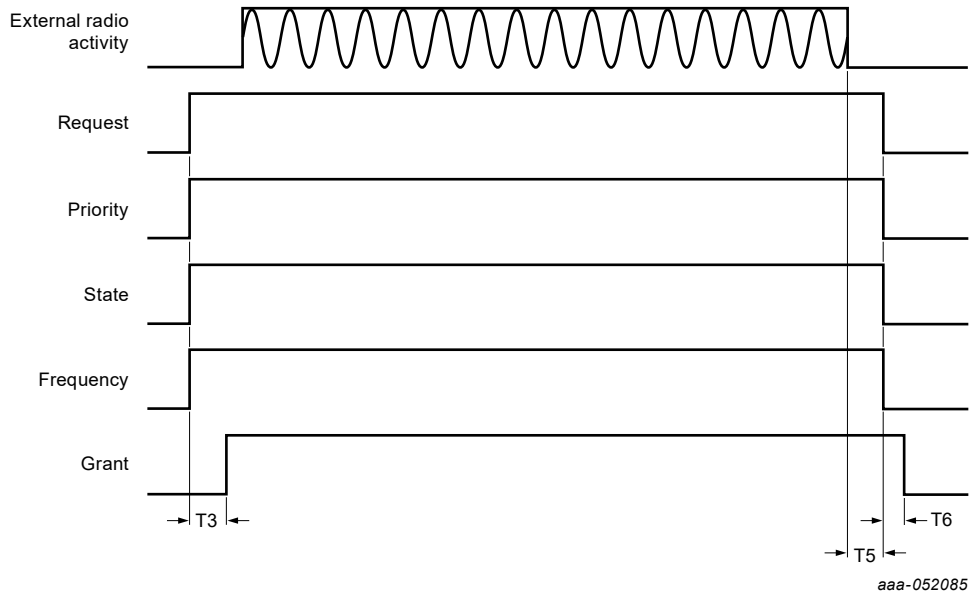


Figure 45. PTA coexistence interface timing diagram - Example 3

Figure 46 shows PTA coexistence interface timing diagram for the example where:

- Input: request, 1-bit priority
  - Priority signal is ready at Request signal assertion
- Output: grant
  - Grant signal is de-asserted before Request signal de-assertion due to a traffic abort caused by other traffic with higher priority

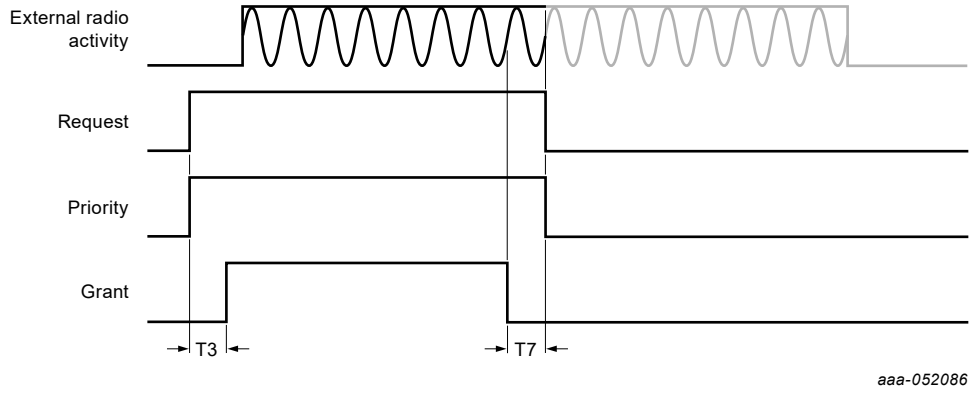


Figure 46. PTA coexistence interface timing diagram - Example 4

Figure 47 shows PTA coexistence interface timing diagram for the example where:

- Input: request and priority
  - Priority pin is sampled three times to obtain two priority bits and Tx/Rx info. No input from State pin.
- Output: grant

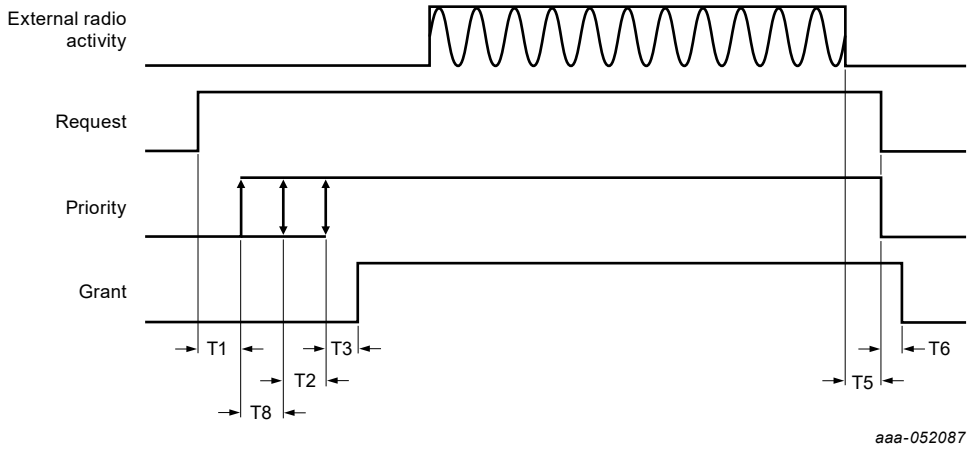


Figure 47. PTA coexistence interface timing diagram - Example 5

Table 57 provides the timing specifications for PTA coexistence interface signals.

Table 57. PTA coexistence interface signal timing data

Paramete	Conditions	Min	Typ.	Max	Unit
T1[1]	Priority[0] is sampled on Priority pin at T1 from Request assertion.	0	—	100	µs
T8[1]	Optional: priority[1], if present on Priority pin, is sampled at T1+T8 from Request assertion.	0.025	—	100	µs
T2[1]	Optional: Tx/Rx Info, if present on Priority pin, is sampled at T1+T2 (one priority bit on Priority pin) or T1+T8+T2 (two priority bits on Priority pin) from Request assertion.	0.025	—	100	µs
T3[2]	Time from all information available to BCA to grant decision ready	0.1	—	0.4	µs
T5[2]	The Request signal de-asserts T5 after the last symbol is done	—	—	—	µs
T6[2]	The Grant signal de-asserts T6 after the Request de-assertion	0.1	—	0.3	µs
T7[2]	The Request signal de-asserts T7 after the grant de-assertion due to a traffic abort.	—	—	—	µs

[1] Valid for serially sampled Priority pin
[2] Valid for all implementations

11.4 Current consumption

Note: *The power consumption values refer to 3.3 V supply source (85% eff) and 25°C. TX current is measured at chip pin.*

Table 58. Power consumption values

Mode	Conditions	Min	Typ	Max	Unit
Tx @ 4 dBm	—	49	—	mA	
Tx @ 15 dBm	—	84	—	mA	
Bluetooth LE only (Wi-Fi powered down)					
Bluetooth LE in sleep mode[1]	RAM retention	—	0.13	—	mA
Bluetooth LE advertising[1]	1.28 interval, unconnectable	—	0.18	—	mA
Bluetooth LE scanning[1]	1.28 interval, 11.25 ms window	—	0.27	—	mA
Bluetooth LE receive[2]	Bluetooth LE Rx 1 Mbps	—	39	—	mA
Bluetooth LE transmit[2]	Bluetooth LE Tx 0 dBm	—	46	—	mA
	Bluetooth LE Tx 4 dBm	—	49	—	mA
	Bluetooth LE Tx 15 dBm	—	84	—	mA
IEEE power save mode (MCU in Deep-sleep mode with no memory retention, narrow band subsystem powered down, beacon interval = 102.4 ms, short beacon frame)[3]					
DTIM 1 (2.4 GHz, 20 MHz)	2.4 GHz basic rate for beacon transmit: 1 Mbps	—	0.89	—	mA
DTIM 3 (2.4 GHz, 20 MHz)		—	0.44	—	mA
DTIM 5 (2.4 GHz, 20 MHz)		—	0.36	—	mA
DTIM 10 (2.4 GHz, 20 MHz)		—	0.33	—	mA
DTIM 1 (5 GHz, 20 MHz)	5 GHz basic rate for beacon transmit: 6 Mbps	—	0.59	—	mA
DTIM 3 (5 GHz, 20 MHz)		—	0.34	—	mA
DTIM 5 (5 GHz, 20 MHz)		—	0.30	—	mA
DTIM 10 (5 GHz, 20 MHz)		—	0.28	—	mA
IEEE power save mode (MCU in Deep-sleep mode with no memory retention, narrow band subsystem powered down, beacon interval = 102.4 ms)[4]					
DTIM 1 (2.4 GHz, 20 MHz)	2.4 GHz basic rate for beacon transmit: 1 Mbps	—	1.03	—	mA
DTIM 3 (2.4 GHz, 20 MHz)		—	0.49	—	mA
DTIM 5 (2.4 GHz, 20 MHz)		—	0.37	—	mA
DTIM 10 (2.4 GHz, 20 MHz)		—	0.33	—	mA
DTIM 1 (5 GHz, 20 MHz)	5 GHz basic rate for beacon transmit: 6 Mbps	—	0.61	—	mA
DTIM 3 (5 GHz, 20 MHz)		—	0.35	—	mA
DTIM 5 (5 GHz, 20 MHz)		—	0.30	—	mA
DTIM 10 (5 GHz, 20 MHz)		—	0.28	—	mA

Table 58. Power consumption values*...continued*

Mode	Conditions	Min	Typ	Max	Unit
IEEE 802.11ax target wake-up time (TWT) (Partial RAM retention for Wi-Fi subsystem, narrow band subsystem powered down)[5]					
TWT 1 min	2.4 GHz, 20 MHz	—	0.28	—	mA
TWT 5 min		—	0.24	—	mA
TWT 10 min		—	0.23	—	mA
TWT 20 min		—	0.225	—	mA
TWT 30 min		—	0.22	—	mA
TWT 1 min	5 GHz, 20 MHz	—	0.27	—	mA
TWT 5 min		—	0.25	—	mA
TWT 10 min		—	0.23	—	mA
TWT 20 min		—	0.228	—	mA
TWT 30 min		—	0.22	—	mA
Wi-Fi mode (narrow band subsystem powered down)					
Wi-Fi in sleep mode	Wi-Fi subsystem in sleep mode, RAM retention	—	0.21	—	mA
Wi-Fi idle mode[6]	2.4 GHz, Rx, 802.11n, 20 MHz, listening	—	45	—	mA
	2.4 GHz, Rx, 802.11ax, 20 MHz, listening	—	45	—	mA
Wi-Fi idle mode[6]	5 GHz, Rx, 802.11n, 20 MHz, listening	—	57	—	mA
	5 GHz, Rx, 802.11ax, 20 MHz, listening	—	57	—	mA
Wi-Fi receive mode[7]	2.4 GHz, 802.11n, 20 MHz, MCS7	—	63	—	mA
	2.4 GHz, 802.11ax, 20 MHz, MCS9	—	63	—	mA
Wi-Fi receive mode[7]	5 GHz, 802.11n, 20 MHz, MCS7	—	71	—	mA
	5 GHz, 802.11ax, 20 MHz, MCS9	—	74	—	mA
Wi-Fi transmit mode, max power[7]	2.4 GHz, 802.11n, 20 MHz, MCS7 @ 20 dBm	—	261	—	mA
	2.4 GHz, 802.11ax, 20 MHz, MCS9 @ 20 dBm	—	264	—	mA
Wi-Fi transmit mode, max power[7]	5 GHz, 802.11n, 20 MHz, MCS7 @ 20 dBm	—	429	—	mA
	5 GHz, 802.11ax, 20 MHz, MCS9 @ 20 dBm	—	414	—	mA
Wi-Fi transmit mode[7]	2.4 GHz, 802.11n, 20 MHz, MCS0 @ 15 dBm	—	208	—	mA
Wi-Fi transmit mode[7]	5 GHz, 802.11n, 20 MHz, MCS0 @ 15 dBm	—	305	—	mA
Peak current during device initialization					
Maximum current consumption	5 GHz, 802.11n, 20 MHz, MCS7@Max Power; MCU active; BRF active	—	469	—	mA
Peak digital pre-distortion (DPD) current	@ 25°C	—	576	—	mA

[1] MCU in Deep-sleep mode, 0 KB Ram retention.
[2] MCU in Active mode
[3] Frame length for short beacon in IEEE-PS current measurement:
- 2.4 GHz and 5 GHz: 125 bytes

[4] Frame length in IEEE-PS current measurement:
- 2.4 GHz: 159 bytes
- 5 GHz: 144 bytes

[5] Nominal TWT receive window duration: 50 ms
[6] MCU in Deep-sleep mode
[7] MCU in active state

12 Microcontroller specifications

12.1 Reference clock specifications

12.1.1 Crystal oscillator specifications

Table 59. 40 MHz (38.4 MHz) crystal oscillator (XTAL) specifications

Unless otherwise specified, the values apply per Section 10 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
Fundamental frequencies	--	--	40 (38.4)[1]	--	MHz
Equivalent differential load capacitance	--	--	8	--	pF
Shunt capacitance	--	--	2	--	pF
Frequency stability	Over operating temperature	--	±20	--	ppm
Aging	--	--	±2	--	ppm/ 5 years
Series resistance (ESR)	40 MHz/38.4 MHz XTAL	--	--	40	Ω
Negative resistance	40 MHz/38.4 MHz XTAL	-211	-280	—	Ω
Insulation resistance	at DC 100V	500	--	--	MΩ
Drive level	--	120	--	--	µW

[1] 40 MHz or 38.4 MHz are supported.

12.1.2 32 kHz crystal oscillator specifications

Table 60. 32 kHz crystal oscillator (XTAL32K) specifications

Unless otherwise specified, the values apply per Section 10 "Recommended operating conditions"

Parameter	Conditions	Min	Typ	Max	Unit
Output frequency	—	—	32.768	—	kHz
Frequency accuracy	Over process, voltage, temperature (PVT)	—	—	-22/-192	PPM
Temperature tolerance	From -40°C to 120°C	—	0.0192	—	%
Start-up time	From power on to CLK_RDY without noise injection	—	208	380	ms
Start-up time	From power on to CLK_RDY with noise injection	—	15	170	ms
Duty cycle	—	46.7	47.4	49.77	%
Current consumption (V18)	—	—	150	300	nA
Current consumption (V11)		—	0.1	3.7	µA
Crystal ESR resistance	—	—	50	80	kΩ

12.1.3 RC 32K internal oscillator specifications

Table 61. RC 32K internal oscillator specifications

Unless otherwise specified, the values apply per Section 10 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
Output frequency	—	—	32	—	kHz

12.2 General purpose I/O specifications

12.2.1 Digital pad ratings

12.2.1.1 VIO 1.8V operation

Table 62. Digital pad ratings—1.8V operation (VIO)

Unless otherwise specified, the values apply per Section 10 "Recommended operating conditions".

Symbol	Parameter	Condition	Min	Typ	Max	Units
VIO	I/O pad supply voltage	—	1.62	1.8	1.98	V
V_{IL}	Input low voltage	—	-0.4	—	0.3*VIO	V
V_{IH}	Input high voltage	—	0.7*VIO	—	VIO+0.4	V
V_{HYS}	Input hysteresis	—	100	—	—	mV
V_{OH}	Output high voltage	—	VIO-0.4	—	—	V
V_{OL}	Output low voltage	—	—	—	0.4	V

12.2.1.2 VIO 3.3V operation

Table 63. Digital pad ratings—3.3V operation (VIO)

Unless otherwise specified, the values apply per Section 10 "Recommended operating conditions"

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIO	I/O pad supply voltage	—	2.97	3.3	3.63	V
V_{IH}	Input high voltage	—	0.7*VIO	—	VIO+0.4	V
V_{IL}	Input low voltage	—	-0.4	—	0.3*VIO	V
V_{HYS}	Input hysteresis	—	100	—	—	mV
V_{OH}	Output high voltage	—	VIO-0.4	—	—	V
V_{OL}	Output low voltage	—	—	—	0.4	V

12.2.2 GPIO specifications

Table 64. GPIO specifications

Unless otherwise specified, the values apply per Section 10 "Recommended operating conditions"

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Freq_gpio	Performance level	SR[1:0] = 00	—	—	25	MHz
Freq_gpio	Performance level	SR[1:0] = 01	—	—	40	MHz
Freq_gpio	Performance level	SR[1:0] = 10	—	—	75	MHz
Freq_gpio	Performance level	SR[1:0] = 11	—	—	100	MHz

12.3 Communication peripherals

12.3.1 USB host/device interface specifications

12.3.1.1 USB high-speed electrical characteristics

Table 65. USB high-speed electrical specifications

Symbol	Parameter	Min	Typ	Max	Unit
Driver specifications					
T_{HSR}	Data rise time Defined from 10% to 90% for rise time and 90% to 10% for fall time.	500	--	--	ps
T_{HSF}	Data fall time Defined from 10% to 90% for rise time and 90% to 10% for fall time.	500	--	--	ps
Clock timings					
T_{HSDRAT}	High-speed data rate	479.76	—	480.24	Mbps
$T_{HSD\ RATPPM}$	High-speed data rate tolerance	-500	—	500	ppm
High-speed data timings					
—	Data source jitter: refer to Figure 50	—	—	—	—
—	Receiver jitter tolerance[1]	—	—	—	—
t_{EOPP}	EOP width at receiver	15.6	—	17.68	ns
Input voltage levels for high-speed					
V_{HSSQ}	High-speed squelch detection threshold (differential signal amplitude)	100	—	150	mV
V_{HSDSC}	High-speed disconnect detection threshold (differential signal amplitude)	525	—	625	mV
—	Differential input signaling levels - Refer to Figure 49 "USB HS Tx eye diagram pattern template diagram".	—	—	—	—
V_{HSCM}	High-speed data signaling common mode voltage range (guideline for receiver)	-50	—	500	mV
Output voltage levels for high-speed					
V_{HSOI}	High-speed idle level	-10	—	10	mV
V_{HSOH}	High-speed data signaling high	360	--	440	mV
V_{HSOL}	High-speed data signaling low	-10	--	10	mV
V_{CHIRPJ}	Chirp J level (differential voltage)	700	—	1100	mV
V_{CHIRPK}	Chirp J level (differential voltage)	-900	—	500	mV
Terminations in high-speed					
V_{HSTERM}	Termination voltage in high speed	-10	--	10	mV

[1] Guaranteed by the stability of the 480 MHz source clock

12.3.1.2 USB device full-speed (FS) electrical characteristics

Table 66. USB device full-speed (FS) electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Driver characteristics					
t_{FR}	Rise time	4	—	20	ns
t_{FF}	Fall time	4	—	20	ns
t_{FRFM}	Differential rise and fall time matching	90	—	111.11	%
Clock timings					
$t_{DFRATHS}$	Full-speed data rate for hubs and devices which are high-speed capable	11.994	—	12.006	Mbps
$t_{DFRATHS\_PPM}$	Full-speed data rate tolerance	-500	—	500	ppm
Full-speed data timings					
t_{DJ1}	Source jitter total (including frequency tolerance): to next transition	-3.5	—	3.5	ns
t_{DJ2}	Source jitter total (including frequency tolerance): for paired transitions	-4	—	4	ns
t_{JR1}	Receiver jitter total: to next transition	-18.5	—	18.5	ns
t_{JR2}	Receiver jitter: for paired transitions	-9	—	9	ns
t_{FDEOP}	Source jitter for differential transition to SE0 transition	-2	—	5	ns
t_{FEOPT}	Source SE0 interval of EOP	160	—	175	ns
Output levels for low-/full-speed					
V_{OL}	Output low	0	—	0.3	V
V_{OH}	Output high	2.8	—	3.6	V
V_{CRS}	Output single crossover voltage	1.3	—	2	V
Input levels for low-/full-speed					
V_{IH}	High (driven)	2	—	—	V
V_{IL}	Low	—	—	0.8	V
V_{DI}	Differential input sensitivity	0.2	—	—	V

12.3.1.3 USB device low-speed electrical characteristics

Table 67. USB LS driver and receiver specifications data

Symbol	Parameter	Min	Typ	Max	Unit
Driver specifications					
t_{LR}	Rise time	75	—	300	ns
t_{LF}	Data rise time	75	—	300	ns
t_{LRFM}	Rise and fall time matching	80	—	125	%
Clock timings					
$t_{LDRATHS}$	Low-speed data rate for hubs which are high-speed capable	1.49925	—	1.50075	Mbit/s
$t_{DFRATHS\_PPM}$	Low-speed data rate tolerance	-500	—	500	ppm
Low-speed data timings					
tT_{UDJ1}	Upstream facing port source jitter. Total (including frequency tolerance) : to next transition	-95	—	95	ns
t_{UDJ2}	Upstream facing port source jitter. Total (including frequency tolerance) : for paired transition	-150	—	150	ns

12.3.1.4 USB interface driver waveforms

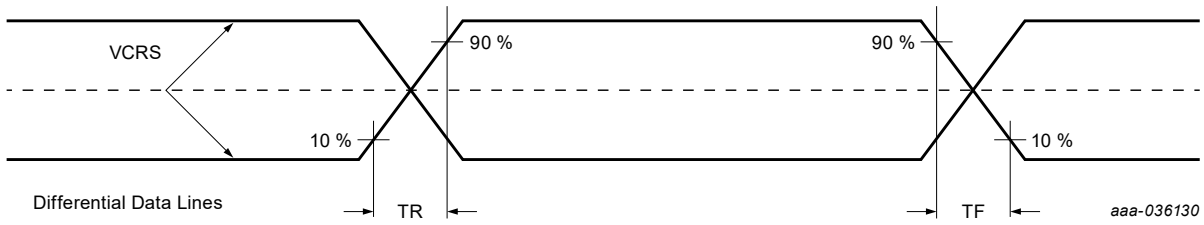


Figure 48. USB LS/FS data rise and fall time diagram

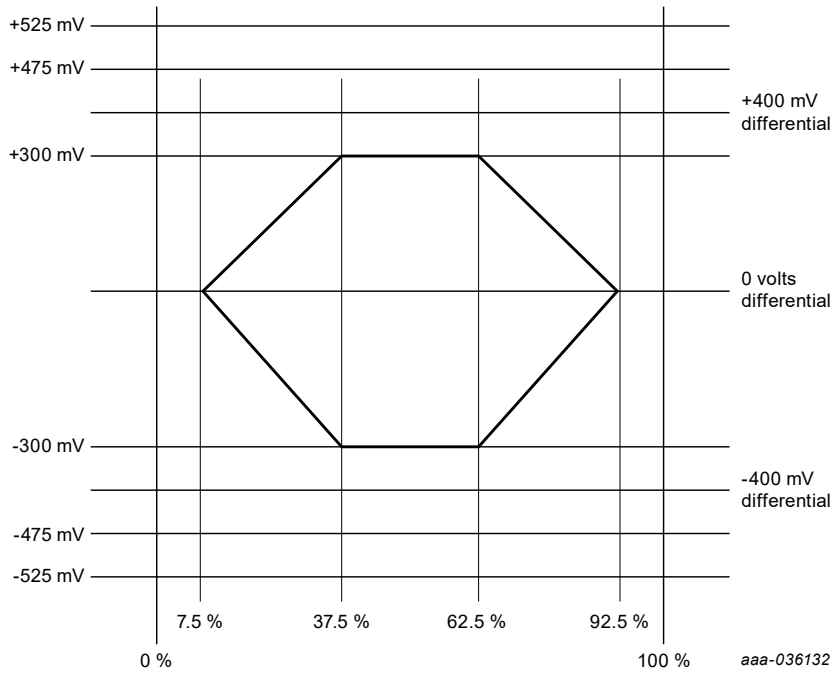


Figure 49. USB HS Tx eye diagram pattern template diagram

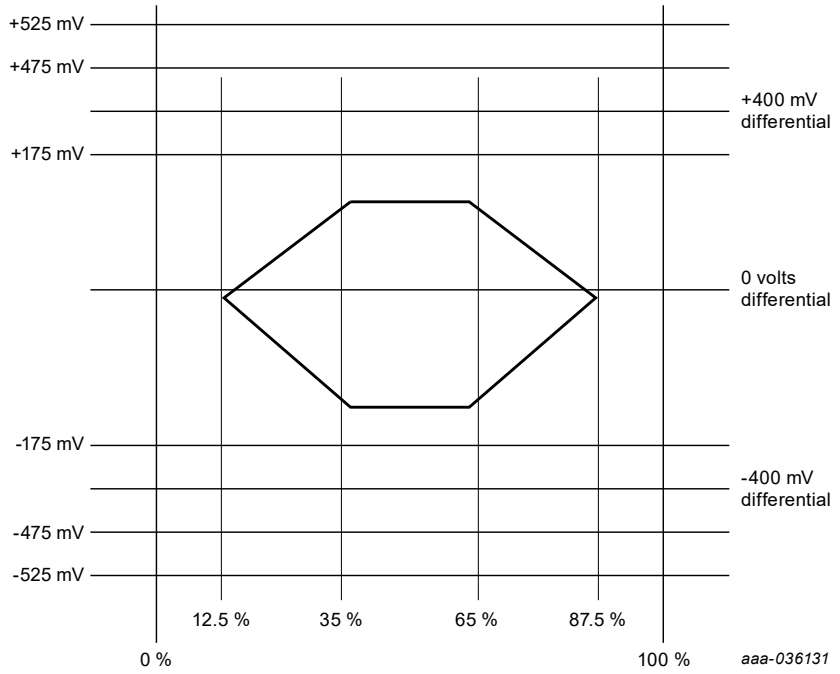


Figure 50. USB HS Rx eye diagram pattern template diagram

12.3.2 FlexSPI flash interface specifications

Table 68. Dynamic characteristics - FlexSPI flash interface

Unless otherwise specified, the values apply per Section 10 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
SDR mode						
t_{CK}	Clock frequency	Transmit	—	—	160	MHz
		RX clock source = 0 (internal dummy read strobe and loop backed internally)	—	—	70	MHz
		RX clock source = 1 (internal dummy read strobe and loop backed from DQS pad)	—	—	130	MHz
		RX clock source = 3 (external DQS. The flash provides the read strobe)	—	—	160	MHz
t_{CSS}	Chip select setup time	This value is the default value and configurable by software	3 x t_{CK} - 1	—	—	ns
t_{CSH}	Chip select hold time	This value is the default value and configurable by software	3 x t_{CK}	—	—	ns
t_{DS}	Data setup time	RX clock source = 0 (internal dummy read strobe and loop backed internally)	6	—	—	ns
		RX clock source = 1 (internal dummy read strobe and loop backed from DQS pad)	1.3	—	—	ns
		RX clock source = 3 (external DQS. The flash provides the read strobe)	0.8	—	—	ns
t_{DH}	Data hold time	RX clock source = 0 (internal dummy read strobe and loop backed internally)	0	—	—	ns
		RX clock source = 1 (internal dummy read strobe and loop backed from DQS pad)	1	—	—	ns
		RX clock source = 3 (external DQS. The flash provides the read strobe)	0	—	—	ns
t_{DVO}	Data output valid time	—	—	—	1	ns
t_{DHO}	Data output hold time	—	-1	—	—	ns

Table 68. Dynamic characteristics - FlexSPI flash interface*...continued*

Unless otherwise specified, the values apply per Section 10 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
DDR mode (with and without DQS)						
t_{CK}	Clock frequency	Transmit	—	—	160	MHz
		RX clock source = 0	—	—	35	MHz
		RX clock source = 1	—	—	64	MHz
		RX clock source = 3	—	—	160	MHz
t_{CSS}	Chip select setup time	This value is the default value and configurable by software	3 x t_{CK}/2 - 0.7	—	—	ns
t_{CSH}	Chip select hold time	This value is the default value and configurable by software	3 x t_{CK}/2	—	—	ns
t_{DS}	Data set-up time	RX clock source = 0 (internal dummy read strobe and loop backed internally)	6	—	—	ns
		RX clock source = 1 (internal dummy read strobe and loop backed from DQS pad)	1.3	—	—	ns
		RX clock source = 3 (external DQS. The flash provides the read strobe)	0.6	—	—	ns
t_{DH}	Data hold time	RX clock source = 0 (internal dummy read strobe and loop backed internally)	0	—	—	ns
		RX clock source = 1 (internal dummy read strobe and loop backed from DQS pad)	1	—	—	ns
		RX clock source = 3 (external DQS. The flash provides the read strobe)	0	—	—	ns
t_{DVO}	Data output valid time	—	—	—	2.3	ns
t_{DHO}	Data output hold time	—	0.8	—	—	ns

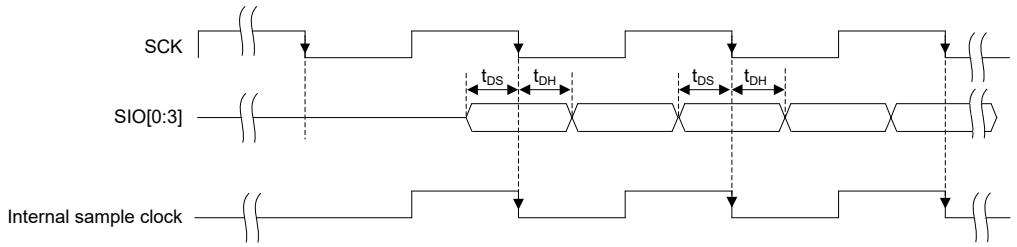


Figure 51. SDR mode (input timing, mode 0 and mode 1)

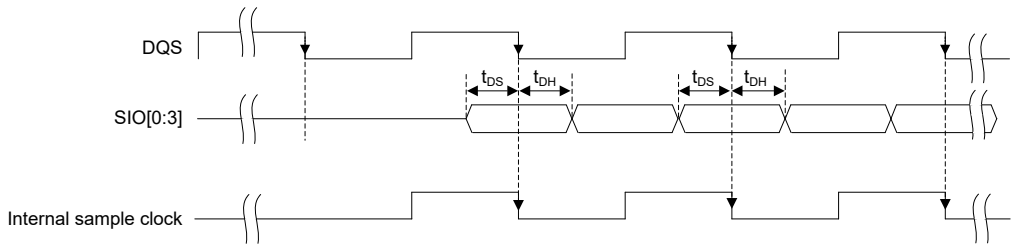


Figure 52. SDR mode (input timing, mode 3)

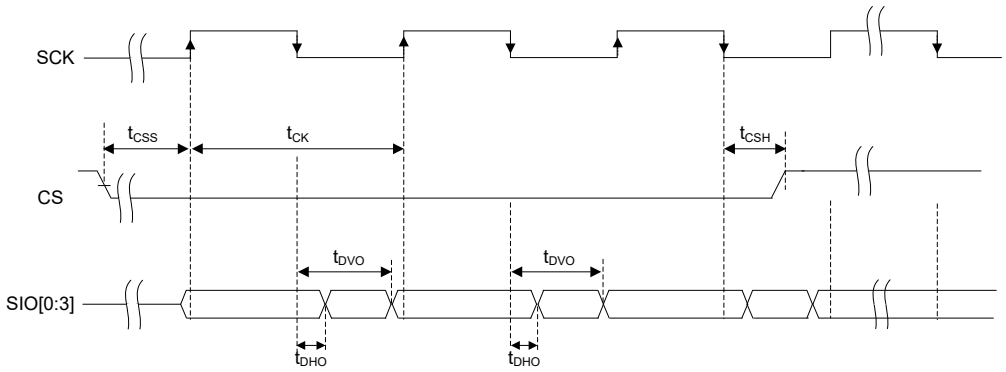


Figure 53. SDR mode (output timing)

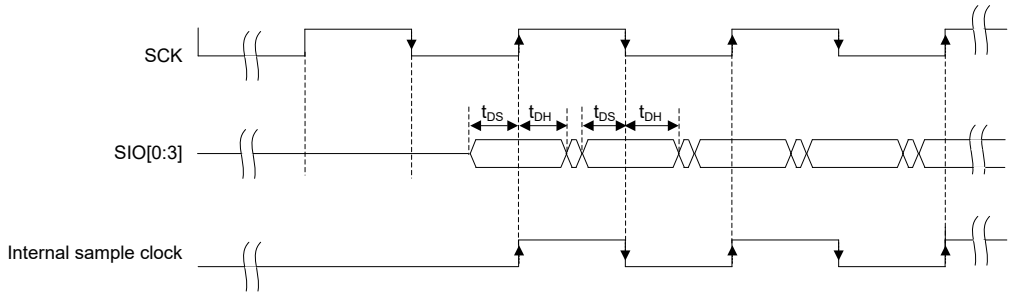


Figure 54. DDR mode (input timing, mode 0 and mode 1)

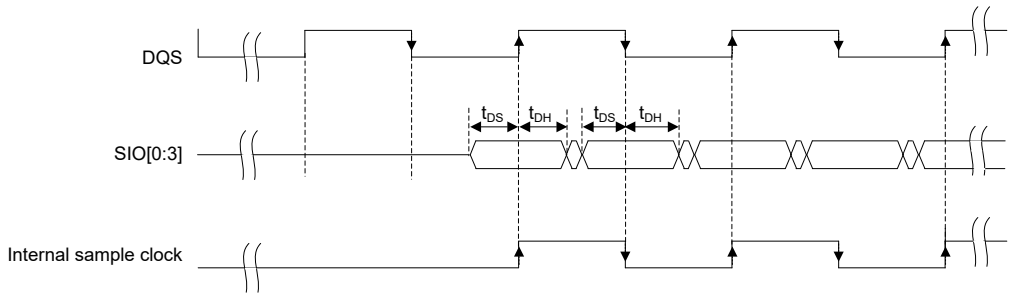


Figure 55. DDR mode (input timing, mode 3)

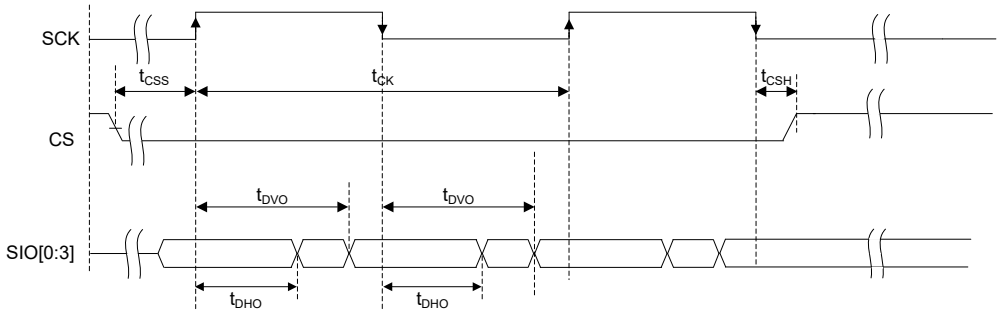


Figure 56. DDR mode (output timing)

12.3.3 SDIO 3.0 interface specifications

12.3.3.1 Default speed, high-speed modes

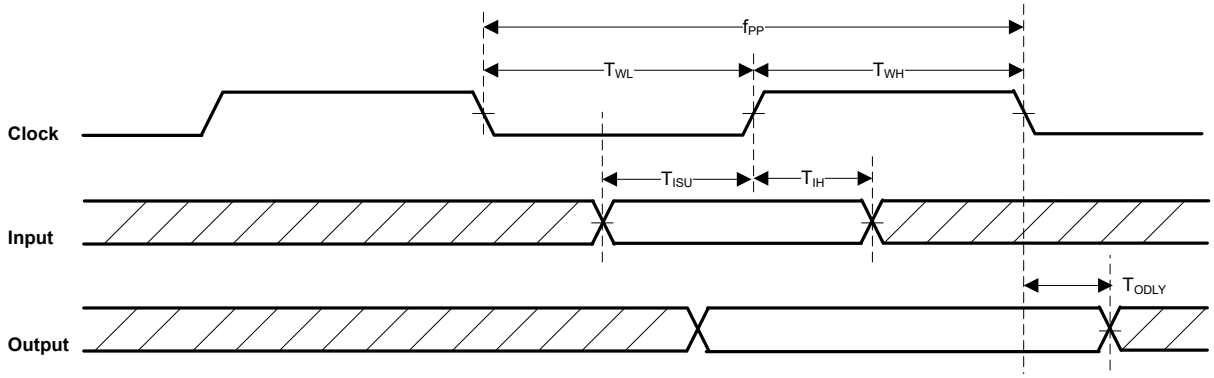


Figure 57. SDIO protocol timing diagram—Default speed mode

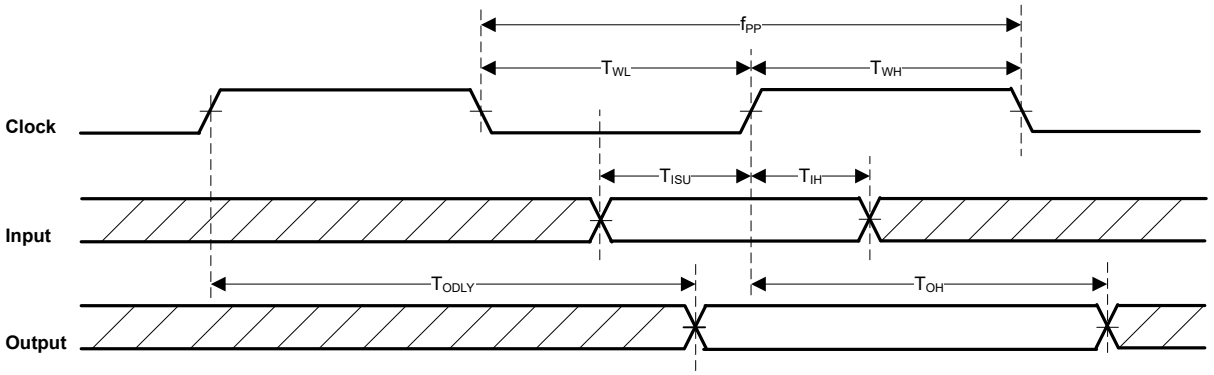


Figure 58. SDIO protocol timing diagram—High-speed mode

Table 69. SDIO timing data—Default speed, high-speed modes (3.3 V)

Unless otherwise specified, the values apply per Section 10 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PP}	Clock frequency	Normal	0	--	25	MHz
		High-speed	0	--	50	MHz
T_{WL}	Clock low time	Normal	19.76	--	--	ns
		High-speed	9.04	--	--	ns
T_{WH}	Clock high time	Normal	20.24	--	--	ns
		High-speed	9.13	--	--	ns
T_{ISU}	Input setup time	Normal	0.751	--	--	ns
		High-speed	1.52	--	--	ns
T_{IH}	Input hold time	Normal	0.9	--	--	ns
		High-speed	0.9	--	--	ns
T_{ODLY}	Output delay time	Normal	--	--	8.4	ns
	CL ≤ 40 pF (1 card)	High-speed	--	--	7.2	ns
T_{OH}	Output hold time	High-speed	2.5	--	--	ns

12.3.3.2 SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8V)

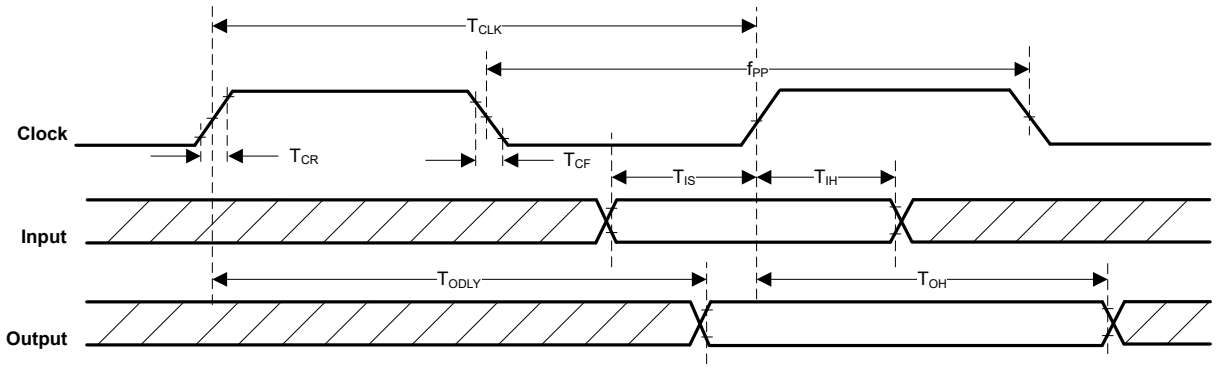


Figure 59. SDIO protocol timing diagram—SDR12, SDR25, SDR50 Modes (up to 100 MHz) (1.8V)

Table 70. SDIO timing data——SDR12, SDR25, SDR50 Modes (up to 100 MHz) (1.8V)

Unless otherwise specified, the values apply per Section 10 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PP}	Clock frequency	SDR12/25/50	25	--	100	MHz
T_{IS}	Input setup time	SDR12/25/50	3	--	--	ns
T_{IH}	Input hold time	SDR12/25/50	0.8	--	--	ns
T_{CLK}	Clock time	SDR12/25/50	10	--	40	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 2 ns (max) at 100 MHz C_{CARD} = 10 pF	SDR12/25/50	--	--	0.2*T_{CLK}	ns
T_{ODLY}	Output delay time C_L ≤ 30 pF	SDR12/25/50	--	--	7.5	ns
T_{OH}	Output hold time C_L = 15 pF	SDR12/25/50	1.5	--	--	ns

12.3.3.3 SDR104 mode (208 MHz) (1.8V)

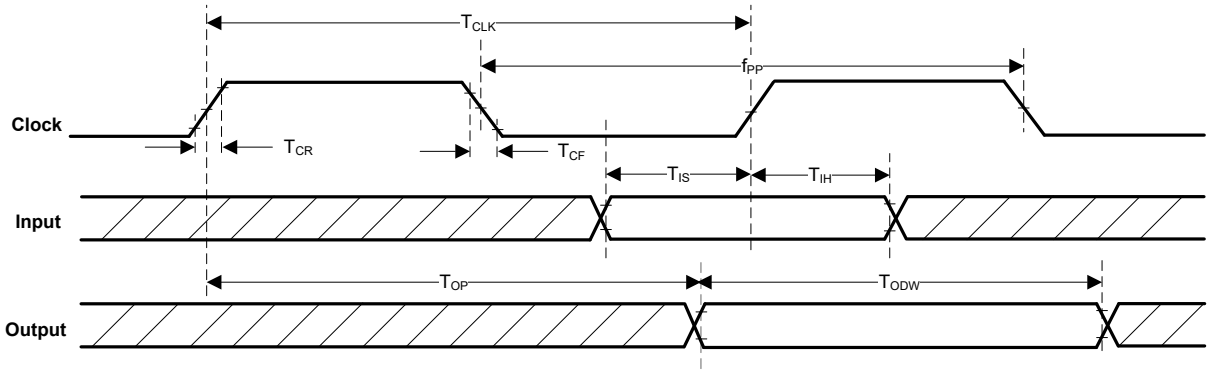


Figure 60. SDIO protocol timing diagram—SDR104 mode (208 MHz)

Table 71. SDIO timing data—SDR104 mode (208 MHz)

Unless otherwise specified, the values apply per Section 10 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PP}	Clock frequency	SDR104	0	--	208	MHz
T_{IS}	Input setup time	SDR104	1.4	--	--	ns
T_{IH}	Input hold time	SDR104	0.8	--	--	ns
T_{CLK}	Clock time	SDR104	4.8	--	--	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 0.96 ns (max) at 208 MHz C_{CARD} = 10 pF	SDR104	--	--	0.2*T_{CLK}	ns
T_{OP}	Card output phase	SDR104	0	--	10	ns
T_{ODW}	Output timing of variable data window	SDR104	2.88	--	--	ns

12.3.3.4 DDR50 mode (50 MHz) (1.8V)

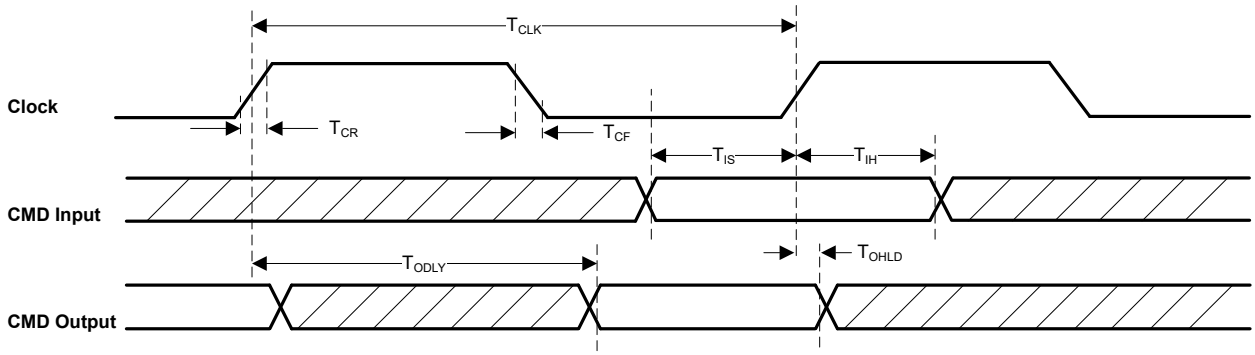
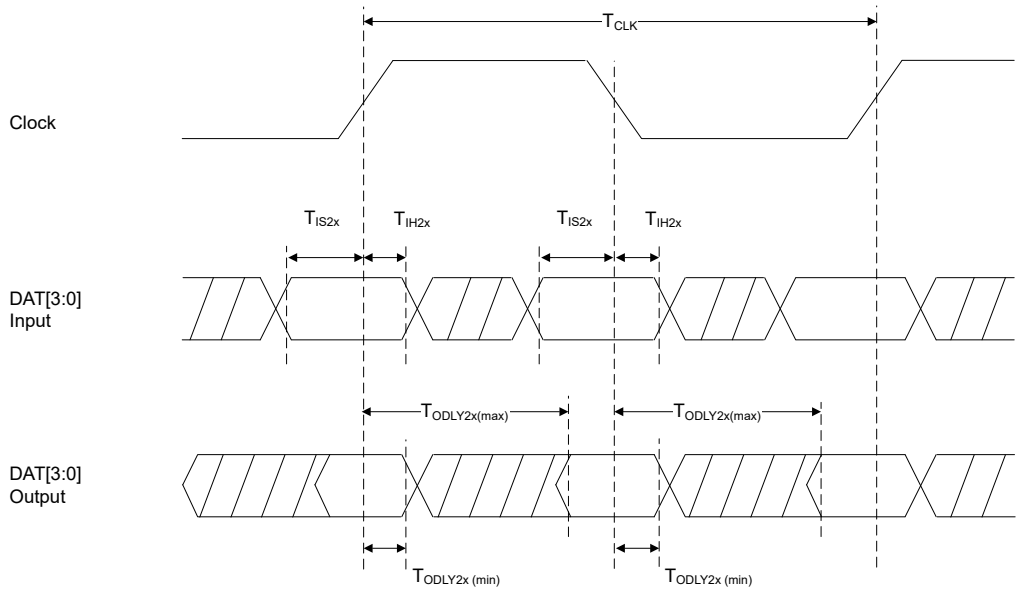


Figure 61. SDIO CMD timing diagram—DDR50 mode (50 MHz)



In DDR50 mode, DAT[3:0] lines are sampled on both edges of the clock (not applicable for CMD line).)

Figure 62. SDIO DAT[3:0] timing diagram—DDR50 mode (50 MHz

Table 72. SDIO timing data—DDR50 mode (50 MHz)

Unless otherwise specified, the values apply per Section 10 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Clock						
T_{CLK}	Clock time 50 MHz (max) between rising edges	DDR50	20	--	--	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 4.00 ns (max) at 50 MHz C_{CARD} = 10 pF	DDR50	--	--	0.2*T_{CLK}	ns
Clock duty	--	DDR50	45	--	55	%
CMD input (referenced to clock rising edge)						
T_{IS}	Input setup time C_{CARD} ≤ 10 pF (1 card)	DDR50	6	--	--	ns
T_{IH}	Input hold time C_{CARD} ≤ 10 pF (1 card)	DDR50	0.8	--	--	ns
CMD output (referenced to clock rising edge)						
T_{ODLY}	Output delay time during data transfer mode C_L ≤ 30 pF (1 card)	DDR50	--	--	13.7	ns
T_{OHLD}	Output hold time C_L ≥ 15 pF (1 card)	DDR50	1.5	--	--	ns
DAT[3:0] Input (referenced to clock rising and falling edges)						
T_{IS2x}	Input setup time C_{CARD} ≤ 10 pF (1 card)	DDR50	3	--	--	ns
T_{IH2x}	Input hold time C_{CARD} ≤ 10 pF (1 card)	DDR50	0.8	--	--	ns
DAT[3:0] Output (referenced to clock rising and falling edges)						
$T_{ODLY2x\ (max)}$	Output delay time during data transfer mode C_L ≤ 25 pF (1 card)	DDR50	--	--	7.0	ns
$T_{ODLY2x\ (min)}$	Output hold time C_L ≥ 15 pF (1 card)	DDR50	1.5	--	--	ns

12.3.3.5 SDIO internal pull-up/pull-down specifications

Table 73. SDIO internal pull-up/pull-down specifications

Unless otherwise specified, the values apply per Section 10 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
Internal nominal pull-up/pull-down resistance	--	70	100	140	kΩ

12.3.4 Ethernet interface specifications

In RMII mode, ENET_CLK is used as the continuous reference clock (REF_CLK). ENET_CLK value is 50 MHz ± 50 ppm.

Figure 63 RMII mode timings.

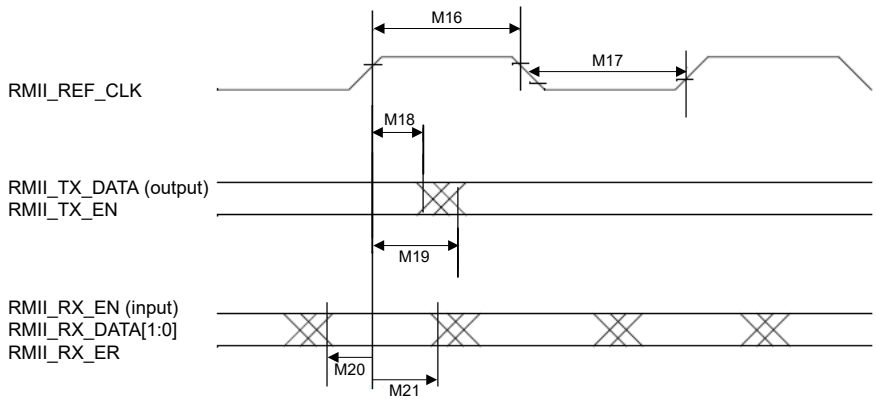


Figure 63. Ethernet RMII mode timing diagram

Table 74 describes the timing parameters (M16-M21) shown in Figure 63.

Table 74. Ethernet RMII mode timing data

ID	Parameter	Min.	Max.	Unit
M16	RMII_REF_CLK pulse width high	35%	65%	ENET_CLK period
M17	RMII_REF_CLK pulse width low	35%	65%	ENET_CLK period
M18	RMII_REF_CLK to RMII_TXD1/RMII_TXD0, RMII_TX_DATA invalid	4	—	ns
M19	RMII_REF_CLK to RMII_TXD1/RMII_TXD0, RMII_TX_DATA valid	—	13	ns
M20	RMII_RXD1/RMII_RXD0, RMII_RX_EN, RMII_RX_ER to RMII_REF_CLK setup	3	—	ns
M21	RMII_REF_CLK to RMII_RXD1/RMII_RXD0, RMII_RX_EN, RMII_RX_ER hold	2	—	ns

12.3.5 LCD interface specifications

12.3.5.1 LCD SPI 3-wire specifications

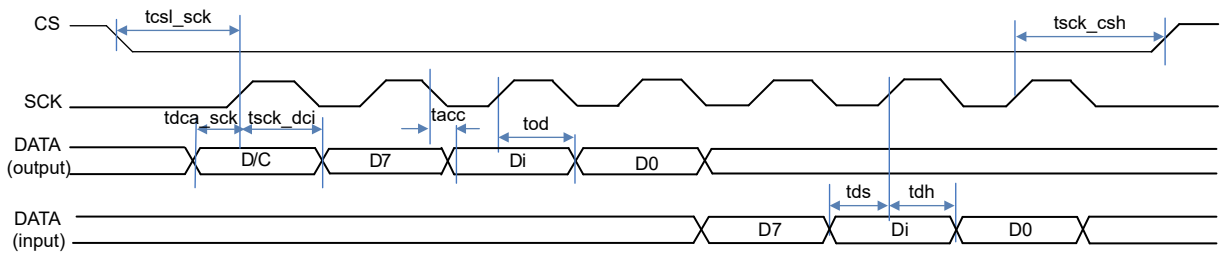


Figure 64. LCD SPI 3-wire interface timing diagram

Table 75. LCD SPI 3-wire interface timing

Signal	Symbol	Parameter	Min	Max	Unit
SCK	tck	SCK frequency	—	32	MHz
CS	tcsl_sck	CS low to SCK time	1/tck	—	ns
	tsck_csh	SCK to CS high time	1/tck	—	ns
DATA(output)	tdca_sck	DC active to SCK time	5	—	ns
	tsck_dci	SCK to DC inactive time	5	—	ns
	tacc	DATA output access time	10.6	—	ns
	tod	DATA output disable time	5	—	ns
DATA(input)	tds	DATA input setup time	7.6	—	ns
	tdh	DATA input hold time	0	—	ns

12.3.5.2 LCD SPI 4-wire specifications

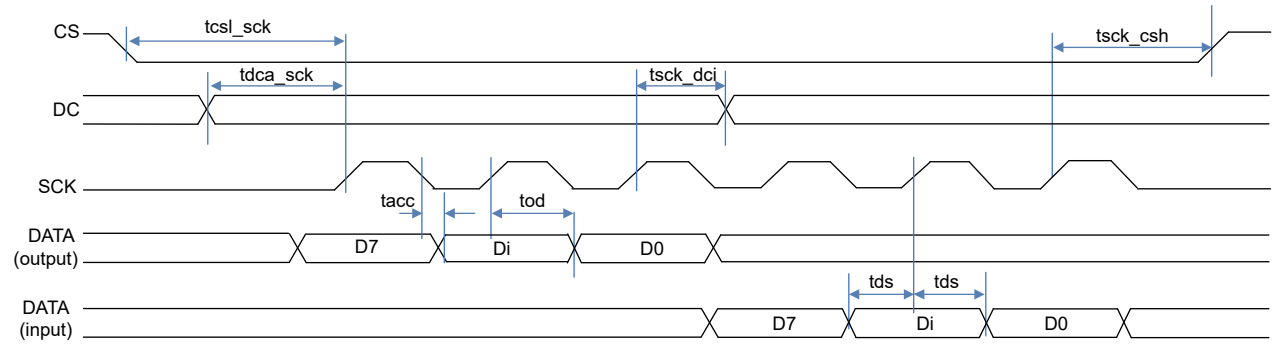


Figure 65. LCD interface timing diagram

Table 76. LCD SPI 4-wire timing

Signal	Symbol	Parameter	Min	Max	Unit
SCK	tck	SCK frequency	—	32	MHz
CS	tcsl_sck	CS low to SCK time	1/tck	—	ns
	tsck_csh	SCK to CS high time	1/tck	—	ns
DC	tdca_sck	DC active to SCK time	5	—	ns
	tsck_dci	SCK to DC inactive time	5	—	ns
DATA(output)	tacc	DATA output access time	10.6	—	ns
	tod	DATA output disable time	5	—	ns
DATA(input)	tds	DATA input setup time	7.6	—	ns
	tdh	DATA input hold time	0	—	ns

12.3.5.3 LCD 8080 specifications

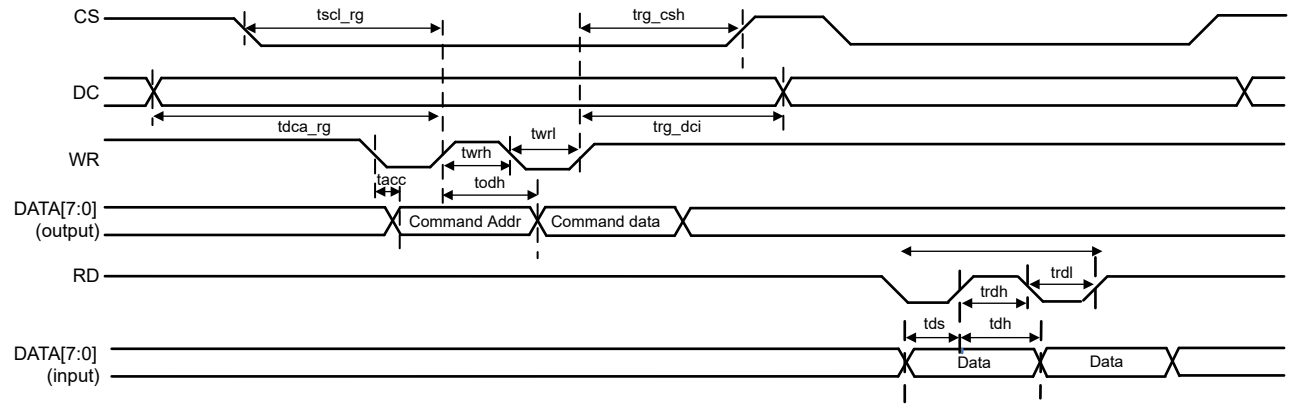


Figure 66. LCD 8080 interface timing diagram

Table 77. LCD 8080 interface timing

Signal	Symbol	Parameter	Min	Max	Unit
CS	tcsl_rg	CS low to WR/RD rising edge time. This value is the minimum value and configurable by software	6	–	ns
	trg_csh	WR/RD rising edge to CS high time. This value is the minimum value and configurable by software	6	–	ns
DC	tdca_rg	DC active to WR/RD rising edge time. This value is the minimum value and configurable by software	10	–	ns
	trg_dci	WR/RD rising edge to DC inactive time. This value is the minimum value and configurable by software	10	–	ns
WR	twrh	write enable inactive pulse width. This value is the minimum value and configurable by software	31	–	ns
	twrl	write enable active pulse width. This value is the minimum value and configurable by software	31	–	ns
RD	trdh	read enable inactive pulse width. This value is the minimum value and configurable by software	62.5	–	ns
	trdl	read enable active pulse width. This value is the minimum value and configurable by software	62.5	–	ns
DATA[7:0] (output)	tacc	output data access time. This value is the minimum value and configurable by software	21	–	ns
	tod	output data disable time. This value is the minimum value and configurable by software	10	–	ns
DATA[7:0] (input)	tds	input data setup time	18	–	ns
	tdh	input data hold time	20	–	ns

12.3.6 USART interface specifications

Excluding delays introduced by external device and PCB, the maximum supported bit rate for USART master synchronous mode is 20 Mbit/s, and the maximum supported bit rate for USART client synchronous mode is 20.0 Mbit/s.

Excluding delays introduced by external device and PCB, the maximum bit rates of 6.25 Mbit/s in asynchronous mode.

The actual USART bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading.

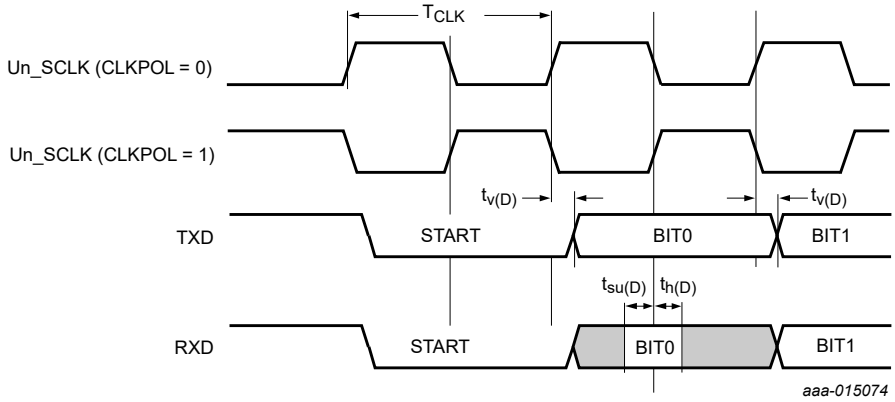


Figure 67. USART timing diagram

Table 78. USART timing data[1]

Over full range of values specified in Section 10 "Recommended operating conditions" unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
USART master (in synchronous mode)						
T_{CLK}	Clock period	—	50	—	—	ns
$T_{su(D)}$	Data input set-up time	—	13.5	—	—	ns
$T_{h(D)}$	Data input hold time	—	0	—	—	ns
$T_{v(D)}$	Data output valid time	—	0	—	4	ns
USART client (in synchronous mode)						
T_{CLK}	Clock period	—	50	—	—	ns
$T_{su(D)}$	Data input set-up time	—	6	—	—	ns
$T_{h(D)}$	Data input hold time	—	0	—	—	ns
$T_{v(D)}$	Data output valid time	—	0	—	13	ns

[1] Based on simulation; not tested in production.

12.3.7 I2C bus interface specifications

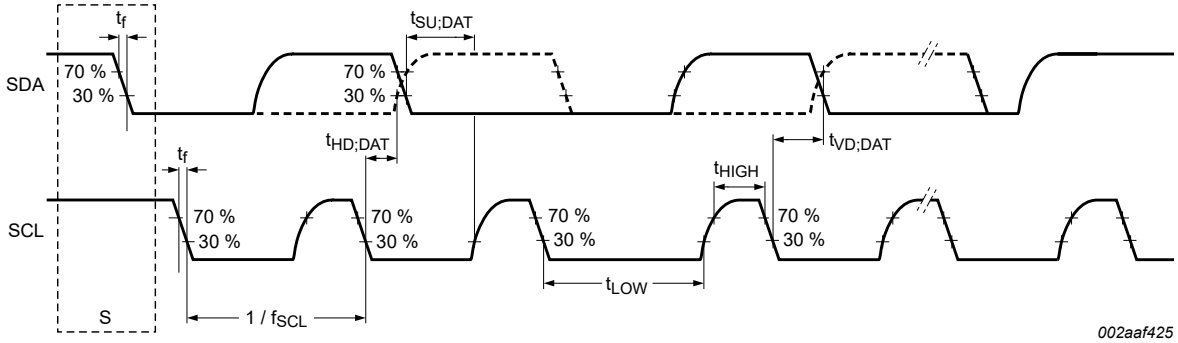


Figure 68. I2C timing diagram

Table 79. I2C timing data

Unless otherwise specified, the values apply per Section 10 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{SCL}	SCLK clock frequency	Standard mode	0	—	100	kHz
		Fast mode	0	—	400	kHz
		Fast mode plus	0	—	1	MHz
t_{LOW}	Low period of the CLK clock	Standard mode	4.7	—	—	µs
		Fast mode	1.3	—	—	µs
		Fast mode plus	0.5	—	—	µs
t_{HIGH}	High period of the CLK clock	Standard mode	4	—	—	µs
		Fast mode	0.6	—	—	µs
		Fast mode plus	0.26	—	—	µs
$t_{HD;DAT}$	Data hold time	Standard mode	0	—	—	µs
		Fast mode	0	—	—	µs
		Fast mode plus	0	—	—	µs
$T_{SU;DAT}$	Data set-up time	Standard mode	250	—	—	ns
		Fast mode	100	—	—	ns
		Fast mode plus	50	—	—	ns

12.3.8 SPI interface

The actual SPI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading.

Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI controller mode (transmit/receive) is 30 Mbit/s and the maximum supported bit rate for SPI target mode (transmit/receive) is 30 Mbps.

Table 80. SPI host interface timing data[1]

Unless otherwise specified, the values apply per Section 10 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
SPI controller						
SPI Freq	Clock frequency	—	—	—	30	MHz
T_{DS}	Data set-up time	—	5.4	—	—	ns
T_{DH}	Data hold time	—	0	—	—	ns
$T_{v(Q)}$	Data output valid time	—	0	—	9.6	ns
SPI target						
SPI Freq	Clock frequency	—	—	—	30	MHz
T_{DS}	Data set-up time	—	5	—	—	ns
T_{DH}	Data hold time	—	0	—	—	ns
$T_{v(Q)}$	Data output valid time	—	0	—	10.2	ns

[1] Based on simulation; not tested in production.

12.3.9 I2S bus interface specifications

The I2S pins are supplied by VIO. See Section 12.2.

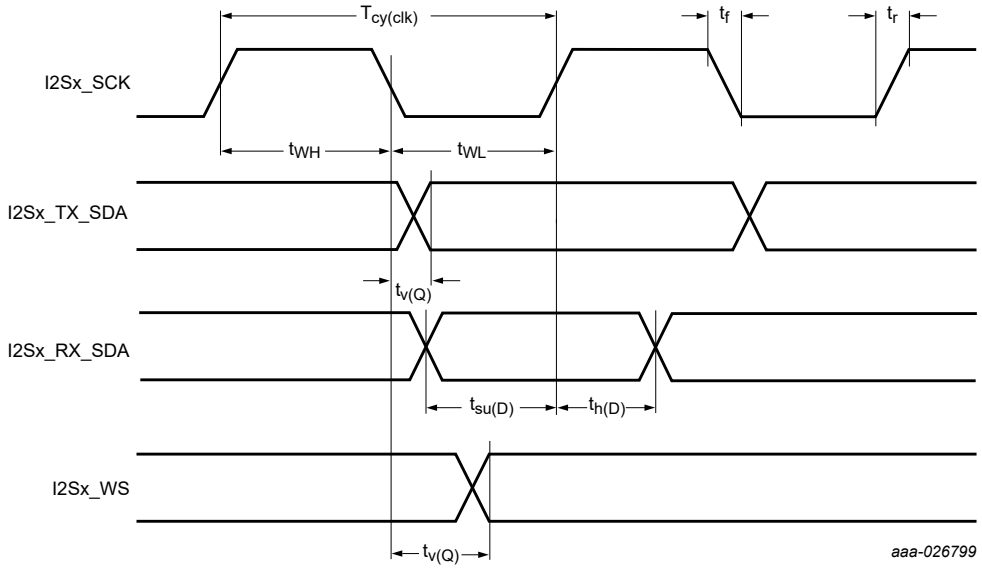


Figure 69. I2S bus timing (master)

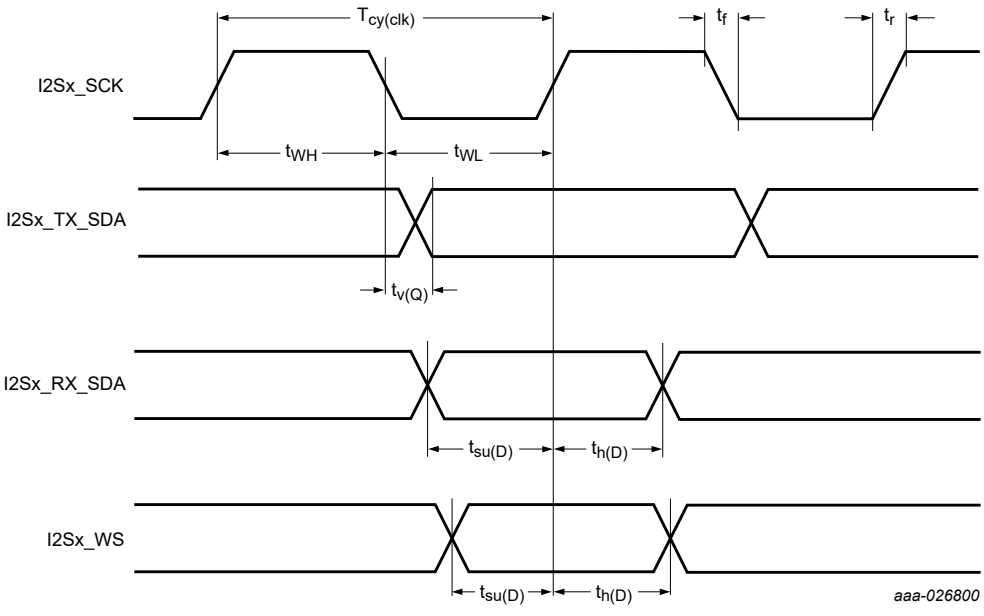


Figure 70. I2S bus timing (central)

Table 81. I2S timing data[1]

Over full range of values specified in Section 10 "Recommended operating conditions" unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Common to central and peripheral						
t_{WH}	pulse width HIGH	on pins I2Sx_TX_SCK and I2Sx_RX_SCK	(T_{CYC}/2) -1	—	(T_{CYC}/2) +1	ns
t_{WL}	pulse width LOW	on pins I2Sx_TX_SCK and I2Sx_RX_SCK	(T_{CYC}/2) -1	—	(T_{CYC}/2) +1	ns
Central (25 MHz)						
$T_{v(Q)}$	Data output valid time	on pin I2Sx_TX_SDA	0	—	15	ns
		on pin I2Sx_WS	0	—	20	ns
$T_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	13	—	—	ns
$T_{h(D)}$	Data input hold time	on pin I2Sx_RX_SDA	0	—	—	ns
Peripheral (20 MHz)						
$T_{v(Q)}$	Data output valid time	on pin I2Sx_TX_SDA	0	—	18	ns
$T_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	6	—	—	ns
		on pin I2Sx_WS	6	—	—	ns
$T_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	0	—	—	ns
		on pin I2Sx_WS	0	—	—	ns

[1] Based on simulation; not tested in production.

12.4 Audio interface specifications

PCM is implemented with two Flexcomm I2S where one I2S is set as central (PCM_DOUT) and the other I2S is set as peripheral (PCM_DIN). The timing specification follows I2S bus interface specifications (Section 12.3.9).

Figure 71 shows the example of connection to a bidirectional PCM codec with one I2S set as central. In the figure, *Wireless SoC* is RW610.

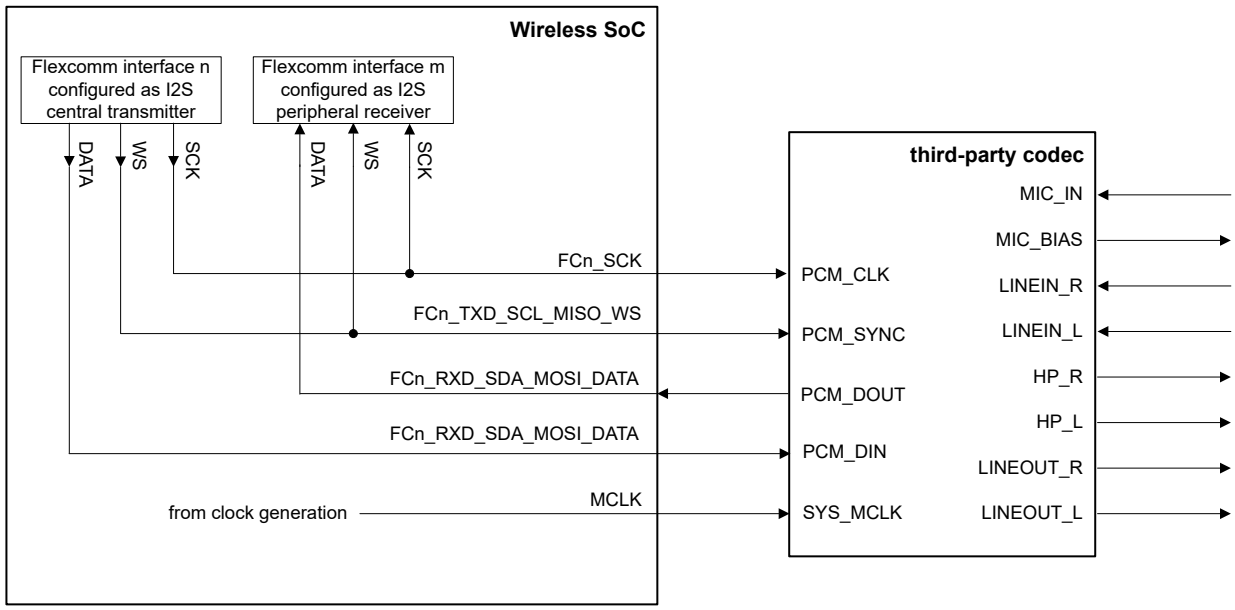


Figure 71. Example of connection to a bidirectional PCM codec - (PCM_SYNC as central)

Table 82 shows the signal name mapping for Figure 72 to Figure 76

Table 82. PCM pin mapping

I2S signal	PCM signal
I2S_SCLK	FCn_SCK
I2Sx_WS	FCn_TXD_SCL_MISO_WS
I2S_TX_SDA	FCn_RXD_SDA_MOSI_DATA
I2S_RX_SDA	FCn_RXD_SDA_MOSI_DATA

Figure 72 shows the timing specification for the data signals in central mode.

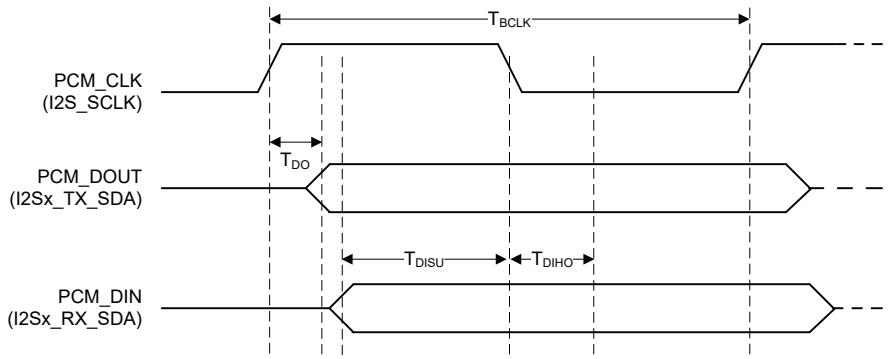


Figure 72. PCM timing specification for data signals—Central mode

Figure 73 shows the timing specification for PCM_SYNC signal in central mode.

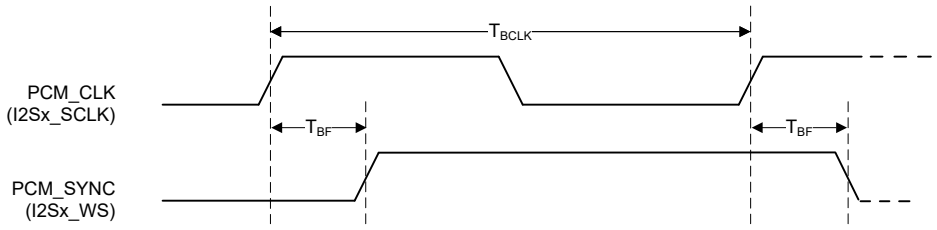


Figure 73. PCM timing specification for PCM_SYNC signal—Central mode

Figure 74 shows the example of connection to a bidirectional PCM codec with one I2S set as peripheral. In the figure, *Wireless SoC* is RW610.

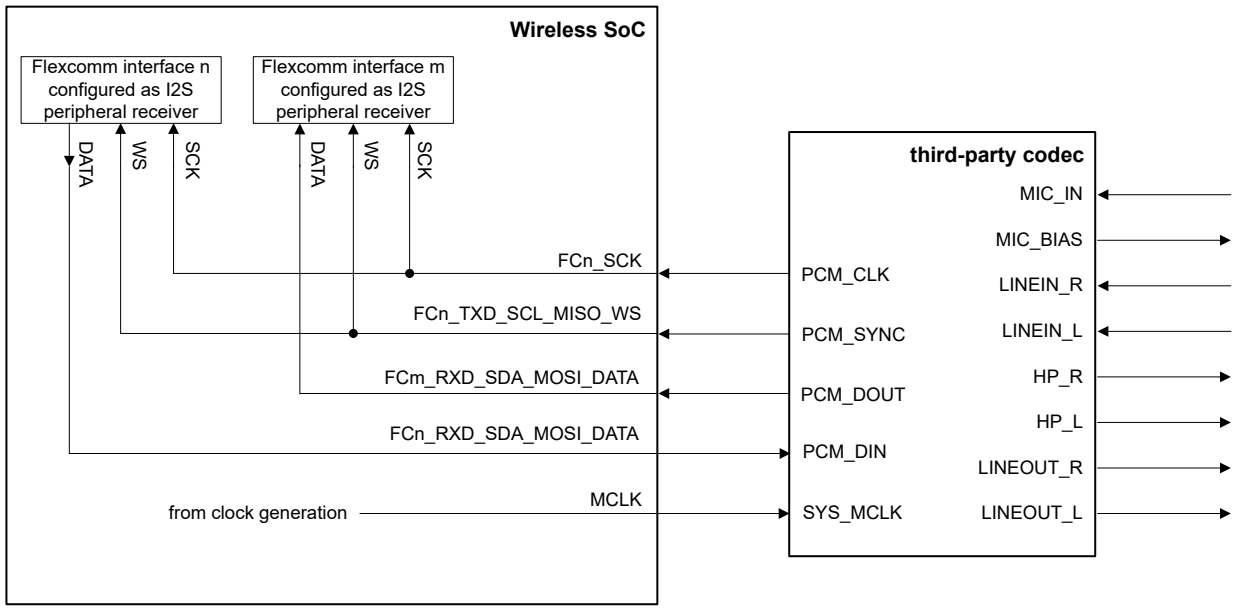


Figure 74. Second example of connection to a bidirectional PCM codec - (PCM_SYNC as peripheral)

Figure 75 shows the timing specification for the data signals in peripheral mode.

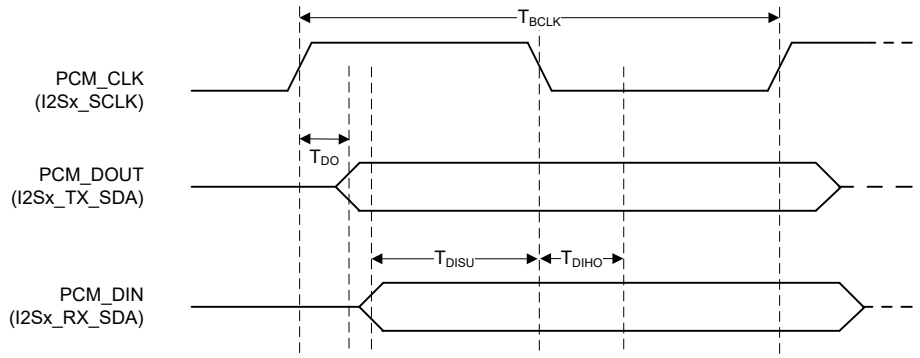


Figure 75. PCM timing specification for data signals—Peripheral mode

Figure 76 shows the timing specification for PCM_SYNC signal in peripheral mode.

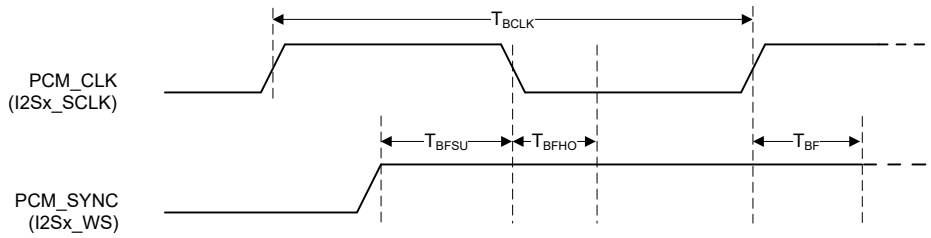


Figure 76. PCM timing specification for PCM_SYNC signal—Peripheral mode

12.5 Analog peripherals

12.5.1 ACOMP specifications

These are design guidelines and are based on bench characterization results and/or design simulation.

Minimum and maximum values: Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage, and frequencies by tests on bench.

Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value ±3 times the standard deviation.

Table 83. ACOMP specifications

Unless otherwise specified, the values apply per Section 10 "Recommended operating conditions".

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Analog input						
--	Analog input voltage	Any pin (in analog input mode)	0	--	VIO_6	V
--	Common mode input range	--	0	--	VIO_6	V
Reference voltage						
--	Internal reference voltage	--	1.20	1.22	1.23	V
Analog response time (no digital delay)[1][2]						
--	Fast response mode MODE 3, Vcm = 1.5V	Overdrive (COMP_P – COMP_ N = ±100 mV	--	130	--	ns
--	Medium response mode MODE 2, Vcm = 1.5V	Overdrive (COMP_P – COMP_ N = ±100 mV	--	190	--	ns
--	Slow response mode MODE 1, Vcm = 1.5V	Overdrive (COMP_P – COMP_ N = ±100 mV	--	450	--	ns
DC offset						
--	Offset voltage	--	--	±14	--	mV
--	Hysteresis	Programmed in 7 steps and 0	--	10	--	mV
--			--	20	--	mV
--			--	30	--	mV
--			--	40	--	mV
--			--	50	--	mV
--			--	60	--	mV
--			--	70	--	mV
Warm-up time						
TWARM	Warm-up time of ACOMP and internal reference generator	VIO_6 = 3.3V	--	0.5	1.0	µs
		VIO_6 = 1.8V	--	1.0	1.3	µs

[1] Digital delay can be up to a maximum of 2, 19.6 MHz clock periods).
[2] Vcm is the common-mode voltage on COMP_P and COMP_N

12.5.2 DAC specifications

These are design guidelines and are based on bench characterization results and/or design simulation.

Minimum and maximum values: Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage, and frequencies by tests on bench.

Table 84. DAC specifications

Unless otherwise specified, the values apply per Section 10 "Recommended operating conditions".

Parameter	Condition	Min	Typ	Max	Unit
DAC main clock	FVCO = 128 MHz post divider ratio = 2	--	64	--	MHz
Reference voltage (Vref)					
Internal reference voltage	gpdac_a_range[1:0]=11	--	1.42	--	V
	gpdac_a_range[1:0]=10/01	--	1.01	--	V
	gpdac_a_range[1:0]=00	--	0.64	--	V
External reference voltage	gpdac_a_range[1:0]=11	--	Vref_ext*0.71	--	V
	gpdac_a_range[1:0]=10/01	--	Vref_ext*0.505	--	V
	gpdac_a_range[1:0]=00	--	Vref_ext*0.32	--	V
Externally supplied reference voltage (Vref_ext)	Ref_sel=1	1.5	--	2	V
Conversion range					
Analog output range	Single ended	0.12	--	1.6	V
Output load					
Resistive load (minimum resistive load between DAC output and VSS)	single-ended	5	--	--	kΩ
	differential	5	--	--	kΩ
Capacitive load (maximum capacitive load at DAC output)	--	--	--	50	pF
Conversion rate					
Conversion rate	clk_ctrl[1:0]=2'b11	--	500	--	kHz
	clk_ctrl[1:0]=2'b10	--	250	--	kHz
	clk_ctrl[1:0]=2'b01	--	125	--	kHz
	clk_ctrl[1:0]=2'b00 (default)	--	62.5	--	kHz

Table 84. DAC specifications*...continued*

Unless otherwise specified, the values apply per Section 10 "Recommended operating conditions".

Parameter	Condition	Min	Typ	Max	Unit
DC accuracy					
Resolution	single-ended	--	--	10	bits
	differential	--	--	10	bits
Differential non-linearity (RMS)	Guaranteed monotonic, internal 1.2V reference	--	±0.5	--	LSb[1]
Integral non-linearity (best-fit method)	Internal reference	--	±2	--	LSb
Offset error	a_range=2'b11, internal vref (difference between measured value at code 0x0 and the ideal value (0.18V))	--	±20	--	mV
Gain error (after offset removal)	a_range=2'b11, internal vref	--	2	--	%
PSRR	Power supply rejection ratio (to AVDD18) (static DC measurement)	--	60	--	dB

[1] 1 LSb= Vref/1024

12.5.3 ADC specifications

These are design guidelines and are based on bench characterization results and/or design simulation.

Minimum and maximum values: Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage, and frequencies by tests on bench.

Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value ±3 times the standard deviation.

Table 85. ADC specifications

Unless otherwise specified, the values apply per Section 10 "Recommended operating conditions".

Symbol	Parameter	Condition	Min	Typ	Max	Unit
--	ADC main clock	FVCO=128 MHz post divider ratio = 2	--	64	--	MHz
Reference voltage						
--	Internal reference voltage	--	1.20	1.22	1.23	V
--	External reference voltage	--	0.6	--	1.8	V
Analog inputs						
--	Input voltage	Input buffer disabled	0	--	VIO_6	V
		Input buffer enabled	0.2	--	VIO_6 - 0.2	V
--	ADC voltage conversion range • For 16-bit and 16-bit audio setting, input signal should be limited within 99.7% of the ADC voltage conversion range. • Vref stands for the voltage reference of the ADC. Could be an internal 1.22V, analog 1.8V power supply(1.8 V), or an external voltage (<1.8V).	--	-2*vref or -VIO_6	--	2*vref or VIO_6	V
CADC	Internal sampling and hold capacitance	--	--	1000	--	fF
RADC	Internal sampling switch resistance	--	1	--	--	kΩ
RMUX	Input multiplexer impedance	--	1	--	--	kΩ
RS	External input resistance RS maximum formula: 1/fADC RS < (RADC + RMUX) 15 4 × ln (2) × CADC	2 MHz ADC operating clock without input buffer 16-bit settling accuracy	--	--	8	kΩ
		2 MHz ADC operating clock with input buffer 16-bit settling accuracy	--	--	46	kΩ
--	Input frequency range Defined as input signal -3 dB bandwidth through analog path.	With input buffer	--	31	--	MHz
		Without input buffer	--	130	--	MHz

Table 85. ADC specifications*...continued*

Unless otherwise specified, the values apply per Section 10 "Recommended operating conditions".

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Conversion rate (ADC main clock frequency is 64 MHz)						
--	ADC sampling clock frequency	Fast mode	--	2	--	MHz
		Low-power mode	--	0.2	2	MHz
--	Conversion time in ADC clocks	12-bit setting	--	1	--	clock cycles
		14-bit setting	--	11	--	clock cycles
		16-bit setting	--	35	--	clock cycles
		16-bit audio setting	--	131	--	clock cycles
--	1-shot latency (It is recommended to perform a calibration after each power-up.)	16-bit audio setting @ 2 MHz	65.5 + TWARM	--	--	µs
		16-bit setting @ 2 MHz	17.5 + TWARM	--	--	µs
		14-bit setting @ 2 MHz	5.5 + TWARM	--	--	µs
		12-bit setting @ 2 MHz	0.5 + TWARM	--	--	µs
--	Data rate	16-bit audio setting @ 2 MHz	--	15.27	--	kHz
		16-bit setting @ 2 MHz	--	57.14	--	kHz
		14-bit setting @ 2 MHz	--	181.81	--	kHz
		12-bit setting @ 2 MHz	--	2000	--	kHz
DC accuracy						
--	Resolution	Single-ended	--	11	15	bits
		Differential	--	12	16	bits
	Offset error	Before calibration 16-bit setting	--	±30	--	LSb
		After calibration 16-bit setting	--	±4	--	LSb

Table 85. ADC specifications*...continued*

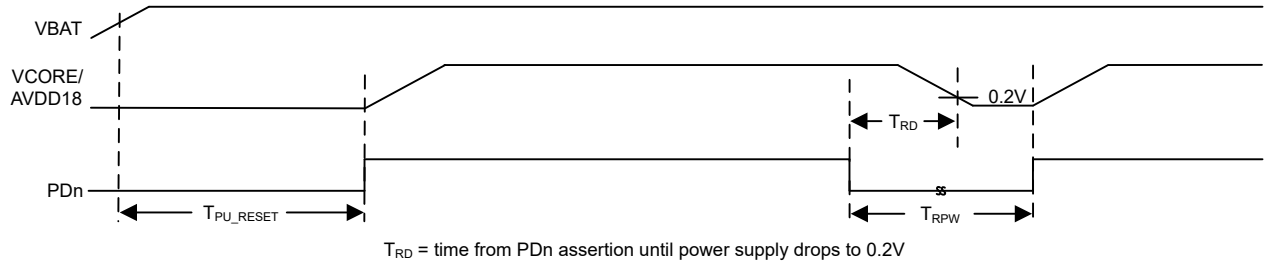
Unless otherwise specified, the values apply per Section 10 "Recommended operating conditions".

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Dynamic performance						
SNDR	Signal-to-Noise and-Distortion Ratio • With internal 1.22V reference, signal amplitude is 1.15Vp. • 1 kHz sine-wave differential input, 0 dB of full scale, 2 MHz ADC clock.	12-bit setting	--	64	--	dB
		14-bit setting	--	70	--	dB
		16-bit setting	--	76	--	dB
		16-bit audio setting	--	82	--	dB
--	Dynamic Range • With internal 1.22V reference, signal amplitude is 1mVp. • 1 kHz sine-wave differential input, -60 dB of full scale, 4 MHz ADC clock.	12-bit setting	--	66	--	dB
		14-bit setting	--	72	--	dB
		16-bit setting	--	78	--	dB
		16-bit audio setting	--	84	--	dB
Warm-up time						
TWARM	Warm-up time of ADC and internal reference generator (TWARM) • Total warm-up time (TWARM) depends on the current energy mode and 'gpadc_timebase' setting. • Programmable ADC main clock frequency = 64 MHz	--	1	--	32	µs

12.6 Power-down specifications

12.6.1 PDn asserted Low

Figure 77 and Table 86 show the specifications for the PDn signal when it is asserted (low) while AVDD18 ramps down.



T_{RD} = time from PDn assertion until power supply drops to 0.2V

Figure 77. Power-down (PDn) pin timing—Power ramps down at PDn assertion

Table 86. Power-down (PDn) pin specifications—Power ramps down at PDn assertion

Unless otherwise specified, the values apply per Section 10 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{PU_RESET}	Valid power to PDn de-asserted	--	0	—	—	ms
T_{RPW}	PDn pulse width	--	T_{RD}[1]	—	—	µs
V_{IH}	Input high voltage	--	1.75	—	3.63	V
V_{IL}	Input low voltage	--	-0.4	—	0.2	V

[1] Minimum value guaranteed for a valid reset. Smaller values may put the device in an undefined state.

12.7 Current consumption

Note: *The power consumption values refer to 3.3 V supply source (85% eff) and 25°C.*

Table 87. Power consumption values

The power consumption values are preliminary information subject to change based on the final device characterization results.

Mode	Conditions	Min	Typ	Max	Unit
MCU only (Wi-Fi and Bluetooth LE powered down)					
MCU in deep sleep mode	AON with 8 kB RAM retention	—	0.03	—	mA
MCU in sleep mode	512 kB RAM retention	—	0.14	—	mA
MCU in standby mode	Full clock gating	—	4.22	—	mA
MCU in idle mode	Partial clock gating	—	15.6	—	mA
MCU active	260 MHz, USB off	—	23.7	—	mA
MCU active	260 MHz, USB on	—	41	—	mA
MCU active	260 MHz, USB on, AUPLL on	—	51	—	mA

13 Package information

Table 88. Feature summary for each package

Feature	TFBGA145	HVQFN116	WLCSP151
Timers			
Counter timers (CTMAT)	CTMAT0 CTMAT1 CTMAT5 CTMAT10_8 CTMAT14_11	—	CTMAT0 CTMAT1 CTMAT5 CTMAT10_8 CTMAT14_11
SCTimers	SCT7_6	—	SCT7_6
SCTimer/PWM output	SCT0_OUT1_0 SCT0_OUT5_4 SCT0_OUT8 SCT0_OUT7_6 SCT0_OUT9	SCT0_OUT1_0 SCT0_OUT5_4 SCT0_OUT8	SCT0_OUT1_0 SCT0_OUT5_4 SCT0_OUT8 SCT0_OUT7_6 SCT0_OUT9
Analog peripherals			
DAC	Channel A Channel B	Channel A Channel B	Channel A Channel B
ADC	ADC0 channel7_0 ADC1_channel3_0 ADC1_channel7_6	ADC0 channel7_0 ADC1_channel7_6	ADC0 channel7_0 ADC1_channel7_6
ACOMP	ACOMP channel7_0 ACOMP0_GPIO_OUT ACOMP1_GPIO_OUT ACOMP0_EDGE_PULSE ACOMP1_EDGE_PULSE	ACOMP channel7_0	ACOMP channel7_0 ACOMP0_GPIO_OUT ACOMP1_GPIO_OUT ACOMP0_EDGE_PULSE ACOMP1_EDGE_PULSE
FlexSPI			
FlexSPI	FlexSPI_Flash FlexSPI_pSRAM	FlexSPI_Flash	FlexSPI_Flash FlexSPI_pSRAM
GPIO			
GPIO	GPIO[63:0]	GPIO[50:42] [34:22] [20:2]	GPIO[55:0]
Secure GPIO	SPIO0[31:0]	SPIO0[18:10] [2:0]	SPIO0[23:0]
Flexcomm			
Flexcomm	Flexcomm3_0 Flexcomm14	Flexcomm3_0	Flexcomm3_0
USART	Up to 5	Up to 3	Up to 4
I2C	Up to 5	Up to 4	Up to 4
I2S	Up to 5	Up to 4	Up to 4
SPI	Up to 5	Up to 3	Up to 4

Table 88. Feature summary for each package ***...continued***

Feature	TFBGA145	HVQFN116	WLCSP151
Other features			
LCD	LCD_SPI LCD_8080	LCD_SPI	LCD_SPI
Ethernet	ENET_RMII	—	—
Digital microphone (DMIC)	PDM	—	PDM

13.1 Package thermal conditions

13.1.1 TFBGA145 thermal conditions

Table 89. Package thermal conditions—TFBGA145 package

Symbol	Rating	Board type[1]	Value	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance[2]	JESD51-7, 2s2p	35.8	°C/W
$R_{\psi JT}$	Junction to top of package thermal characterization parameter[2]	JESD51-7, 2s2p	7.2	°C/W
$R_{\theta JC}$	Junction to case thermal resistance[2]	JESD51-7, 2s2p	14.2	°C/W

[1] The thermal test board meets JEDEC specification for this package (JESD51-7).
[2] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

13.1.2 HVQFN116 thermal conditions

Table 90. Package thermal conditions—HVQFN116 package

Symbol	Rating	Board type[1]	Value	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance[2]	JESD51-7, 2s2p	36.1	°C/W
$R_{\psi JT}$	Junction to top of package thermal characterization parameter[2]	JESD51-7, 2s2p	7.3	°C/W
$R_{\theta JC}$	Junction to case thermal resistance[2]	JESD51-7, 2s2p	12.0	°C/W

[1] The thermal test board meets JEDEC specification for this package (JESD51-7).
[2] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

13.1.3 WLCSP151 thermal conditions

Table 91. Package thermal conditions—WLCSP151 package

Symbol	Rating	Board type[1]	Value	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance[2]	JESD51-7, 2s2p	48.9	°C/W
$R_{\psi JT}$	Junction to top of package thermal characterization parameter[2]	JESD51-7, 2s2p	4.2	°C/W
$R_{\theta JC}$	Junction to case thermal resistance[2]	JESD51-7, 2s2p	12.6	°C/W

[1] The thermal test board meets JEDEC specification for this package (JESD51-7).
[2] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

13.2 WLCSP underfill

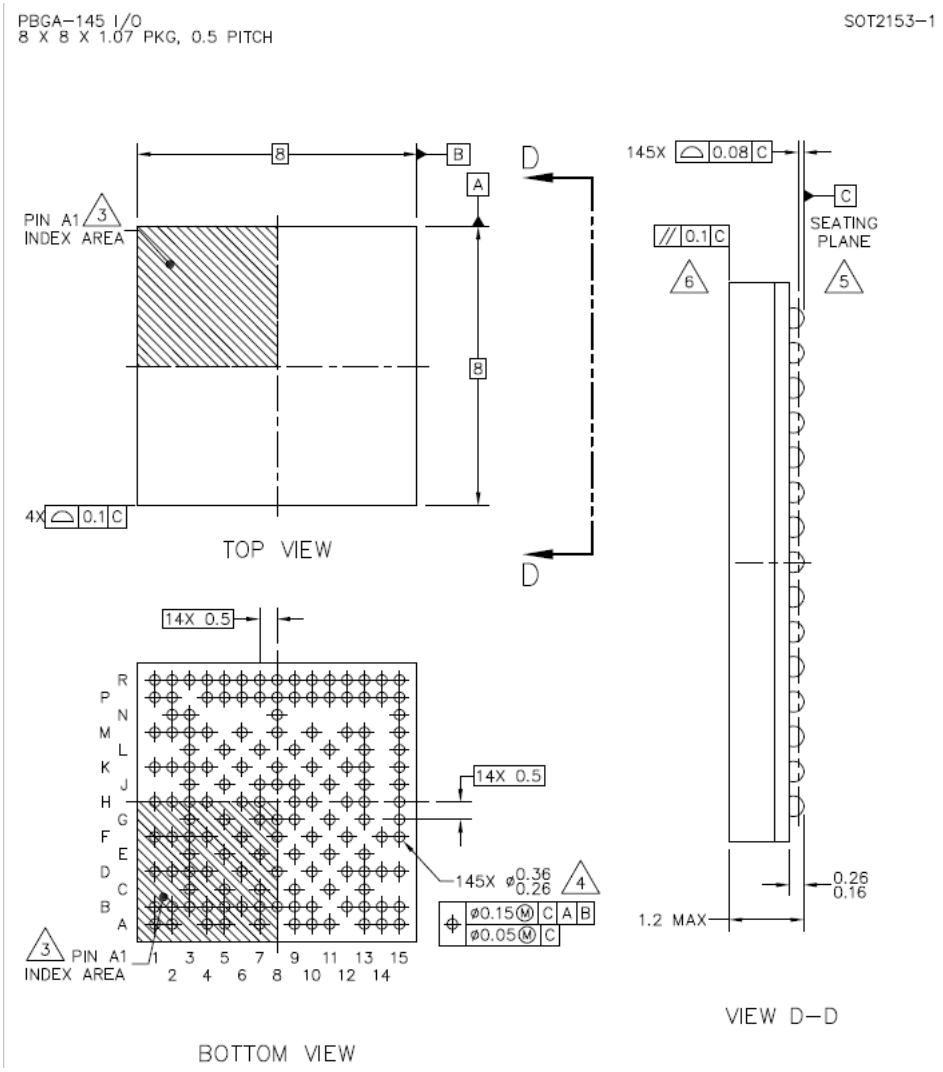
To meet NXP board level reliability (BLR) requirements of 500 temperature cycles between -40°C to +125°C (Ta) and prevent WLCSP reliability issues, it is mandatory to select a molded underfill (for molded module application) or capillary underfill material (for unmolded module applications). The molded underfill or capillary underfill material must have less than 20 ppm halide like chloride as per the material supplier specifications.

13.3 Package mechanical drawings

Table 92. Package information

Package name	Link to package information on NXP website
TFBGA145	SOT2153-1
HVQFN116	SOT2086-2
WLCSP151	SOT2152-1

13.3.1 TFBGA145 package mechanical drawing



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 78. TFBGA145 package mechanical drawing

13.3.2 HVQFN116 package mechanical drawing

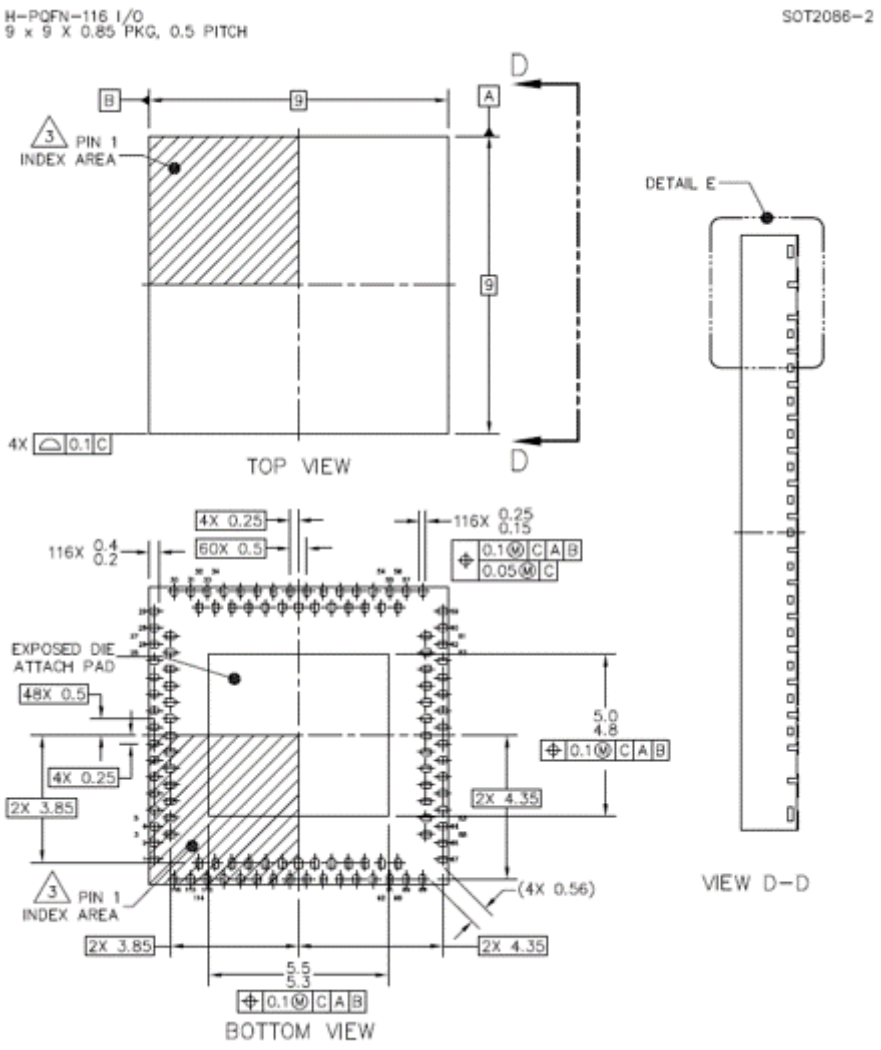
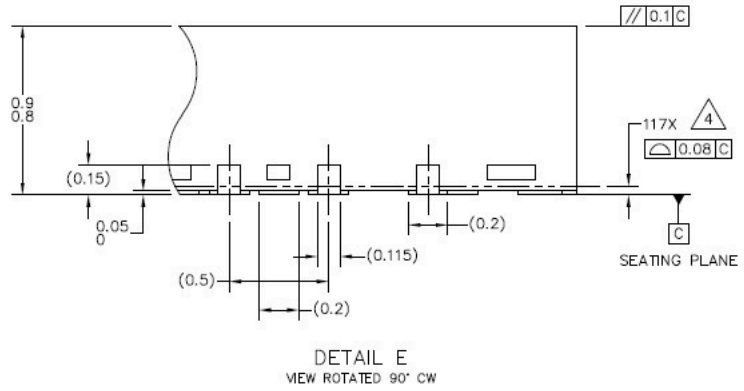


Figure 79. HVQFN116 package drawing



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.
5. MIN. METAL GAP FOR LEAD TO EXPOSED PAD SHALL BE 0.2 MM.

Figure 80. HVQFN116 package drawing - Details E

13.3.3 WLCSP151 package mechanical drawing

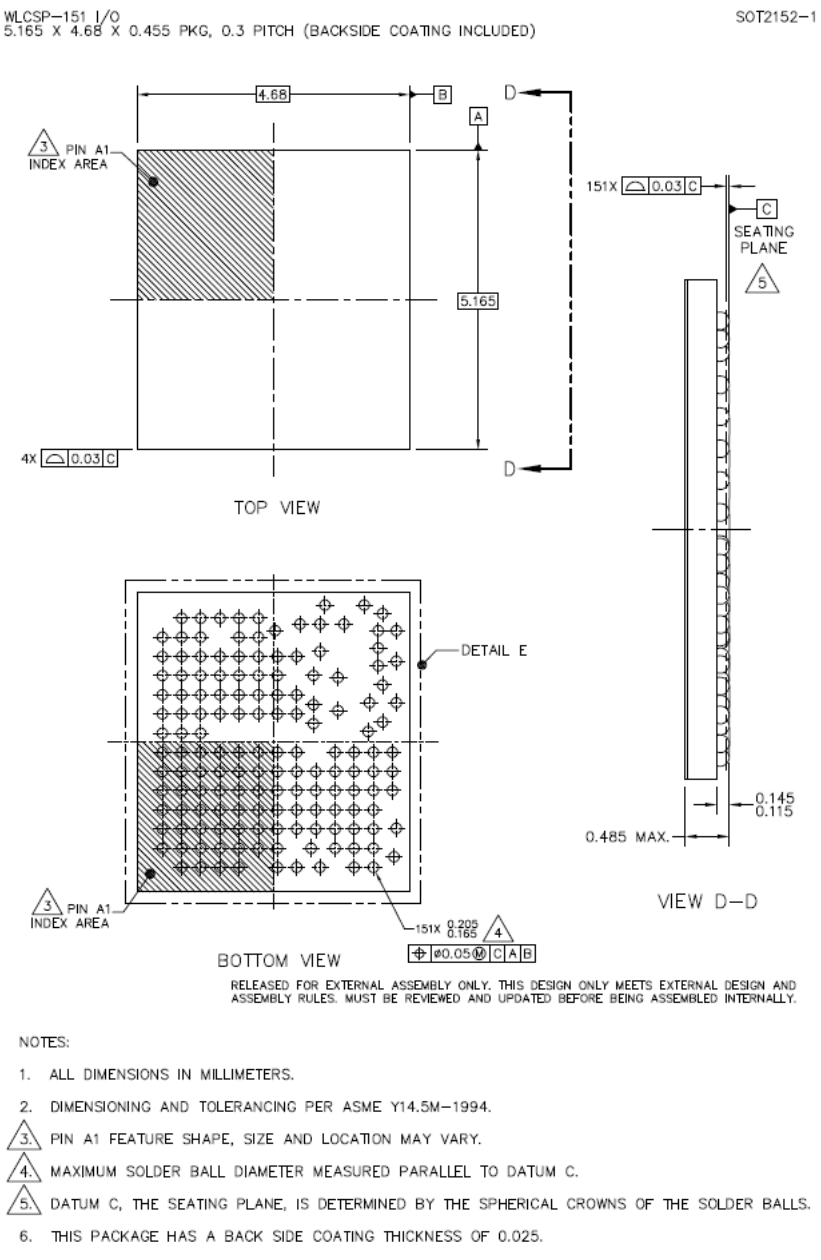
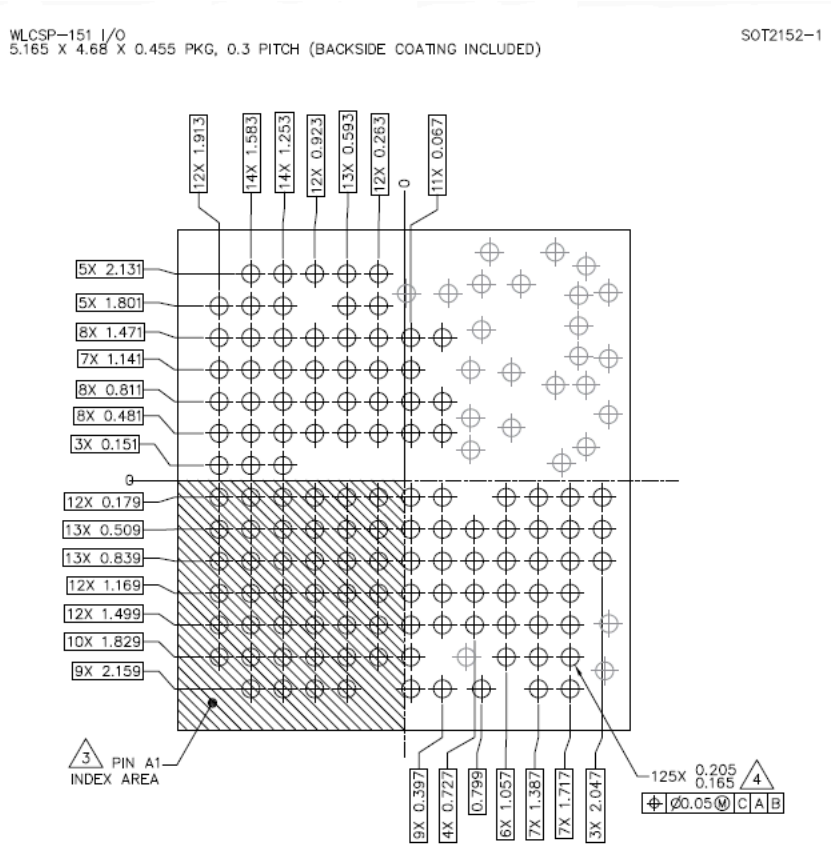


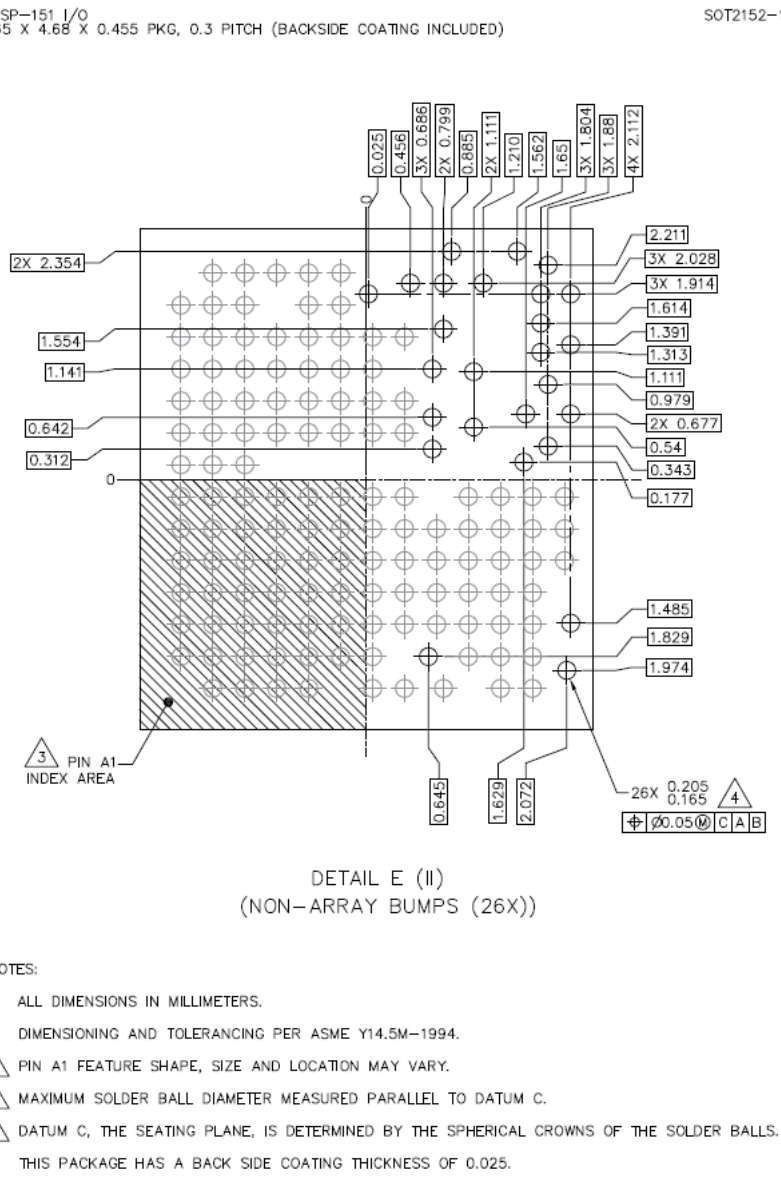
Figure 81. WLCSP151 package drawing



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

Figure 82. WLCSP151 package drawing - Details E (I)



NOTES:

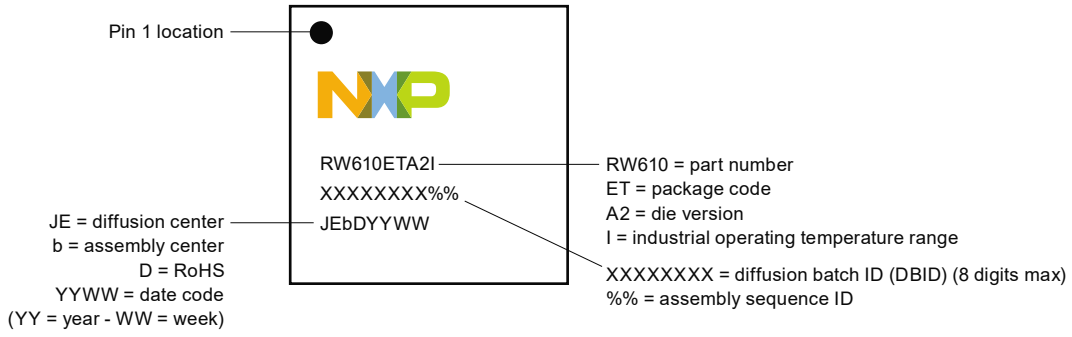
1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

Figure 83. WLCSP151 package drawing - Details E (II)

13.4 Package markings

13.4.1 TFBGA145 package marking

Figure 84 illustrates the location of pin 1 and marking on TFBGA145 package.

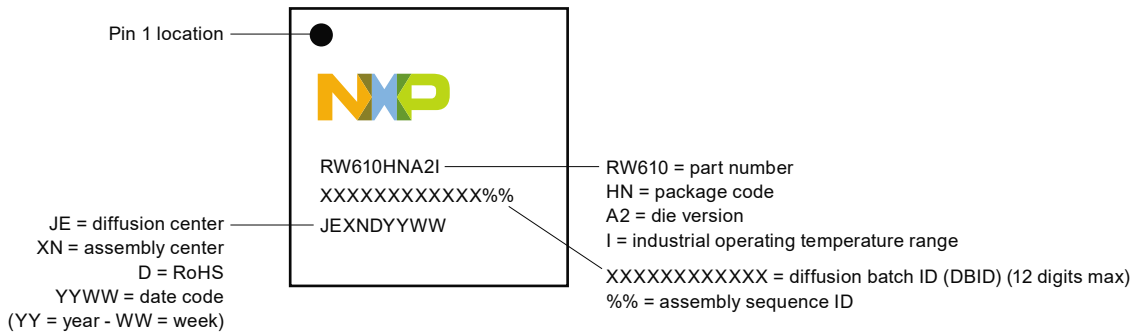


Note: The above drawing is not drawn to scale. The location of markings is approximate. *aaa-052238*

Figure 84. Marking and pin 1 location on TFBGA145 package—industrial operating temperature

13.4.2 HVQFN116 package marking

Figure 85 illustrates the location of pin 1 and marking on HVQFN116 package.

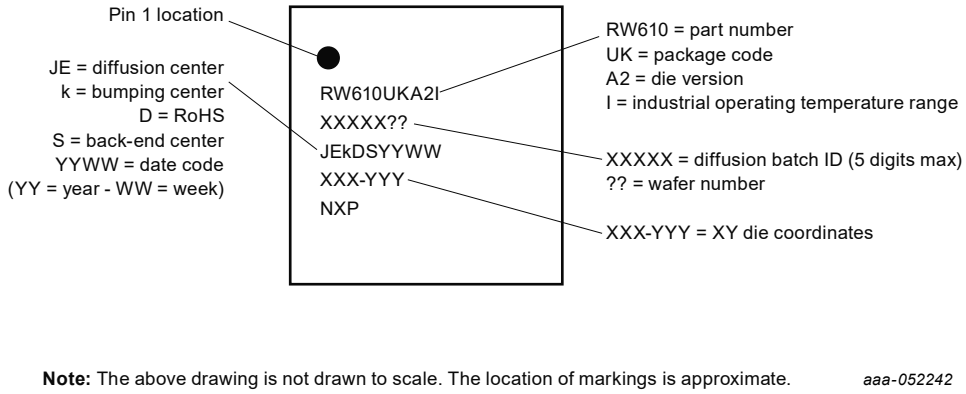


Note: The above drawing is not drawn to scale. The location of markings is approximate. *aaa-052240*

Figure 85. Marking and pin 1 location on HVQFN116 package—industrial operating temperature

13.4.3 WLCSP151 package marking

Figure 86 illustrates the location of pin 1 and marking on WLCSP151 package.



Note: The above drawing is not drawn to scale. The location of markings is approximate. *aaa-052242*

Figure 86. Marking and pin 1 location on WLCSP151 package—industrial operating temperature

14 Acronyms and abbreviations

Table 93. Acronyms and abbreviations

Acronym	Definition
ADC	Analog-to-digital converter
AES	Advanced encryption standard
AFH	Adaptive frequency hopping
AHB	Advanced high-performance bus
APB	Advanced peripheral bus
API	Application program interface
BAR	Base address register
BRF	Bluetooth RF unit
BSS	Basic service set
BTM	BSS transition management
CBC	Cipher block chaining
CCA	Clear channel assessment
CCK	Complementary code keying
CCMP	Counter mode CBC-MAC protocol
CIU	CPU interface unit
CMD	Command
CRC	Cyclic redundancy check
CS	Card select
CTS	Clear to send
DAC	Digital-to-analog converter
DMA	Direct memory access
DPD	Digital pre distortion
DSP	Digital signal processor
DTIM	Delivery traffic indication message
ECDSA	Elliptic curve digital signature algorithm
ELS	Embedded Edgelock® secure subsystem
ER	Extended range
FIFO	First in first out
FPU	Floating point unit
GCMP	Galois/counter mode protocol
GI	Guard interval
GPIO	General purpose input/output
GPT	General purpose timer
HT	High throughput

Table 93. Acronyms and abbreviations...*continued*

Acronym	Definition
HVQFN	Thermal enhanced very thin quad flat package
I/Q	In-phase/quadrature
IEEE	Institute of electrical and electronics engineers
IRQ	Interrupt request
JEDEC	Joint electronic device engineering council
JTAG	Joint test action group
LE	Low energy
LNA	Low noise amplifier
LSb	Least significant bit
LSB	Least significant byte
MAC	Media/medium access controller
MCS	Modulation and coding scheme
MCU	Microcontroller unit
MFP	Multi functional pin
MIB	Management information base
MII	Media independent interface
MIMO	Multiple input multiple output
MPDU	MAC protocol data unit
MPU	Memory protection unit
MSb	Most significant bit
MSB	Most significant byte
MU-MIMO	Multi user MIMO
MU-PPDU	Multi user PPDU
MWS	Mobile wireless system Multimedia wireless system
NAV	Network allocation vector
NVIC	Nested vector interrupt controller
OFDM	Orthogonal frequency division multiplexing
OFDMA	Orthogonal frequency division multiple access
OTP	One time programmable
PA	Power amplifier
PAD	Packet assembler/disassembler
PCB	Printed circuit board
PCI	Peripheral component interconnect
PCM	Pulse code modulation
PDn	Power down

Table 93. Acronyms and abbreviations...*continued*

Acronym	Definition
PHY	Physical layer
PLL	Phase-locked loop
PMU	Power management unit
POS	Point of sale
PPDU	PHY protocol data unit
PPM	Pulse position modulation
PSK	Pre shared keys
PTA	Packet traffic arbitration
PUF	Physically unclonable function
QFN	Quad flat non-leaded package
RF	Radio frequency
RIFS	Reduced inter frame space
ROM	Read only memory
RSSI	Receiver signal strength indication
RTC	Real time clock
RTS	Request to send
SCLK	Serial interface clock
SDA	Serial interface data
SDK	Software development kit
SFD	Start of frame delimiter
SHA	Secure hash algorithm
SoC	System-on-chip
SPI	Serial peripheral interface
STA	Station
SWD	Serial wire debug
SysTick	System tick timer
TEE	Trusted execution environment
TWT	Target wake time
UART	Universal asynchronous receiver/transmitter
UDP	User datagram protocol
USART	Universal synchronous/asynchronous receiver/transmitter
VCO	Voltage controlled oscillator
VHT	Very high throughput
WCI-2	Wireless coexistence interface 2
WEP	Wired equivalent privacy
WFI	Wait for interrupt

Table 93. Acronyms and abbreviations...*continued*

Acronym	Definition
Wi-Fi	Hardware implementation of IEEE 802.11 for wireless connectivity
WLAN	Wireless local area network
WLCSP	Wafer level chip scale package
WPA	Wi-Fi protected access
WPA2	Wi-Fi protected access 2
WPA2-PSK	Wi-Fi protected access 2 - pre shared key
WPA3	Wi-Fi protected access 3
XIP	Execute in place

15 Revision history

Table 94. Revision history

Document ID	Release date	Description
RW610 v.8	02 July 2024	Product data sheet • Updated the access to public **Product overview** • Section 1.2.3 "Platform security": added the last two features. • Section 1.4 "Bluetooth LE 5.4 radio key features": updated Bluetooth support. **Microcontroller (MCU)** • Section 3.12.1.4 "Internal sleep clock CAU_SOC_SLP_REF_GEN_CLK": added. • Section 3.13.1 "Power structure": corrected the range of values for VBAT in the figure. • Section 3.15 "Pin interrupt/pattern engine": updated two features: – Pin interrupts can wake up the device from idle mode and standby mode. – Pattern match engine facilities wake up only from idle and standby modes. • Section 3.19.1 "Analog digital converter (ADC)": removed 0.5x ADC gain support. **Wi-Fi subsystem** • Section 4.3 "Wi-Fi baseband": corrected the definition of TWT feature. **Pin information** • Section 7.1 "Signal diagrams": – Corrected the signal names: SDIO_DAT[3:0], SDIO_CMD, FlexSPI_SRAM_DQS, and FlexSPI_flash_DQS – Corrected ENET_MDIO to bidirectional signal. • Section 7.5 "Pin lists": – Renamed EXT_FREQ (I) as EXT_FREQ, and renamed WCI-2_SOUT (O) as WCI-2_SOUT. – Renamed BUCK11_VX as BUCK11_VOUT, BUCK18_VX as BUCK18_VOUT, BUCK11_VS as BUCK11_VSENSE, and BUCK18_VS as BUCK18_VSENSE. – Renamed AVDD18_CAU as AVDD18, and VDD18_GAU as VDD18. • Section 7.6.1 "General purpose I/O (GPIO)": [GPIO34]: updated the type of FlexSPI_flash_CLK0. • Section 7.6.6 "FlexSPI flash interface": [GPIO34]: updated the type and description of FlexSPI_flash_CLK0. • Section 7.6.7 "FlexSPI SRAM interface":[GPIO35]: updated the type and description of FlexSPI_SRAM_CLK0. • Section 7.6.10 "I2S bus interface": updated the supply for GPIO[2] • Section 7.6.21 "Analog peripheral interface": updated the supply for GPIO[51], GPIO[52], GPIO[53], GPIO[54] • Section 7.7 "Configuration pins": – Replaced the resistor value in the paragraph above the first table. – Renamed EXT_FREQ(I) as EXT_FREQ —- continues ---->

Table 94. Revision history...*continued*

Document ID	Release date	Description
RW610 v.8	02 July 2024	—- continued ------ **Absolute maximum ratings** • Section 9 "Absolute maximum ratings": added USB_VBUS. **Recommended operating conditions** • Section 10 "Recommended operating conditions": added USB_VBUS. **Radio specifications** • Section 11.1.1 "Wi-Fi radio performance measurement": renamed RF_TR_2A as RF_TR_2 in the figure. • Section 11.1.2 "2.4 GHz Wi-Fi receiver performance": removed row with Output power control resolution • Section 11.1.3 "5 GHz Wi-Fi receiver performance": – Updated the min. value of RF frequency range. – Removed the rows with receiver maximum input level DSSS values for 802.11b. • Section 11.1.5 "5 GHz Wi-Fi transmitter performance": – Updated the min. value of RF frequency range. – Removed the extra dash to the typ. value of out-of-band noise floor. • Section 11.2.2 "Bluetooth LE transmitter performance": updated the conditions, values, and unit of TX output transmit power accuracy. • Section 12.3.2 "FlexSPI flash interface specifications": updated t_{CSH} min. values in DDR and SDR modes. **Microcontroller specifications** • Section 12.3.6 "USART interface specifications": aligned T_{CLK} and $T_{v(D)}$ parameter names in the figure and table. • Section 12.4 "Audio interface specifications": renamed FCm_RXD_SDA_MOSI_DATA as FCn_RXD_SDA_MOSI_DATA. **Package information** • Section 13.4.1 "TFBGA145 package marking": renamed RoHF as RoHS (typo). • Section 13.4.3 "WLCSP151 package marking": renamed RoHF as RoHS (typo). **Acronyms and abbreviations** • Section 14 "Acronyms and abbreviations": updated.
RW610 v.7	6 February 2024	Product data sheet

16 References

1. Cortex-M33 DGUG - Arm Cortex-M33 Devices Generic User Guide

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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