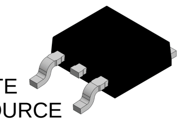
DATA SHEET
www.onsemi.com

MOSFET – Power, N-Channel

50 V, 14 A, 100 mΩ

RFD14N05SM9A

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
50 V	100 mΩ @ 10 V	14 A



DPAK3 (TO−252 3 LD)
JEDEC
CASE 369AS

Description

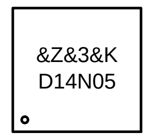
These are N−channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA09770.

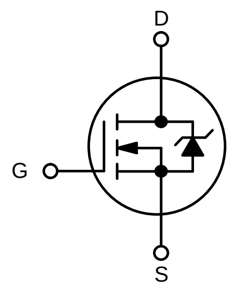
Features

- 14 A, 50 V
- $R_{DS(ON)}$ = 0.100 Ω
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"
- This is a Pb−Free Device

MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= 3−Digit Date Code
&K	= 2−Digits Lot Run Code
D14N05	= Specific Device Code



N−Channel MOSFET

ORDERING INFORMATION

Device	Package	Shipping†
RFD14N05SM9A	DPAK3 (TO−252 3 LD) (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise noted)

Parameter	Symbol	Ratings	Unit
Drain to Source Voltage (Note 1)	V_{DSS}	50	V
Drain to Gate Voltage (R_{GS} = 20 kΩ) (Note 1)	V_{DGR}	50	V
Gate to Source Voltage	V_{GS}	±20	V
Continuous Drain Current	I_D	14	A
Pulsed Drain Current (Note 3)	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation	P_D	48	W
Derate above 25°C		0.32	W/°C
Operating and Storage Temperature	T_J, T_{STG}	−55 to 175	°C
Maximum Temperature for Soldering			
Leads at 0.063 in (1.6 mm) from Case for 10 s	T_L	300	°C
Package Body for 10 s, See Techbrief 334	T_{pkg}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. T_J = 25°C to 150°C.

August, 2023 − Rev. 3
Publication Order Number:
RFD14N05SM9A/D

ELECTRICAL SPECIFICATIONS (T_C = 25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250 μA, V_{GS} = 0 V (Figure 9)		50	–	–	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250 μA		2	–	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0 V		–	–	25	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0 V, T_C = 150°C		–	–	250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V		–	–	±100	nA
Drain to Source On Resistance (Note 2)	$R_{DS(ON)}$	I_D = 14 A, V_{GS} = 10 V, (Figure 11)		–	–	0.100	Ω
Turn−On Time	t_{ON}	V_{DD} = 25 V, I_D ≈ 14 A, V_{GS} = 10 V, R_{GS} = 25 Ω, R_L = 1.7 Ω (Figure 13)		–	–	60	ns
Turn−On Delay Time	$t_{d(ON)}$			–	14	–	ns
Rise Time	t_r			–	26	–	ns
Turn−Off Delay Time	$t_{d(OFF)}$			–	45	–	ns
Fall Time	t_f			–	17	–	ns
Turn−Off Time	t_{OFF}			–	–	100	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0 V to 20 V	V_{DD} = 40 V, I_D = 14 A, R_L = 2.86 Ω $I_{g(REF)}$ = 0.4 mA (Figure 13)	–	–	40	nC
Gate Charge at 5 V	$Q_{g(10)}$	V_{GS} = 0 V to 10 V		–	–	25	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0 V to 2 V		–	–	1.5	nC
Input Capacitance	C_{ISS}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1MHz (Figure 12)		–	570	–	pF
Output Capacitance	C_{OSS}			–	185	–	pF
Reverse Transfer Capacitance	C_{RSS}			–	50	–	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			–	–	3.125	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			–	–	100	°C/W

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

SOURCE TO DRAIN DIODE SPECIFICATIONS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = 14 A	–	–	1.5	V
Diode Reverse Recovery Time	t_{rr}	I_{SD} = 14 A, dI_{SD}/dt = 100 A/μs	–	–	125	ns

2. Pulse Test: Pulse Width ≤300 ms, Duty Cycle ≤2%.
3. Repetitive Rating: Pulse Width limited by max junction temperature. See Transient Thermal Impedance Curve (Figure 3) and Peak Current Capability Curve (Figure 5).

TYPICAL PERFORMANCE CURVES

(UNLESS OTHERWISE NOTED)

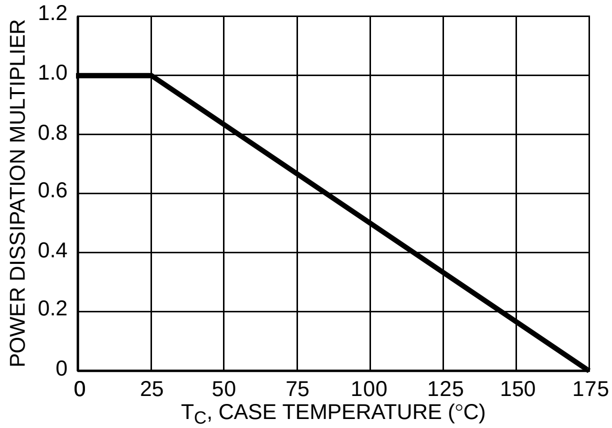


Figure 1. Normalized Power Dissipation vs. Case Temperature

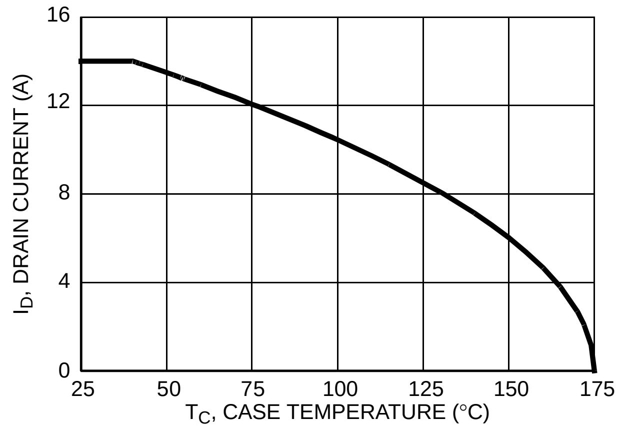


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

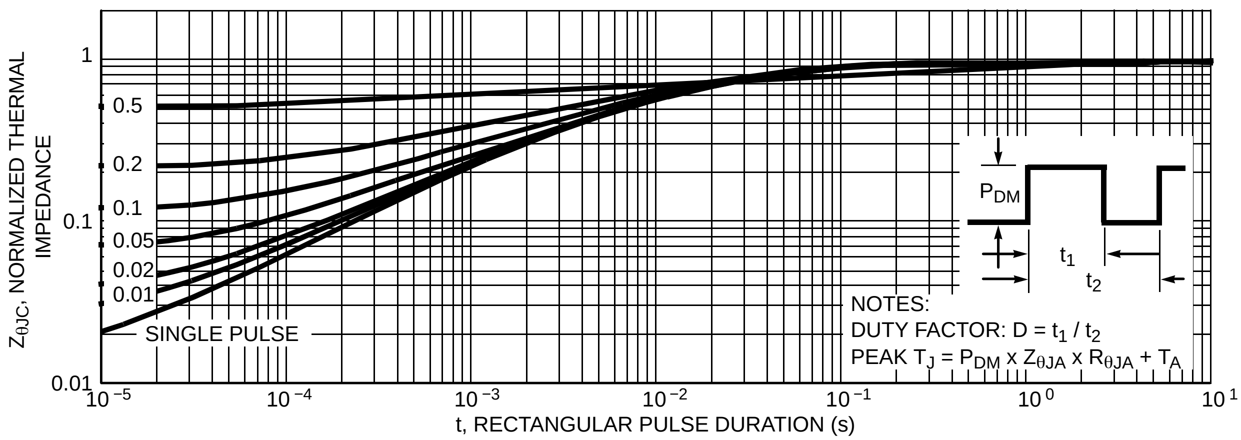


Figure 3. Normalized Maximum Transient Thermal Impedance

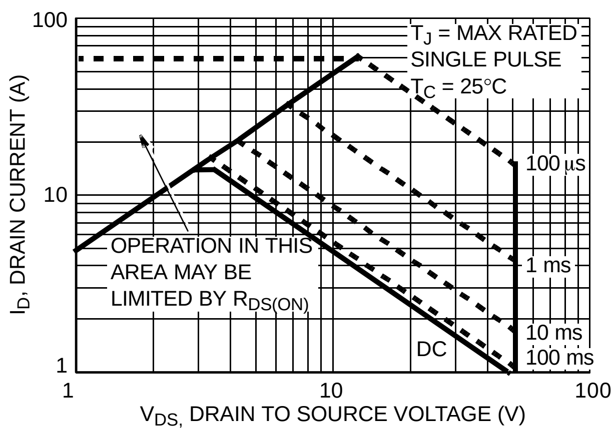


Figure 4. Forward Bias Safe Operating Area

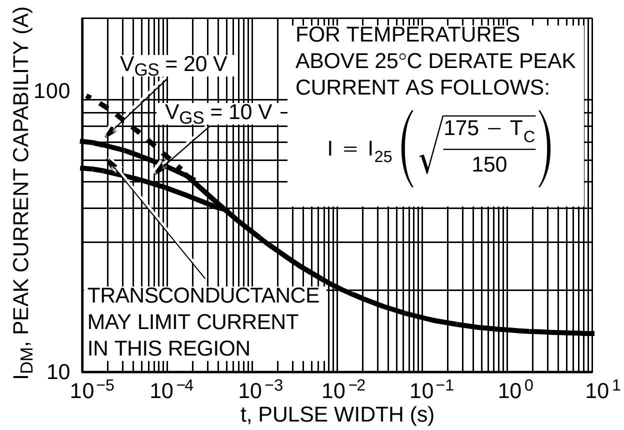
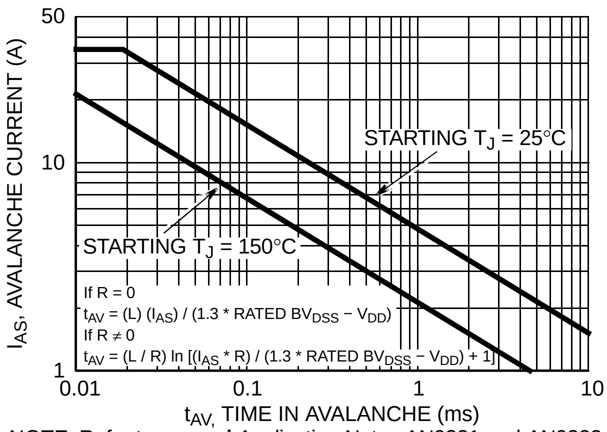


Figure 5. Peak Current Capability

TYPICAL PERFORMANCE CURVES

(UNLESS OTHERWISE NOTED) (CONTINUED)



NOTE: Refer to **onsemi** Application Notes AN9321 and AN9322.

Figure 6. Unclamped Inductive Switching

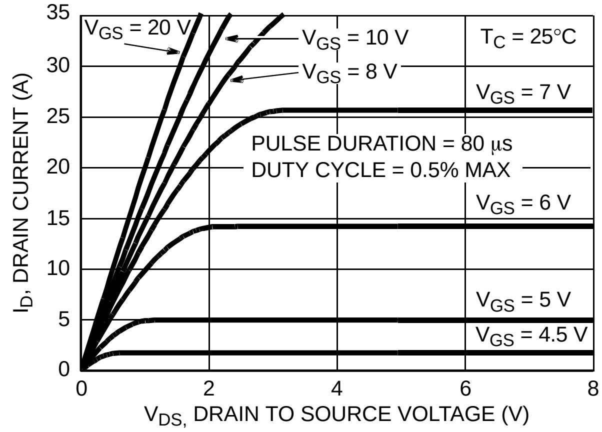


Figure 7. Saturation Characteristics

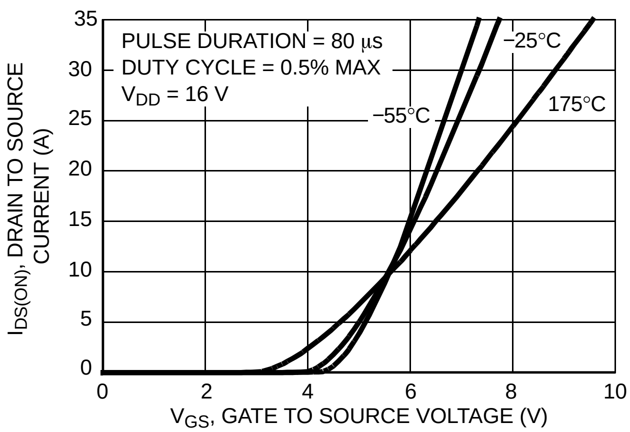


Figure 8. Transfer Characteristics

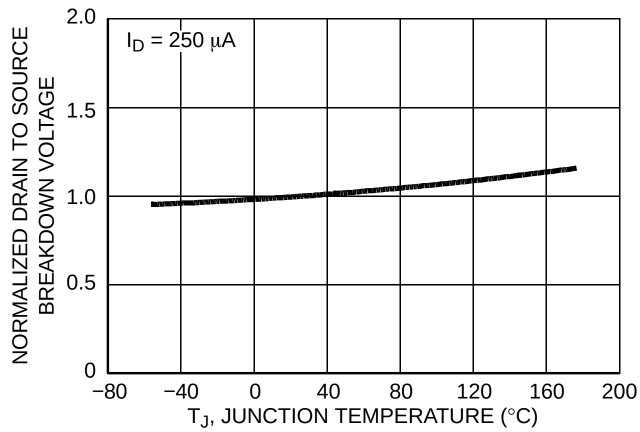


Figure 9. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

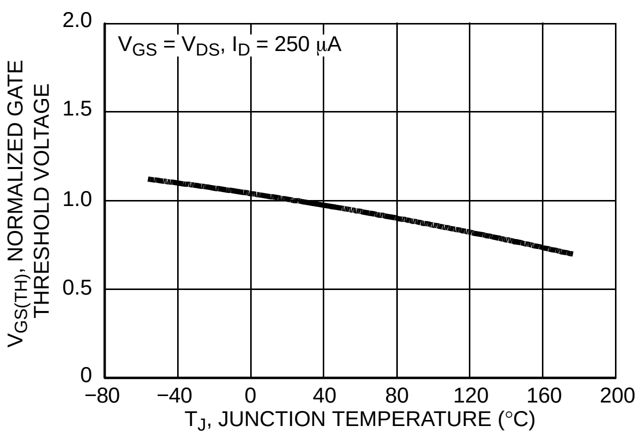


Figure 10. Normalized Gate Threshold Voltage vs. Junction Temperature

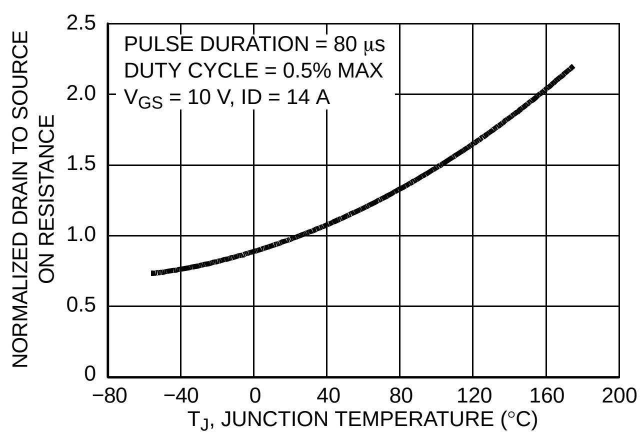


Figure 11. Normalized Gate to Source On Resistance vs. Junction Temperature

TYPICAL PERFORMANCE CURVES

(UNLESS OTHERWISE NOTED) (CONTINUED)

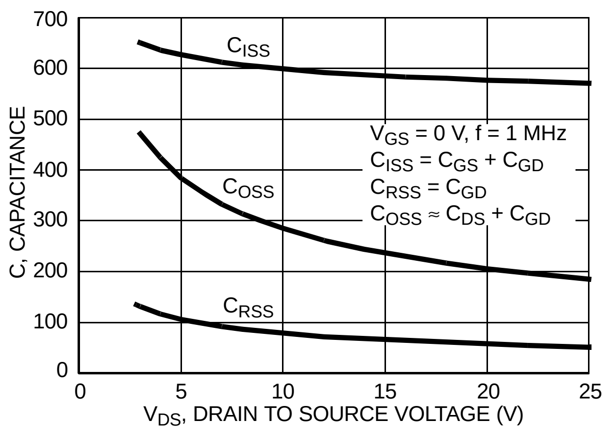
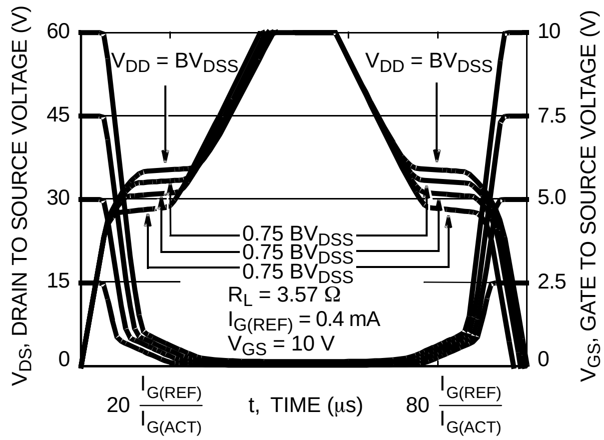


Figure 12. Capacitance vs. Drain to Source Voltage



NOTE: Refer to **onsemi** Application Notes AN7254 and AN7260.

Figure 13. Normalized Switching Waveforms for Constant Current Gate Drive

TEST CIRCUITS AND WAVEFORMS

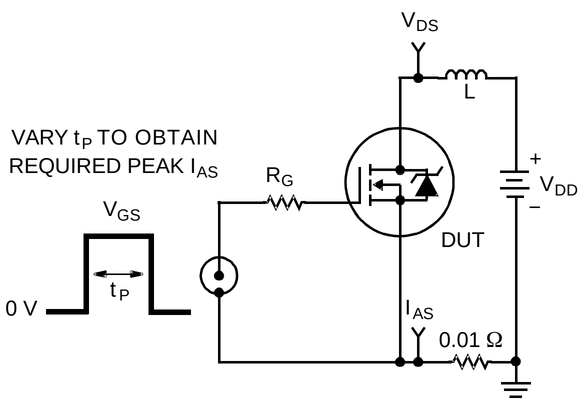


Figure 14. Unclamped Energy Test Circuit

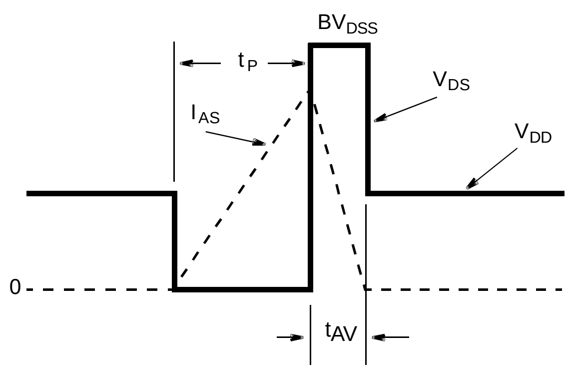


Figure 15. Unclamped Energy Waveforms

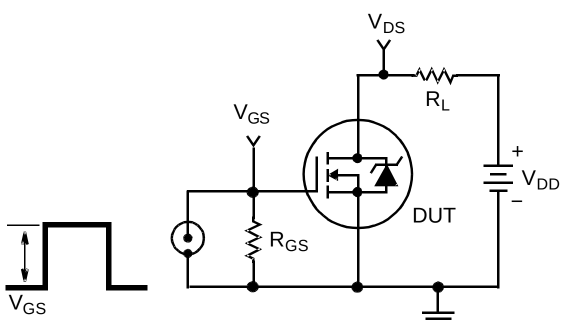


Figure 16. Switching Time Test Circuit

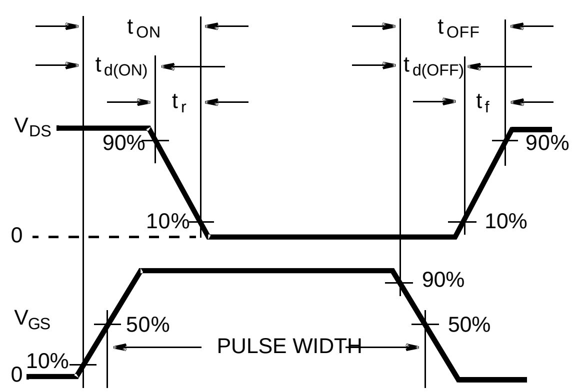


Figure 17. Resistive Switching Waveforms

TEST CIRCUITS AND WAVEFORMS

(CONTINUED)

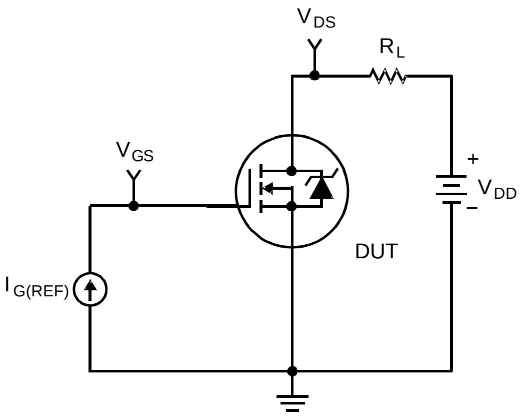


Figure 18. Gate Charge Test Circuit

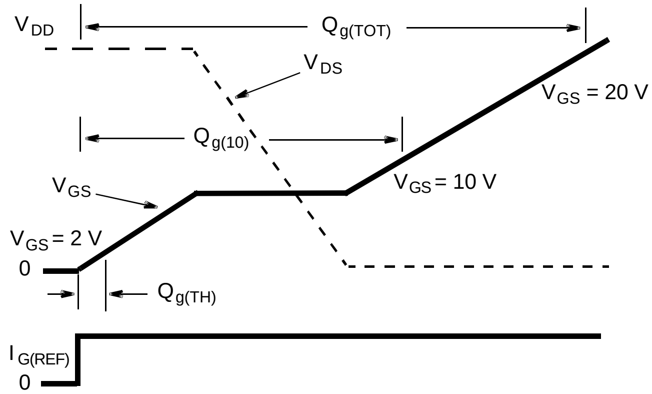


Figure 19. Gate Charge Waveforms

PSPICE ELECTRICAL MODEL

```
.SUBCKT RFD14N05 2 1 3 ;        rev 9/12/94

CA 12 8 8.84e−10
CB 15 14 9.34e−10
CIN 6 8 5.2e−10

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 62.87
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e−9
LGATE 1 9 4.34e−9
LSOURCE 3 7 3.79e−9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 2.2e−3
RGATE 9 20 5.64
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e−6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 42.3e−3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6  0.82

ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/50,6))}

.MODEL DBDMOD D (IS = 1.5e−13 RS = 10.9e−3 TRS1 = 2.3e−3 TRS2 = −1.75e−5 CJO = 6.84e−10 TT = 4.2e−8)
.MODEL DBKMOD D (RS = 4.15e−1 TRS1 = 3.73e−3 TRS2 = −3.21e−5)
.MODEL DPLCAPMOD D (CJO = 26.2e−11 IS = 1e−30 N = 10)
.MODEL MOSMOD NMOS (VTO = 3.91 KP = 12.68 IS = 1e−30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 7.73e−4 TC2 = 2.12e−6)
.MODEL RDSMOD RES (TC1 = 5.0e−3 TC2 = 2.53e−5)
.MODEL RSCLMOD RES (TC1 = 2.05e−3 TC2 = 1.35e−5)
.MODEL RVTOMOD RES (TC1 = −4.44e−3 TC2 = −6.45e−6)
.MODEL S1AMOD VSWITCH (RON = 1e−5 ROFF = 0.1 VON = −5.29 VOFF= −3.29)
.MODEL S1BMOD VSWITCH (RON = 1e−5 ROFF = 0.1 VON = −3.29 VOFF= −5.29)
.MODEL S2AMOD VSWITCH (RON = 1e−5 ROFF = 0.1 VON = −2.25 VOFF= 2.75)
```

.MODEL S2BMOD VSWITCH (RON = 1e−5 ROFF = 0.1 VON = 2.75 VOFF= −2.25)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub−circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

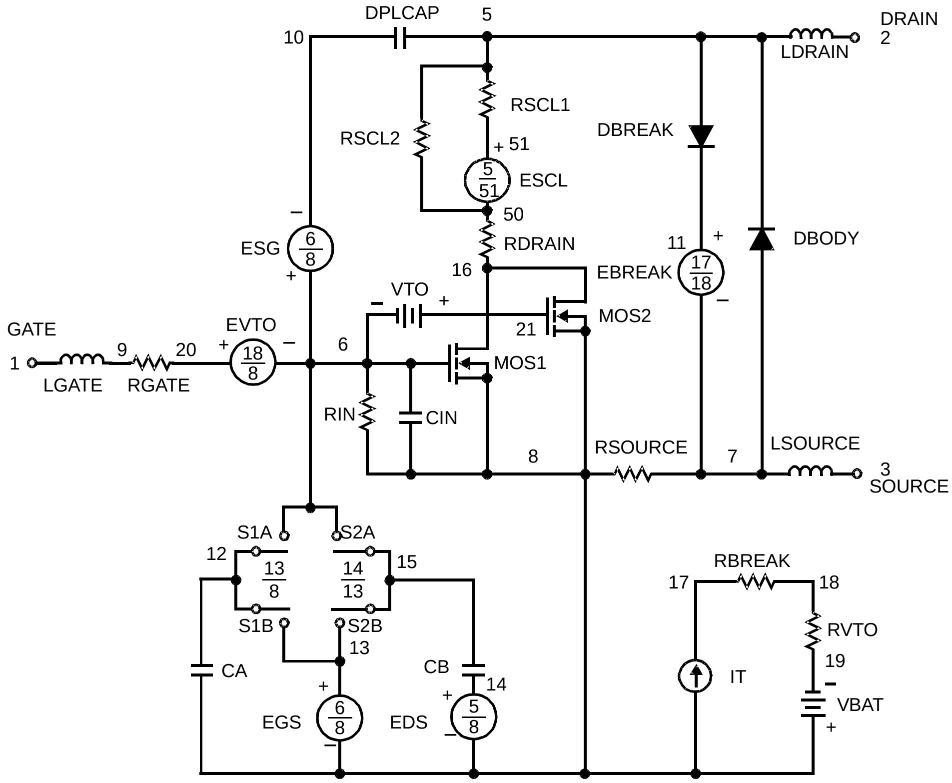
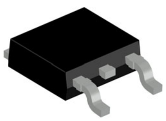


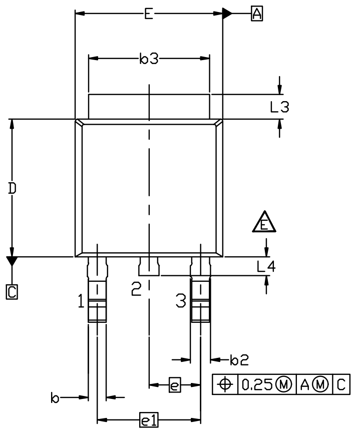
Figure 20. PSPICE Electrical Model

PSPICE is a trademark of MicroSim Corporation.



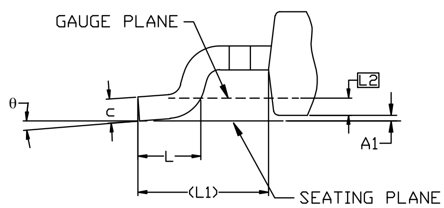
DPAK3 6.10x6.54x2.29, 4.57P
CASE 369AS
ISSUE B

DATE 20 DEC 2023



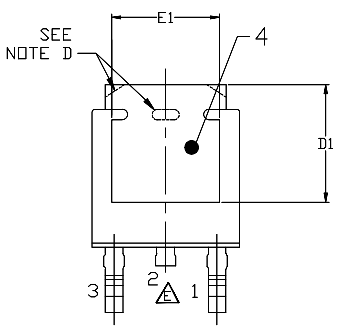
NON-DIODE PRODUCTS VERSION

NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE F, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2018.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX PLASTIC BODY STUB WITHOUT CENTER LEAD.
F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.

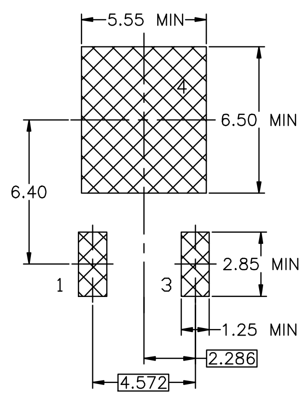


DETAIL A
(ROTATED -90°)
SCALE: 12X

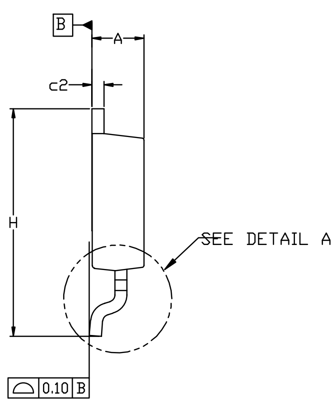
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	-	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	---	---
E	6.35	6.54	6.73
E1	4.32	---	---
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	---	---	1.02
θ	0°	---	10°



NON-DIODE PRODUCTS VERSION



LAND PATTERN RECOMMENDATION



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXXXX
XXXXXX
AYWWZZ

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON13810G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**DPAK3 6.10x6.54x2.29, 4.57P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

◊