

E4M0060075K1

Silicon Carbide Power MOSFET

E-Series Automotive

N-Channel Enhancement Mode

Features

- Optimized package with separate driver source pin
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant
- Automotive Qualified (AEC-Q101) and PPAP Capable

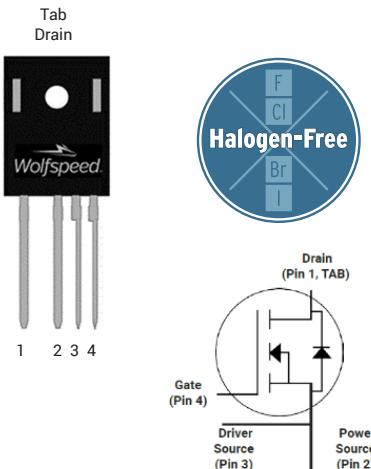
Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Applications

- Motor Control
- EV Battery Chargers
- High Voltage DC/DC Converters

Package



Maximum Ratings ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit	Note
$V_{DS\text{max}}$	Drain - Source Voltage	750	V	
$V_{GS\text{max}}$	Gate - Source Voltage	-8/+19	V	Note: 1
I_D	Continuous Drain Current, $V_{GS} = 15\text{ V}$	$T_c = 25^\circ\text{C}$	35	A Fig. 19 Note: 2
		$T_c = 100^\circ\text{C}$	26	
$I_{D(\text{pulse})}$	Pulsed Drain Current, Pulse width t_p limited by $T_{j\text{max}}$	101	A	Fig. 22
P_D	Power Dissipation, $T_c = 25^\circ\text{C}$, $T_j = 175^\circ\text{C}$	126	W	Fig. 20 Note: 2
T_j, T_{stg}	Operating Junction and Storage Temperature	-55 to +175	°C	
T_L	Solder Temperature, 1.6mm (0.063") from case for 10s	260	°C	
M_d	Mounting Torque, M3 or 6-32 screw	1 8.8	Nm lbf-in	

Note (1): Recommended turn off / turn on gate voltage V_{GS} - 4V...0V / +15V

Note (2): Verified by design

Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	750			V	$V_{\text{GS}} = 0 \text{ V}$, $I_D = 100 \mu\text{A}$	
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	1.8	2.6	3.8	V	$V_{\text{DS}} = V_{\text{GS}}$, $I_D = 3.67 \text{ mA}$	Fig. 11
			2.1		V	$V_{\text{DS}} = V_{\text{GS}}$, $I_D = 3.67 \text{ mA}$, $T_J = 175^\circ\text{C}$	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	μA	$V_{\text{DS}} = 750 \text{ V}$, $V_{\text{GS}} = 0 \text{ V}$	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	$V_{\text{GS}} = 15 \text{ V}$, $V_{\text{DS}} = 0 \text{ V}$	
$R_{\text{DS}(\text{on})}$	Drain-Source On-State Resistance		60	78	$\text{m}\Omega$	$V_{\text{GS}} = 15 \text{ V}$, $I_D = 13.4 \text{ A}$	Fig. 4, 5, 6
			87			$V_{\text{GS}} = 15 \text{ V}$, $I_D = 13.4 \text{ A}$, $T_J = 175^\circ\text{C}$	
g_{fs}	Transconductance		10		S	$V_{\text{DS}} = 20 \text{ V}$, $I_{\text{DS}} = 13.4 \text{ A}$	Fig. 7
			8			$V_{\text{DS}} = 20 \text{ V}$, $I_{\text{DS}} = 13.4 \text{ A}$, $T_J = 175^\circ\text{C}$	
C_{iss}	Input Capacitance		1203		pF	$V_{\text{GS}} = 0 \text{ V}$, $V_{\text{DS}} = 0 \text{ V}$ to 500 V $F = 100 \text{ kHz}$ $V_{\text{AC}} = 25 \text{ mV}$	Fig. 17, 18
C_{oss}	Output Capacitance		69				
C_{rss}	Reverse Transfer Capacitance		7				
E_{oss}	C_{oss} Stored Energy		10		μJ	$V_{\text{GS}} = 0 \text{ V}$, $V_{\text{DS}} = 0 \dots 500 \text{ V}$	Fig. 16
$C_{\text{o(er)}}$	Effective Output Capacitance (Energy Related)		90		pF		
$C_{\text{o(tr)}}$	Effective Output Capacitance (Time Related)		129		pF		
E_{ON}	Turn-On Switching Energy (External Diode)		52		μJ	$V_{\text{DS}} = 500 \text{ V}$, $V_{\text{GS}} = -4 \text{ V}/15 \text{ V}$, $I_D = 13.4 \text{ A}$, $R_{\text{G(ext)}} = 2.5 \Omega$, $L = 135 \mu\text{H}$, $T_J = 175^\circ\text{C}$ FWD = External SiC DIODE	Fig. 26, 28
E_{OFF}	Turn Off Switching Energy (External Diode)		16				
E_{ON}	Turn-On Switching Energy (Body Diode FWD)		56		μJ	$V_{\text{DS}} = 500 \text{ V}$, $V_{\text{GS}} = -4 \text{ V}/15 \text{ V}$, $I_D = 13.4 \text{ A}$, $R_{\text{G(ext)}} = 2.5 \Omega$, $L = 135 \mu\text{H}$, $T_J = 175^\circ\text{C}$ FWD = Internal Body Diode	Fig. 26, 28
E_{OFF}	Turn-Off Switching Energy (Body Diode FWD)		16				
$t_{\text{d(on)}}$	Turn-On Delay Time		8		ns	$V_{\text{DD}} = 500 \text{ V}$, $V_{\text{GS}} = -4 \text{ V}/15 \text{ V}$ $I_D = 13.4 \text{ A}$, $R_{\text{G(ext)}} = 2.5 \Omega$, $L = 135 \mu\text{H}$ Timing relative to V_{DS} Inductive load	Fig. 27, 28
t_r	Rise Time		9				
$t_{\text{d(off)}}$	Turn-Off Delay Time		16				
t_f	Fall Time		9				
$R_{\text{G(int)}}$	Internal Gate Resistance		3.0		Ω	$f = 1 \text{ MHz}$, $V_{\text{AC}} = 25 \text{ mV}$	
Q_{gs}	Gate to Source Charge		14		nC	$V_{\text{DS}} = 500 \text{ V}$, $V_{\text{GS}} = -4 \text{ V}/15 \text{ V}$ $I_D = 13.4 \text{ A}$ Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		18				
Q_g	Total Gate Charge		52				

Note (3): $C_{\text{o(er)}}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{DS} is rising from 0 to 500V

$C_{\text{o(tr)}}$, a lumped capacitance that gives same charging time as C_{oss} while V_{DS} is rising from 0 to 500V

Reverse Diode Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.8		V	$V_{GS} = -4\text{ V}$, $I_{SD} = 6.7\text{ A}$, $T_J = 25^\circ\text{C}$	Fig. 8, 9, 10
		4.2		V	$V_{GS} = -4\text{ V}$, $I_{SD} = 6.7\text{ A}$, $T_J = 175^\circ\text{C}$	
I_S	Continuous Diode Forward Current		22	A	$V_{GS} = -4\text{ V}$, $T_c = 25^\circ\text{C}$	
$I_{S,pulse}$	Diode pulse Current		101	A	$V_{GS} = -4\text{ V}$, pulse width t_p limited by T_{jmax}	
t_{rr}	Reverse Recovery time	14		ns	$V_{GS} = -4\text{ V}$, $I_{SD} = 13.4\text{ A}$, $V_R = 500\text{ V}$ dif/dt = 6160 A/μs, $T_J = 175^\circ\text{C}$	
Q_{rr}	Reverse Recovery Charge	327		nC		
I_{rrm}	Peak Reverse Recovery Current	40		A		
t_{rr}	Reverse Recovery time	23		ns	$V_{GS} = -4\text{ V}$, $I_{SD} = 13.4\text{ A}$, $V_R = 500\text{ V}$ dif/dt = 2150 A/μs, $T_J = 175^\circ\text{C}$	
Q_{rr}	Reverse Recovery Charge	220		nC		
I_{rrm}	Peak Reverse Recovery Current	18		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{θJC}$	Thermal Resistance from Junction to Case	0.91	1.19	°C/W		Fig. 21

Typical Performance

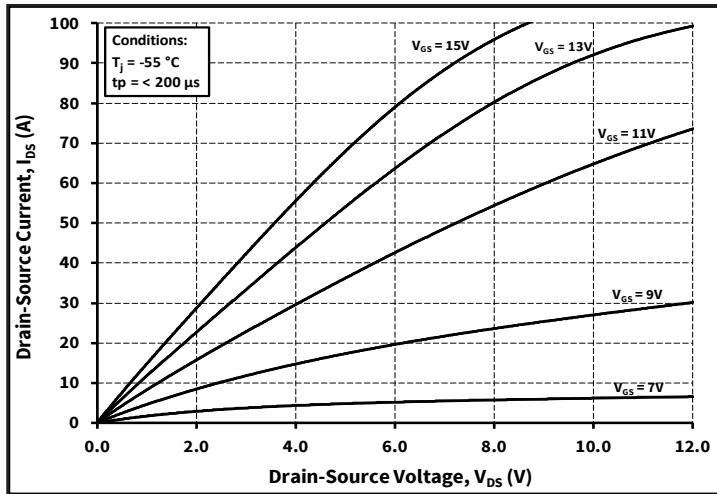


Figure 1. Output Characteristics $T_J = -55\text{ }^{\circ}\text{C}$

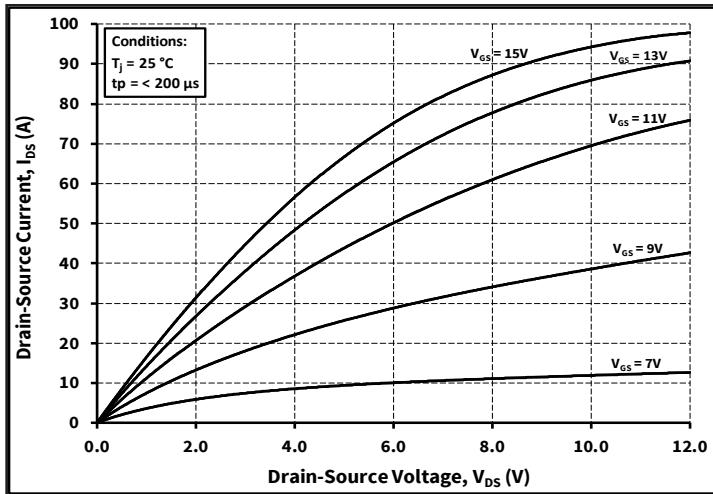


Figure 2. Output Characteristics $T_J = 25\text{ }^{\circ}\text{C}$

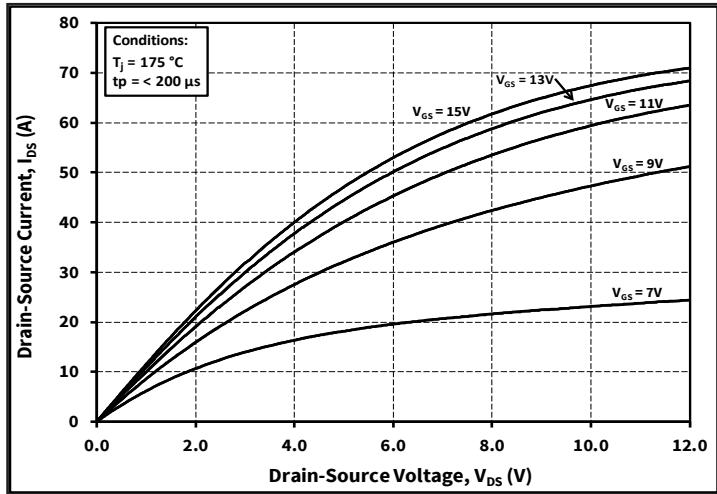
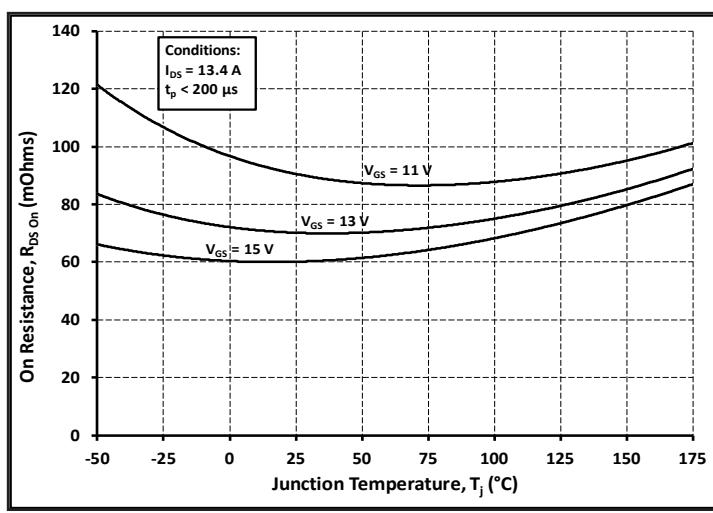
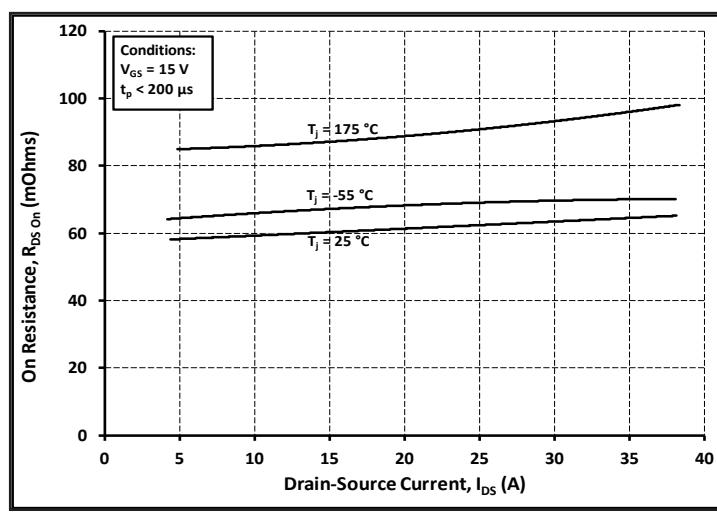
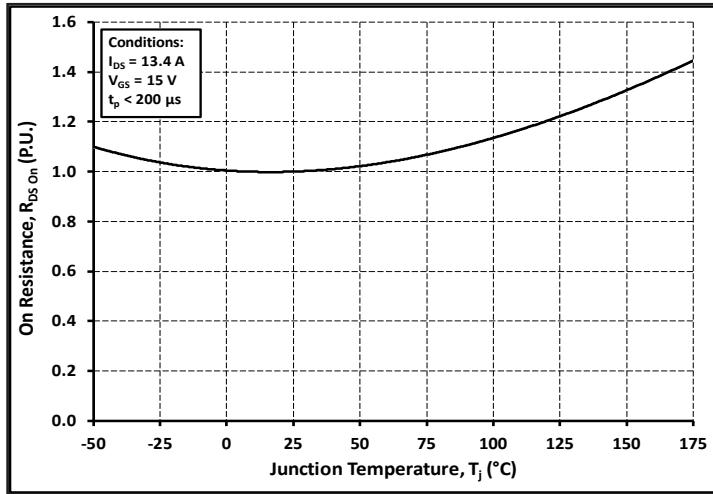
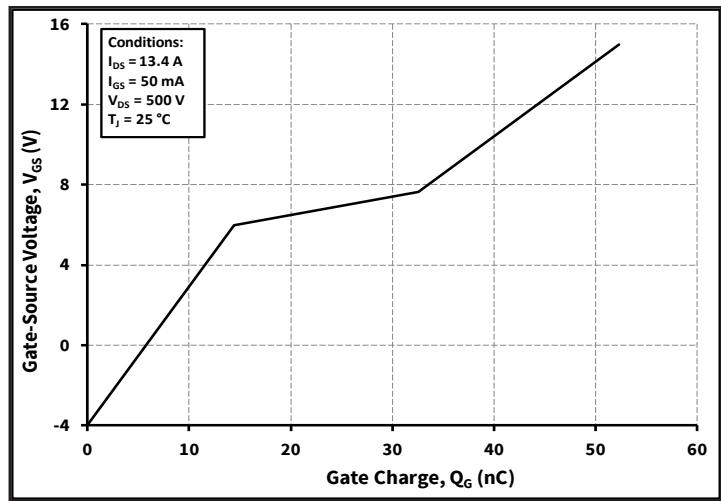
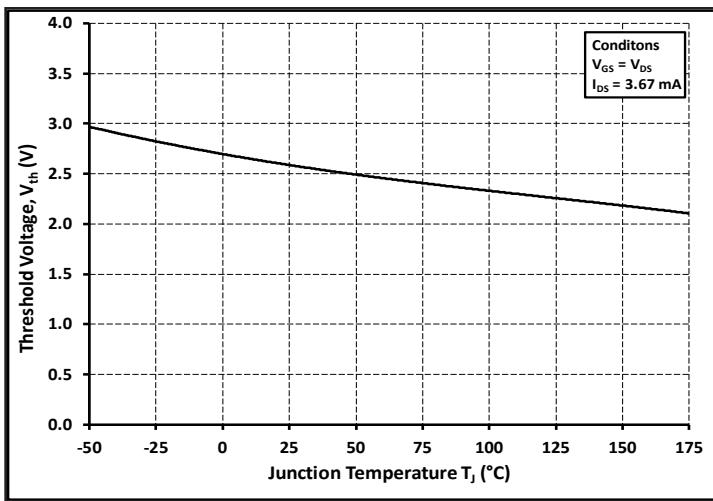
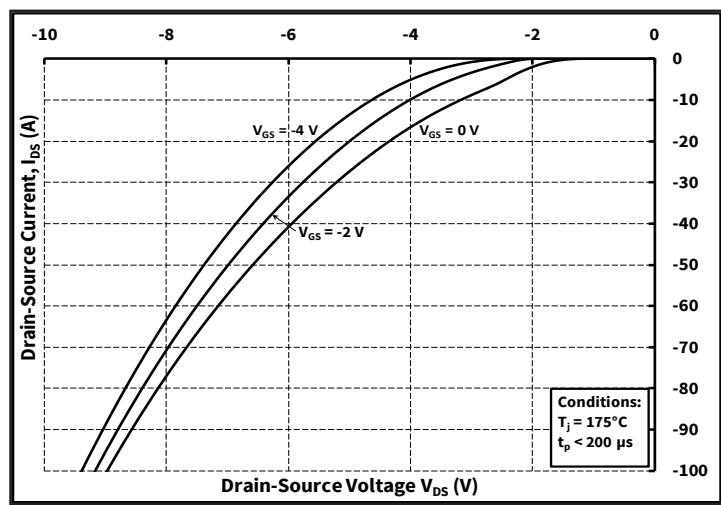
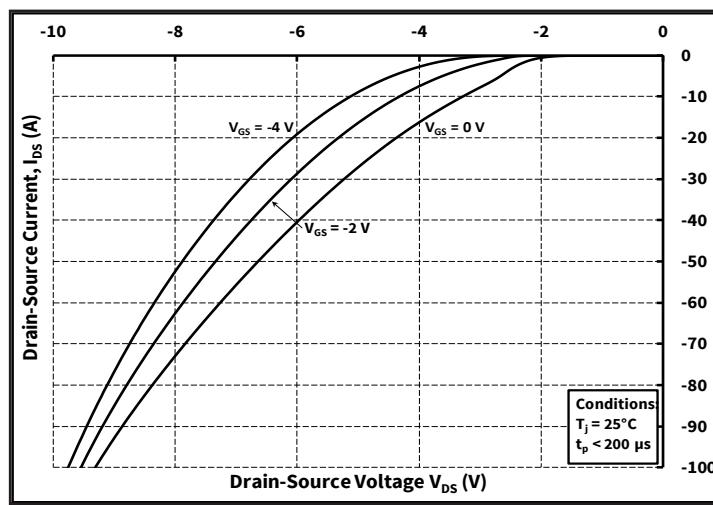
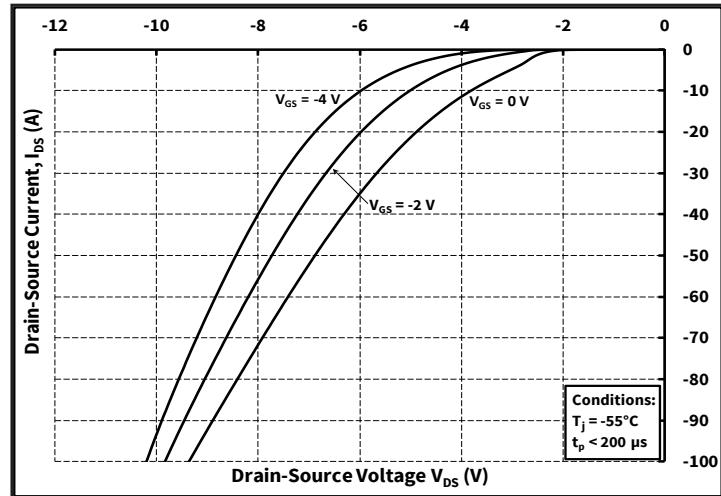
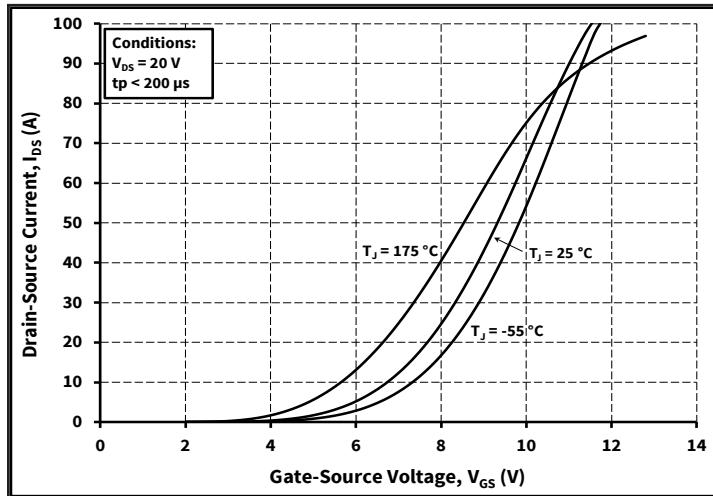


Figure 3. Output Characteristics $T_J = 175\text{ }^{\circ}\text{C}$



Typical Performance



Typical Performance

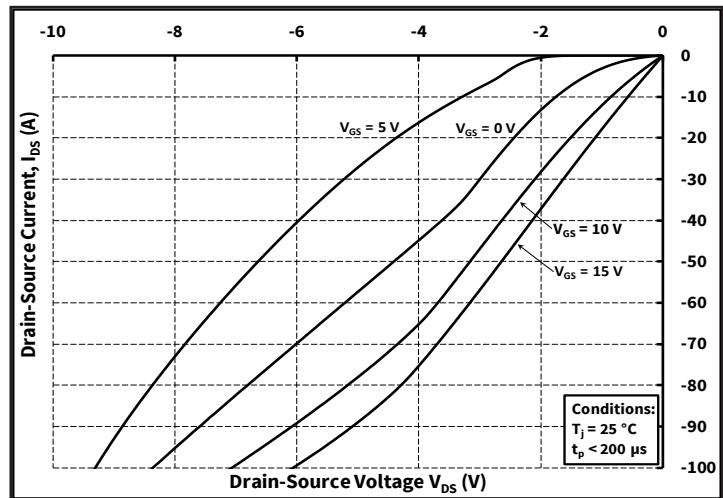
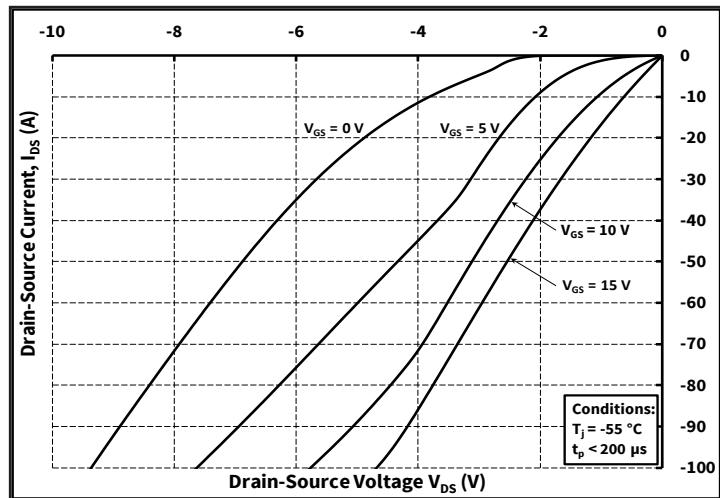
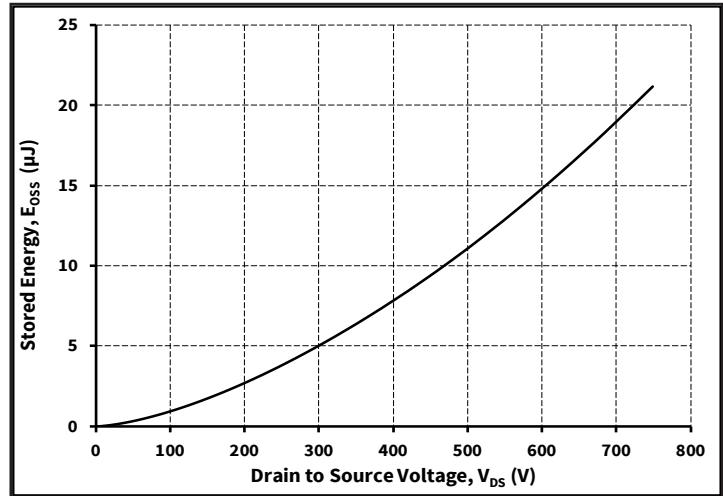
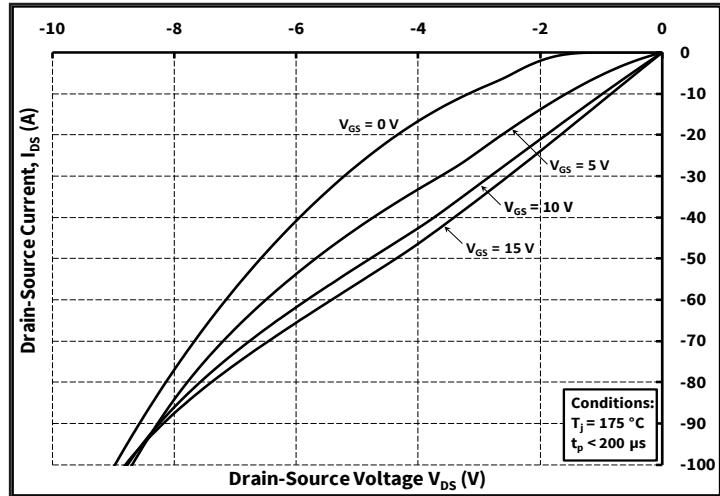
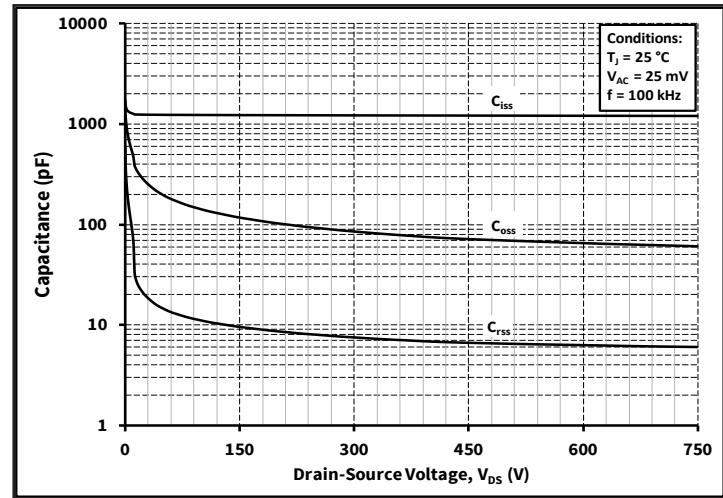
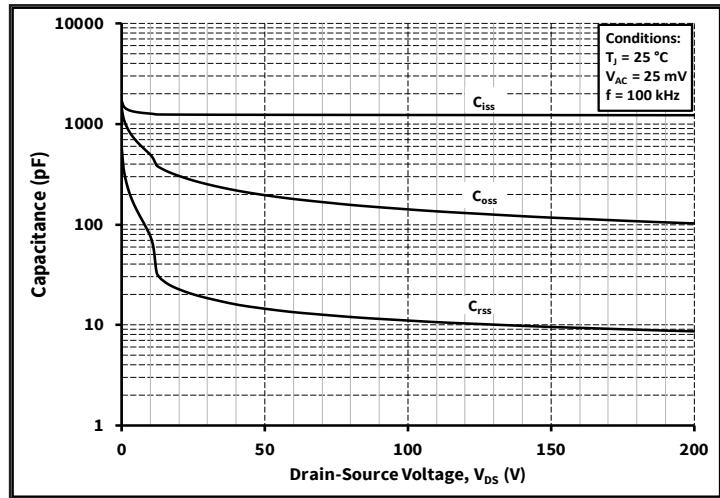
Figure 13. 3rd Quadrant Characteristic at $-55\text{ }^{\circ}\text{C}$ Figure 14. 3rd Quadrant Characteristic at $25\text{ }^{\circ}\text{C}$ Figure 15. 3rd Quadrant Characteristic at $175\text{ }^{\circ}\text{C}$

Figure 16. Output Capacitor Stored Energy



Typical Performance

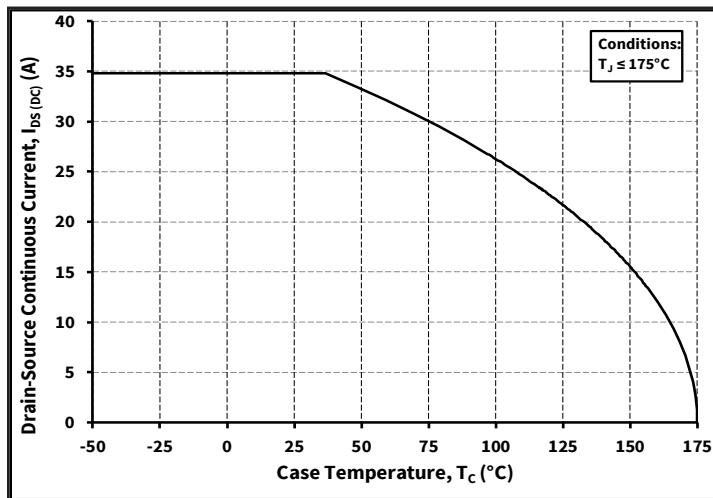


Figure 19. Continuous Drain Current Derating vs. Case Temperature

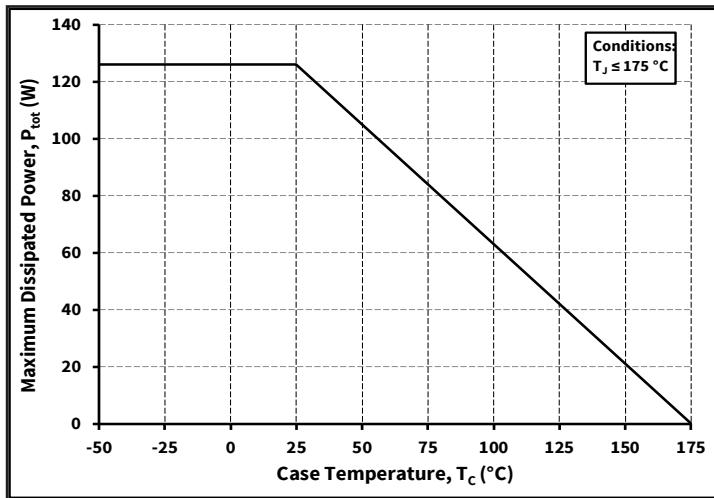


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

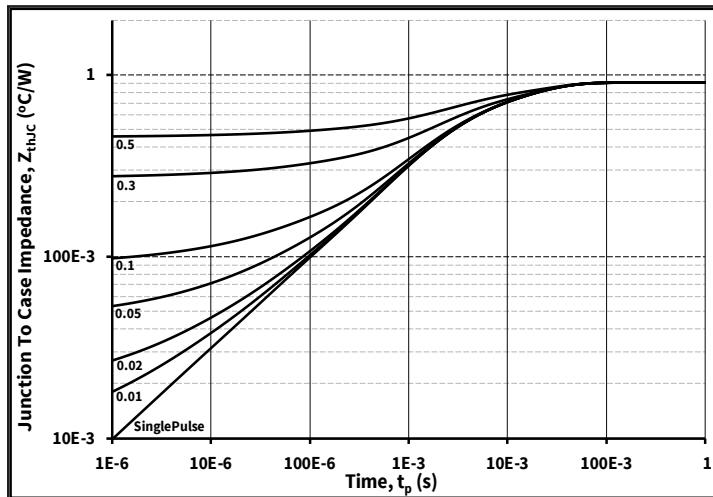


Figure 21. Transient Thermal Impedance (Junction - Case)

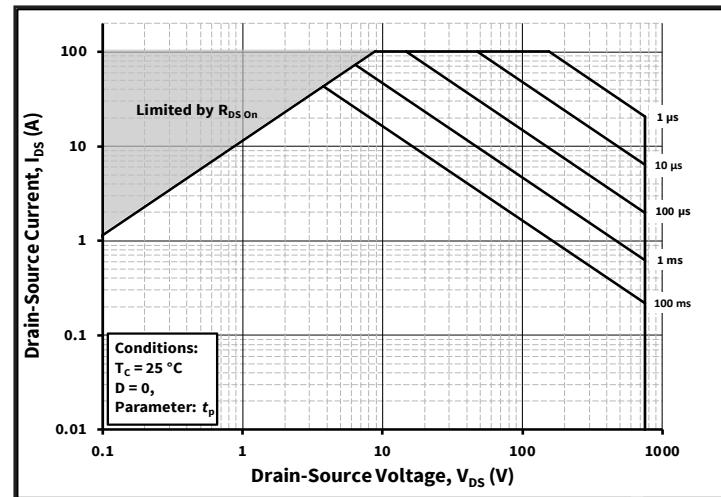


Figure 22. Safe Operating Area

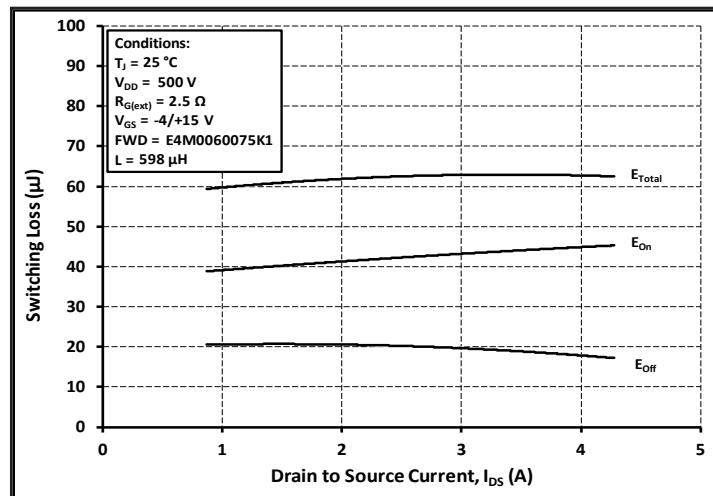


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 500V$)

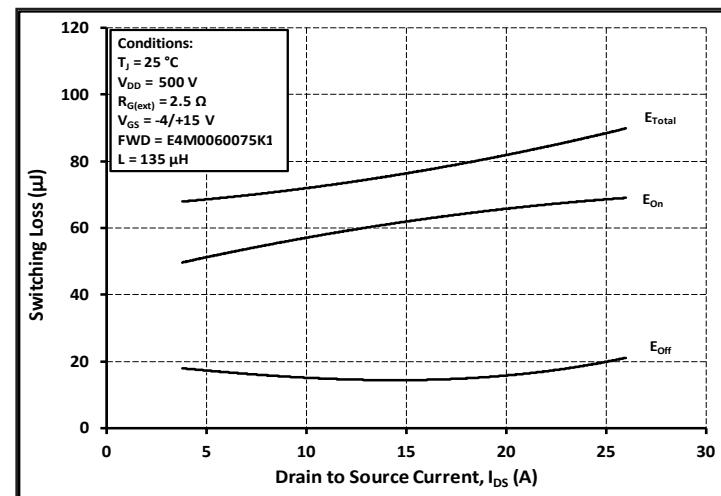


Figure 24. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 500V$)

Typical Performance

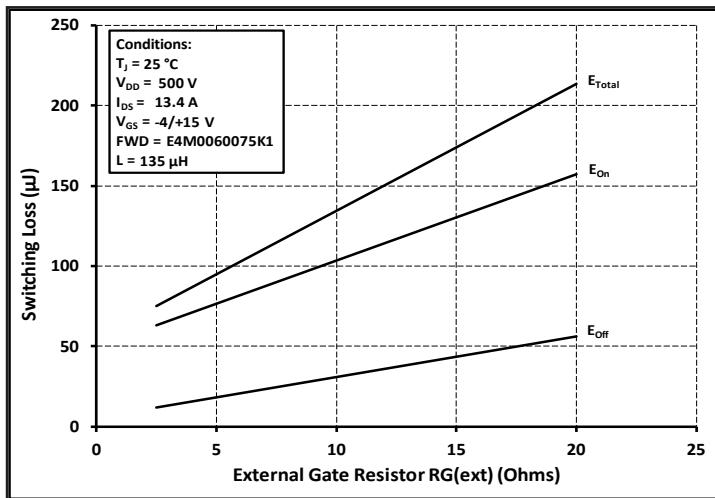
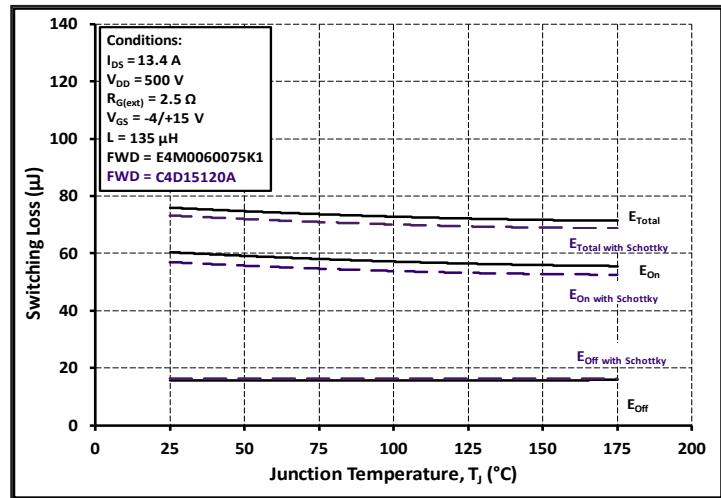
Figure 25. Clamped Inductive Switching Energy vs. $R_{G(\text{ext})}$ 

Figure 26. Clamped Inductive Switching Energy vs. Temperature

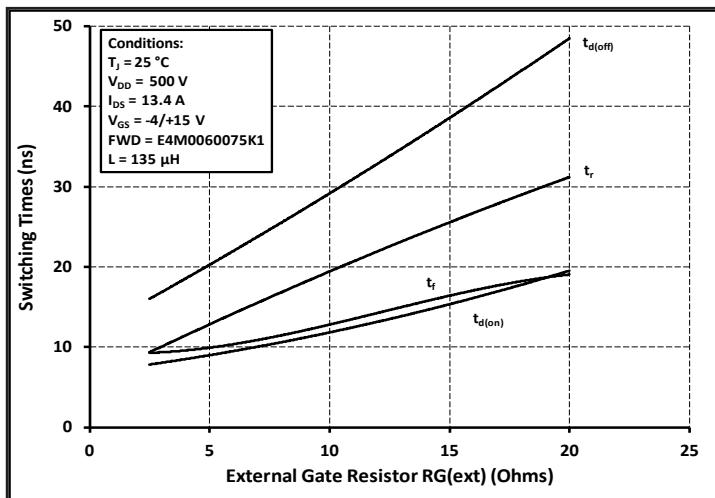
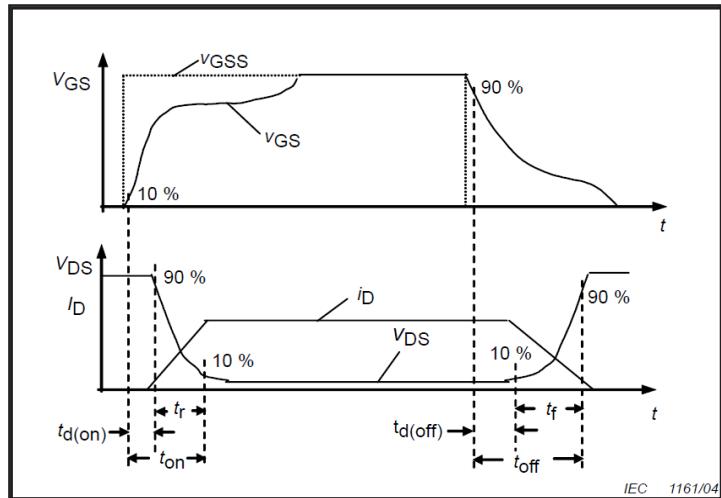
Figure 27. Switching Times vs. $R_{G(\text{ext})}$ 

Figure 28. Switching Times Definition

Test Circuit Schematic

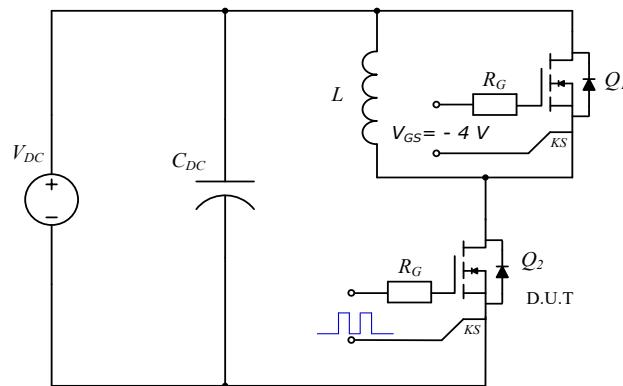
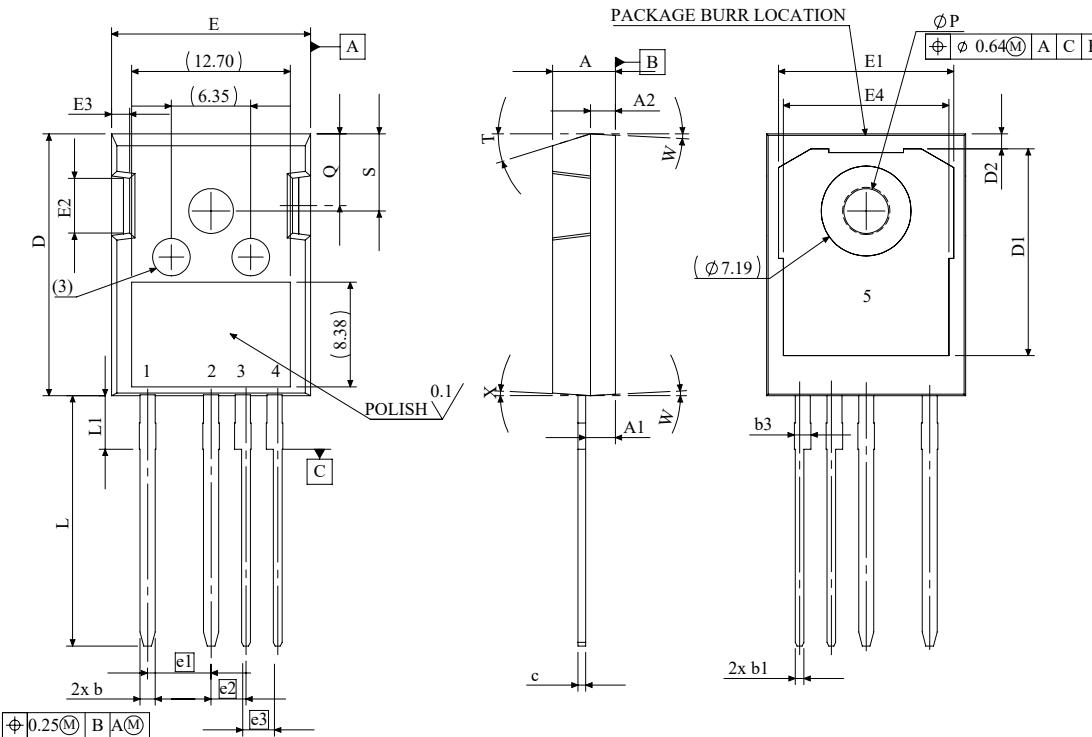


Figure 29. Clamped Inductive Switching Waveform Test Circuit

Package Dimensions



SYMBOL	MIN (mm)	MAX (mm)
A	4.83	5.21
A1	2.22	2.6
A2	1.91	2.16
b	1.10	1.30
b1	0.65	0.79
b3	1.34	1.44
c	0.55	0.68
D	20.76	21.14
D1	16.25	17.65
D2	0.92	1.42
E	15.75	16.13
E1	13.1	14.15
E2	3.68	5.10
E3	1.00	1.90
E4	12.38	13.43
e1	5.08	BSC
e2	2.79	BSC
e3	2.54	BSC
L	19.72	20.32
L1	3.87	4.47
ØP	3.51	3.65
Q	5.49	6.00
S	6.04	6.30
T	17.5° REF.	
W	3.5° REF.	
X	4° REF.	

1	DRAIN
2	SOURCE
3	SOURCE
4	GATE
5	DRAIN

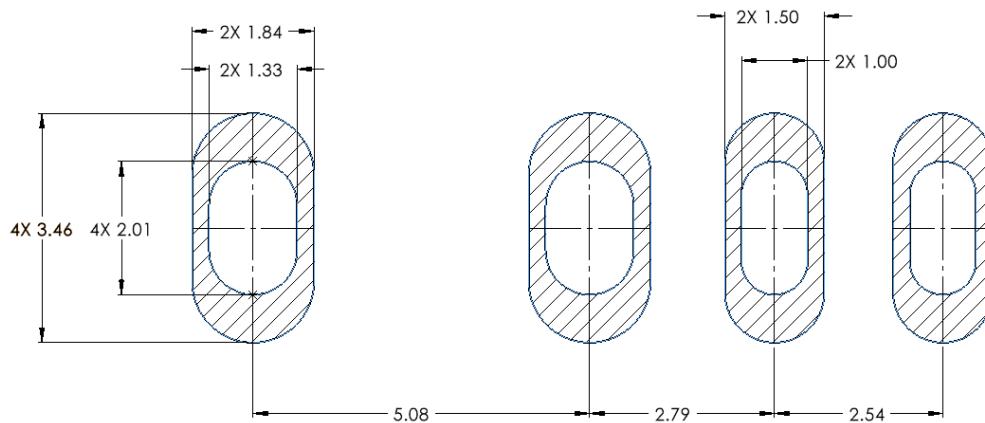
NOTE:

1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
 2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
 3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
 4. BURR OR MOLD FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS



Recommended Solder Pad Layout

All dimensions in mm



Revision history

Document Version	Date of release	Description of changes
1.0	March-2024	Initial datasheet



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