# MOSFET – Power, Dual N-Channel

## 40 V, 17.0 mΩ, 27 A

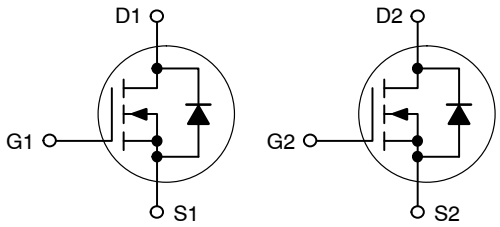
## NVMFD5C478N

| $V_{(BR)DSS}$ | $R_{DS(on)}$ MAX | $I_D$ MAX |
|---|---|---|
| 40 V | 17.0 mΩ @ 10 V | 27 A |

**Features**

- Small Footprint (5 x 6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVMFD5C478NWF – Wettable Flanks Product
- AEC–Q101 Qualified and PPAP Capable
- These Devices are Pb–Free and are RoHS Compliant

**Dual–Channel**




**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

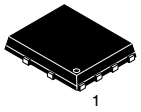
| Parameter | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain–to–Source Voltage | | | $V_{DSS}$ | 40 | V |
| Gate–to–Source Voltage | | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3, 4) | Steady State | $T_C$ = 25°C | $I_D$ | 27 | A |
| | | $T_C$ = 100°C | | 19 | |
| Power Dissipation $R_{\theta JC}$ (Notes 1, 2, 3) | | $T_C$ = 25°C | $P_D$ | 23 | W |
| | | $T_C$ = 100°C | | 12 | |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1 & 3, 4) | Steady State | $T_A$ = 25°C | $I_D$ | 9.8 | A |
| | | $T_A$ = 100°C | | 6.9 | |
| Power Dissipation $R_{\theta JA}$ (Notes 1, 3) | | $T_A$ = 25°C | $P_D$ | 3.1 | W |
| | | $T_A$ = 100°C | | 1.5 | |
| Pulsed Drain Current | $T_A$ = 25°C, $t_p$ = 10 μs | | $I_{DM}$ | 90 | A |
| Operating Junction and Storage Temperature | | | $T_J$, $T_{stg}$ | –55 to +175 | °C |
| Source Current (Body Diode) | | | $I_S$ | 19 | A |
| Single Pulse Drain–to–Source Avalanche Energy ($I_{L(pk)}$ = 1.4 A) | | | $E_{AS}$ | 48 | mJ |
| Lead Temperature for Soldering Purposes (1/8″ from case for 10 s) | | | $T_L$ | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**THERMAL RESISTANCE MAXIMUM RATINGS** (Note 1)

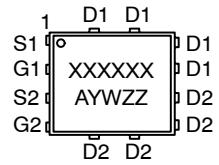
| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Junction–to–Case – Steady State (Note 3) | $R_{\theta JC}$ | 6.5 | °C/W |
| Junction–to–Ambient – Steady State (Note 3) | $R_{\theta JA}$ | 48.8 | |

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi (Ψ) is used as required per JESD51–12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface–mounted on FR4 board using a 650 $mm^2$, 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



**DFN8, 5x6**
**(S08FL)**
**CASE 506BT**

**PIN CONNECTION & MARKING DIAGRAM**




XXXXXX = 5C478N (NVMFD5C478N) or 478NWF (NVMFD5C478NWF)
A = Assembly Location
Y = Year
ZZ = Lot Traceability
WW = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

**ORDERING INFORMATION**

See detailed ordering, marking and shipping information on page 5 of this data sheet.

© Semiconductor Components Industries, LLC, 2017


Downloaded from Arrow.com.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 μA | | 40 | | | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 40 V | $T_J$ = 25°C | | | 10 | μA |
| | | | $T_J$ = 125°C | | | 250 | |
| Gate−to−Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = 20 V | | | | 100 | nA |
| **ON CHARACTERISTICS** (Note 5) | | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 20 μA | | 2.5 | | 3.5 | V |
| Drain−to−Source On Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 7.5 A | | | 14 | 17 | mΩ |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ = 3 V, $I_D$ = 7.5 A | | | 2 | | S |
| **CHARGES AND CAPACITANCES** | | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, f = 1.0 MHz, $V_{DS}$ = 25 V | | | 325 | | pF |
| Output Capacitance | $C_{oss}$ | | | | 165 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | | 10 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 10 V, $V_{DS}$ = 32 V, $I_D$ = 7.5 A | | | 6.3 | | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | | 1.3 | | nC |
| Gate−to−Source Charge | $Q_{GS}$ | | | | 2.0 | | |
| Gate−to−Drain Charge | $Q_{GD}$ | | | | 1.2 | | |
| **SWITCHING CHARACTERISTICS** (Note 6) | | | | | | | |
| Turn−On Delay Time | $t_{d(on)}$ | $V_{GS}$ = 10 V, $V_{DS}$ = 32 V, $I_D$ = 7.5 A, $R_G$ = 1 Ω | | | 7 | | ns |
| Rise Time | $t_r$ | | | | 13 | | |
| Turn−Off Delay Time | $t_{d(off)}$ | | | | 14 | | |
| Fall Time | $t_f$ | | | | 4.5 | | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| Forward Diode Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = 7.5 A | $T_J$ = 25°C | | 0.84 | 1.2 | V |
| | | | $T_J$ = 125°C | | 0.72 | | |
| Reverse Recovery Time | $t_{RR}$ | $V_{GS}$ = 0 V, $dI_S/dt$ = 100 A/μs, $I_S$ = 7.5 A | | | 18 | | ns |
| Charge Time | $t_a$ | | | | 7.0 | | |
| Discharge Time | $t_b$ | | | | 11 | | |
| Reverse Recovery Charge | $Q_{RR}$ | | | | 6 | | nC |

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.



Share Feedback
Your Opinion Matters

Downloaded from Arrow.com.

## TYPICAL CHARACTERISTICS

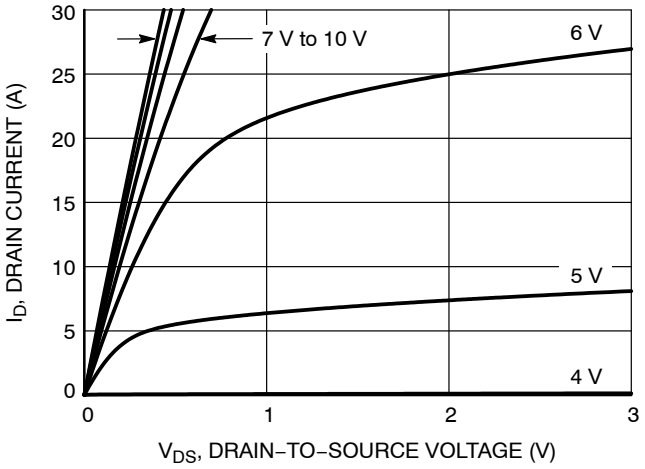



**Figure 1. On−Region Characteristics**

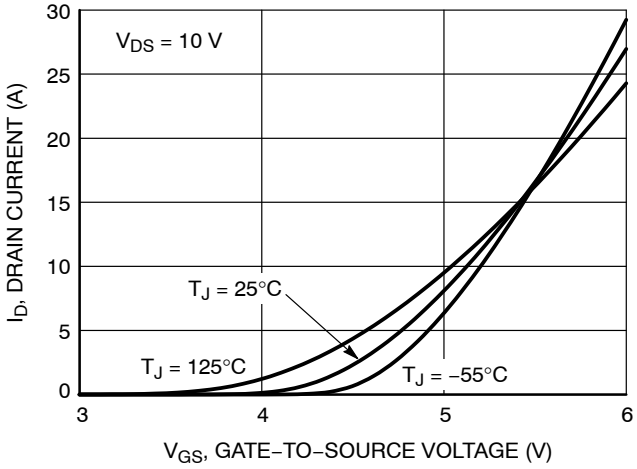



**Figure 2. Transfer Characteristics**

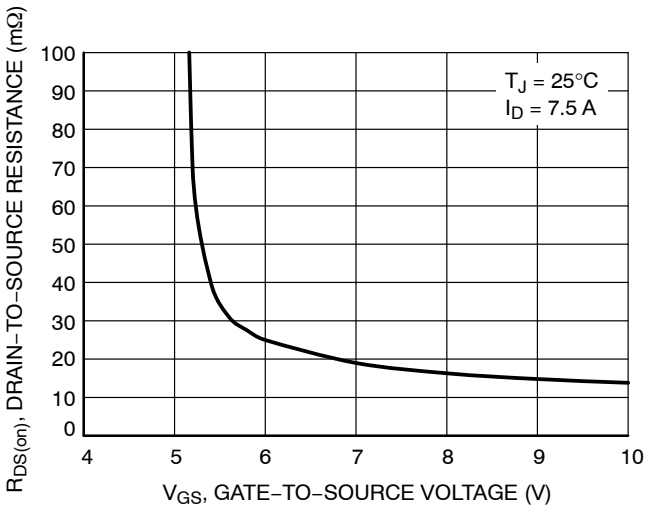



**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

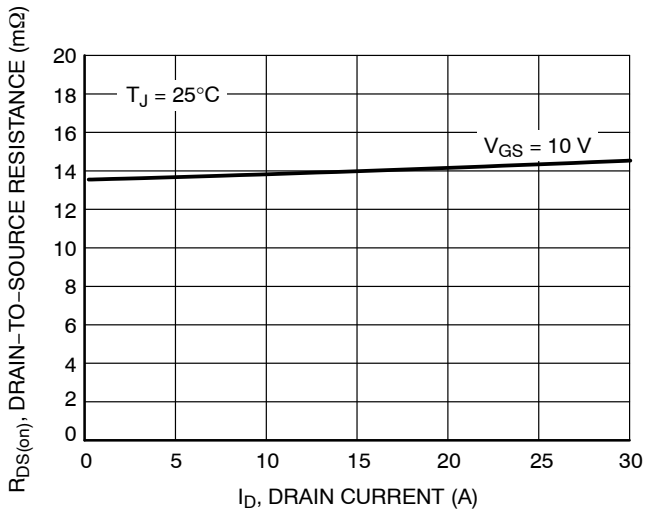



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

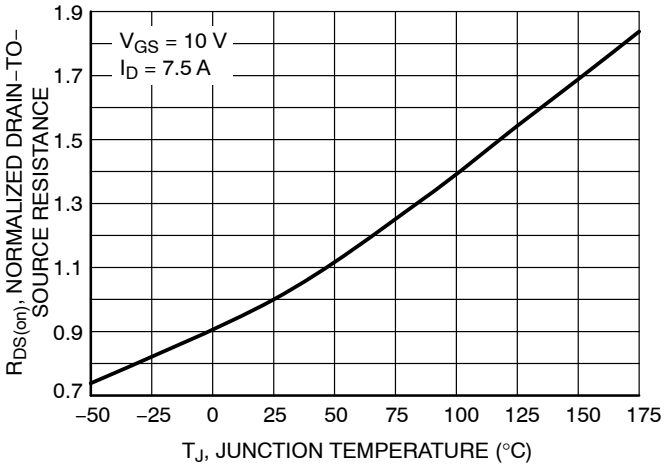



**Figure 5. On−Resistance Variation with Temperature**

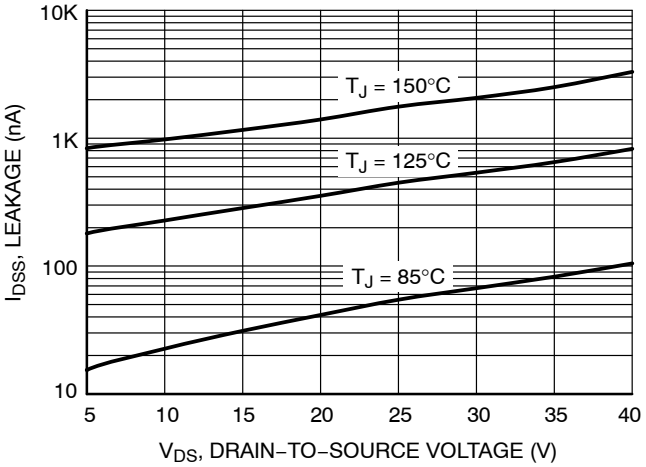



**Figure 6. Drain−to−Source Leakage Current vs. Voltage**



Share Feedback
Your Opinion Matters

Downloaded from Arrow.com.

## TYPICAL CHARACTERISTICS

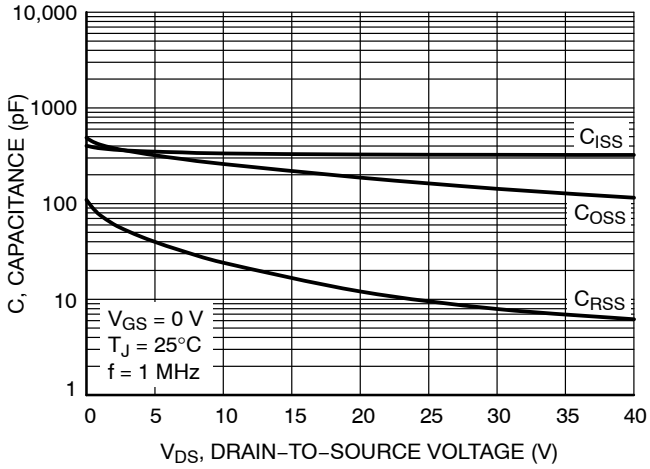



**Figure 7. Capacitance Variation**

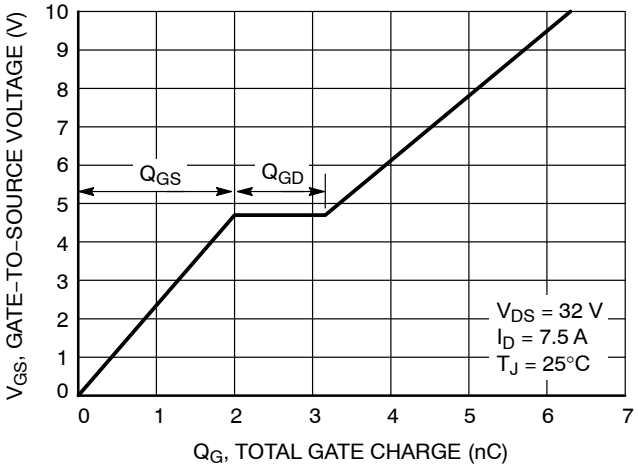



**Figure 8. Gate−to−Source Voltage vs. Total Charge**

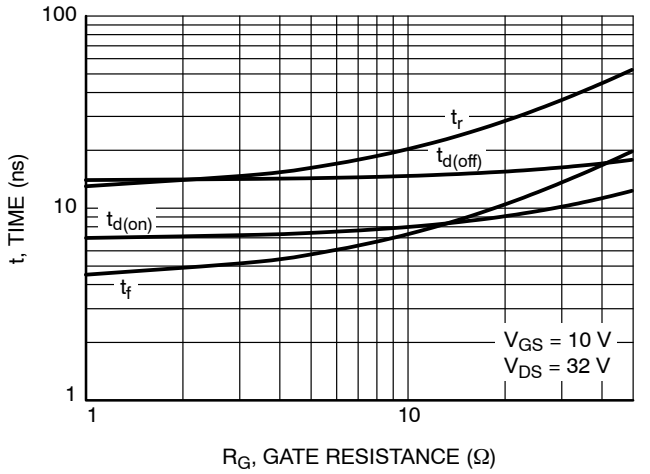



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

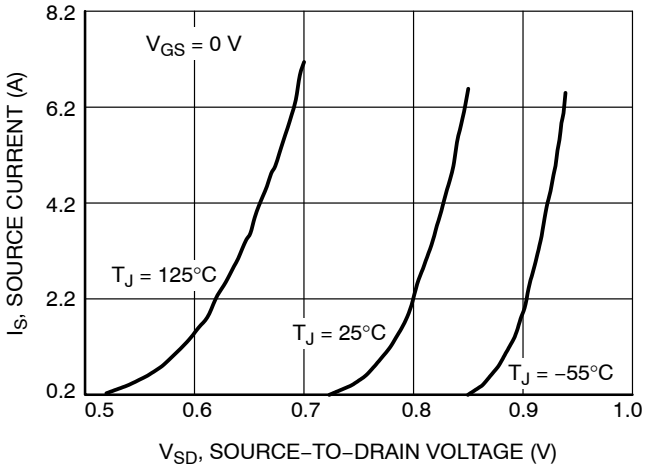



**Figure 10. Diode Forward Voltage vs. Current**

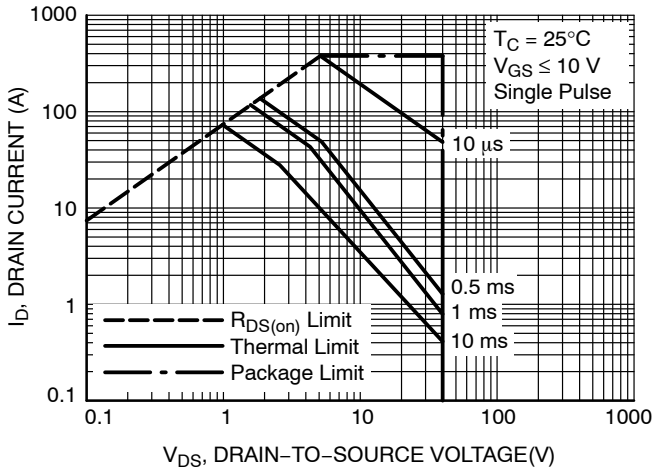



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

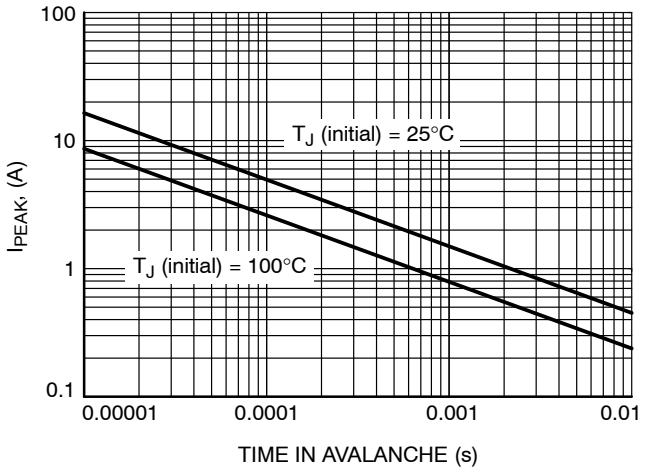



**Figure 12. $I_{PEAK}$ vs. Time in Avalanche**



Share Feedback
Your Opinion Matters

Downloaded from Arrow.com.

## TYPICAL CHARACTERISTICS

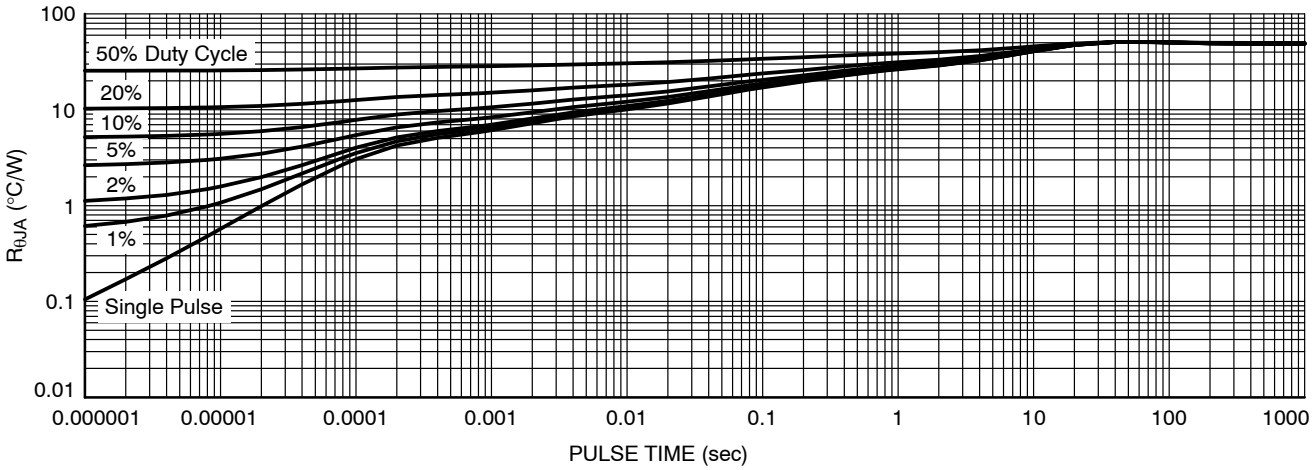



**Figure 13. Thermal Characteristics**

### DEVICE ORDERING INFORMATION

| Device | Marking | Package | Shipping† |
|---|---|---|---|
| NVMFD5C478NT1G | 5C478N | DFN8<br>(Pb−Free) | 1500 / Tape & Reel |
| NVMFD5C478NWFT1G | 478NWF | DFN8<br>(Pb−Free) | 1500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



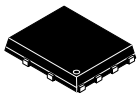
Share Feedback
Your Opinion Matters

Downloaded from Arrow.com.

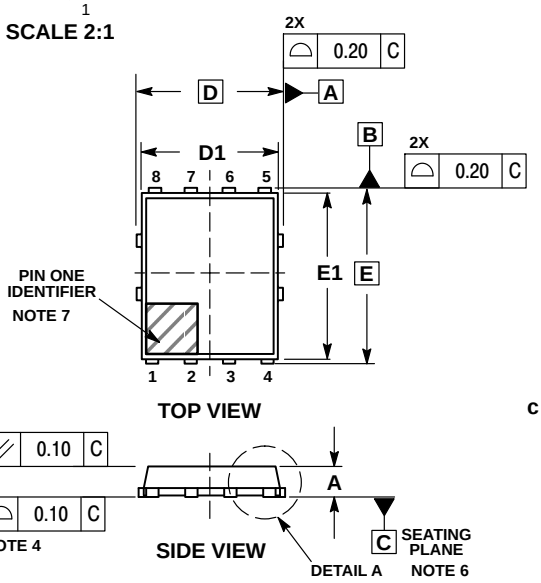
# DFN8 5x6, 1.27P Dual Flag (SO8FL−Dual)

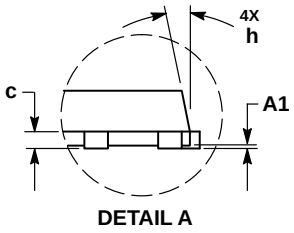
CASE 506BT
ISSUE F

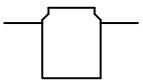
DATE 23 NOV 2021



SCALE 2:1



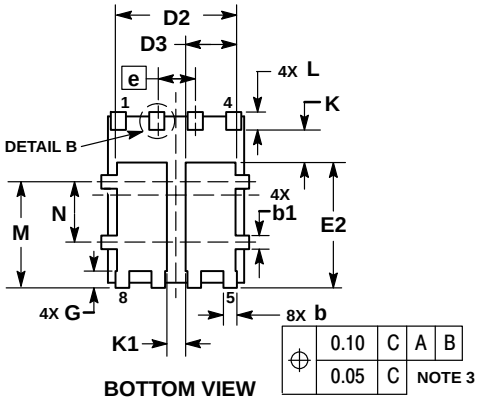



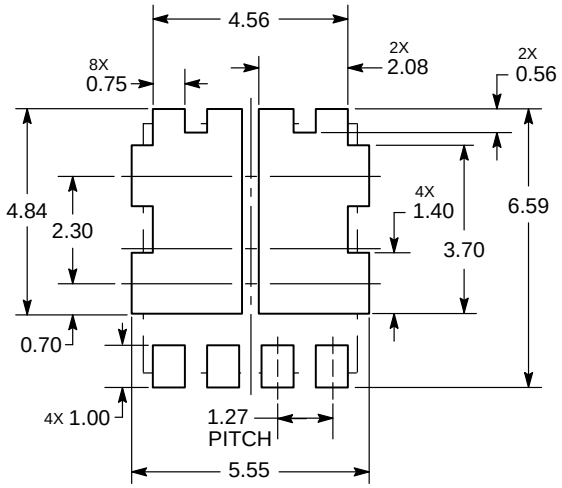
DETAIL B
ALTERNATE
CONSTRUCTION

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. PROFILE TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. A VISUAL INDICATOR FOR PIN 1 MUST BE LOCATED IN THIS AREA.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.90 | ––– | 1.10 |
| A1 | ––– | ––– | 0.05 |
| b | 0.33 | 0.42 | 0.51 |
| b1 | 0.33 | 0.42 | 0.51 |
| c | 0.20 | ––– | 0.33 |
| D | | 5.15 BSC | |
| D1 | 4.70 | 4.90 | 5.10 |
| D2 | 3.90 | 4.10 | 4.30 |
| D3 | 1.50 | 1.70 | 1.90 |
| E | | 6.15 BSC | |
| E1 | 5.70 | 5.90 | 6.10 |
| E2 | 3.90 | 4.15 | 4.40 |
| e | | 1.27 BSC | |
| G | 0.45 | 0.55 | 0.65 |
| h | ––– | ––– | 12 ° |
| K | 0.51 | ––– | ––– |
| K1 | 0.56 | ––– | ––– |
| L | 0.48 | 0.61 | 0.71 |
| M | 3.25 | 3.50 | 3.75 |
| N | 1.80 | 2.00 | 2.20 |



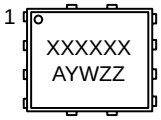

## SOLDERING FOOTPRINT*




DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
| DOCUMENT NUMBER: | 98AON50417E | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| DESCRIPTION: | DFN8 5X6, 1.27P DUAL FLAG (SO8FL−DUAL) | PAGE 1 OF 1 |

**onsemi** and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.



Downloaded from Arrow.com.

**onsemi**, ONSEMI , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales

◊

Downloaded from Arrow.com.