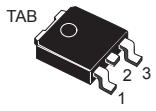
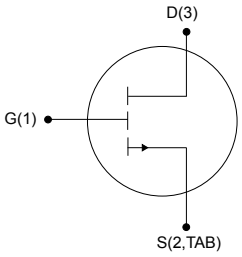
SGT350R70GTK

Datasheet

700 V, 270 mΩ typ., 6 A, e-mode PowerGaN transistor



DPAK



G1S2TAB3D_GaN

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	Series
SGT350R70GTK	700 V	350 mΩ	6 A	G-HEMT

- Enhancement mode normally off transistor
- Very high switching speed
- High power management capability
- Extremely low capacitances
- Zero reverse recovery charge
- ESD safeguard

Applications

- Adapters for tablets, notebook and AIO
- USB type-C PD adapters and quick chargers

Description

The SGT350R70GTK is a 700 V, 6 A e-mode PowerGaN transistor combined with a well-established packaging technology. The resulting G-HEMT device provides extremely low conduction losses, high current capability and ultrafast switching operation to enable high-power density and unbeatable efficiency performances. Recommended for consumer QR applications with zero current turn-on.

Product status link
SGT350R70GTK

Product summary	
Order code	SGT350R70GTK
Marking	350R70G
Package	DPAK
Packing	Tape and reel

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1 Electrical ratings

T_C = 25 °C unless otherwise specified.

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	700(1)	V
	Drain-source voltage (transient, t_p < 200 µs)	800	
V_{GS}	Gate-source voltage	-1.4 to 7	V
I_D	Drain current (continuous) at T_C = 25 °C	6(2)	A
I_{DM}	Pulse drain current (t_p = 10 µs)	10	A
P_{TOT}	Total power dissipation at T_C = 25 °C	47	W
ESD	Human body model, R = 1.5 kΩ, C = 100 pF	2	kV
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Recommended continuous maximum bus voltage during switching operations should not exceed 450 V.*
2. *Limited by design.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	2.63	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	56(1)	°C/W

1. *When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.*

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2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{DSS}	Drain-source leakage current	V_{GS} = 0 V, V_{DS} = 700 V		0.6	12	µA
		V_{GS} = 0 V, V_{DS} = 700 V, T_J = 150 °C		5		
I_{GSS}	Gate-source leakage current	V_{DS} = 0 V, V_{GS} = 6 V		30		µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 6.6 mA	1.2	1.7	2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 6 V, I_D = 2.2 A		270	350	mΩ
		V_{GS} = 6 V, I_D = 2.2 A, T_J = 150 °C		580		

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 400 V, f = 100 kHz	-	50	-	pF
C_{oss}	Output capacitance		-	15	-	pF
C_{rss}	Reverse transfer capacitance		-	0.2	-	pF
$C_{o(er)}$ (1)	Equivalent output capacitance energy related	V_{GS} = 0 V, V_{DS} = 0 to 400 V	-	20	-	pF
$C_{o(tr)}$ (2)	Equivalent output capacitance time related		-	28	-	pF
R_g	Intrinsic gate resistance	f = 5 MHz, I_D = 0 A	-	11	-	Ω
V_{plat}	Gate plateau voltage	V_{DS} = 400 V, I_D = 2.2 A	-	2.2	-	V
Q_g	Total gate charge	V_{GS} = 0 to 6 V, V_{DS} = 400 V, I_D = 2.2 A	-	1.5	-	nC
Q_{gs}	Gate-source charge		-	0.15	-	nC
Q_{gd}	Gate-drain charge		-	0.5	-	nC
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V, V_{DS} = 400 V	-	0	-	nC
Q_{oss}	Output charge		-	13	-	nC

1. *$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to the stated value.*
2. *$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to the stated value.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DS} = 400 V, I_D = 4.4 A, V_{GS} = 6 V, $R_{G(on)}$ = 10 Ω, $R_{G(off)}$ = 2 Ω, L= 318 µH	-	0.9	-	ns
t_r	Rise time		-	3.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	1.2	-	ns
t_f	Fall time		-	6.1	-	ns

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Table 6. Reverse conduction

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Source-drain reverse voltage	V_{GS} = 0 V, I_{SD} = 2.2 A	-	2.6	-	V

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2.1 Electrical characteristics (curves)

Figure 1. Safe operating area (T_C = 25 °C)

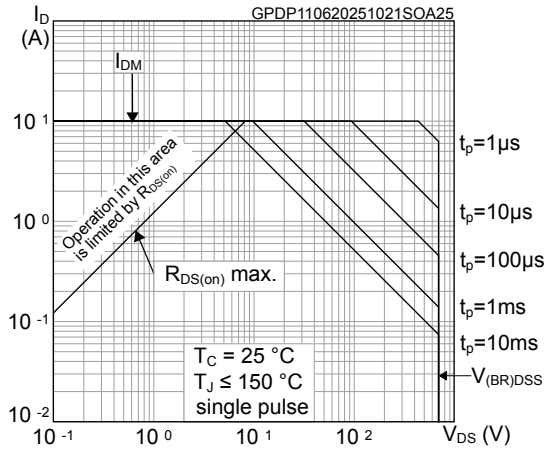


Figure 2. Safe operating area (T_C = 125 °C)

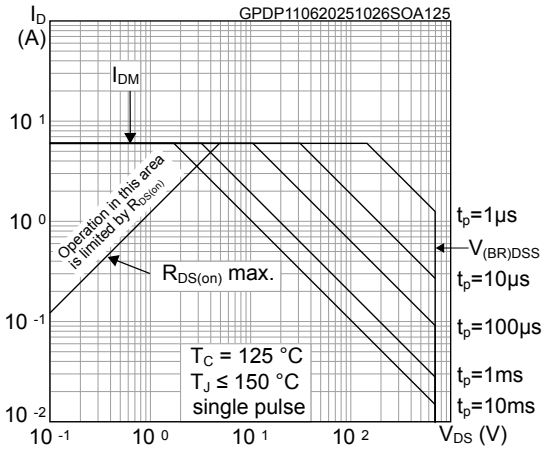


Figure 3. Maximum transient thermal impedance

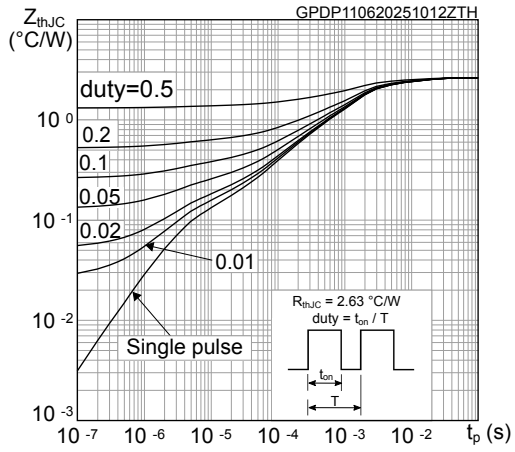


Figure 4. Total power dissipation

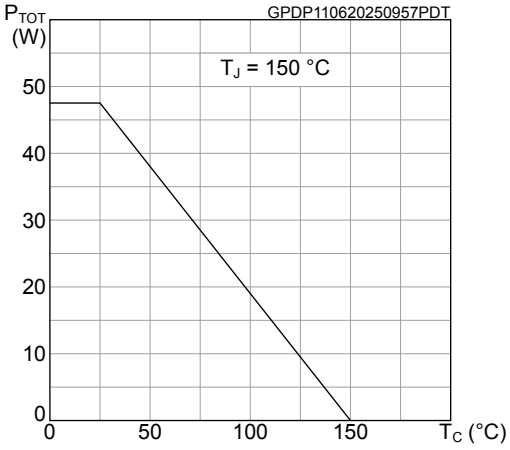


Figure 5. Typical output characteristics (T_J = 25 °C)

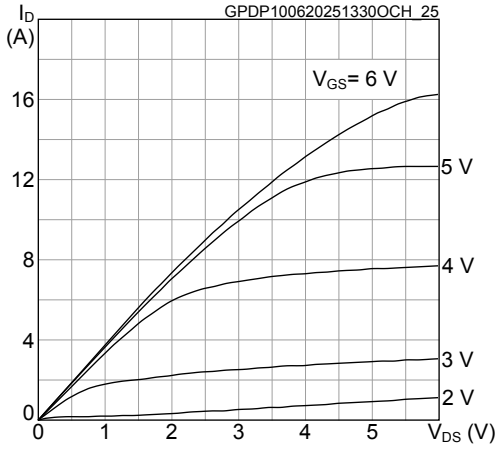
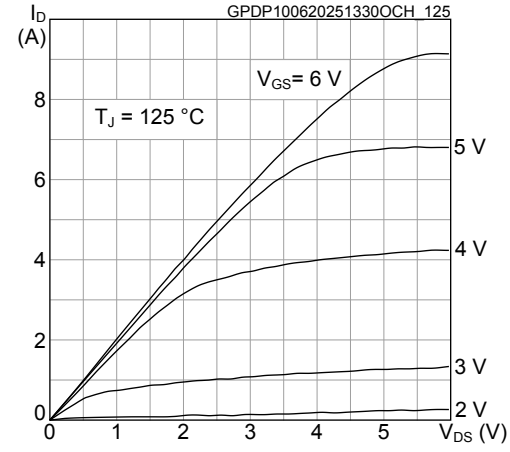


Figure 6. Typical output characteristics (T_J = 125 °C)



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Figure 7. Typical transfer characteristics

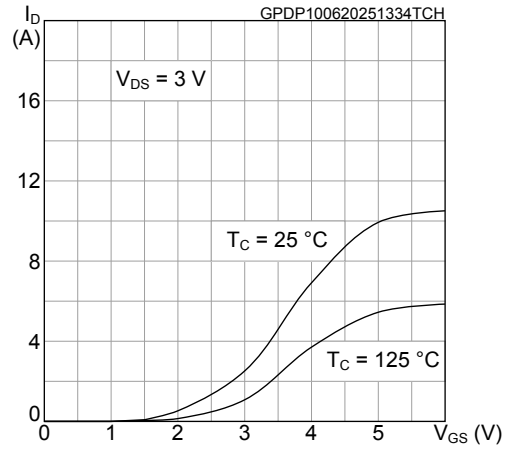


Figure 8. Normalized on-resistance vs temperature

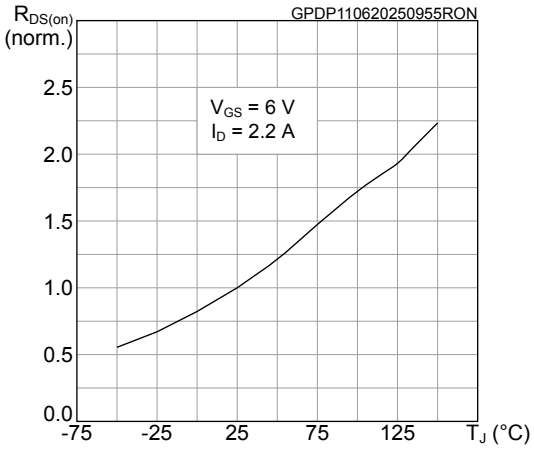


Figure 9. Typical drain-source on-resistance (T_J = 25 °C)

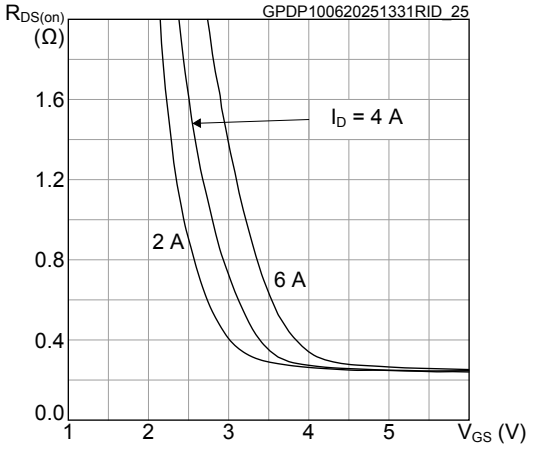


Figure 10. Typical drain-source on-resistance (T_J = 125 °C)

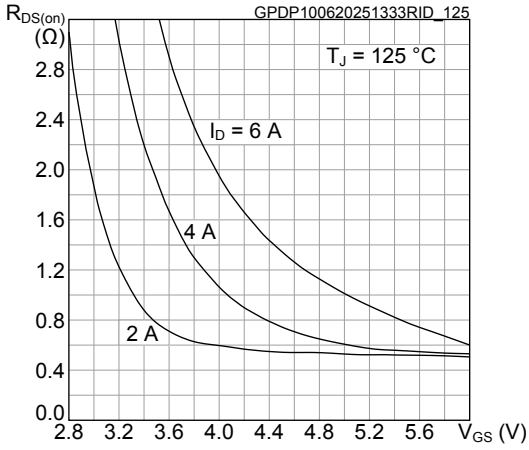


Figure 11. Typical gate charge characteristics

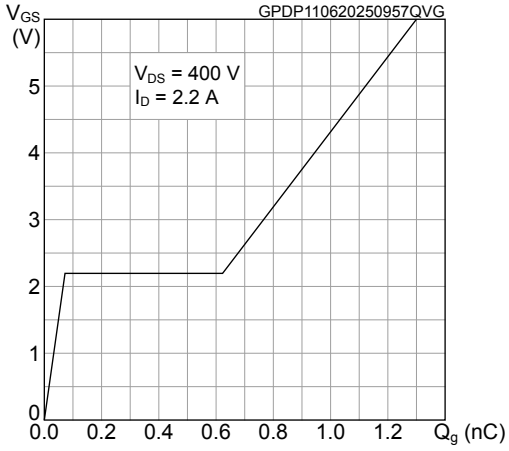
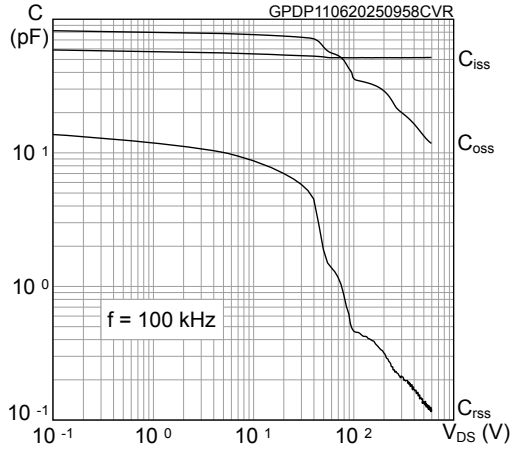


Figure 12. Typical capacitance characteristics



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Figure 13. Typical output capacitance charge

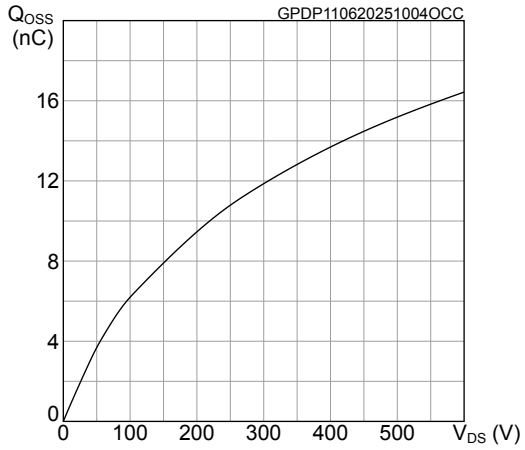


Figure 14. Typical output capacitance stored energy

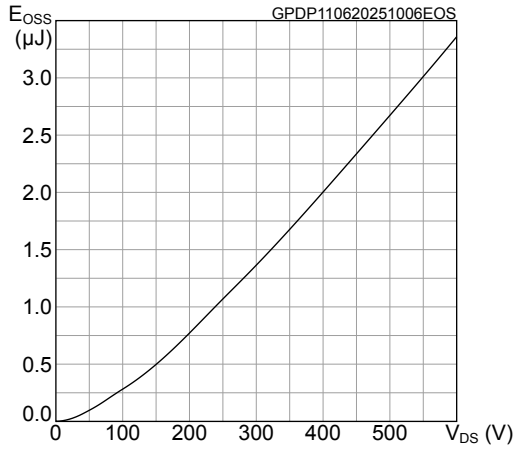


Figure 15. Typical diode reverse conduction characteristics (T_J = 25 °C)

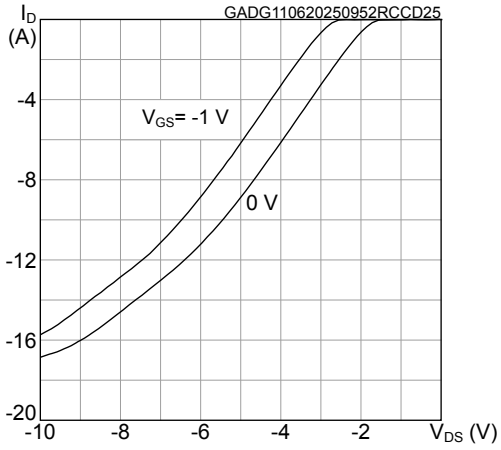


Figure 16. Typical diode reverse conduction characteristics (T_J = 125 °C)

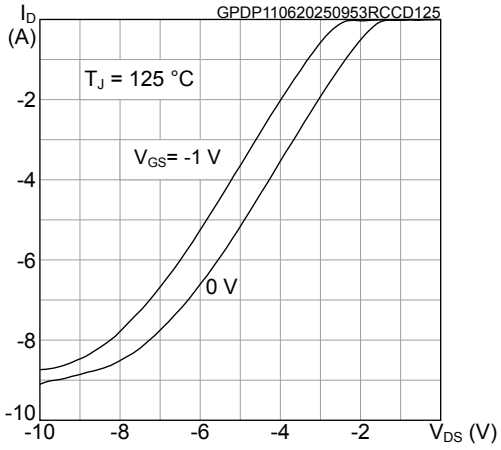


Figure 17. Typical reverse conduction characteristics (T_J = 25 °C)

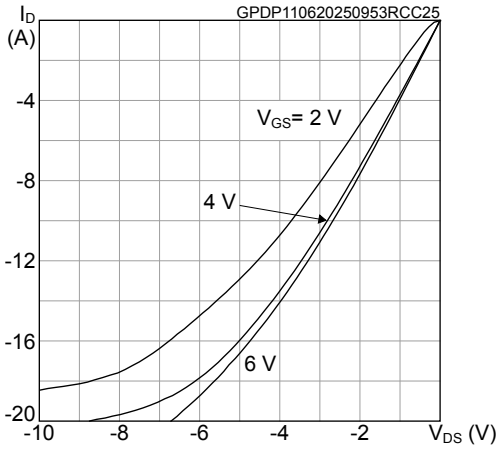
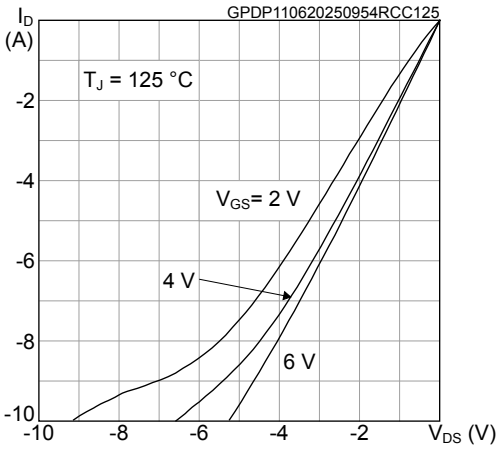
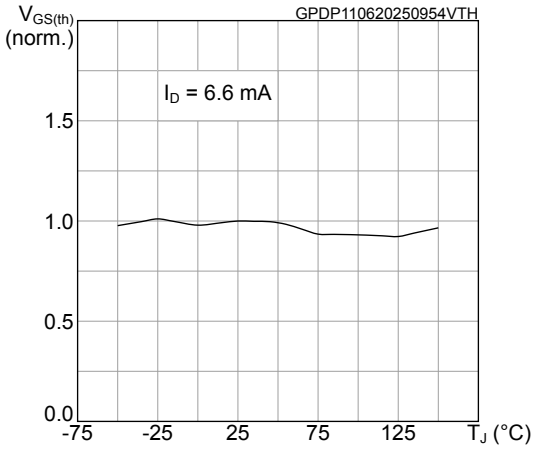


Figure 18. Typical reverse conduction characteristics (T_J = 125 °C)



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Figure 19. Normalized gate threshold vs temperature



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3 Test circuits

Figure 20. Test circuit for inductive load switching times

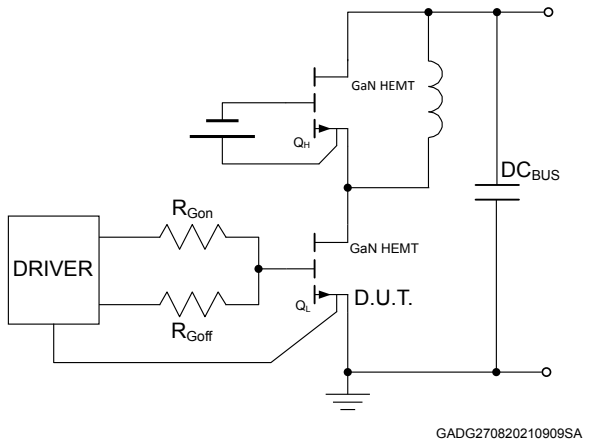
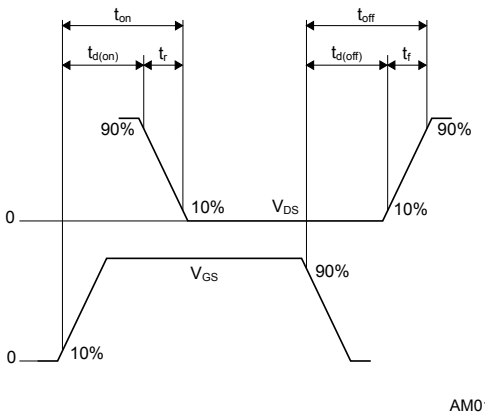


Figure 21. Switching time waveforms



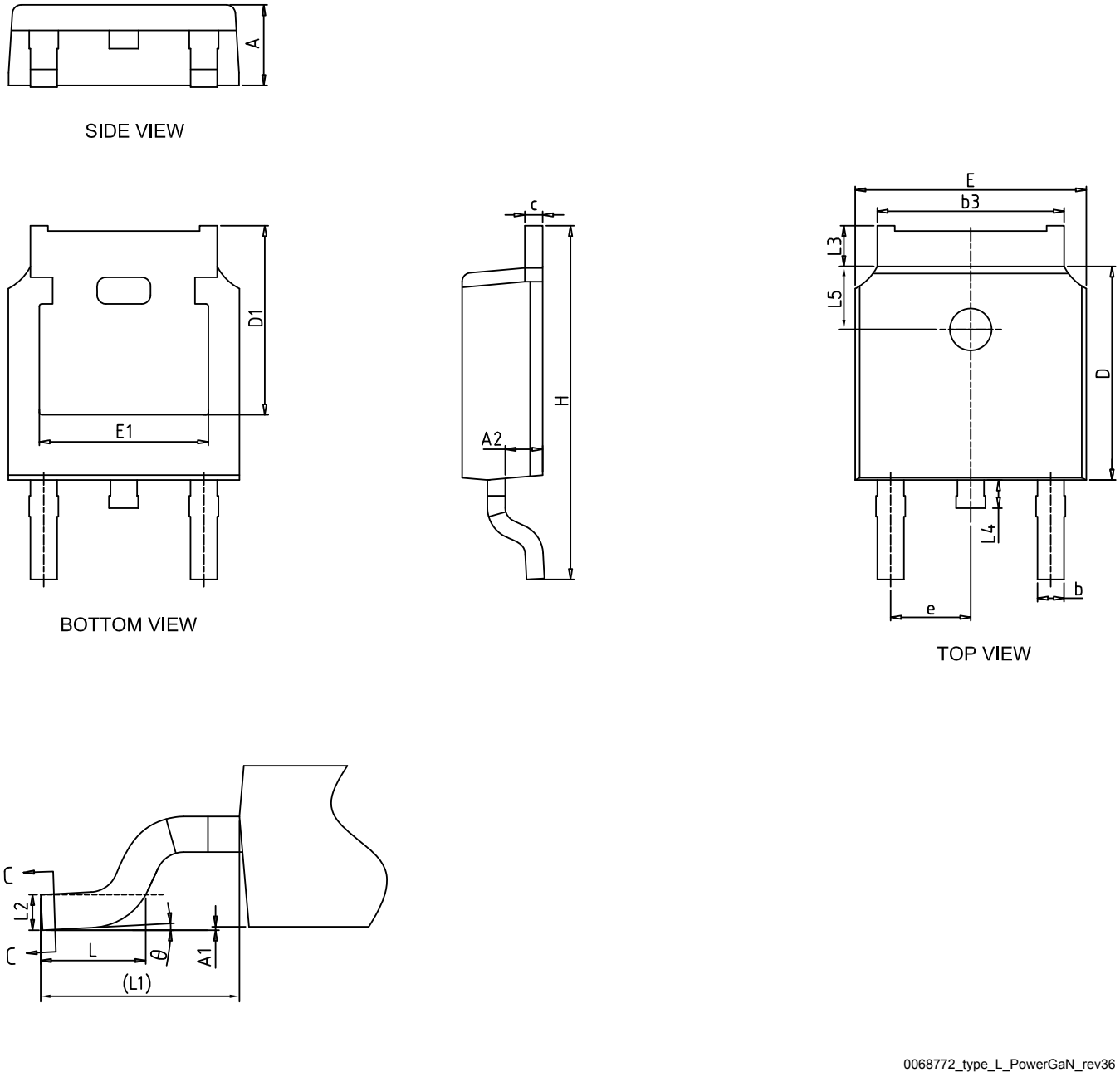
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type L for PowerGaN package information

Figure 22. DPAK (TO-252) type L for PowerGaN package outline



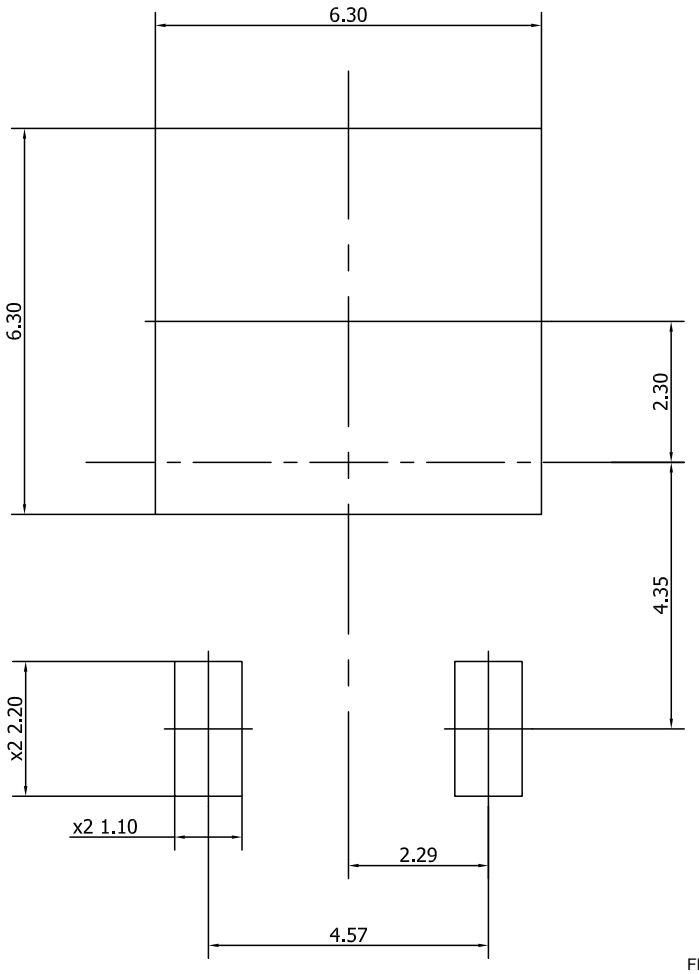
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Table 7. **DPAK (TO-252) type L for PowerGaN mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.00		0.12
A2	0.97	1.07	1.17
b	0.68	0.78	0.90
b3	5.20	5.33	5.46
c	0.43	0.53	0.61
D	5.98	6.10	6.22
D1		5.30 REF	
E	6.40	6.60	6.73
E1	4.63		
e		2.286 BSC	
H	9.40	10.10	10.50
L	1.38	1.50	1.75
L1		2.90 REF	
L2		0.51 BSC	
L3	0.88		1.28
L4	0.50		1.00
L5	1.65	1.80	1.95
V2	0°		8°

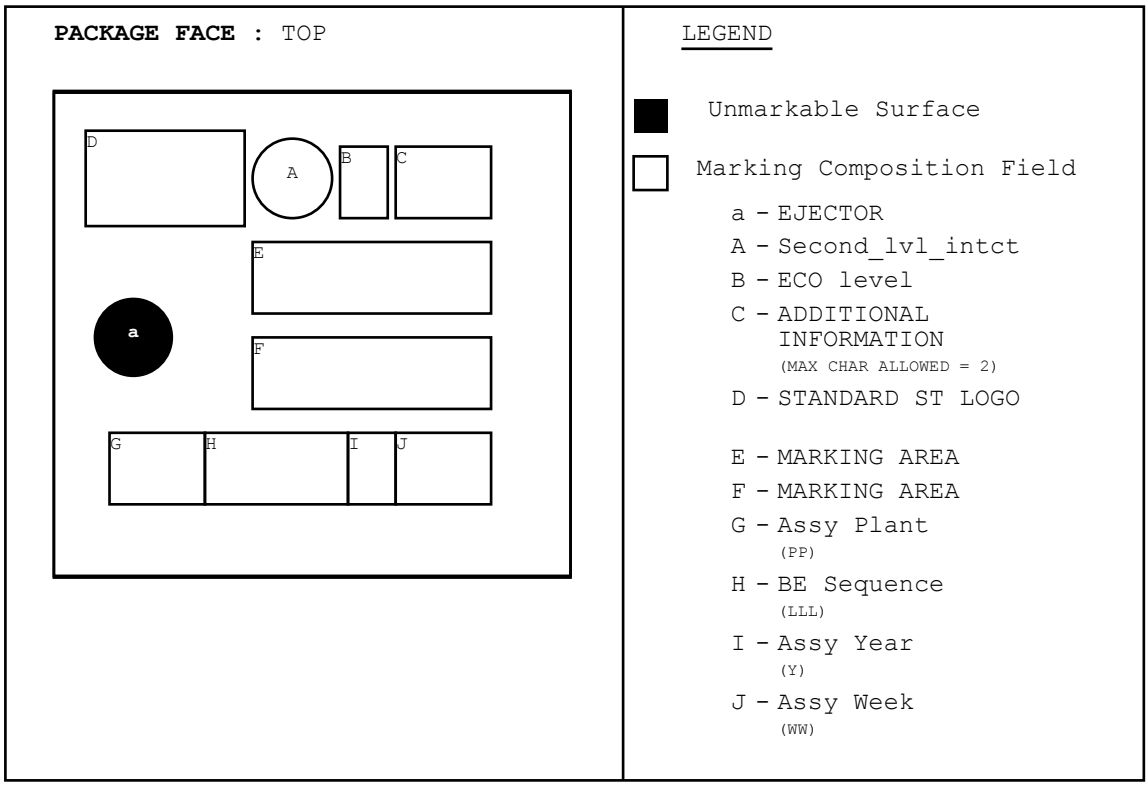
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Figure 23. **DPAK (TO-252) type L for PowerGaN recommended footprint (dimensions are in mm)**



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Figure 24. **Marking composition for DPAK (TO-252) type L for PowerGaN for PowerGaN**



CD00330413_Rev.2

Engineering samples

These samples are clearly identified by “ES” digits in the marking additional information field of each unit. These samples are intended to be used for electrical compatibility evaluation only; usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.

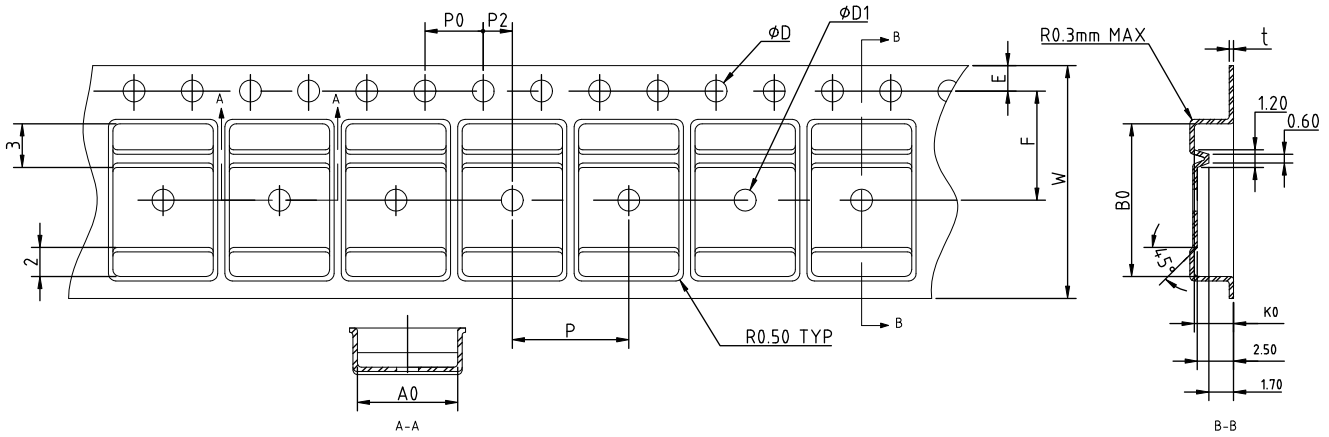
Commercial samples

Fully qualified parts from ST standard production with no limitations of use or special identification marking.

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4.2 DPAK (TO-252) type L for PowerGaN packing information

Figure 25. **DPAK (TO-252) type L for PowerGaN tape drawing (dimensions are in mm)**



Symbol	Spec.
E	1.75± 0.10
F	7.50± 0.10
P_2	2.00± 0.10
D	$1.50^{+0.1}_{0}$
D_1	1.50MIN
P_0	4.00± 0.10
10P_0	40.0± 0.20

Symbol	Spec.
W	$16.00^{+0.3}_{-0.2}$
P	8.00± 0.10
A_0	6.90± 0.10
B_0	10.50± 0.10
K_0	2.70± 0.10
t	0.30± 0.05
R	0.50TYP

069909_typeL_GaN_12

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Revision history

Table 8. **Document revision history**

Date	Revision	Changes
16-Jun-2025	1	First release.
18-Jul-2025	2	Updated Applications and Description.

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