SM802123

ClockWorks™ 125MHz/25MHz Ultra-Low Jitter, LVCMOS Frequency Synthesizer

General Description

The SM802123 is a member of the ClockWorks™ family of devices from Micrel and provides an extremely low-noise timing solution. It is based upon a unique patented RotaryWave® architecture that provides very-low phase noise.

The device operates from a 2.5V or 3.3V power supply and synthesizes 16 LVCMOS output clocks, eight at 125MHz and eight at 25MHz. The SM802123 accepts a 25MHz LVCMOS reference input.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

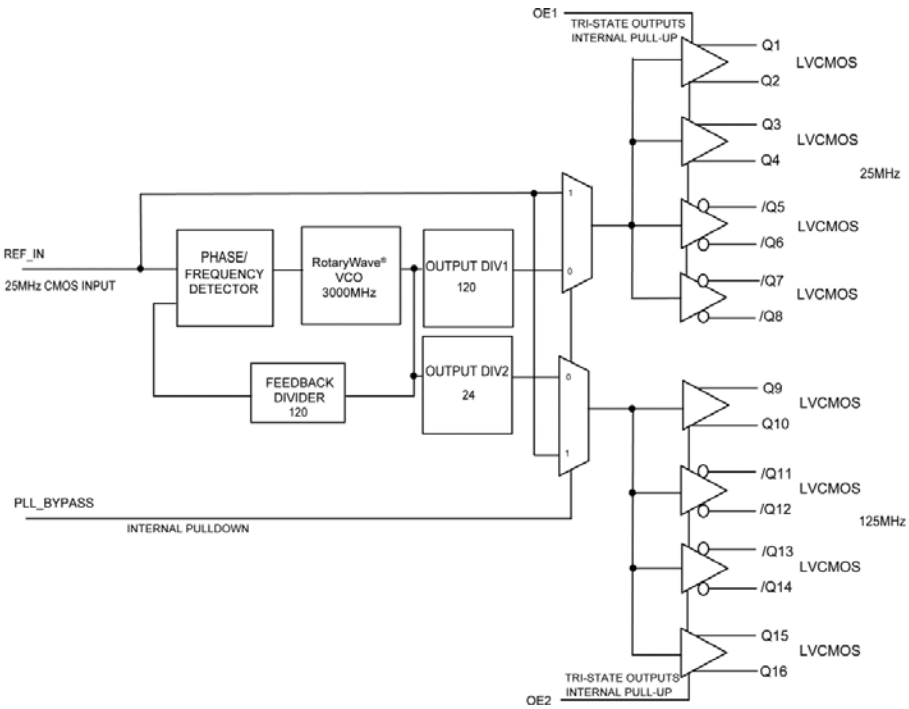
Features

- Generates eight LVCMOS output clocks at 125MHz and eight LVCMOS output clocks at 25MHz
- 2.5V or 3.3V operating range
- Typical phase jitter @ 125MHz (1.875MHz to 20MHz): 115fs
- Industrial temperature range
- Green, RoHS, and PFOS compliant
- Available in 44-pin 7mm × 7mm QFN package

Applications

- Gigabit Ethernet – (GbE)

Block Diagram Top Level Schematic



ClockWorks is a trademark of Micrel, Inc
RotaryWave is a registered trademark of Multigig, Inc.

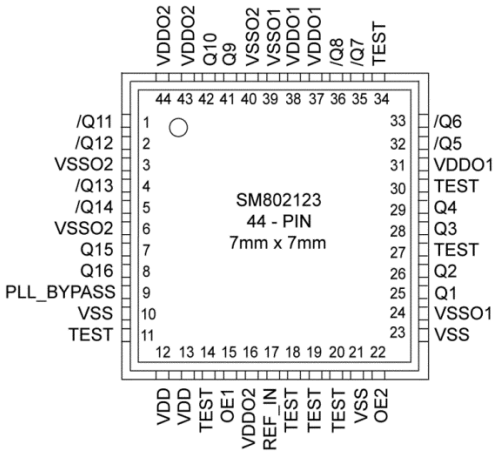
Ordering Information

Part Number	Marking	Shipping	Junction Temperature Range[1]	Package
SM802123UMG	802123	Tray	–40°C to +85°C	44-Pin QFN
SM802123UMGTR	802123	Tape and Reel	–40°C to +85°C	44-Pin QFN

Note:

1. Devices are Green, RoHS, and PFOS compliant.

Pin Configuration



44-Pin QFN
(Top View)

Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
25, 26 28, 29 32, 33 35, 36	Q1, Q2 Q3, Q4 /Q5, /Q6 /Q7, /Q8	O, (DIF)	LVCMOS	Clock Outputs from Bank 1 (25MHz) .
41, 42 1, 2 4, 5 7, 8	Q9, Q10 /Q11, /Q12 /Q13, /Q14 Q15, Q16	O, (DIF)	LVCMOS	Clock Outputs from Bank 2 (125MHz).
31, 37, 38	VDDO1	PWR		Power Supply for the Outputs on Bank 1.
43, 44, 16	VDDO2	PWR		Power Supply for the Outputs on Bank 2.
24, 39	VSSO1	PWR		Power Supply Ground for the Outputs on Bank 1.
3, 6, 40	VSSO2	PWR		Power Supply Ground for the Outputs on Bank 2.
11, 14, 18, 19, 20, 27, 30, 34	TEST			Factory Test Pins. Do not connect anything to these pins.
12, 13	VDD	PWR		Core Power Supply.
10, 21, 23	VSS (Exposed Pad)	PWR		Core Power Supply Ground. The exposed pad must be connected to the VSS ground plane.

Pin Description (Continued)

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
17	REF_IN	I, (SE)	LVCMOS	Reference Clock Input
9	PLL_BYPASS	I, (SE)	LVCMOS	PLL Bypass, Selects Output Source 0 = Normal PLL Operation 1 = Output from Input Reference Clock 45KΩ Pull-Down
15	OE1	I, (SE)	LVCMOS	Output Enable, Q1-/Q8 disables to tri-state, 0 = Disabled, 1 = Enabled, 45KΩ Pull-Up
22	OE2	I, (SE)	LVCMOS	Output Enable, Q9-Q16 disables to tri-state, 0 = Disabled, 1 = Enabled, 45KΩ Pull-Up

Truth Table

OE1/2	OUTPUTS
0	Tri-State
1	LVCMOS

Absolute Maximum Ratings(1)

Supply Voltage (V_{DD}, $V_{DDO1/2}$) ..... +4.6V
Input Voltage (V_{IN})..... –0.5V to V_{DD}+0.5V
Lead Temperature (soldering, 20s.)..... 260°C
Case Temperature ..... 115°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings(2)

Supply Voltage ($V_{DD,}$ $V_{DDO1/2}$)..... +2.375V to +3.465V
Ambient Temperature (T_A)..... –40°C to +85°C
Junction Thermal Resistance(3)
QFN (θ_{JA})
Still-Air ..... 24°C/W
QFN (ψ_{JB})
Junction-to-Board ..... 8°C/W

DC Electrical Characteristics(4)

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{DD,}$ $V_{DDO1/2}$	3.3V Operating Voltage	V_{DDO1} = V_{DDO2}	3.135	3.3	3.465	V
	2.5V Operating Voltage	V_{DDO1} = V_{DDO2}	2.375	2.5	2.625	V
I_{DD}	Total supply current	Outputs floating		130	170	mA

LVCMOS INPUT (OE1, OE2, PLL_BYPASS) DC Electrical Characteristics(4)

V_{DD} = 3.3V ±5%, or 2.5V ±5%, T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IN}	Input Low Voltage		–0.3		0.8	V
I_{IH}	Input High Current	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V, V_{IN} = 0V	–150			µA

LVCMOS OUTPUT DC Electrical Characteristics(4)

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

T_A = –40°C to +85°C. R_L = 50Ω to V_{DDO}/2

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	Figure 4	V_{DDO} – 0.7			V
V_{OL}	Output Low Voltage	Figure 4			0.6	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.
4. The circuit is designed to meet the AC and DC specifications shown in the above table after thermal equilibrium has been established.

REF_IN DC Electrical Characteristics[4]

V_{DD} = 3.3V ±5%, or 2.5V ±5%, T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		1.1		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		–0.3		0.6	V
I_{IN}	Input Current	V_{IN} = 0V to V_{DD}	–5		5	µA

AC Electrical Characteristics[4, 5]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

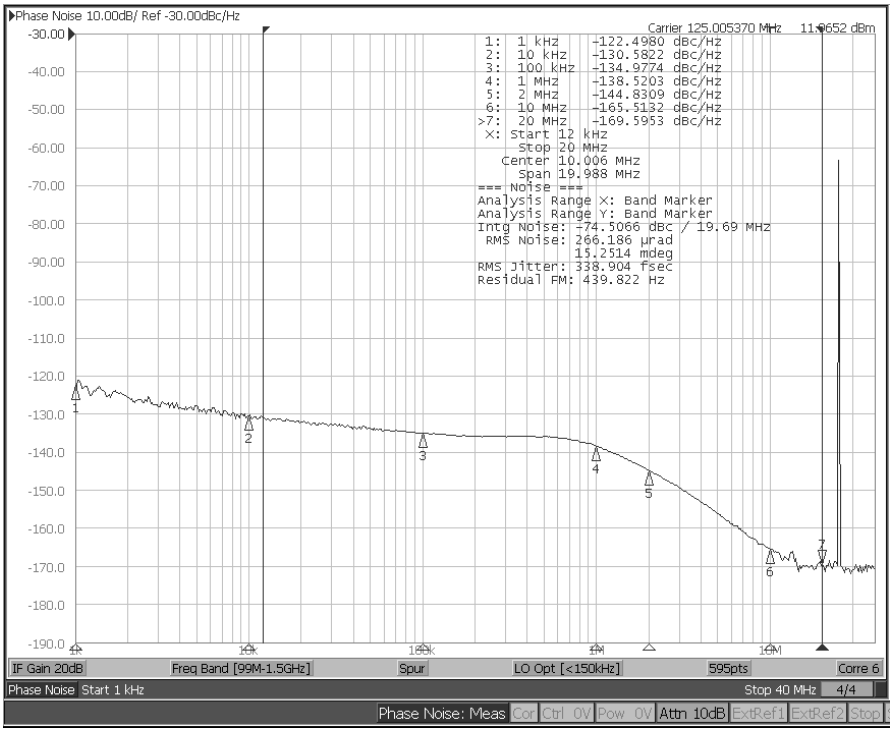
T_A = –40°C to +85°C. R_L = 50Ω to V_{DDO}/2

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{OUT}	Output Frequency	Q1 – /Q8		25		MHz
		Q9 – Q16		125		
T_R/T_F	LVCMOS Output Rise/Fall Time	20% – 80%, Fig. 2	100	200	500	ps
ODC	Output Duty Cycle		45	50	55	%
T_{LOCK}	PLL Lock Time				20	ms
$T_{jit}(\varnothing)$	RMS Phase Jitter [6] (Output = 25MHz)	Integration Range:(12kHz – 5MHz) 5MHz limited by phase-noise system.		315		fs
	RMS Phase Jitter [6] (Output = 125MHz)	Integration Range:(12kHz – 20MHz)		340		fs
		Integration Range:(1.875MHz – 20MHz)		115		fs
	Spurious Noise Components	25MHz		–64		dBc

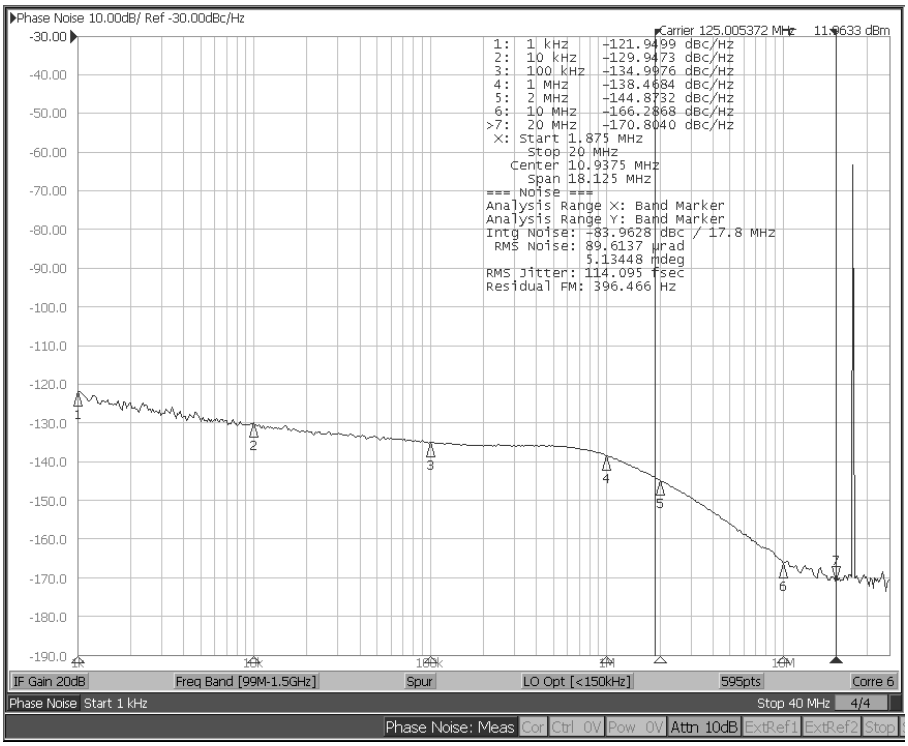
Notes:

1. All phase-noise measurements were taken with an Agilent 5052B phase-noise system.
2. REF_IN driven with a low-noise source ClockWorks™ SM802001 programmed for a 25MHz CMOS output. Phase noise will track the input phase noise up to about 1MHz offset frequency.

Phase Noise Plots

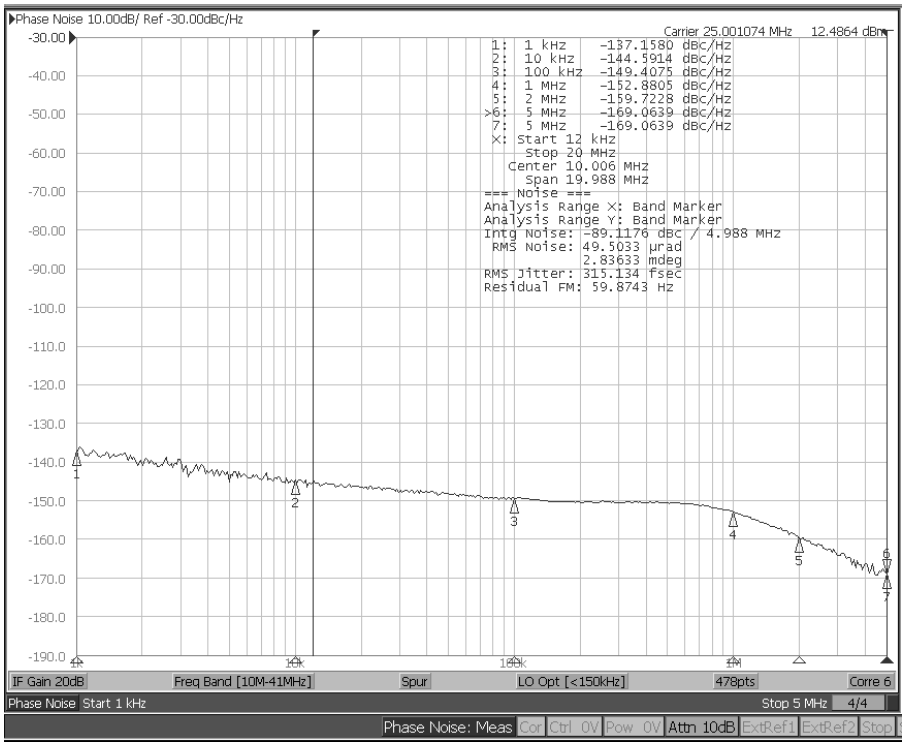


125MHz LVCMOS Integrated Jitter 12kHz – 20MHz 339fs

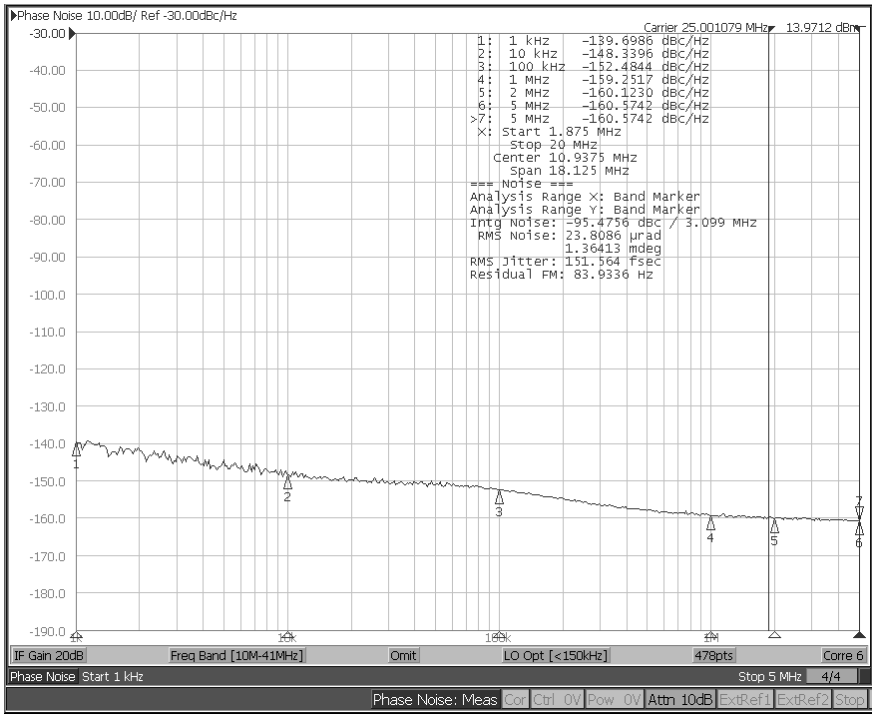


125MHz LVCMOS Integrated Jitter 1.875MHz – 20MHz 114fs

Phase Noise Plots (Continued)

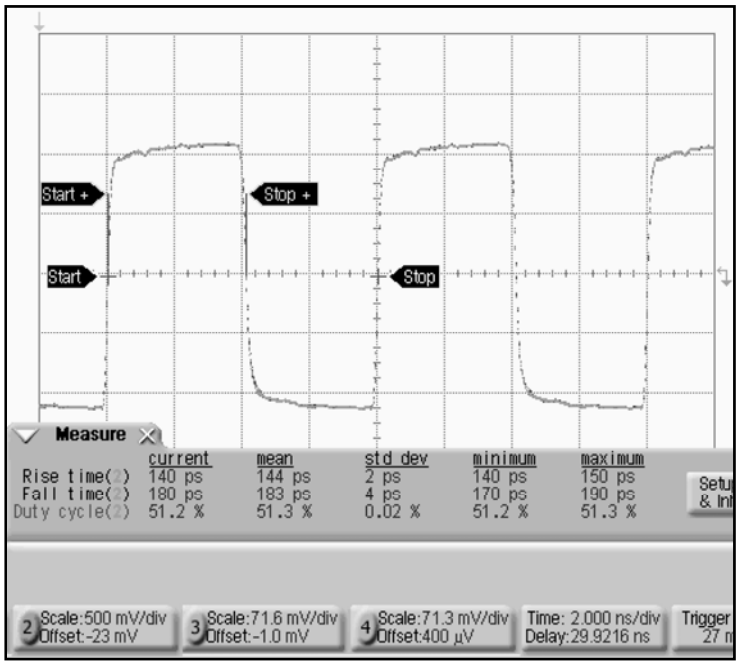


25MHz LVCMOS Integrated Jitter 12kHz – 5MHz 315fs

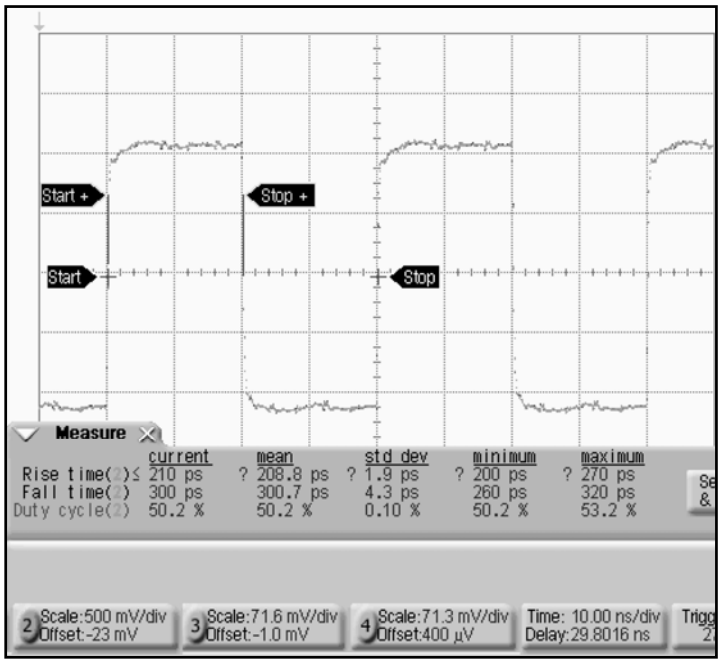


Input Source (25MHz LVCMOS) Programmed from a Clockworks™ Part

Phase Noise Plots (Continued)



125MHz LVCMOS Output Waveform



25MHz LVCMOS Output Waveform

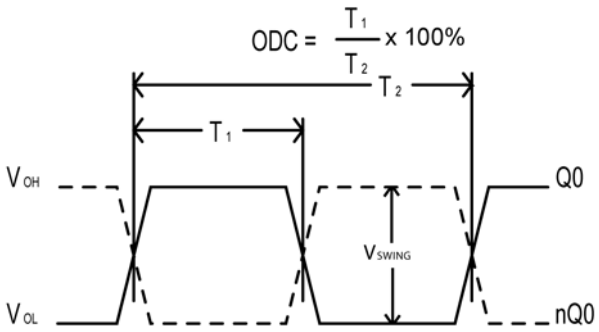


Figure 1. Duty Cycle TIming

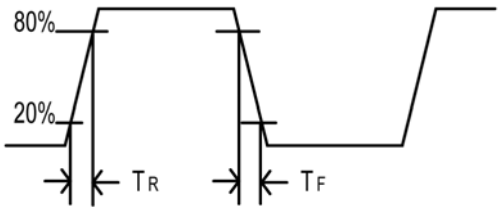


Figure 2. All Outputs Rise/Fall Time

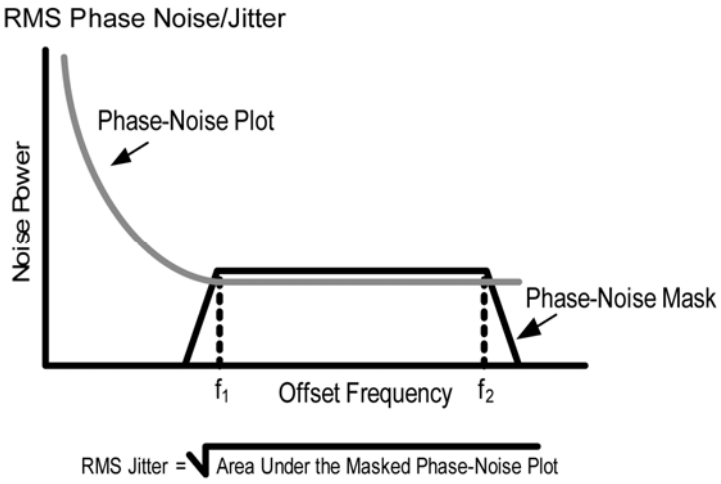


Figure 3. RMS Phase Noise/Jitter

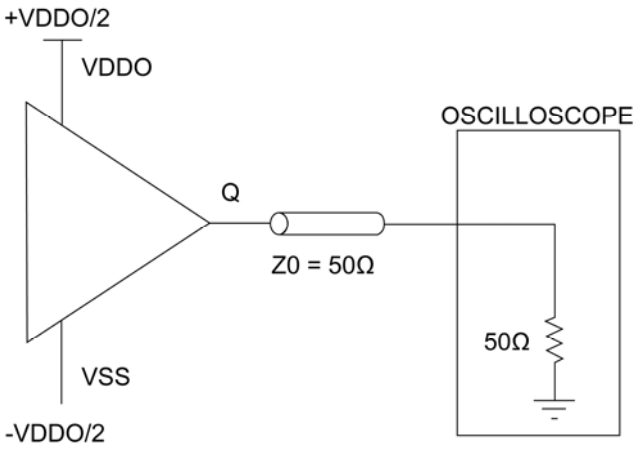
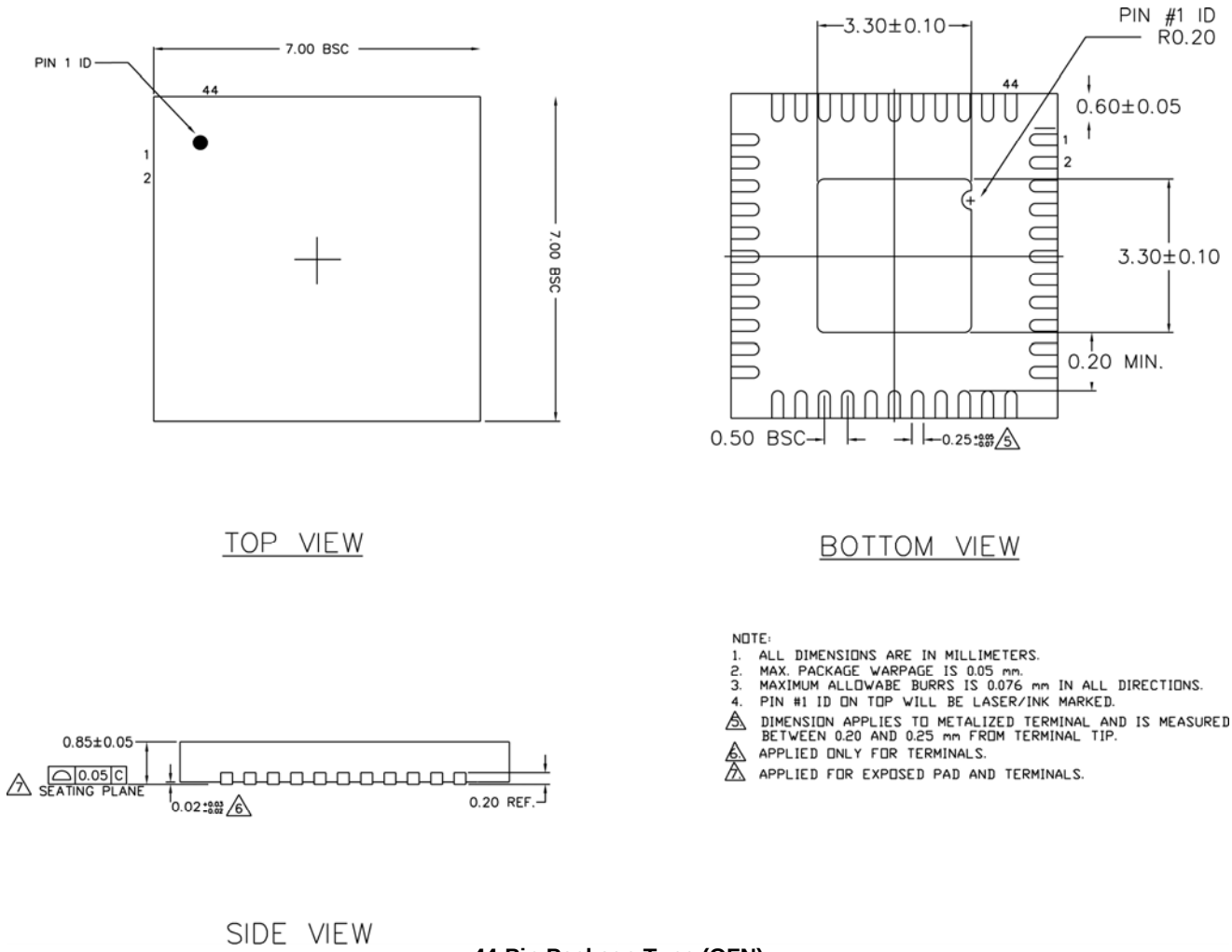


Figure 4. LVCMOS Output Load and Test Circuit

Package Information



44-Pin Package Type (QFN)

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Revision Template History

Date	Change Description/Edits by:	Rev.
8/4/10	Added new paragraph to disclaimer in boiler plate. Per Colin Sturt. M.Galvan	14

HBW Datasheet Revision History

Part Number:

Initial Release Date:

Rev.	Date	Revisions	Reason	Engineer
A				