

NTLJS2103P

MOSFET – Power, Single, P-Channel, μ Cool, WDFN, 2x2 mm -12 V, -7.7 A



ON Semiconductor®

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Features

- Recommended Replacement Device – NTLUS3A40P
- WDFN Package Provides Exposed Drain Pad for Excellent Thermal Conduction
- 2x2 mm Footprint Same as SC-88 Package
- Lowest $R_{DS(on)}$ Solution in 2x2 mm Package
- 1.2 V $R_{DS(on)}$ Rating for Operation at Low Voltage Logic Level Gate Drive
- Low Profile (< 0.8 mm) for Easy Fit in Thin Environments
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

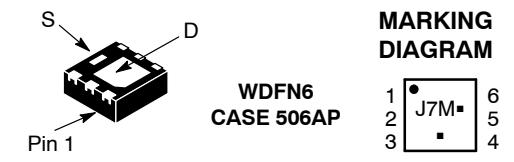
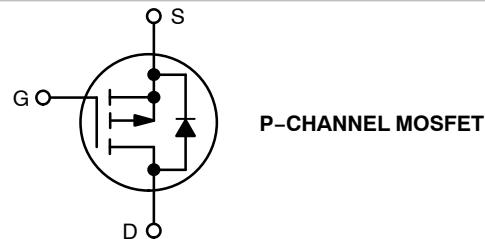
- High Side Load Switch
- DC-DC Converters (Buck and Boost Circuits)
- Optimized for Battery and Load Management Applications in Portable Equipment
- Li-Ion Battery Linear Mode Charging

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

| Parameter | Symbol | Value | Unit |
|---|-----------------------------------|-----------------|------|
| Drain-to-Source Voltage | V _{DSS} | -12 | V |
| Gate-to-Source Voltage | V _{GS} | ± 8.0 | V |
| Continuous Drain Current (Note 1) | I _D | -5.9 | A |
| | | -4.2 | |
| | | -7.7 | |
| Power Dissipation (Note 1) | P _D | 1.9 | W |
| | | 3.3 | |
| Continuous Drain Current (Note 2) | I _D | -3.5 | A |
| | | -2.5 | |
| Power Dissipation (Note 2) | P _D | 0.7 | W |
| Pulsed Drain Current | t _p = 10 μ s | I _{DM} | -24 |
| Operating Junction and Storage Temperature | T _J , T _{STG} | -55 to 150 | °C |
| Source Current (Body Diode) (Note 2) | I _S | -2.7 | A |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | T _L | 260 | °C |

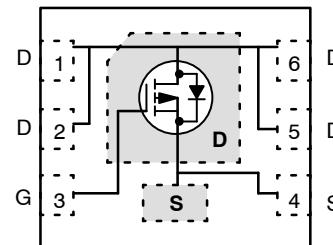
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

| V _{(BR)DSS} | R _{DS(on)} TYP | I _D MAX (Note 1) |
|----------------------|-------------------------|-----------------------------|
| -12 V | 25 m Ω @ -4.5 V | -5.9 A |
| | 35 m Ω @ -2.5 V | -5.3 A |
| | 45 m Ω @ -1.8 V | -2.0 A |
| | 60 m Ω @ -1.5 V | -1.0 A |
| | 95 m Ω @ -1.2 V | -0.2 A |



J7 = Specific Device Code
M = Date Code
- = Pb-Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|---------------|-----------------|-----------------------|
| NTLJS2103PTAG | WDFN6 (Pb-Free) | 3000/Tape & Reel |
| NTLJS2103PTBG | WDFN6 (Pb-Free) | 3000/Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTLJS2103P

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface Mounted on FR4 Board using the minimum recommended pad size, (30 mm², 2 oz Cu).

THERMAL RESISTANCE RATINGS

| Parameter | Symbol | Max | Unit |
|---|-----------------|-----|-----------------------------|
| Junction-to-Ambient – Steady State (Note 3) | $R_{\theta JA}$ | 65 | $^{\circ}\text{C}/\text{W}$ |
| Junction-to-Ambient – $t \leq 5 \text{ s}$ (Note 3) | $R_{\theta JA}$ | 38 | |
| Junction-to-Ambient – Steady State Min Pad (Note 4) | $R_{\theta JA}$ | 180 | |

3. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).

4. Surface Mounted on FR4 Board using the minimum recommended pad size (30 mm², 2 oz Cu).MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise noted)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|-----------|--------|-----------------|-----|-----|-----|------|
|-----------|--------|-----------------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | | |
|---|---------------------------------|--|----------------------------|------|-----------|------------------------------|
| Drain-to-Source Breakdown Voltage | $V_{(\text{BR})\text{DSS}}$ | $V_{\text{GS}} = 0 \text{ V}, I_D = -250 \mu\text{A}$ | -12 | | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | $V_{(\text{BR})\text{DSS}/T_J}$ | $I_D = -250 \mu\text{A}$, Ref to 25°C | | -8.0 | | $\text{mV}/^{\circ}\text{C}$ |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{\text{DS}} = -12 \text{ V}, V_{\text{GS}} = 0 \text{ V}$ | $T_J = 25^{\circ}\text{C}$ | | -1.0 | μA |
| | | | $T_J = 85^{\circ}\text{C}$ | | -5.0 | μA |
| Gate-to-Source Leakage Current | I_{GSS} | $V_{\text{DS}} = 0 \text{ V}, V_{\text{GS}} = \pm 8.0 \text{ V}$ | | | ± 0.1 | μA |

ON CHARACTERISTICS (Note 5)

| | | | | | | |
|---|--------------------------------|---|------|-----|------|------------------------------|
| Gate Threshold Voltage | $V_{\text{GS}(\text{TH})}$ | $V_{\text{GS}} = V_{\text{DS}}, I_D = -250 \mu\text{A}$ | -0.3 | | -0.8 | V |
| Negative Gate Threshold Temperature Coefficient | $V_{\text{GS}(\text{TH})/T_J}$ | | | 2.6 | | $\text{mV}/^{\circ}\text{C}$ |
| Drain-to-Source On-Resistance | $R_{\text{DS}(\text{on})}$ | $V_{\text{GS}} = -4.5, I_D = -5.9 \text{ A}$ | | 25 | 40 | $\text{m}\Omega$ |
| | | $V_{\text{GS}} = -4.5, I_D = -3.0 \text{ A}$ | | 25 | 40 | |
| | | $V_{\text{GS}} = -2.5, I_D = -5.3 \text{ A}$ | | 35 | 50 | |
| | | $V_{\text{GS}} = -2.5, I_D = -3.0 \text{ A}$ | | 35 | 50 | |
| | | $V_{\text{GS}} = -1.8, I_D = -2.0 \text{ A}$ | | 45 | 75 | |
| | | $V_{\text{GS}} = -1.5, I_D = -1.0 \text{ A}$ | | 60 | 100 | |
| | | $V_{\text{GS}} = -1.2, I_D = -200 \text{ mA}$ | | 95 | 400 | |
| Forward Transconductance | g_{FS} | $V_{\text{DS}} = -6.0 \text{ V}, I_D = -2.0 \text{ A}$ | | 8.8 | | S |

CHARGES, CAPACITANCES AND GATE RESISTANCE

| | | | | | | |
|------------------------------|----------------------------|--|--|------|----|----------|
| Input Capacitance | C_{ISS} | $V_{\text{GS}} = 0 \text{ V}, f = 1.0 \text{ MHz}, V_{\text{DS}} = -6.0 \text{ V}$ | | 1157 | | pF |
| Output Capacitance | C_{OSS} | | | 300 | | |
| Reverse Transfer Capacitance | C_{RSS} | | | 200 | | |
| Total Gate Charge | $Q_{\text{G}(\text{TOT})}$ | $V_{\text{GS}} = -4.5 \text{ V}, V_{\text{DS}} = -9.6 \text{ V}, I_D = -5.9 \text{ A}$ | | 12.8 | 15 | nC |
| Threshold Gate Charge | $Q_{\text{G}(\text{TH})}$ | | | 0.4 | | |
| Gate-to-Source Charge | Q_{GS} | | | 1.6 | | |
| Gate-to-Drain Charge | Q_{GD} | | | 3.6 | | |
| Gate Resistance | R_{G} | | | 15.7 | | Ω |

SWITCHING CHARACTERISTICS (Note 6)

| | | | | | | |
|---------------------|----------------------------|---|--|-----|--|----|
| Turn-On Delay Time | $t_{\text{d}(\text{ON})}$ | $V_{\text{GS}} = -4.5 \text{ V}, V_{\text{DD}} = -8.0 \text{ V}, I_D = -5.9 \text{ A}, R_{\text{G}} = 2.0 \Omega$ | | 8.0 | | ns |
| Rise Time | t_r | | | 27 | | |
| Turn-Off Delay Time | $t_{\text{d}(\text{OFF})}$ | | | 74 | | |
| Fall Time | t_f | | | 88 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | | |
|--------------------------|-----------------|--|----------------------------|--|------|-----|----|
| Forward Recovery Voltage | V_{SD} | $V_{\text{GS}} = 0 \text{ V}, I_S = -1.0 \text{ A}$ | $T_J = 25^{\circ}\text{C}$ | | 0.62 | 1.0 | V |
| | | | $T_J = 85^{\circ}\text{C}$ | | 0.56 | | |
| Reverse Recovery Time | t_{RR} | $V_{\text{GS}} = 0 \text{ V}, dI_{\text{SD}}/dt = 100 \text{ A}/\mu\text{s}, I_S = -1.0 \text{ A}$ | | | 27 | 50 | ns |
| Charge Time | t_a | | | | 10 | | |
| Discharge Time | t_b | | | | 17 | | |
| Reverse Recovery Time | Q_{RR} | | | | 14 | | nC |

5. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

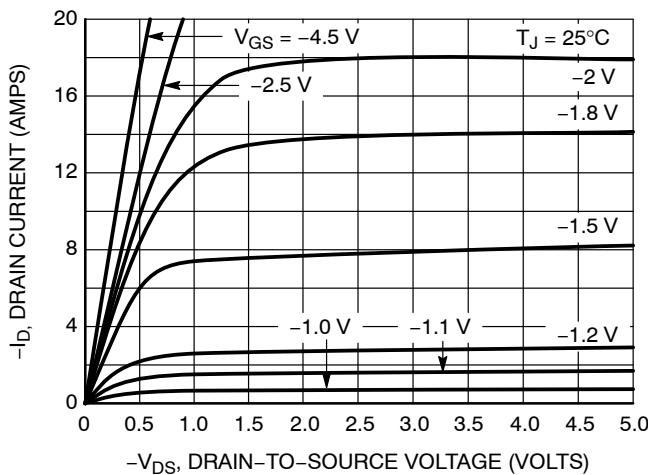


Figure 1. On-Region Characteristics

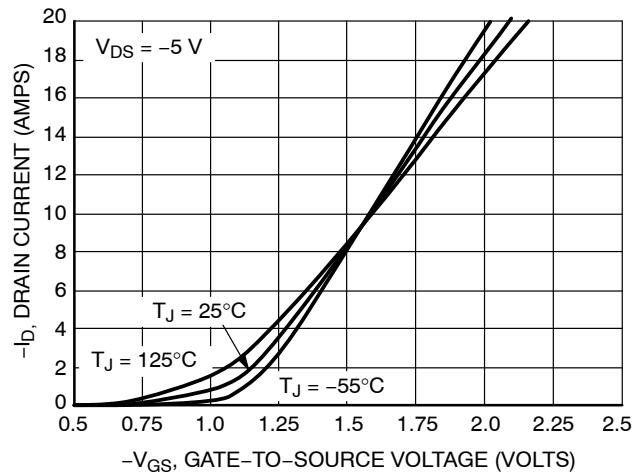


Figure 2. Transfer Characteristics

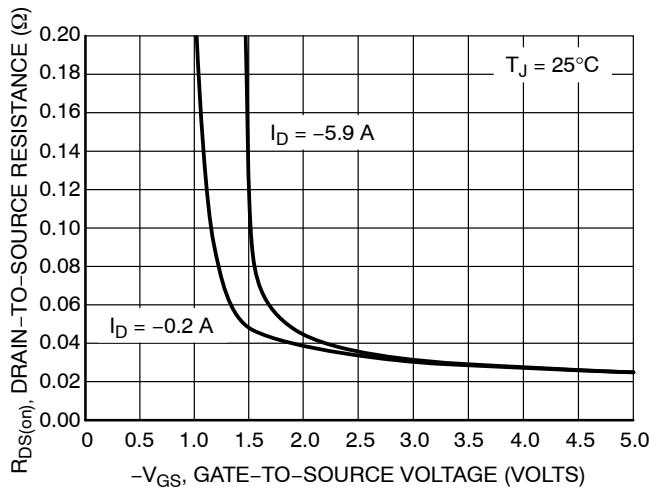


Figure 3. On-Resistance vs. Gate-to-Source Voltage

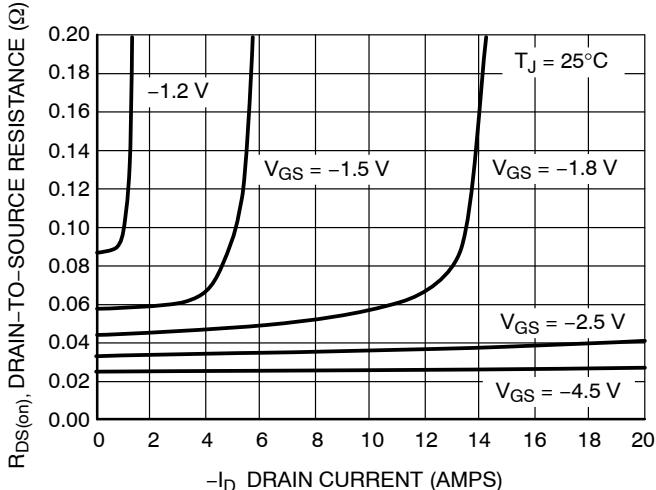


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

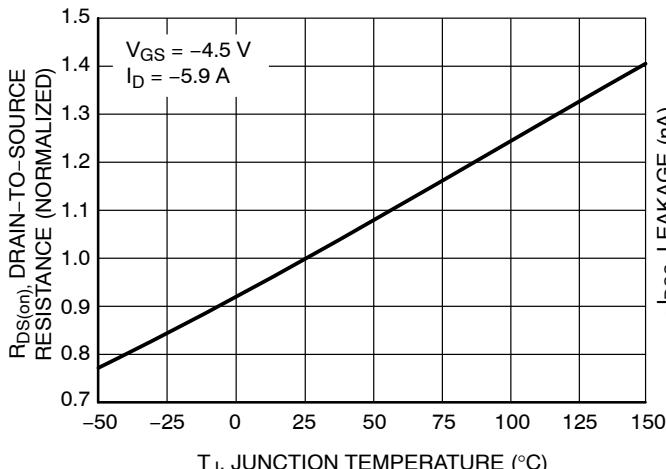


Figure 5. On-Resistance Variation with Temperature

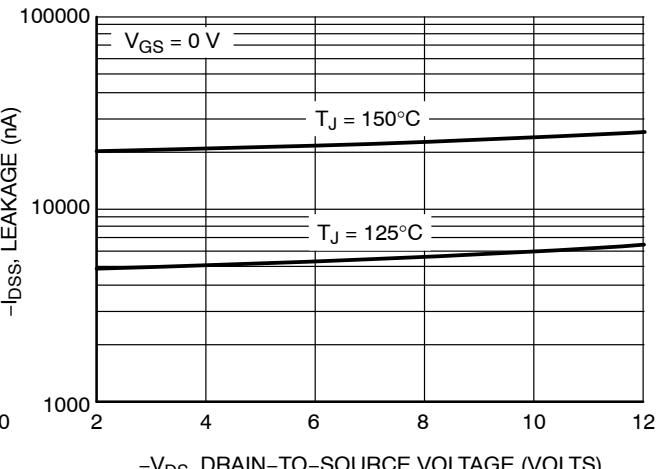


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

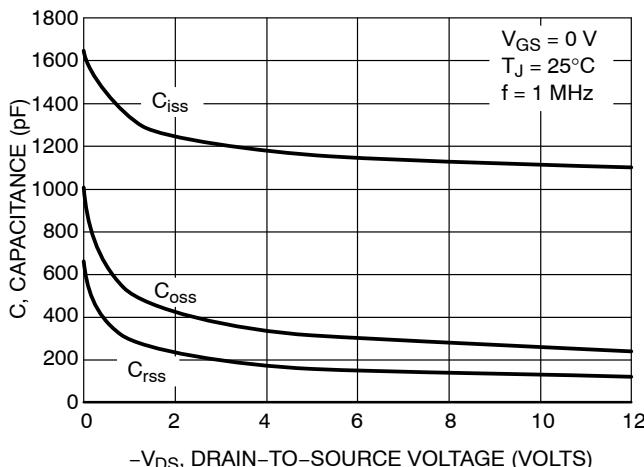


Figure 7. Capacitance Variation

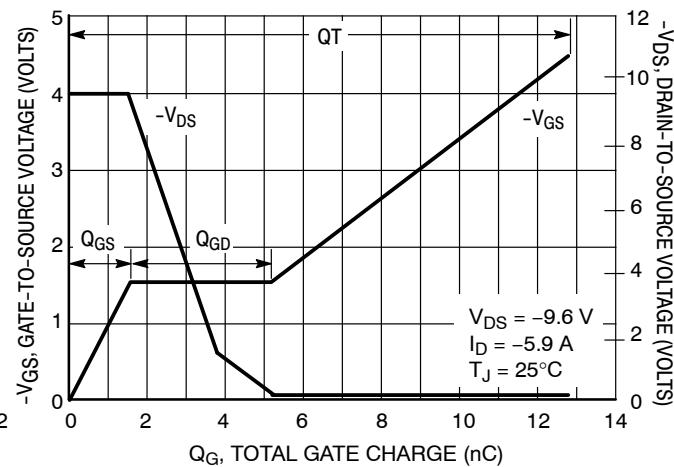


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

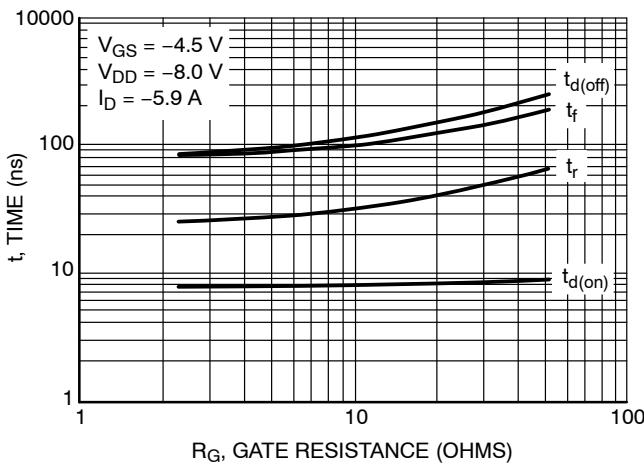


Figure 9. Resistive Switching Time Variation versus Gate Resistance

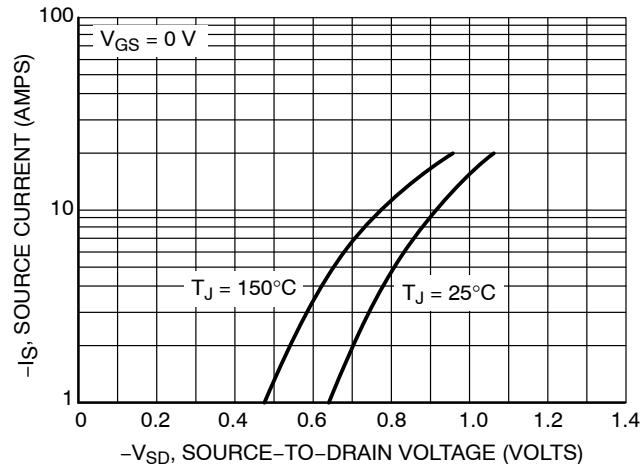


Figure 10. Diode Forward Voltage vs. Current

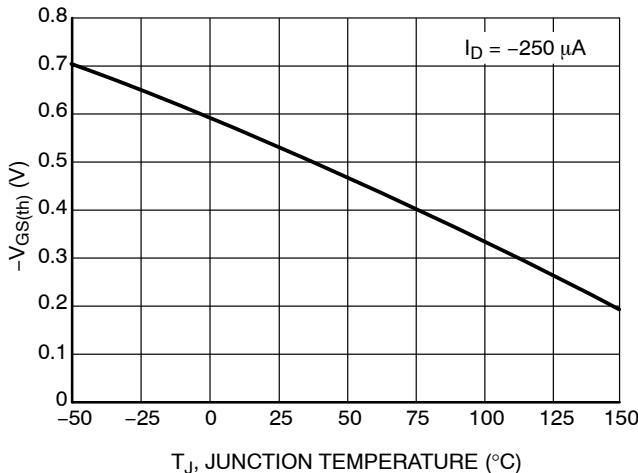


Figure 11. Threshold Voltage

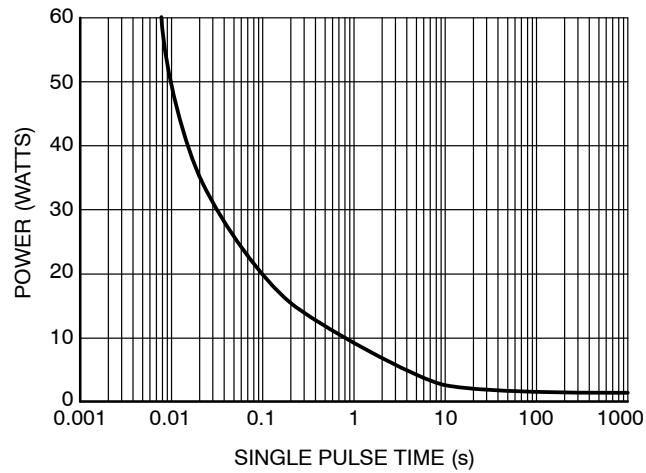


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

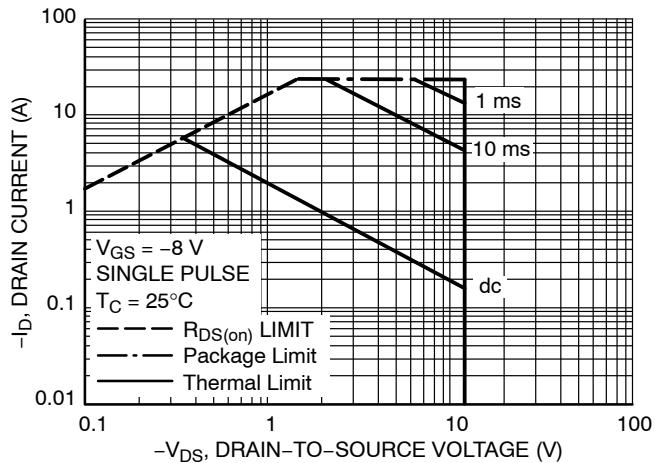


Figure 13. Maximum Rated Forward Biased Safe Operating Area

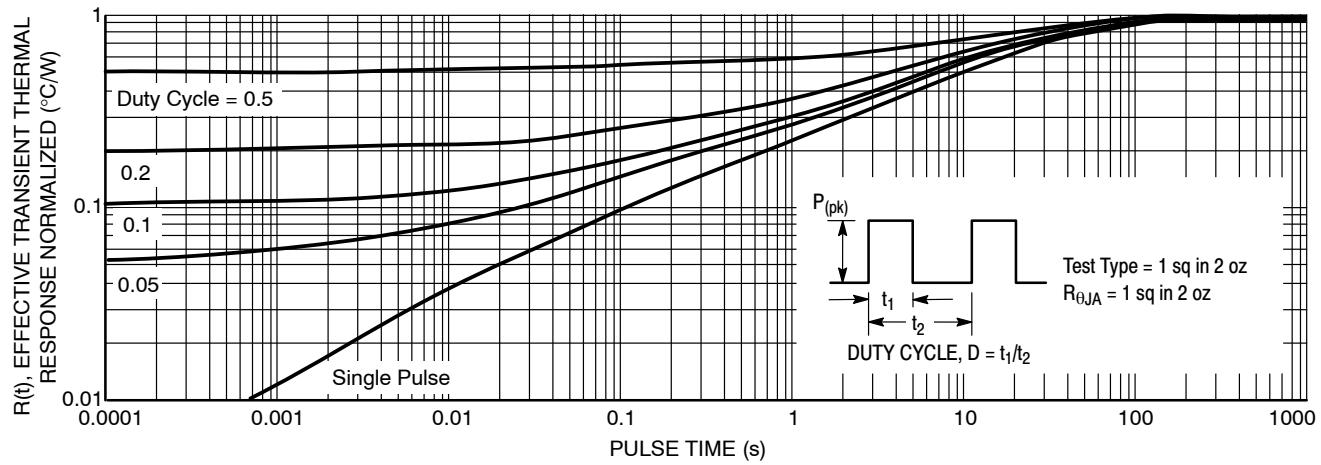
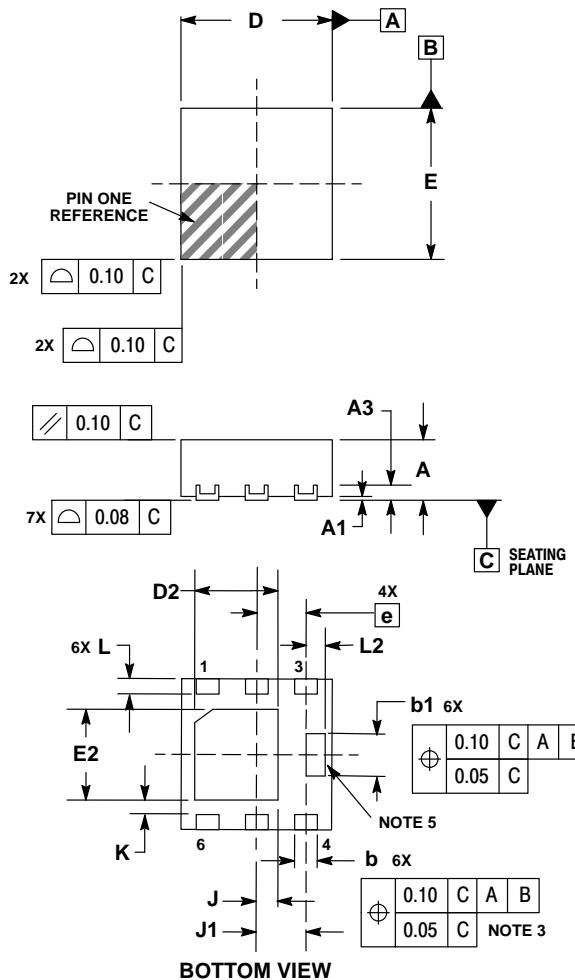


Figure 14. FET Thermal Response

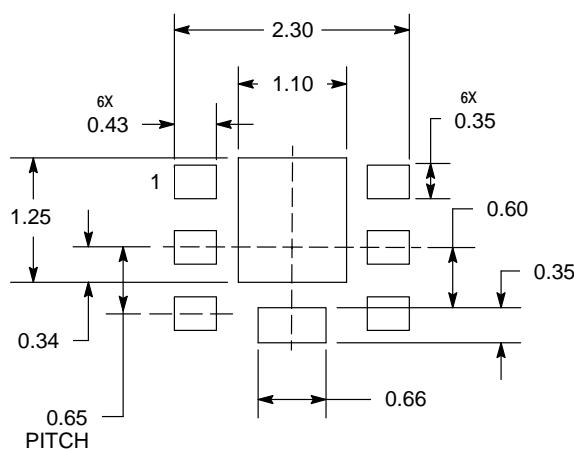


SCALE 4:1



STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. Emitter
5. COLLECTOR
6. COLLECTOR



| | | |
|------------------|-----------------------|---|
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| DESCRIPTION: | 6 PIN WDFN 2X2, 0.65P | PAGE 1 OF 1 |

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