

Product Summary

BV _{DSS}	R _{D(S)}	I _D T _A = +25°C
30V	460mΩ @ V _{GS} = 4.5V	1.3A
	560mΩ @ V _{GS} = 2.5V	1.25A

Description and Applications

This new generation MOSFET is designed to minimize the on-state resistance (R_{D(S)}) yet maintain superior switching performance, making it ideal for high-efficiency power-management applications.

- Power-management functions
- Backlighting
- Load switches

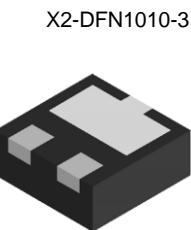
Features and Benefits

- Low On-Resistance
- Low Input/Output Leakage
- Fast Switching Speed
- ESD Protected Gate
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](#) or your local Diodes representative.

<https://www.diodes.com/quality/product-definitions/>

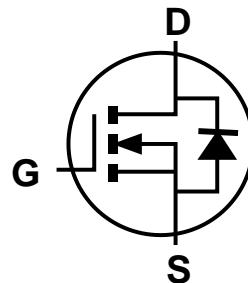
Mechanical Data

- Package: X2-DFN1010-3
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish — NiPdAu over Copper Leadframe; Solderable per MIL-STD-202, Method 208 ^④
- Weight: 0.0015 grams (Approximate)

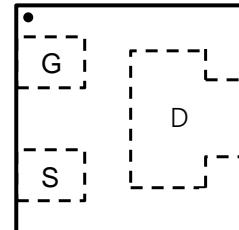


X2-DFN1010-3

Bottom View



Equivalent Circuit



Pin-Out Top View

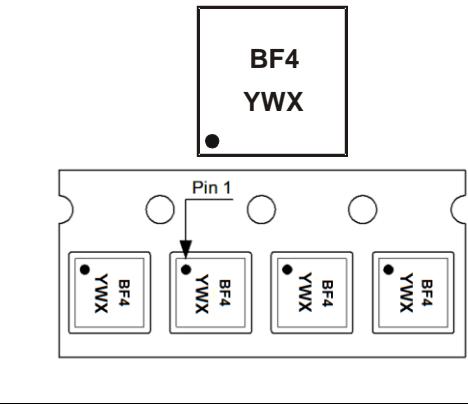
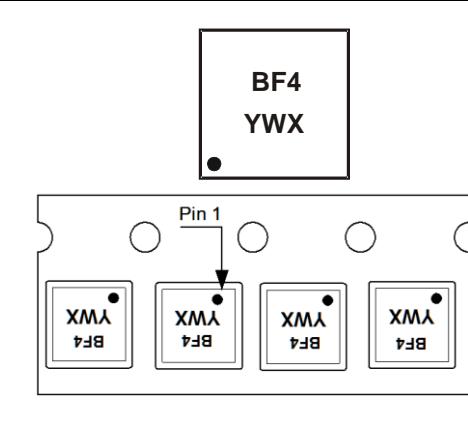
Ordering Information (Note 4)

Orderable Part Number	Package	Tape Width (mm)	Tape Pitch (mm)	Packing	
				Qty.	Carrier
DMN3731UFR4-7	X2-DFN1010-3	8	4	5000	Tape & Reel
DMN3731UFR4-7R	X2-DFN1010-3	8	4	5000	Tape & Reel

Notes:

- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information

DMN3731UFR4-7		<p>BF4 = Product Type Marking Code YWX = Date Code Marking Y = Year (ex: 4 = 2024) W = Week (ex: a = Week 27; z Represents Week 52 and 53) X = Internal Code (ex: U = Monday)</p>
DMN3731UFR4-7R		<p>BF4 = Product Type Marking Code YWX = Date Code Marking Y = Year (ex: 4 = 2024) W = Week (ex: a = Week 27; z Represents Week 52 and 53) X = Internal Code (ex: U = Monday)</p>

Date Code Key

Year	2021	-	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033
Code	1	-	4	5	6	7	8	9	0	1	2	3

Week	1-26	27-52	53
Code	A-Z	a-z	z

Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Code	T	U	V	W	X	Y	Z

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	± 8	V
Continuous Drain Current (Note 6) $V_{GS} = 4.5\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +100^\circ\text{C}$	I_D	1.3 0.84	A
Maximum Continuous Body Diode Forward Current (Note 6)			I_S	1.4	A
Pulsed Drain Current (10 μs Pulse, Duty Cycle = 1%)			I_{DM}	3.3	A

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)		P_D	0.67	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	187	$^\circ\text{C/W}$
Total Power Dissipation (Note 6)		P_D	1.32	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	95	$^\circ\text{C/W}$
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

 Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	—	—	V	$V_{GS} = 0\text{V}, I_D = 10\mu\text{A}$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$
		—	—	100	nA	$V_{DS} = 12\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	—	—	3	μA	$V_{GS} = \pm 8\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(\text{TH})}$	0.45	—	0.95	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(\text{ON})}$	—	210	460	$\text{m}\Omega$	$V_{GS} = 4.5\text{V}, I_D = 200\text{mA}$
		—	225	560		$V_{GS} = 2.5\text{V}, I_D = 100\text{mA}$
		—	250	730		$V_{GS} = 1.8\text{V}, I_D = 75\text{mA}$
Diode Forward Voltage	V_{SD}	—	0.7	1.2	V	$V_{GS} = 0\text{V}, I_S = 300\text{mA}$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	73	—	pF	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	—	7.2	—		
Reverse Transfer Capacitance	C_{rss}	—	5	—		
Gate Resistance	R_g	—	902	—	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge	Q_g	—	5.5	—	nC	$V_{GS} = 4.5\text{V}, V_{DS} = 15\text{V}, I_D = 1\text{A}$
Gate-Source Charge	Q_{gs}	—	0.8	—		
Gate-Drain Charge	Q_{gd}	—	1.4	—		
Turn-On Delay Time	$t_{D(\text{ON})}$	—	2.5	—	ns	$V_{DS} = 10\text{V}, I_D = 1\text{A}$ $V_{GS} = 10\text{V}, R_G = 6\Omega$
Turn-On Rise Time	t_R	—	3.1	—		
Turn-Off Delay Time	$t_{D(\text{OFF})}$	—	477	—		
Turn-Off Fall Time	t_F	—	123	—		
Reverse Recovery Time	t_{RR}	—	59	—	ns	$I_F = 1\text{A}, di/dt = 100\text{A}/\mu\text{s}$
Reverse Recovery Charge	Q_{RR}	—	25	—	nC	

Notes:

5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to production testing.

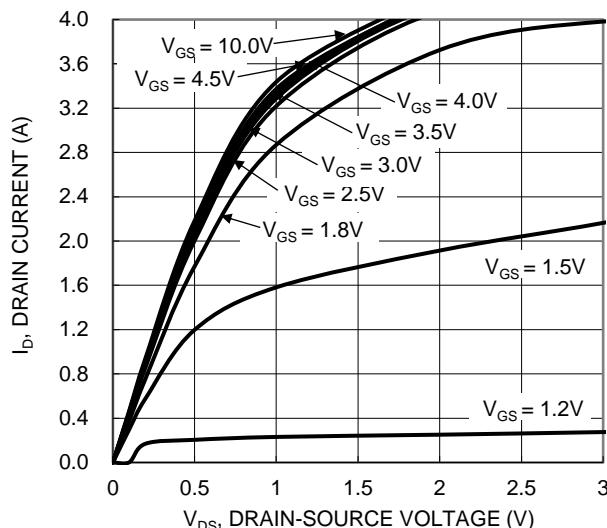


Figure 1. Typical Output Characteristic

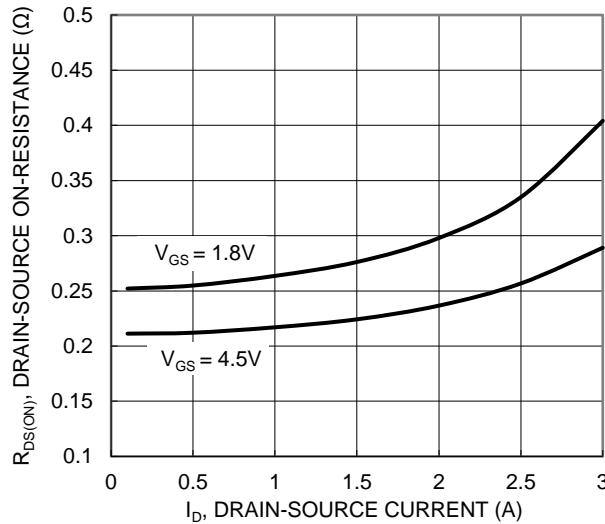


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

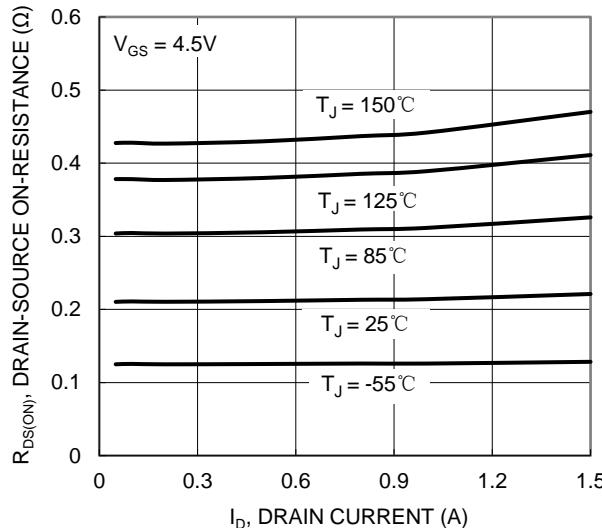


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

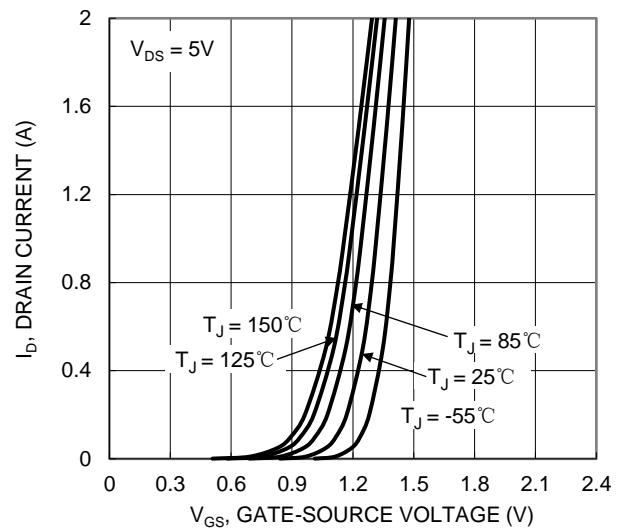


Figure 2. Typical Transfer Characteristic

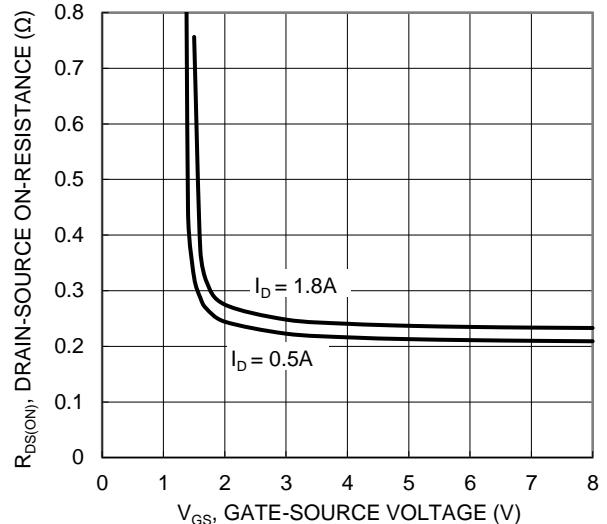


Figure 4. Typical Transfer Characteristic

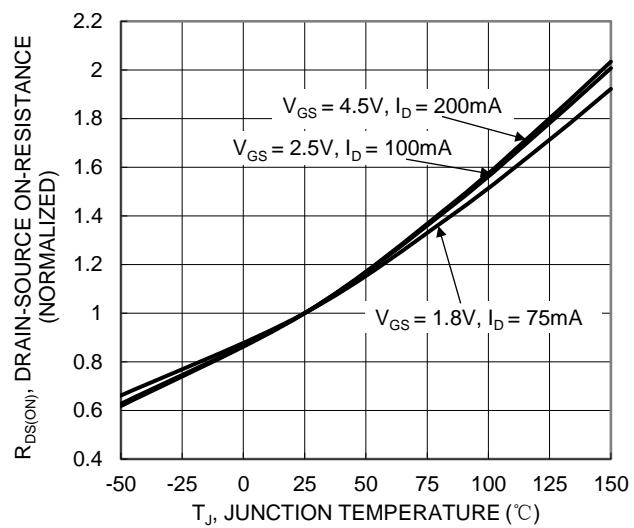


Figure 6. On-Resistance Variation with Junction Temperature

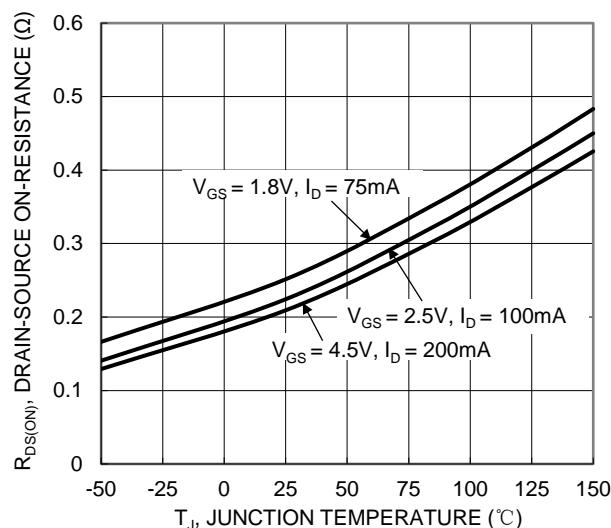


Figure 7. On-Resistance Variation with Junction Temperature

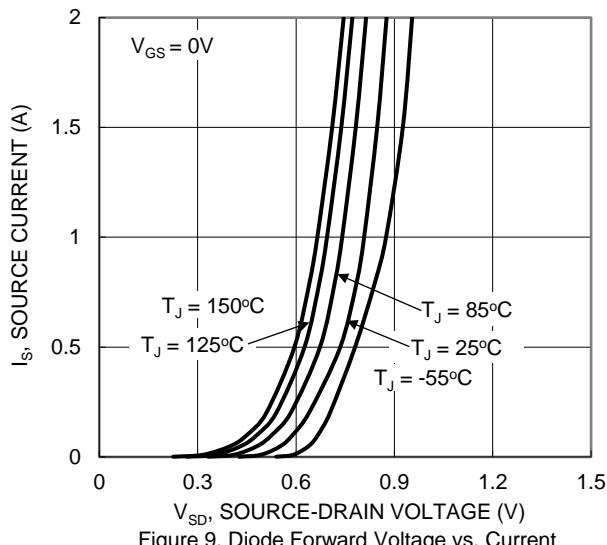


Figure 9. Diode Forward Voltage vs. Current

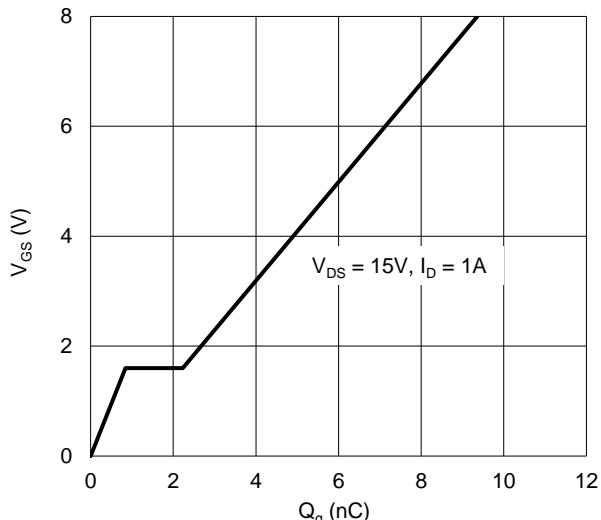


Figure 11. Gate Charge

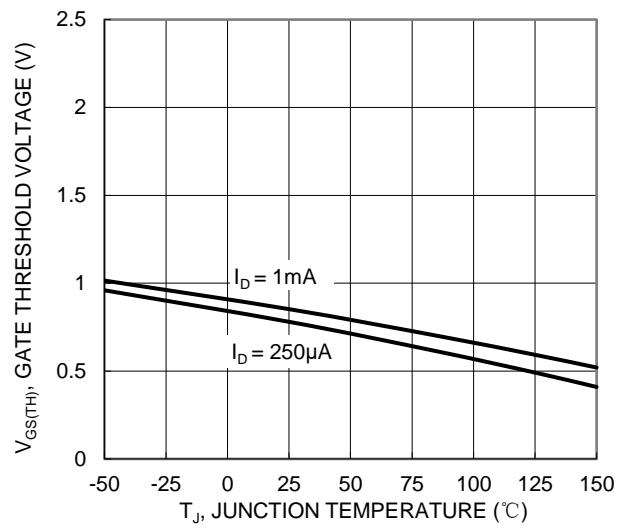


Figure 8. Gate Threshold Variation vs. Junction Temperature

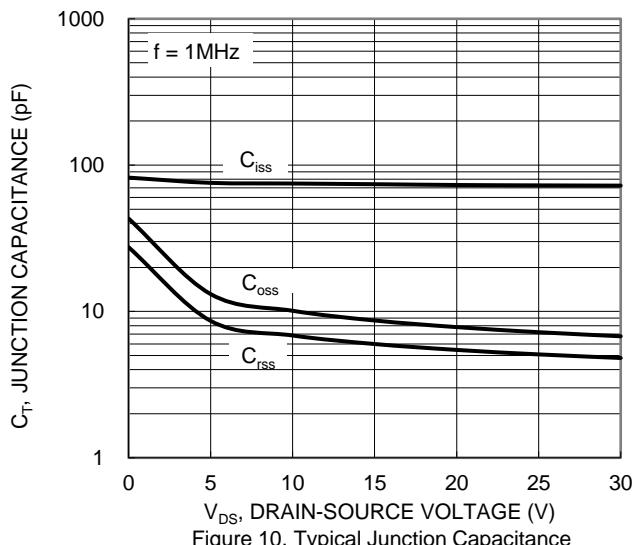


Figure 10. Typical Junction Capacitance

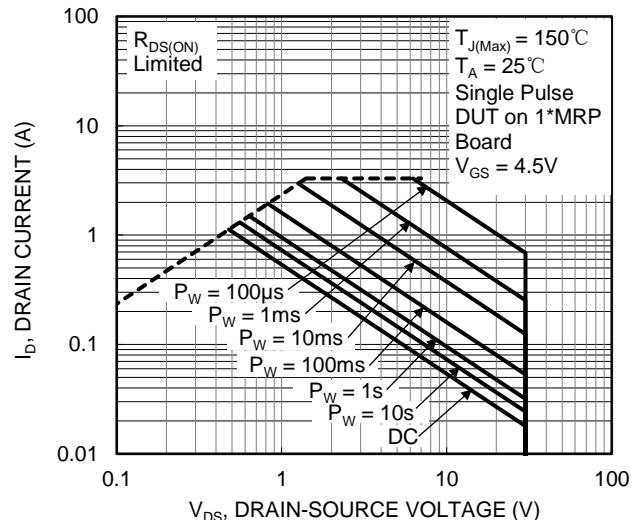


Figure 12. SOA, Safe Operation Area

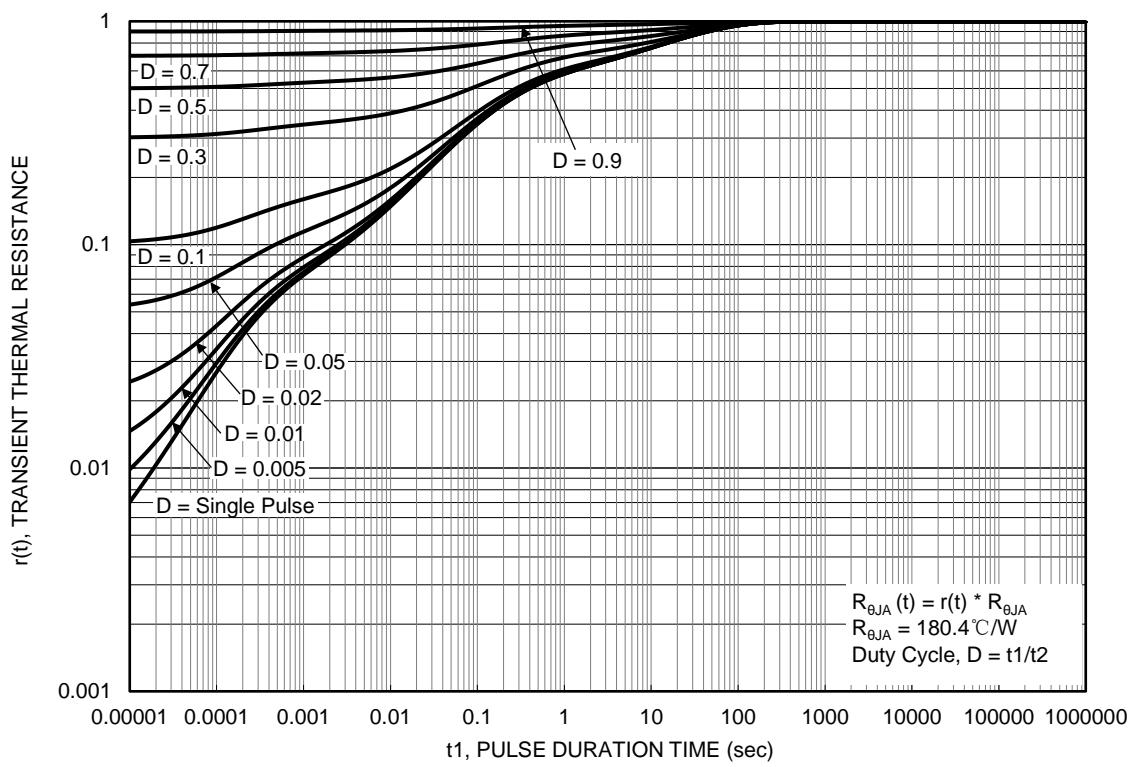
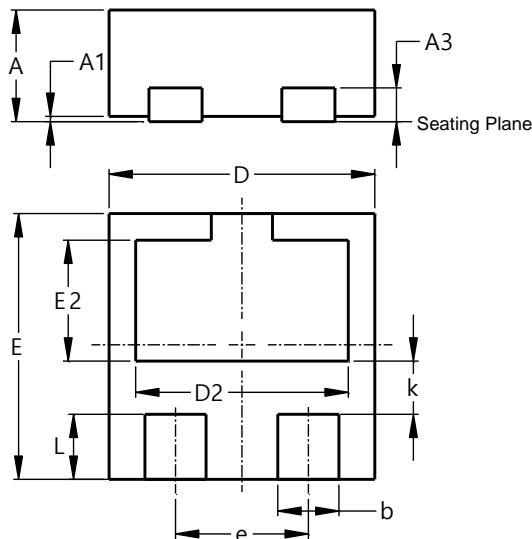


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

X2-DFN1010-3



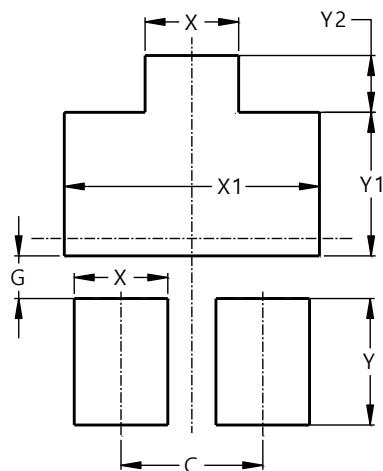
X2-DFN1010-3			
Dim	Min	Max	Typ
A	-	0.40	0.39
A1	0.00	0.05	0.02
A3	-	-	0.13
b	0.18	0.28	0.23
D	0.95	1.05	1.00
D2	0.70	0.90	0.80
E	0.95	1.05	1.00
E2	0.36	0.56	0.46
e	-	-	0.50
k	-	-	0.20
L	0.195	0.295	0.245

All Dimensions in mm

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

X2-DFN1010-3



Dimensions	Value (in mm)
C	0.500
G	0.150
X	0.330
X1	0.900
Y	0.445
Y1	0.505
Y2	0.200

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