CY7C4265

16K × 18 Deep Sync FIFOs

Features

- High speed, low power, first-in first-out (FIFO) memories
  - 16K × 18 (CY7C4265)
- 0.5 micron CMOS for optimum speed and power
- High speed 100 MHz operation (10 ns read/write cycle times)
- Low power - I_{CC} = 45 mA
- Fully asynchronous and simultaneous read and write operation
- Empty, full, half full, and programmable almost empty and almost full status flags
- TTL compatible
- Retransmit function
- Output enable ($\overline{OE}$) pins
- Independent read and write enable pins
- Center power and ground pins for reduced noise
- Supports free-running 50 percent duty cycle clock inputs
- Width and depth expansion capability
- 64-pin TQFP and 64-pin STQFP
- Pb-free packages available

Functional Description

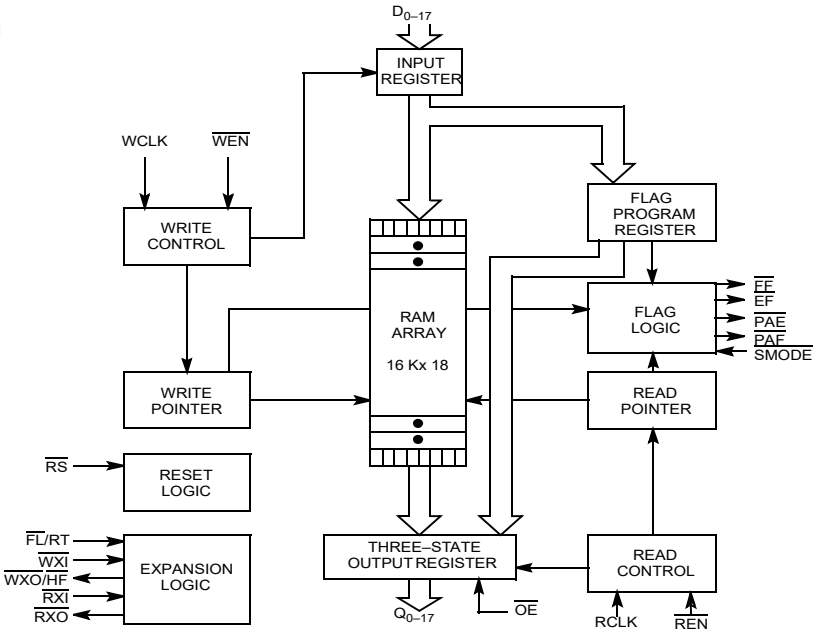
The CY7C4265 are high speed, low power, first-in first-out (FIFO) memories with clocked read and write interfaces. All are 18 bits wide and are pin/functionally compatible to the CY7C42X5 Synchronous FIFO family. The CY7C4265 can be cascaded to increase FIFO depth. Programmable features include Almost Full/Almost Empty flags. These FIFOs provide solutions for a wide variety of data buffering needs, including high speed data acquisition, multiprocessor interfaces, and communications buffering.

These FIFOs have 18-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free running Clock (WCLK) and a Write Enable pin ($\overline{WEN}$). When $\overline{WEN}$ is asserted, data is written into the FIFO on the rising edge of the WCLK signal. While $\overline{WEN}$ is held active, data is continually written into the FIFO on each cycle. The output port is controlled in a similar manner by a free-running Read Clock (RCLK) and a Read Enable pin ($\overline{REN}$). In addition, the CY7C4265 has an Output Enable pin ($\overline{OE}$). The read and write clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 100 MHz are achievable.

Retransmit and Synchronous Almost Full/Almost Empty flag features are available on these devices. Depth expansion is possible using the Cascade Input ($\overline{WXI}$, $\overline{RXI}$), Cascade Output ($\overline{WXO}$, $\overline{RXO}$), and First Load ($\overline{FL}$) pins. The $\overline{WXO}$ and $\overline{RXO}$ pins are connected to the $\overline{WXI}$ and $\overline{RXI}$ pins of the next device, and the $\overline{WXO}$ and $\overline{RXO}$ pins of the last device should be connected to the $\overline{WXI}$ and $\overline{RXI}$ pins of the first device. The $\overline{FL}$ pin of the first device is tied to V_{SS} and the $\overline{FL}$ pin of all the remaining devices should be tied to V_{CC}.

For a complete list of related documentation, click here.

Logic Block Diagram



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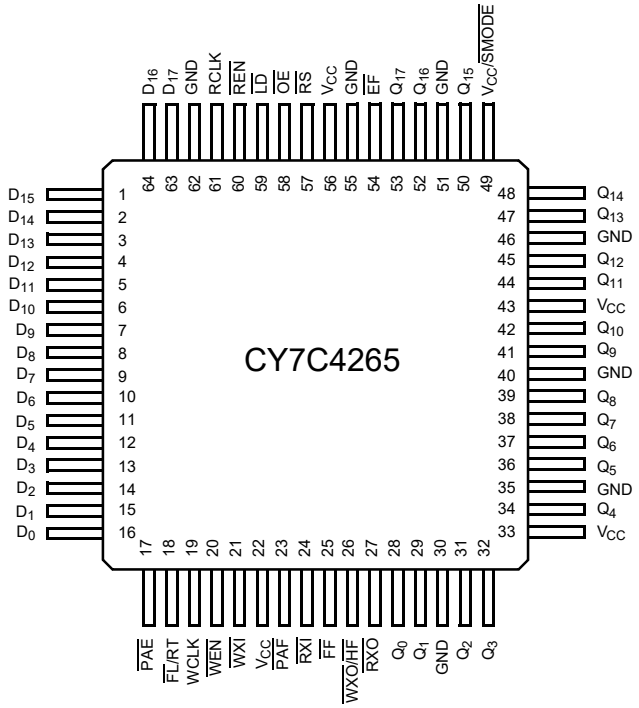
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Pin Configurations

Figure 1. 64-pin TQFP/STQFP pinout (Top View)



Pin Description

The CY7C4265 provides five status pins. These pins are decoded to determine one of five states: Empty, Almost Empty, Half Full, Almost Full, and Full. The Half Full flag shares the WXO pin. This flag is valid in the standalone and width-expansion configurations. In the depth expansion, this pin provides the expansion out (WXO) information that is used to signal the next FIFO when it is activated.

The Empty and Full flags are synchronous, that is, they change state relative to either the Read Clock (RCLK) or the Write Clock (WCLK). When entering or exiting the Empty states, the flag is updated exclusively by the RCLK. The flag denoting Full states is updated exclusively by WCLK. The synchronous flag architecture guarantees that the flags remain valid from one clock cycle to the next. The Almost Empty/Almost Full flags become synchronous if the V_{CC}/SMODE is tied to V_{SS}. All configurations are fabricated using an advanced 0.5µ CMOS technology. Input ESD protection is greater than 2001 V, and latch up is prevented by the use of guard rings.

Selection Guide

Description		7C4265-10	7C4265-15
Maximum Frequency (MHz)		100	66.7
Maximum Access Time (ns)		8	10
Minimum Cycle Time (ns)		10	15
Minimum Data or Enable Set-Up (ns)		3	4
Minimum Data or Enable Hold (ns)		0.5	1
Maximum Flag Delay (ns)		8	10
Active Power Supply Current (I_{CC1}) (mA)	Commercial	45	45
	Industrial	50	50

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Density and Package

Description	CY7C4265
Density	16K × 18
Package	64-pin TQFP, STQFP

Pin Definitions

Signal Name	Description	I/O	Function
$D_{0–17}$	Data Inputs	I	Data inputs for an 18-bit bus.
$Q_{0–17}$	Data Outputs	O	Data outputs for an 18-bit bus.
$\overline{WEN}$	Write Enable	I	Enables the WCLK input.
$\overline{REN}$	Read Enable	I	Enables the RCLK input.
WCLK	Write Clock	I	The rising edge clocks data into the FIFO when $\overline{WEN}$ is LOW and the FIFO is not Full. When $\overline{LD}$ is asserted, WCLK writes data into the programmable flag-offset register.
RCLK	Read Clock	I	The rising edge clocks data out of the FIFO when $\overline{REN}$ is LOW and the FIFO is not Empty. When $\overline{LD}$ is asserted, RCLK reads data out of the programmable flag-offset register.
$\overline{WXO}/\overline{HF}$	Write Expansion Out/Half Full Flag	O	Dual-Mode Pin: Single device or width expansion – Half Full status flag. Cascaded – Write Expansion Out signal, connected to $\overline{WXI}$ of next device.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full. $\overline{FF}$ is synchronized to WCLK.
$\overline{PAE}$	Programmable Almost Empty	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the almost-empty offset value programmed into the FIFO. $\overline{PAE}$ is asynchronous when $V_{CC}/\overline{SMODE}$ is tied to V_{CC}; it is synchronized to RCLK when $V_{CC}/\overline{SMODE}$ is tied to V_{SS}.
$\overline{PAF}$	Programmable Almost Full	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the almost full offset value programmed into the FIFO. $\overline{PAF}$ is asynchronous when $V_{CC}/\overline{SMODE}$ is tied to V_{CC}; it is synchronized to WCLK when $V_{CC}/\overline{SMODE}$ is tied to V_{SS}.
$\overline{LD}$	Load	I	When $\overline{LD}$ is LOW, $D_{0–17}$ ($Q_{0–17}$) are written (read) into (from) the programmable-flag-offset register.
$\overline{FL}/RT$	First Load/ Retransmit	I	Dual-Mode Pin: Cascaded – The first device in the daisy chain has $\overline{FL}$ tied to V_{SS}; all other devices has $\overline{FL}$ tied to V_{CC}. In standard mode or width expansion, $\overline{FL}$ is tied to V_{SS} on all devices. Not Cascaded – Tied to V_{SS}. Retransmit function is also available in stand-alone mode by strobing RT.
$\overline{WXI}$	Write Expansion Input	I	Cascaded – Connected to $\overline{WXO}$ of previous device. Not Cascaded – Tied to V_{SS}.
$\overline{RXI}$	Read Expansion Input	I	Cascaded – Connected to $\overline{RXO}$ of previous device. Not Cascaded – Tied to V_{SS}.
$\overline{RXO}$	Read Expansion Output	O	Cascaded – Connected to $\overline{RXI}$ of next device.
$\overline{RS}$	Reset	I	Resets device to empty condition. A reset is required before an initial read or write operation after power-up.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the FIFO's data outputs drive the bus to which they are connected. If $\overline{OE}$ is HIGH, the FIFO's outputs are in High Z (high-impedance) state.
$V_{CC}/\overline{SMODE}$	Synchronous Almost Empty/ Almost Full Flags	I	Dual-Mode Pin: Asynchronous Almost Empty/Almost Full flags – tied to V_{CC}. Synchronous Almost Empty/Almost Full flags – tied to V_{SS}. (Almost Empty synchronized to RCLK, Almost Full synchronized to WCLK.)

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Architecture

The CY7C4265 consists of an array of 16 K words of 18 bits each (implemented by a dual-port array of SRAM cells), a read pointer, a write pointer, control signals (RCLK, WCLK, REN, WEN, RS), and flags (EF, PAE, HF, PAF, FF). The CY7C4265 also includes the control signals WXI, RXI, WXO, RXO for depth expansion.

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Reset (RS) cycle. This causes the FIFO to enter the Empty condition signified by EF being LOW. All data outputs go LOW after the falling edge of RS only if OE is asserted. For the FIFO to reset to its default state, a falling edge must occur on RS and the user must not read or write while RS is LOW.

FIFO Operation

When the WEN signal is active (LOW), data present on the D_{0-17} pins is written into the FIFO on each rising edge of the WCLK signal. Similarly, when the REN signal is active LOW, data in the FIFO memory are presented on the Q_{0-17} outputs. New data is presented on each rising edge of RCLK while REN is active LOW and OE is LOW. REN must setup t_{ENS} before RCLK for it to be a valid read function. WEN must occur tENS before WCLK for it to be a valid write function.

An output enable (OE) pin is provided to three-state the Q_{0-17} outputs when OE is deasserted. When OE is enabled (LOW), data in the output register is available to the Q_{0-17} outputs after t_{OE}. If devices are cascaded, the OE function only outputs data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and under flow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its Q_{0-17} outputs even after additional reads occur.

Programming

The CY7C4265 devices contain two 14-bit offset registers. Data present on D_{0-13} during a program write determines the distance from Empty (Full) that the Almost Empty (Almost Full) flags become active. If the user elects not to program the FIFO's flags, the default offset values are used (see Table 1). When the Load LD pin is set LOW and WEN is set LOW, data on the inputs D_{0-13} is written into the Empty offset register on the first LOW-to-HIGH transition of the Write Clock (WCLK). When the LD pin and WEN are held LOW then data is written into the Full offset register on the second LOW-to-HIGH transition of the Write Clock (WCLK). The third transition of the Write Clock (WCLK) again writes to the Empty offset register (see Table 1). Writing all offset registers does not have to occur at one time. One or two offset registers can be written and then, by bringing the LD pin HIGH, the FIFO is returned to normal read/write operation. When the LD pin is set LOW, and WEN is LOW, the next offset register in sequence is written.

The contents of the offset registers can be read on the output lines when the LD pin is set LOW and REN is set LOW; then, data can be read on the LOW-to-HIGH transition of the Read Clock (RCLK).

Table 1. Write Offset Register

LD	WEN	WCLK[1]	Selection
0	0		Writing to offset registers: Empty Offset Full Offset 
0	1		No Operation
1	0		Write Into FIFO
1	1		No Operation

Flag Operation

The CY7C4265 devices provide five flag pins to indicate the condition of the FIFO contents. Empty and Full are synchronous. PAE and PAF are synchronous if V_{CC}/SMODE is tied to V_{SS}.

Full Flag

The Full Flag (FF) goes LOW when device is Full. Write operations are inhibited whenever FF is LOW regardless of the state of WEN. FF is synchronized to WCLK: it is exclusively updated by each rising edge of WCLK.

Empty Flag

The Empty Flag (EF) goes LOW when the device is empty. Read operations are inhibited whenever EF is LOW, regardless of the state of REN. EF is synchronized to RCLK, i.e., it is exclusively updated by each rising edge of RCLK.

Programmable Almost Empty/Almost Full Flag

The CY7C4265 features programmable Almost Empty and Almost Full Flags. Each flag can be programmed (described in the Programming section) a specific distance from the corresponding boundary flags (Empty or Full). When the FIFO contains the number of words or fewer for which the flags have been programmed, the PAF or PAE are asserted, signifying that the FIFO is either Almost Full or Almost Empty. See Table 2 on page 6 for a description of programmable flags.

When the SMODE pin is tied LOW, the PAF flag signal transition is caused by the rising edge of the write clock and the PAE flag transition is caused by the rising edge of the read clock.

Note
1. The same selection sequence applies to reading from the registers. REN is enabled and read is performed on the LOW-to-HIGH transition of RCLK.

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Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary.

The Retransmit (RT) input is active in the stand-alone and width expansion modes. The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred and at least one word has been read since the last $\overline{RS}$ cycle. A HIGH pulse on RT resets the internal read pointer to the first physical location of the FIFO. WCLK and RCLK may be free running but must be disabled during and t_{RTR} after the retransmit pulse. With every valid read cycle after retransmit, previously accessed data is read and the read pointer is incremented until it is equal to the write pointer. Flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of RT are transmitted also.

The full depth of the FIFO can be repeatedly retransmitted.

Table 2. Flag Truth Table

Number of Words in FIFO CY7C4265 – 16 K × 18	$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
0	H	H	H	L	L
1 to n[2]	H	H	H	L	H
(n + 1) to 8192	H	H	H	H	H
8193 to (16384 – (m + 1))	H	H	L	H	H
(16384 – m)[3] to 16383	H	L	L	H	H
16384	L	L	L	H	H

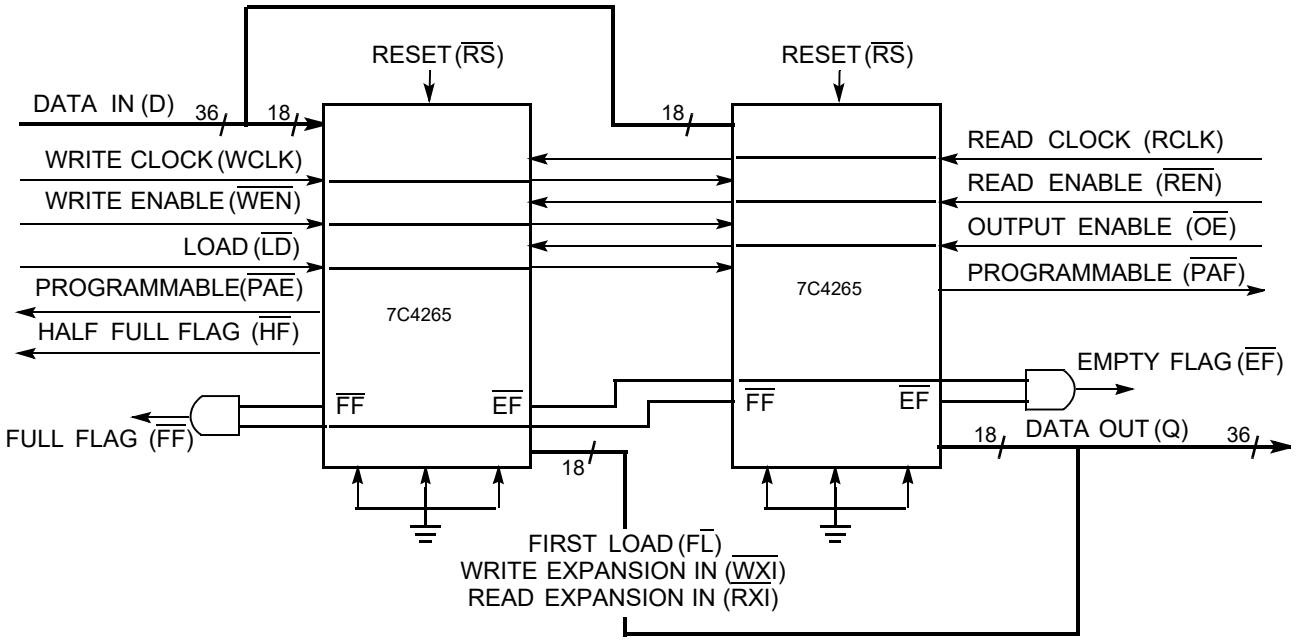
Notes
2. n = Empty Offset (Default Values: CY7C4265 n = 127).
3. m = Full Offset (Default Values: CY7C4265 n = 127).

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Width Expansion Configuration

The CY7C4265 can be expanded in width to provide word widths greater than 18 in increments of 18. During width expansion mode all control line inputs are common and all flags are available. Empty (Full) flags should be created by ANDing the Empty (Full) flags of every FIFO; the PAE and PAF flags can be detected from any one device. This technique avoids reading data from, or writing data to the FIFO that is “staggered” by one clock cycle due to the variations in skew between RCLK and WCLK. Figure 2 demonstrates a 36-word width by using two CY7C4265s.

Figure 2. Block Diagram of 8K × 18/16K × 18 Synchronous FIFO Memory Used in a Width Expansion Configuration



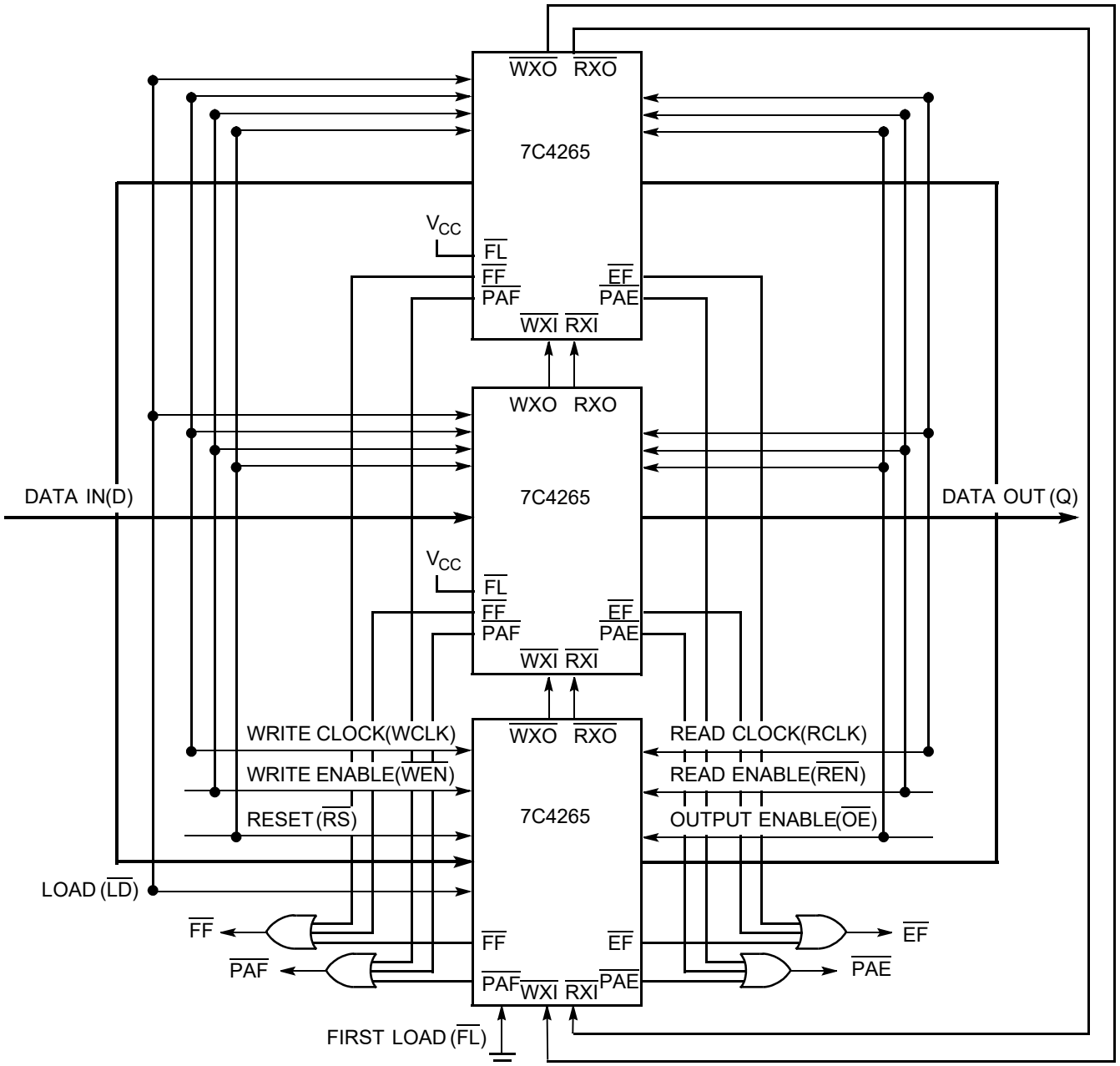
Depth Expansion Configuration (with Programmable Flags)

The CY7C4265 can easily be adapted to applications requiring more than 16384 words of buffering. Figure 3 on page 8 shows Depth Expansion using three CY7C42X5s. Maximum depth is limited only by signal loading. Follow these steps:

1. The first device must be designated by grounding the First Load (FL) control input.
2. All other devices must have FL in the HIGH state.
3. The Write Expansion Out (WXO) pin of each device must be tied to the Write Expansion In (WXI) pin of the next device.
4. The Read Expansion Out (RXO) pin of each device must be tied to the Read Expansion In (RXI) pin of the next device.
5. All Load (LD) pins are tied together.
6. The Half-Full Flag (HF) is not available in the Depth Expansion Configuration.
7. EF, FF, PAE, and PAF are created with composite flags by ORing together these respective flags for monitoring. The composite PAE and PAF flags are not precise.

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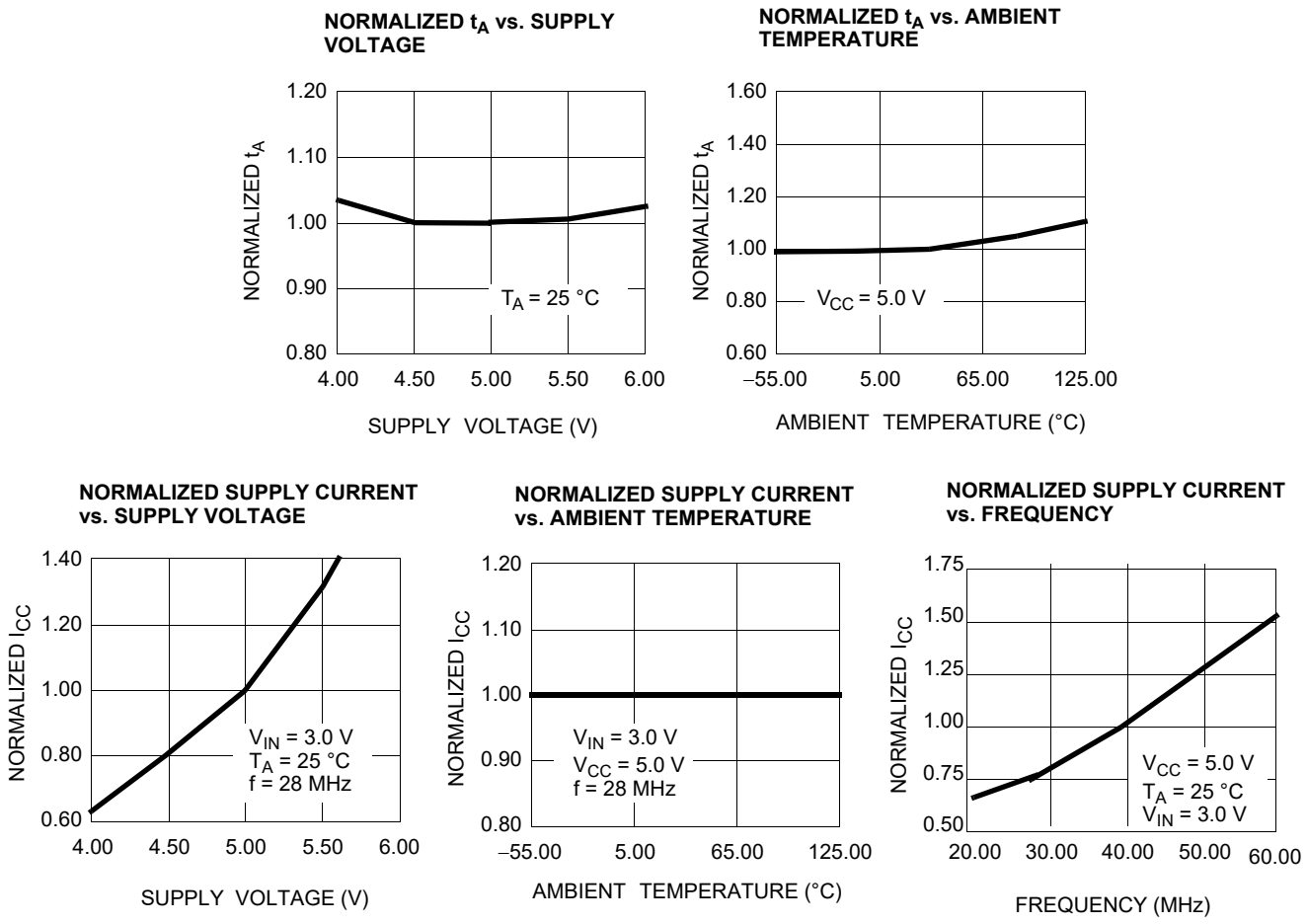
Figure 3. Block Diagram of 16K × 18 Synchronous FIFO Memory with Programmable Flags used in Depth Expansion Configuration



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Typical AC and DC Characteristics

Figure 4. Typical AC and DC Characteristics



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Maximum Ratings

Exceeding maximum ratings[4] may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage to Ground Potential .....–0.5 V to +7.0 V

DC Voltage Applied to Outputs in High Z State .....–0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC}+0.5 V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... >2001 V

Latch-up Current ..... >200 mA

Operating Range

Range	Ambient Temperature [5]	V_{CC}
Commercial	0 °C to +70 °C	5 V ± 10%
Industrial [6]	–40 °C to +85 °C	5 V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter [6]	Description	Test Conditions		7C4265-10		7C4265-15		Unit
				Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0 mA		2.4	–	2.4	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		–	0.4	–	0.4	V
V_{IH}[7]	Input HIGH Voltage			2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}[7]	Input LOW Voltage			–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		–10	+10	–10	+10	µA
I_{OZL} I_{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		–10	+10	–10	+10	µA
I_{CC1}[8]	Active Power Supply Current		Commercial	–	45	–	45	mA
			Industrial	–	50	–	50	mA
I_{CC2}[9]	Average Standby Current		Commercial	–	10	–	10	mA
			Industrial	–	15	–	15	mA

Notes

4. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.
5. T_A is the “Instant On” case temperature.
6. See the last page of this specification for Group A subgroup testing information.
7. The V_{IH} and V_{IL} specifications apply for all inputs except $\overline{WXI}$, $\overline{RXI}$. The $\overline{WXI}$, $\overline{RXI}$ pin is not a TTL input. It is connected to either $\overline{RXO}$, $\overline{WXO}$ of the previous device or V_{SS}.
8. Input signals switch from 0 V to 3 V with a rise/fall time of less than 3 ns, clocks and clock enables switch at 20 MHz, while data inputs switch at 10 MHz. Outputs are unloaded. $I_{CC}1$(typical) = (25 mA + ((freq – 20 MHz) × (1.0 mA/MHz))).
9. All inputs = V_{CC} – 0.2 V, except RCLK and WCLK (which are switching at frequency = 20 MHz), and $\overline{FL}$/RT which is at V_{SS}. All outputs are unloaded.

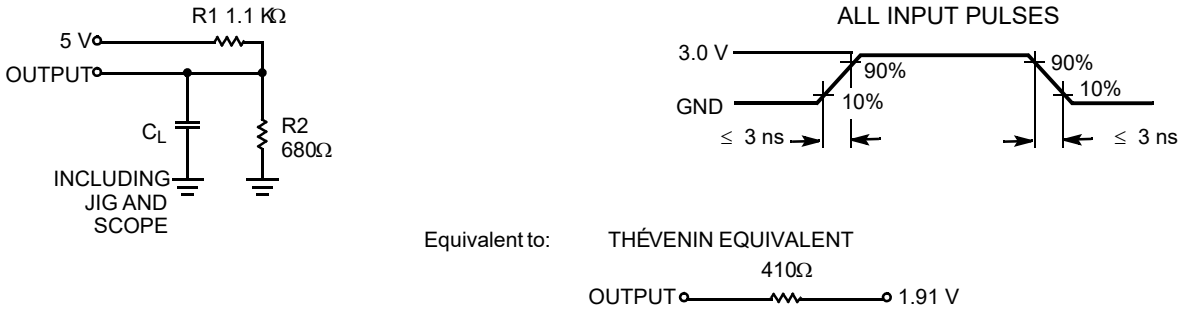
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Capacitance

Parameter [10, 11]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	5	pF
C_{OUT}	Output capacitance		7	pF

AC Test Loads and Waveforms

Figure 5. AC Test Loads and Waveforms [12, 13]



Notes
10. Tested initially and after any design changes that may affect these parameters.
11. Tested initially and after any process changes that may affect these parameters.
12. C_L = 30 pF for all AC parameters except for t_{OHZ}.
13. C_L = 5 pF for t_{OHZ}.

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Switching Characteristics

Over the Operating Range

Parameter	Description	7C4265-10		7C4265-15		Unit
		Min	Max	Min	Max	
t_S	Clock Cycle Frequency	–	100	–	66.7	MHz
t_A	Data Access Time	2	8	2	10	ns
t_{CLK}	Clock Cycle Time	10	–	15	–	ns
t_{CLKH}	Clock HIGH Time	4.5	–	6	–	ns
t_{CLKL}	Clock LOW Time	4.5	–	6	–	ns
t_{DS}	Data Setup Time	3	–	4	–	ns
t_{DH}	Data Hold Time	0.5	–	1	–	ns
t_{ENS}	Enable Setup Time	3	–	4	–	ns
t_{ENH}	Enable Hold Time	0.5	–	1	–	ns
t_{RS}	Reset Pulse Width[14]	10	–	15	–	ns
t_{RSR}	Reset Recovery Time	8	–	10	–	ns
t_{RSF}	Reset to Flag and Output Time	–	10	–	15	ns
t_{PRT}	Retransmit Pulse Width	30	–	35	–	ns
t_{RTR}	Retransmit Recovery Time	60	–	65	–	ns
t_{OLZ}	Output Enable to Output in Low Z[14]	0	–	0	–	ns
t_{OE}	Output Enable to Output Valid	3	7	3	8	ns
t_{OHZ}	Output Enable to Output in High Z[15]	3	7	3	8	ns
t_{WFF}	Write Clock to Full Flag	–	8	–	10	ns
t_{REF}	Read Clock to Empty Flag	–	8	–	10	ns
$t_{PAFasynch}$	Clock to Programmable Almost-Full Flag[15] (Asynchronous mode, V_{CC}/SMODE tied to V_{CC})	–	12	–	16	ns
$t_{PAFsynch}$	Clock to Programmable Almost-Full Flag (Synchronous mode, V_{CC}/$\overline{SMODE}$ tied to V_{SS})	–	8	–	10	ns
$t_{PAEasynch}$	Clock to Programmable Almost-Empty Flag[16] (Asynchronous mode, V_{CC}/SMODE tied to V_{CC})	–	12	–	16	ns
$t_{PAEsynch}$	Clock to Programmable Almost-Full Flag (Synchronous mode, V_{CC}/$\overline{SMODE}$ tied to V_{SS})	–	8	–	10	ns
t_{HF}	Clock to Half-Full Flag	–	12	–	16	ns
t_{XO}	Clock to Expansion Out	–	6	–	10	ns
t_{XI}	Expansion in Pulse Width	4.5	–	6.5	–	ns
t_{XIS}	Expansion in Set-Up Time	4	–	5	–	ns
t_{SKEW1}	Skew Time between Read Clock and Write Clock for Full Flag	5	–	6	–	ns
t_{SKEW2}	Skew Time between Read Clock and Write Clock for Empty Flag	5	–	6	–	ns
t_{SKEW3}	Skew Time between Read Clock and Write Clock for Programmable Almost Empty and Programmable Almost Full Flags (Synchronous Mode only)	10	–	15	–	ns

Notes
14. Pulse widths less than minimum values are not enabled.
15. Values guaranteed by design, not currently tested.
16. $t_{PAFasynch}$, $t_{PAEasynch}$, after program register write is not be valid until 5 ns + $t_{PAF(E)}$.

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Switching Waveforms

Figure 6. Write Cycle Timing

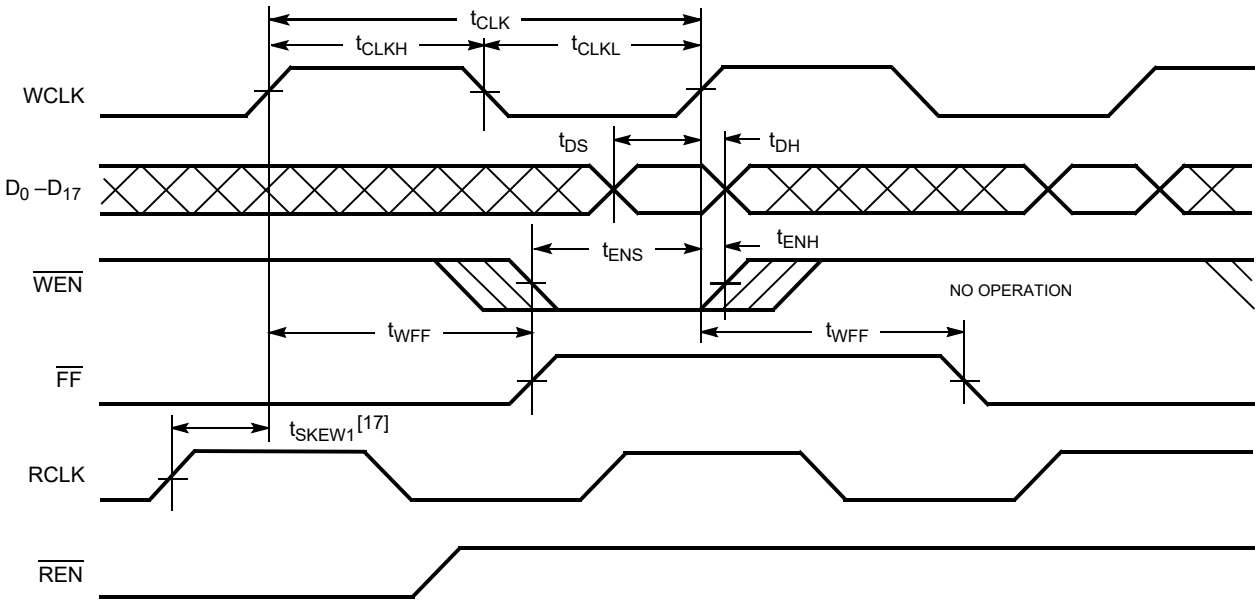
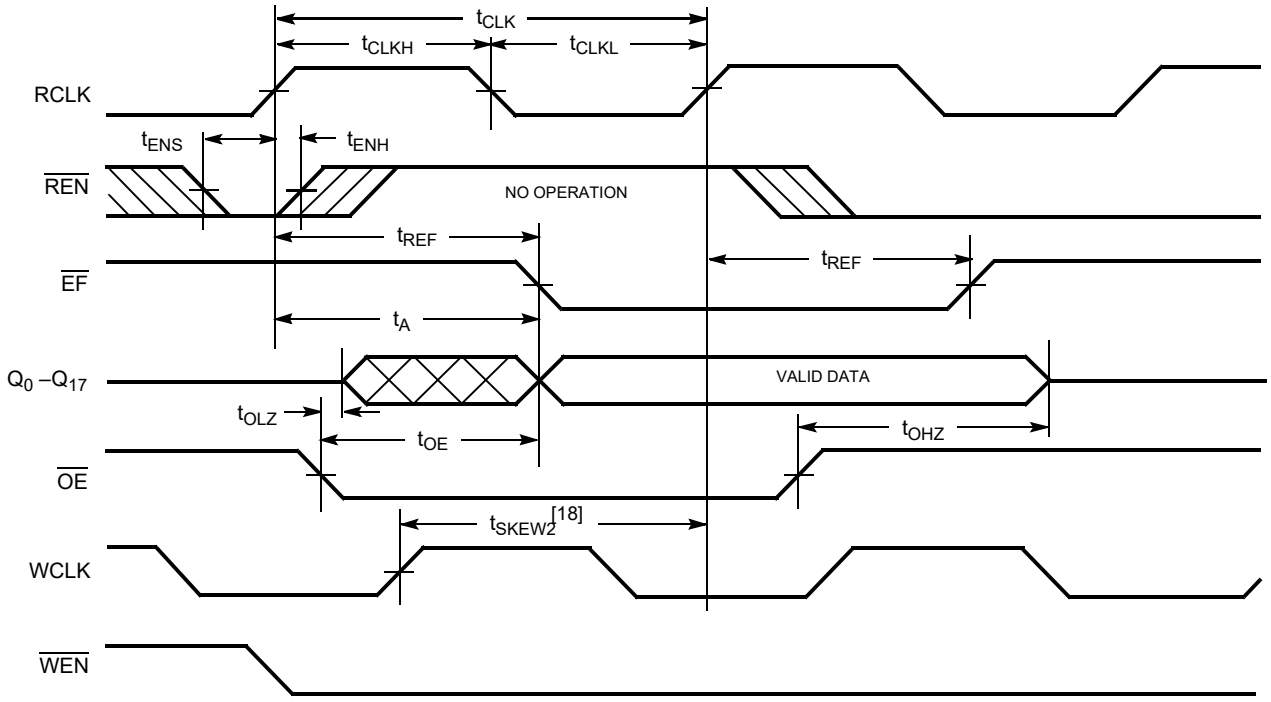


Figure 7. Read Cycle Timing



Notes

17. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ goes HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK rising edge.
18. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ goes HIGH during the current clock cycle. It the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{EF}$ may not change state until the next RCLK rising edge.

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Switching Waveforms (continued)

Figure 8. Reset Timing [19]

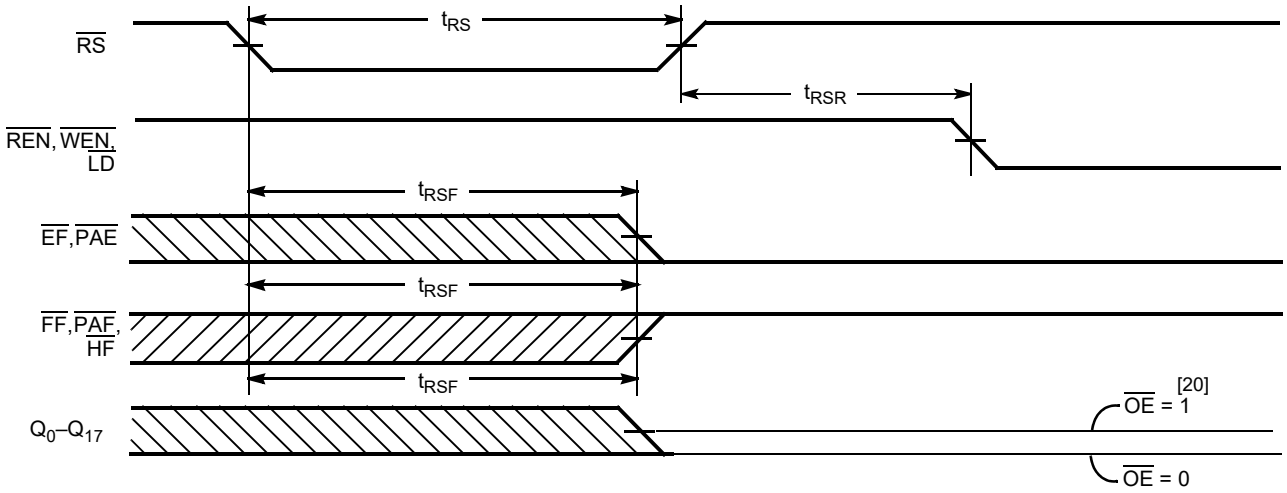
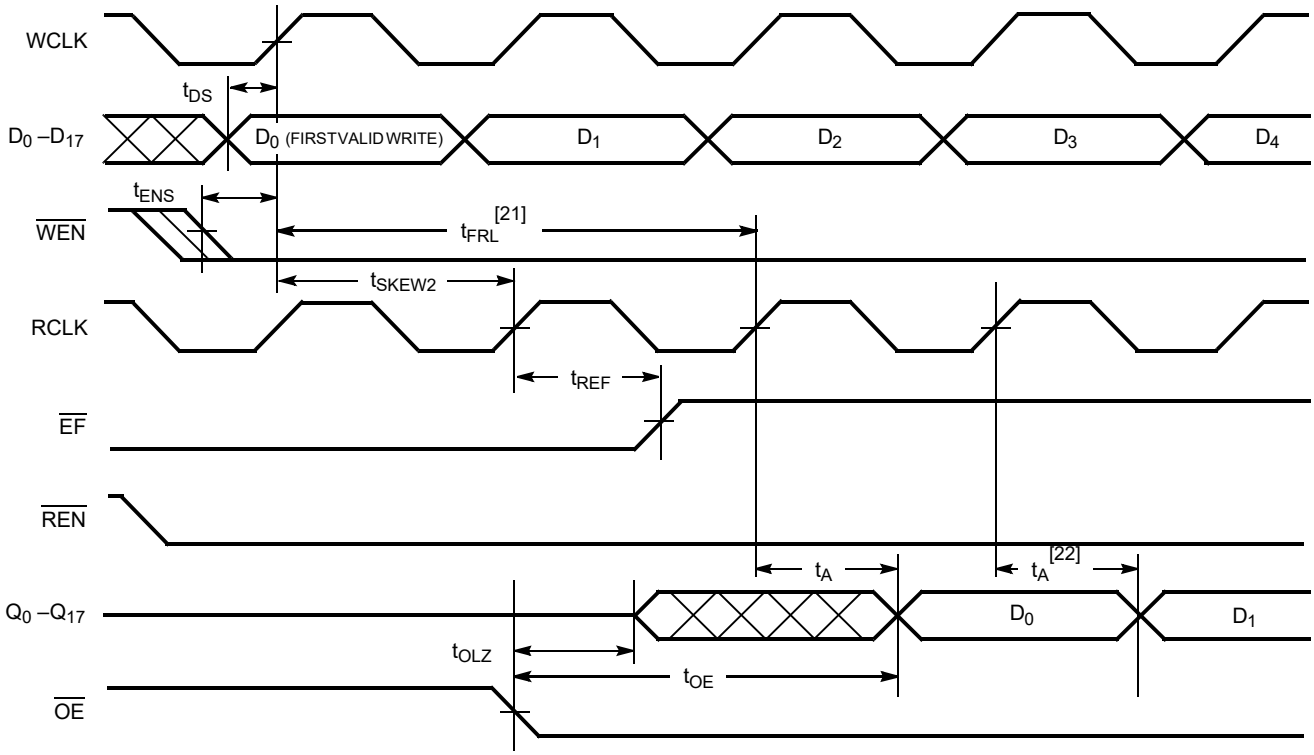


Figure 9. First Data Word Latency after Reset with Simultaneous Read and Write



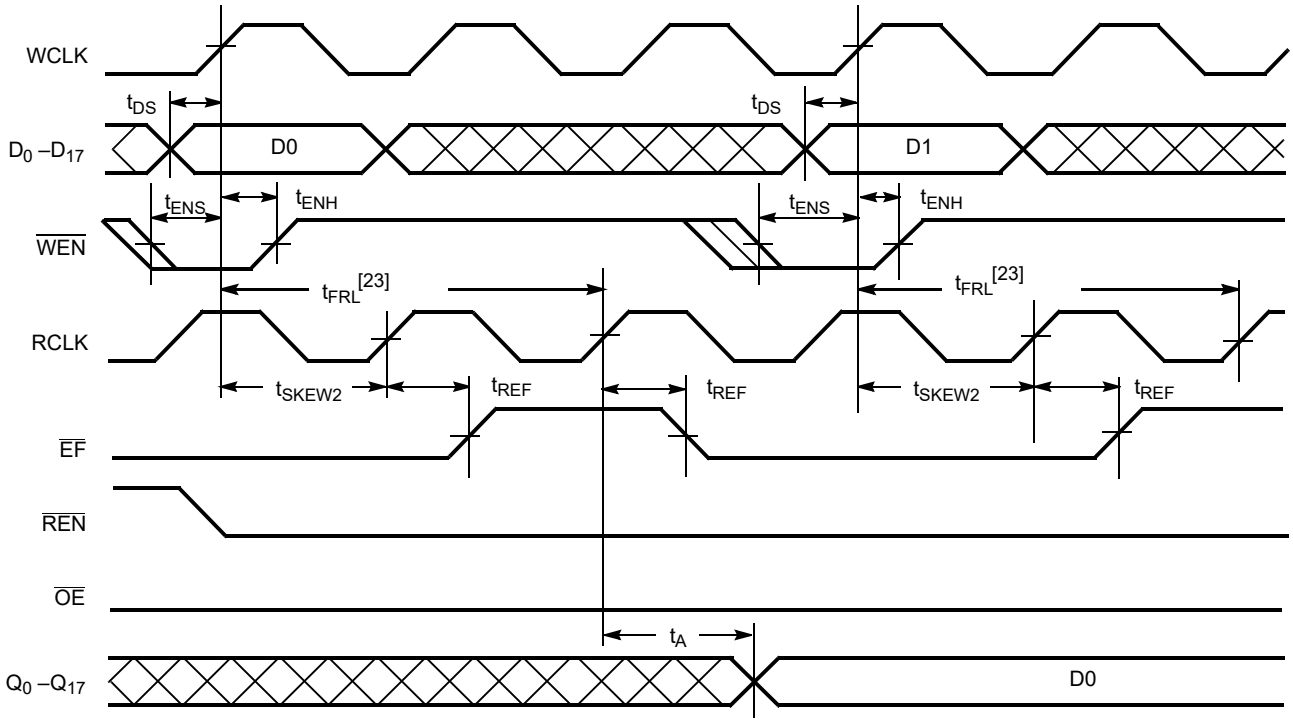
Notes

19. The clocks (RCLK, WCLK) can be free-running during reset.
20. After reset, the outputs are LOW if $\overline{OE}$ = 0 and three-state if $\overline{OE}$ = 1.
21. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = $t_{CLK} + t_{SKEW2}$. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either $2*t_{CLK} + t_{SKEW2}$ or $t_{CLK} + t_{SKEW2}$. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).
22. The first word is available the cycle after $\overline{EF}$ goes HIGH, always.

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Switching Waveforms (continued)

Figure 10. Empty Flag Timing



Note

23. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = t_{CLK} + t_{SKEW2}. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either 2*t_{CLK} + t_{SKEW2} or t_{CLK} + t_{SKEW2}. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).

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Switching Waveforms (continued)

Figure 11. Full Flag Timing

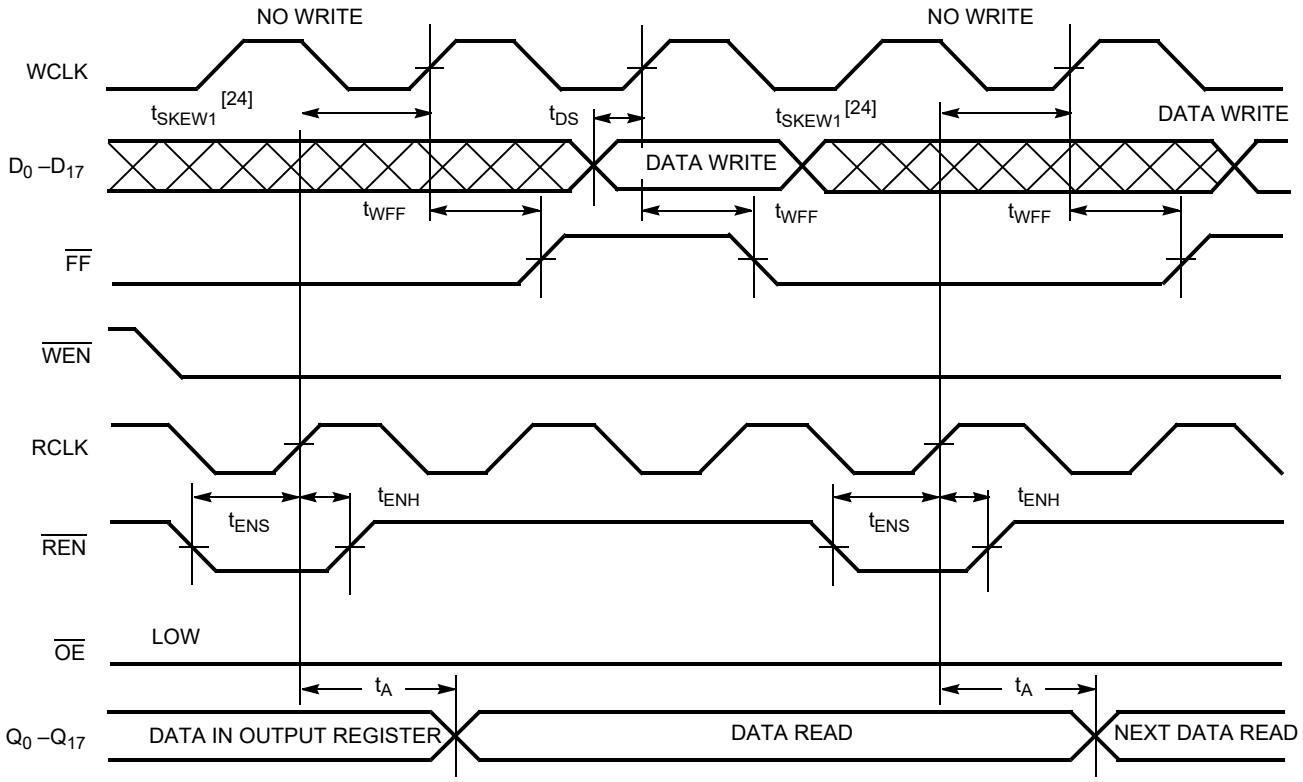
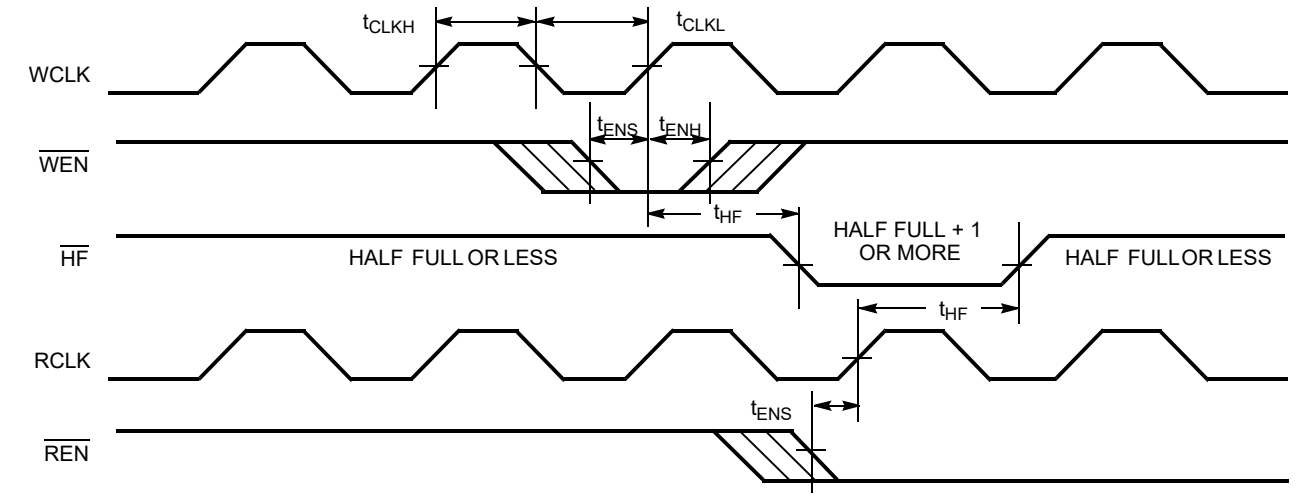


Figure 12. Half-Full Flag Timing



Note

24. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ goes HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK rising edge.

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Switching Waveforms (continued)

Figure 13. Programmable Almost Empty Flag Timing

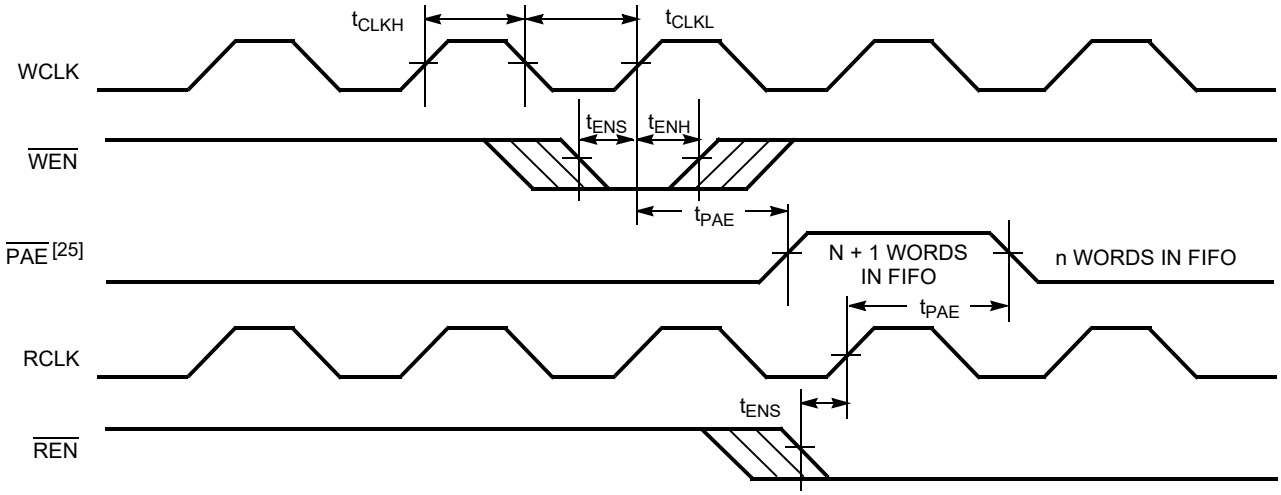
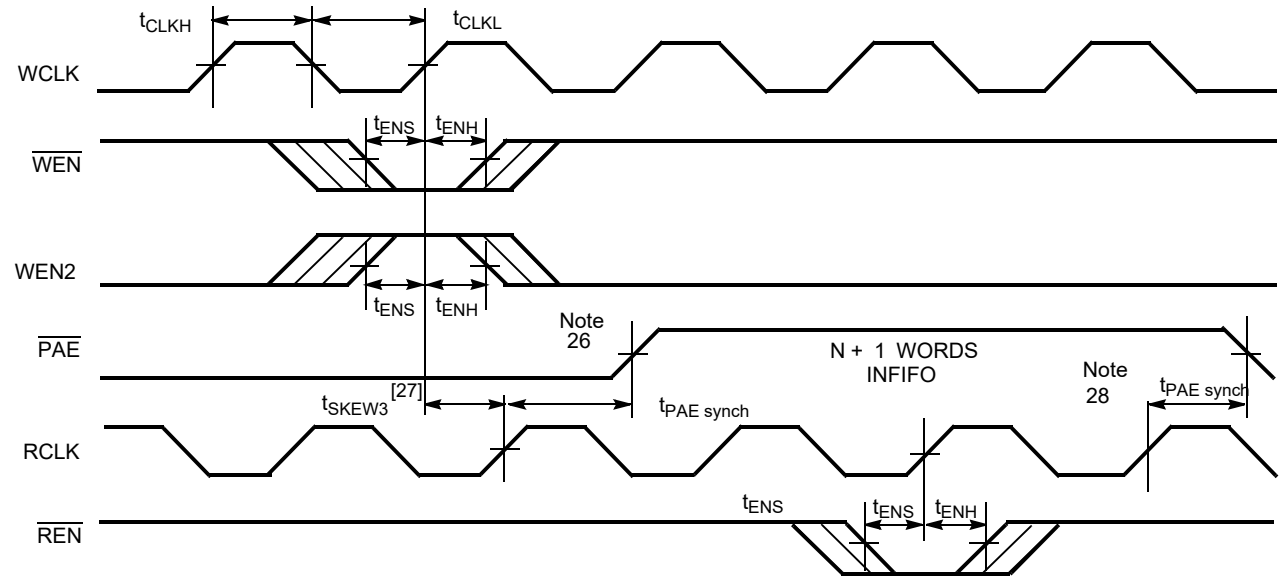


Figure 14. Programmable Almost Empty Flag Timing (applies only in SMODE (SMODE is LOW))



Note

25. PAE is offset = n. Number of data words into FIFO already = n.
26. PAE offset – n.
27. t_{SKEW3} is the minimum time between a rising WCLK and a rising RCLK edge for $\overline{PAE}$ to change state during that clock cycle. If the time between the edge of WCLK and the rising RCLK is less than t_{SKEW3}, then $\overline{PAE}$ may not change state until the next RCLK.
28. If a read is preformed on this rising edge of the read clock, there are Empty + (n–1) words in the FIFO when $\overline{PAE}$ goes LOW.

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Switching Waveforms (continued)

Figure 15. Programmable Almost Full Flag Timing

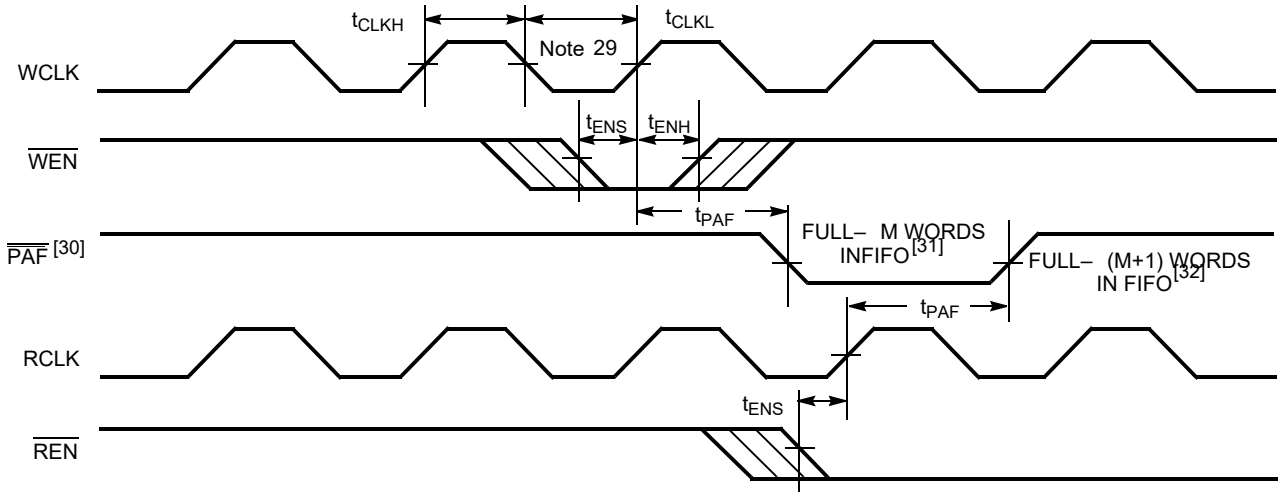
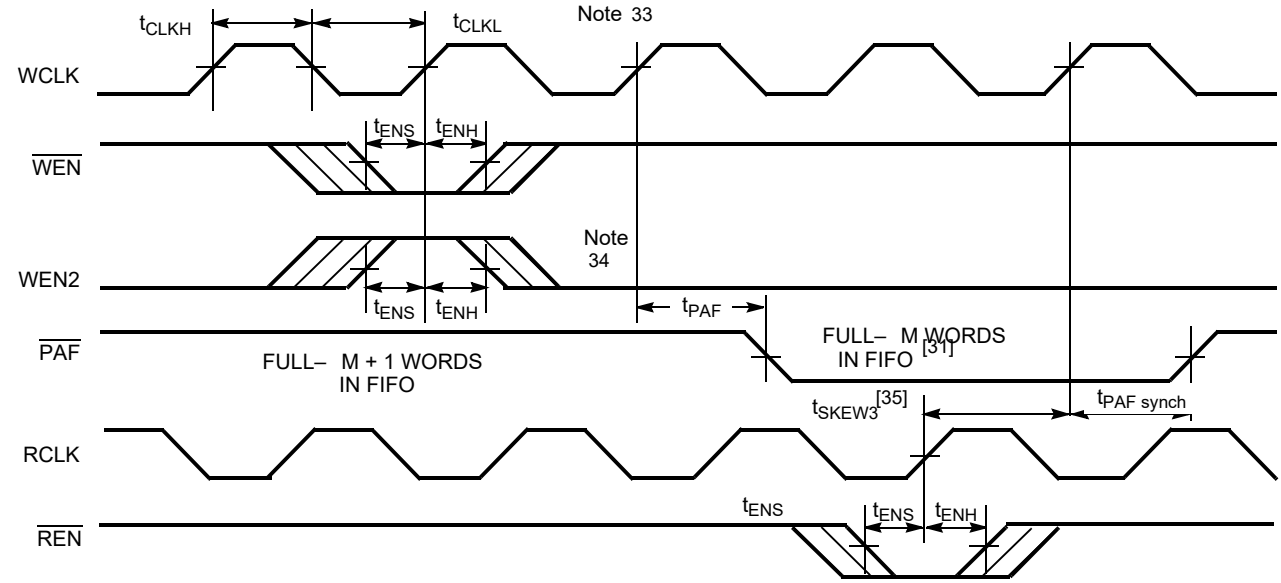


Figure 16. Programmable Almost Full Flag Timing (applies only in $\overline{\text{SMODE}}$ ($\overline{\text{SMODE}}$ is LOW))



Notes

29. PAF offset = m. Number of data words written into FIFO already = 16384 – (m + 1) for the CY7C4265.
30. PAF is offset = m.
31. 16384 – m words in CY7C4265.
32. 16384 – (m + 1) CY7C4265.
33. If a write is performed on this rising edge of the write clock, there are Full – (m – 1) words of the FIFO when $\overline{\text{PAF}}$ goes LOW.
34. PAF offset = m.
35. t_{SKEW3} is the minimum time between a rising RCLK and a rising WCLK edge for $\overline{\text{PAF}}$ to change state during that clock cycle. If the time between the edge of RCLK and the rising edge of WCLK is less than t_{SKEW3}, then PAF may not change state until the next WCLK rising edge.

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Switching Waveforms (continued)

Figure 17. Write Programmable Registers

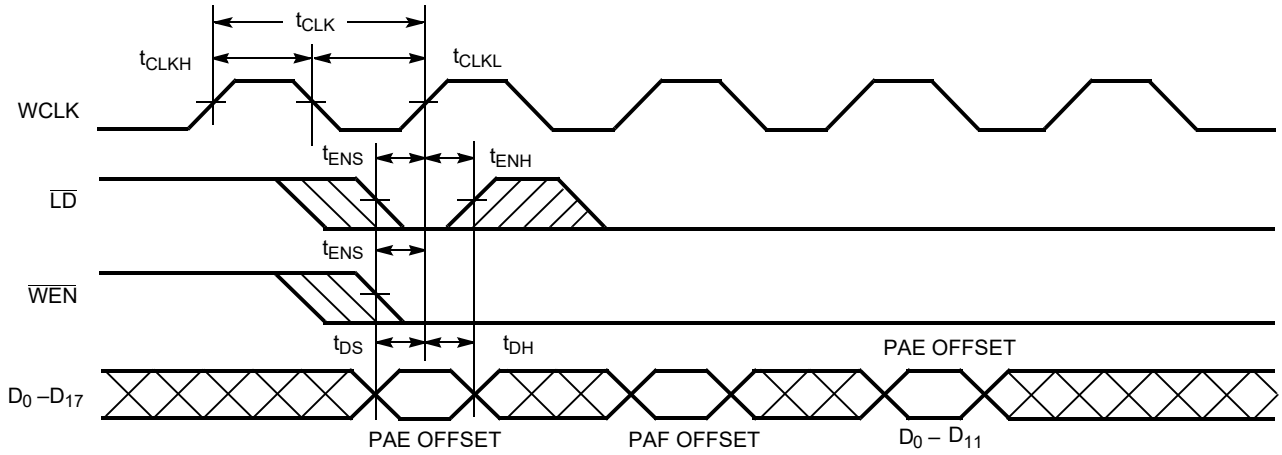


Figure 18. Read Programmable Registers

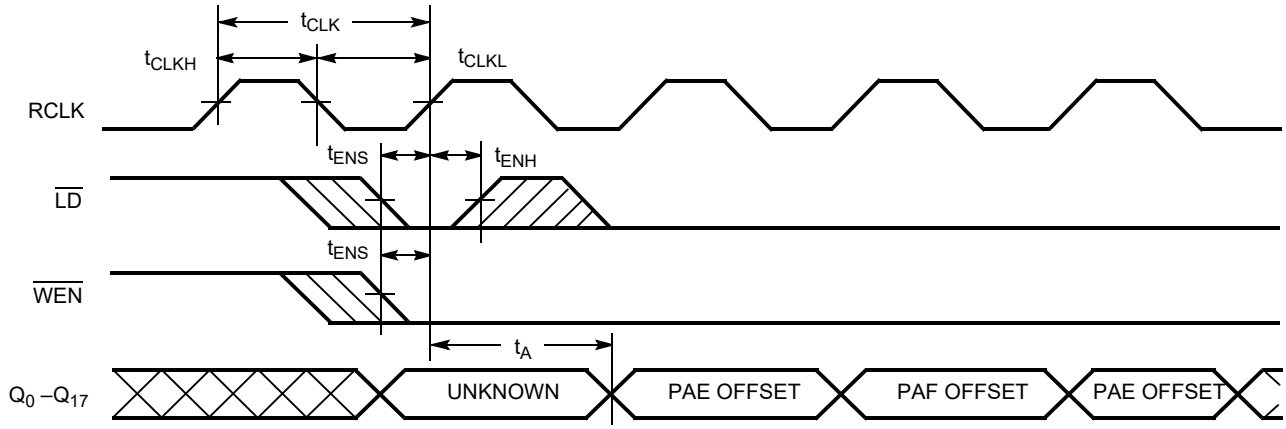
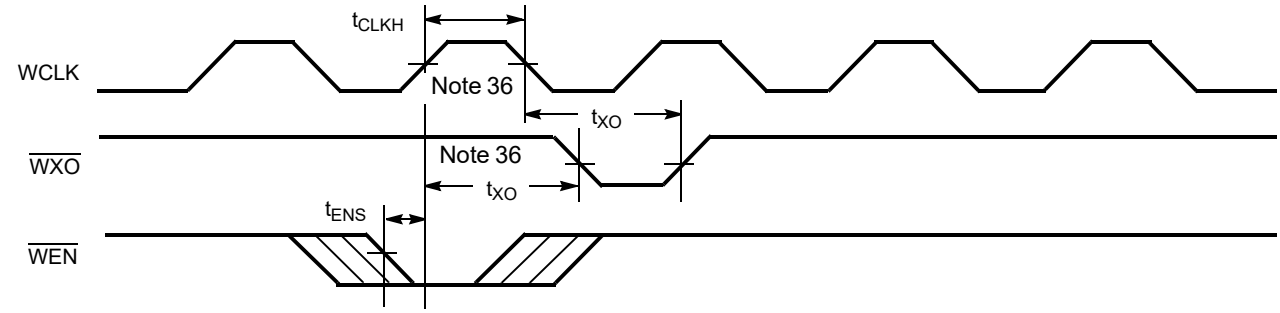


Figure 19. Write Expansion Out Timing



Note
36. Write to Last Physical Location.

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Switching Waveforms (continued)

Figure 20. Read Expansion Out Timing

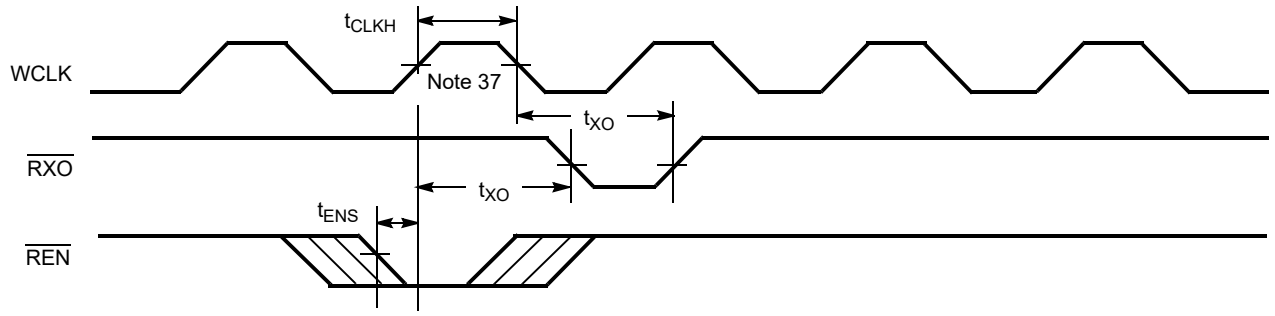


Figure 21. Write Expansion In Timing

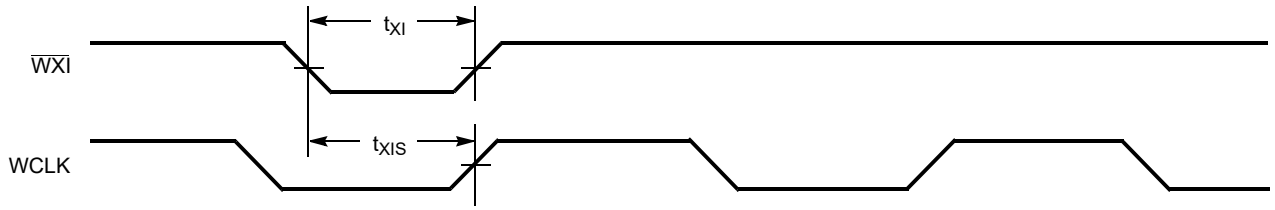


Figure 22. Read Expansion In Timing

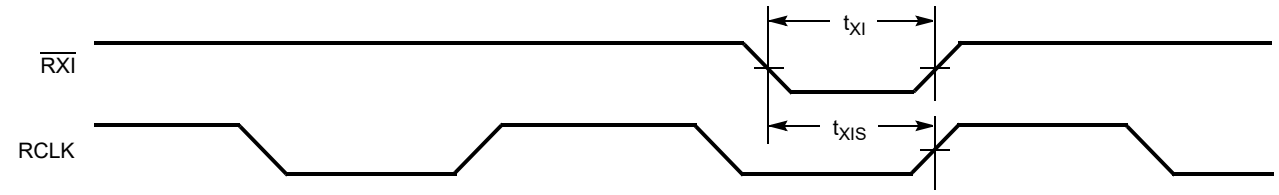
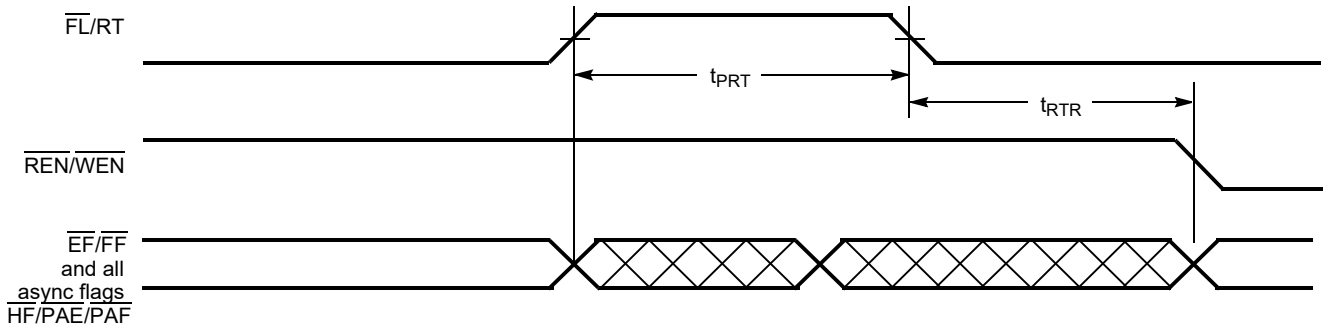


Figure 23. Retransmit Timing [38, 39, 40]



Notes
37. Read from Last Physical Location.
38. Clocks are free-running in this case.
39. The flags may change state during Retransmit as a result of the offset of the read and write pointers, but flags are valid at t_{RTR}.
40. For the synchronous PAE and PAF flags (SMODE), an appropriate clock cycle is necessary after t_{RTR} to update these flags.

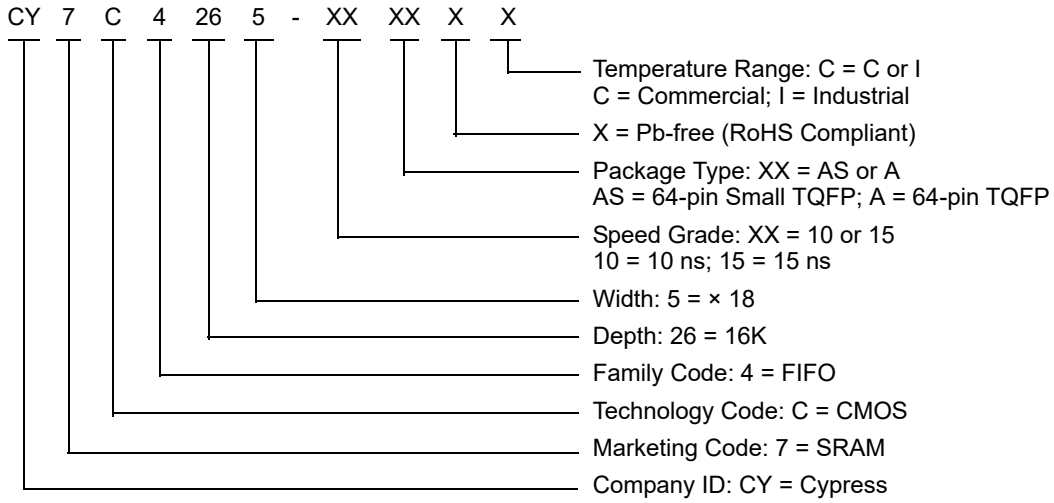
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Ordering Information

16K × 18 Deep Sync FIFO

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C4265-10ASXC	51-85051	64-pin Small TQFP (Pb-free)	Commercial
	CY7C4265-10AXI	51-85046	64-pin TQFP (Pb-free)	Industrial
15	CY7C4265-15AXC	51-85046	64-pin TQFP (Pb-free)	Commercial

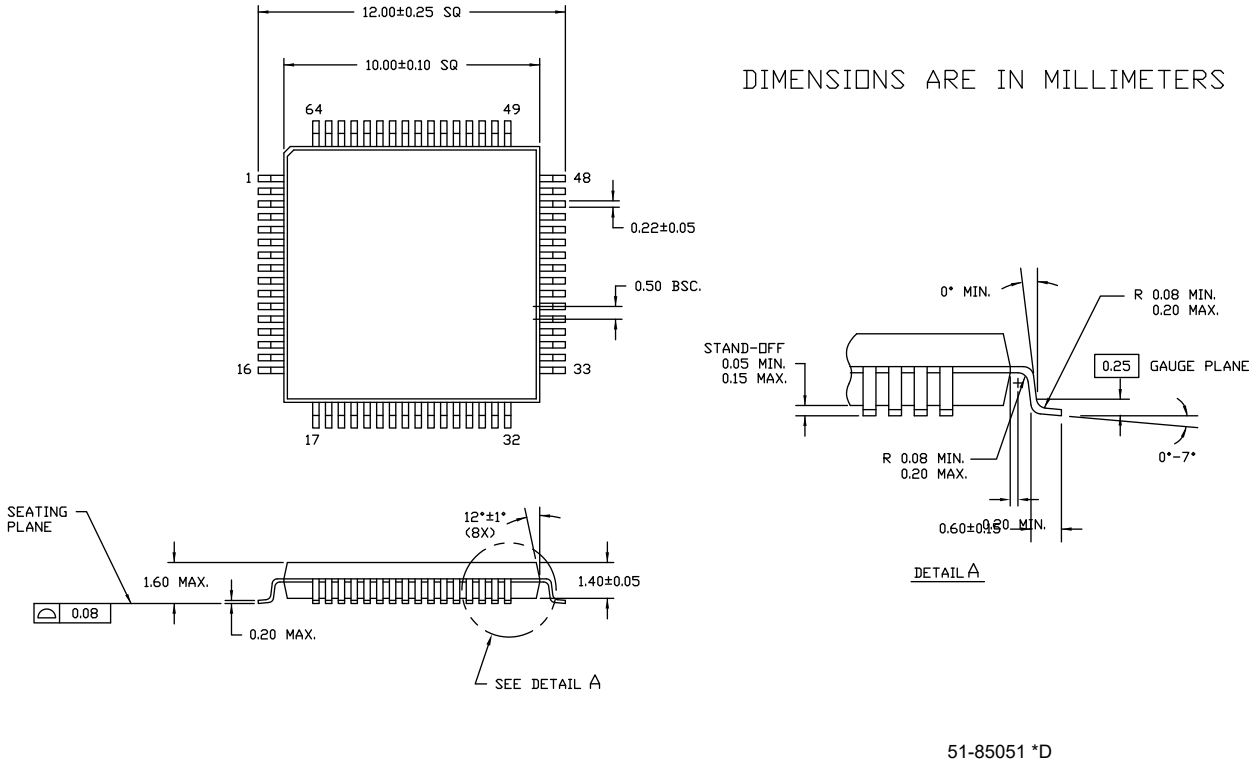
Ordering Code Definitions



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Package Diagrams

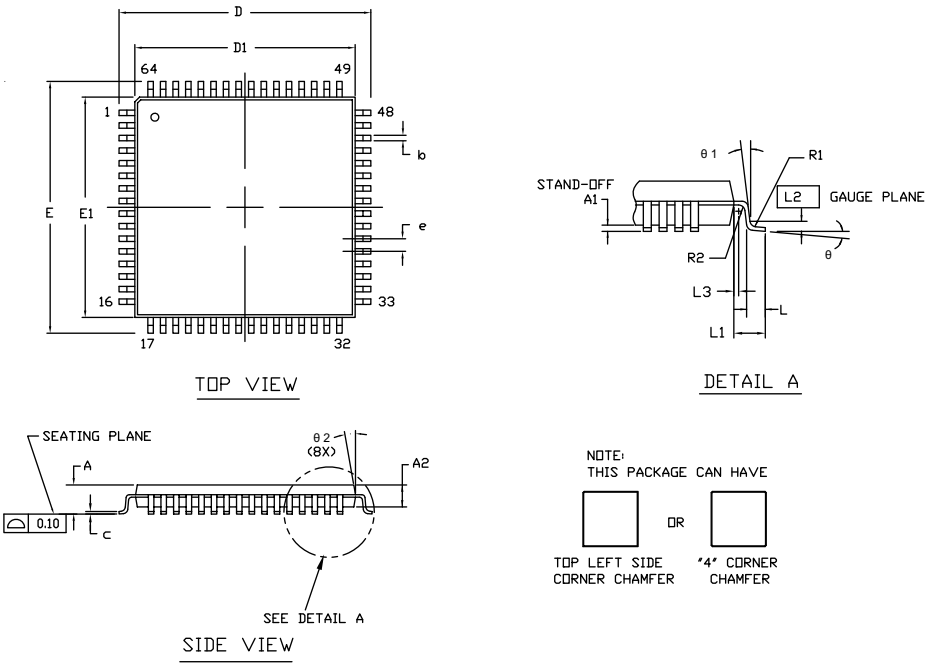
Figure 24. 64-pin TQFP (10 × 10 × 1.4 mm) A64SB Package Outline, 51-85051



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Package Diagrams (continued)

Figure 25. 64-pin TQFP (14 × 14 × 1.4 mm) A64SA Package Outline, 51-85046



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
D	15.75	16.00	16.25
D1	13.95	14.00	14.05
E	15.75	16.00	16.25
E1	13.95	14.00	14.05
R1	0.08	—	0.20
R2	0.08	—	0.20
θ	0°	—	7°
θ1	0°	—	—
θ2	11°	12°	13°
c	—	—	0.20
b	0.30	0.35	0.40
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
L3	0.20	—	—
e	0.80 TYP		

NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85046 *H

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Acronyms

Acronym	Description
BGA	Ball Grid Array
FS	Frequency Select
I/O	Input/Output
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVTTL	Low Voltage Transistor-Transistor Logic
PLL	Phase-Locked Loop
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic
VCO	Voltage Controlled Oscillator

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
KHz	kilohertz
KΩ	kilohm
MHz	megahertz
µA	microampere
mA	milliampere
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt

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Document History Page

Document Title: CY7C4265, 16K × 18 Deep Sync FIFOs Document Number: 38-06004				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	106465	SZV	07/11/2001	Changed Spec Number from 38-00468 to 38-06004.
*A	122257	RBI	12/26/2002	Updated Maximum Ratings: Added Note 4 and referred the same note in “maximum ratings”.
*B	252889	YDT	08/12/2004	Removed 64-pin PLCC package related information in all instances across the document. Updated Ordering Information: Updated part numbers.
*C	385985	ESH	08/04/2005	Added Pb-Free logo to top of first page. Updated Ordering Information: Updated part numbers.
*D	2623658	VKN / PYRS	12/17/2008	Removed Pb-Free logo to top of first page. Added CY7C4265A part related information in all instances across the document. Updated Ordering Information: Updated part numbers. Updated to new template.
*E	2714768	VKN / AESA	06/04/2009	Updated Logic Block Diagram. Updated Pin Configurations: Updated Figure 1.
*F	2896039	RAME	03/19/2010	Updated Document Title to read as “CY7C4265, 16 K × 18 Deep Sync FIFOs”. Updated Ordering Information: Updated part numbers. Updated Package Diagrams: spec 51-85051 – Changed revision from *A to *B. spec 51-85046 – Changed revision from *B to *D.
*G	3094385	ADMU	11/24/2010	Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions. Completing Sunset Review.
*H	3452178	ADMU	12/01/2011	Removed CY7C4255 part related information in all instances across the document. Removed -25 and -35 speed bins related information in all instances across the document. Updated Package Diagrams: spec 51-85051 – Changed revision from *B to *C. spec 51-85046 – Changed revision from *D to *E. Completing Sunset Review.
*I	4197278	ADMU	11/20/2013	Updated Ordering Information: Updated part numbers. Updated to new template. Completing Sunset Review.
*J	4575241	ADMU	11/19/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Package Diagrams: spec 51-85046 – Changed revision from *E to *F. Completing Sunset Review.
*K	6072279	VINI	02/15/2018	Updated Package Diagrams: spec 51-85051 – Changed revision from *C to *D. spec 51-85046 – Changed revision from *F to *H. Updated to new template.

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