

# ADA4620-1, ADA4620-2

36 V, Precision, Low Noise, 16.5 MHz JFET Op Amp with Rail-to-Rail Output

## FEATURES

- ▶ Low offset voltage:  $\pm 30 \mu\text{V}$  typ
- ▶ Low offset voltage drift:  $\pm 0.32 \mu\text{V}/^\circ\text{C}$  typ
- ▶ Low input bias current:  $\pm 0.8 \text{ pA}$  typ,  $\pm 5 \text{ pA}$  max
- ▶ Low  $1/f$  noise:  $225 \text{ nV p-p}$ ,  $0.1 \text{ Hz}$  to  $10 \text{ Hz}$  typ
- ▶ Voltage noise density:  $5.1 \text{ nV}/\sqrt{\text{Hz}}$  at  $1 \text{ kHz}$  typ
- ▶ Gain bandwidth product:  $16.5 \text{ MHz}$  typ
- ▶ High slew rate:  $32 \text{ V}/\mu\text{s}$  typ
- ▶ Low THD:  $-148 \text{ dB}$  at  $1 \text{ kHz}$  typ
- ▶ Low supply current:  $1.3 \text{ mA}$  per amplifier typ
- ▶ Wide power supply range:
  - ▶ Single supply:  $4.5 \text{ V}$  to  $36 \text{ V}$
  - ▶ Dual supplies:  $\pm 2.25 \text{ V}$  to  $\pm 18 \text{ V}$
- ▶ No phase reversal
- ▶ Unity-gain stable
- ▶ Extended high input common-mode range
  - ▶  $(V+) - 4.4 \text{ V} < V_{\text{CM}} \leq (V+)$
- ▶ Multiple channel options:
  - ▶ ADA4620-1 single channel
  - ▶ ADA4620-2 dual channel

## APPLICATIONS

- ▶ Transimpedance amplifiers
- ▶ Electronic test and measurement
- ▶ Scientific and field instruments
- ▶ Semiconductor test
- ▶ Data acquisition systems
- ▶ High impedance sensors

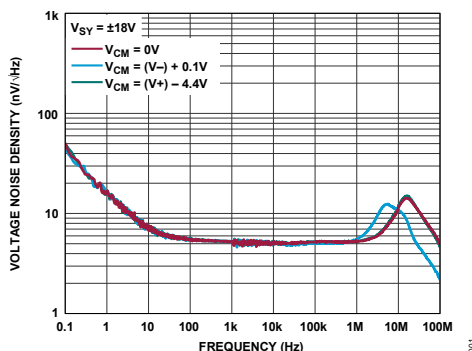


Figure 1. Input Voltage Noise vs. Frequency

## TYPICAL APPLICATION DIAGRAM

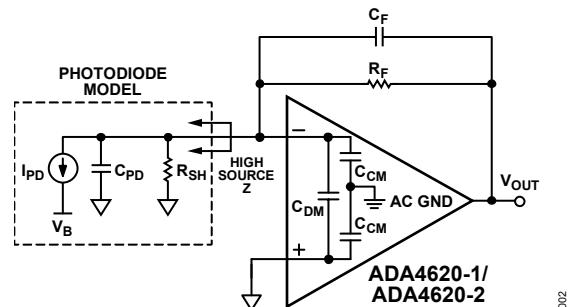


Figure 2. Photodiode Application with Key Elements

## GENERAL DESCRIPTION

The ADA4620-1 and ADA4620-2 are 36 V, precision, low noise, low offset drift, JFET op amps. The parts offer the combination of top precision parameters at speed, and at extended operating range and temperature. The ADA4620 is ideal for high DC precision and AC performance. The specifications make the ADA4620 optimal as a front-end amplifier in a data-acquisition (DAQ) system, or for a TIA circuit with high input impedance.

For only 1.3 mA of supply current per amplifier, the ADA4620 has a gain-bandwidth product of 16.5 MHz, a  $32 \text{ V}/\mu\text{s}$  slew rate,  $5.1 \text{ nV}/\sqrt{\text{Hz}}$  of broadband noise, and  $225 \text{ nV p-p}$  of  $0.1 \text{ Hz}$  to  $10 \text{ Hz}$  noise. The input voltage range includes the negative supply, and the output swings rail-to-rail.

The ADA4620 is specified for operating over the temperature range of  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ , and dual supplies ranging from  $\pm 2.25 \text{ V}$  to  $\pm 18 \text{ V}$ , or on a single supply ranging from  $+4.5 \text{ V}$  to  $+36 \text{ V}$ . The ADA4620-1 and ADA4620-2 are available in an **8-lead SOIC\_N package**.

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## REVISION HISTORY

| Nature of Change                                                                                                        | Page Number |
|-------------------------------------------------------------------------------------------------------------------------|-------------|
| <b>10/2024 – Rev 0</b><br>Initial release                                                                               | —           |
| <b>06/2026 – Rev A</b><br>Changes in <b>Electrical Characteristics</b> and <b>Typical Performance Characteristics</b> . | 7, 31       |

## SPECIFICATIONS

## Electrical Characteristics

Table 1. Electrical Characteristics

(Supply voltage  $V_{SY} = \pm 2.25$  V to  $\pm 18$  V for dual supplies, or 4.5 V to 36 V for single supply; common-mode voltage  $V_{CM} = 0$  V for dual supplies, or  $(V+)/2$  V for single supply;  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

| PARAMETER                         | SYMBOL                   | CONDITIONS/COMMENTS                                                 | MIN                                                     | TYP        | MAX          | UNITS                        |
|-----------------------------------|--------------------------|---------------------------------------------------------------------|---------------------------------------------------------|------------|--------------|------------------------------|
| INPUT CHARACTERISTICS             |                          |                                                                     |                                                         |            |              |                              |
| Offset Voltage                    | $V_{OS}$                 | $V_{CM} = (V-) - 0.1$ V to $(V+) - 4.4$ V                           |                                                         | $\pm 30$   | $\pm 120$    | $\mu\text{V}$                |
|                                   |                          |                                                                     | $0^\circ\text{C} < T_A < +85^\circ\text{C}$             |            | $\pm 135$    |                              |
|                                   |                          |                                                                     | $-40^\circ\text{C} < T_A < +125^\circ\text{C}$          |            | $\pm 250$    |                              |
| Offset Voltage Drift <sup>1</sup> | $\Delta V_{OS}/\Delta T$ | $V_{CM} = (V-) - 0.1$ V to $(V+) - 4.4$ V                           | $-40^\circ\text{C} < T_A < +125^\circ\text{C}$          | $\pm 0.32$ | $\pm 1$      | $\mu\text{V}/^\circ\text{C}$ |
|                                   |                          |                                                                     | $0^\circ\text{C} < T_A < +85^\circ\text{C}$ , ADA4620-1 | $\pm 0.13$ | $\pm 0.63$   |                              |
|                                   |                          |                                                                     | $0^\circ\text{C} < T_A < +85^\circ\text{C}$ , ADA4620-2 | $\pm 0.4$  | $\pm 1.1$    |                              |
| Input Bias Current                | $I_B$                    | $V_{CM} = 0$ V                                                      |                                                         | $\pm 0.8$  | $\pm 5$      | $\text{pA}$                  |
|                                   |                          |                                                                     | $-40^\circ\text{C} < T_A < +125^\circ\text{C}$          |            | $\pm 1.5$    | $\text{nA}$                  |
| Input Offset Current              | $I_{OS}$                 | $V_{CM} = 0$ V                                                      |                                                         | $\pm 0.1$  | $\pm 2.5$    | $\text{pA}$                  |
|                                   |                          |                                                                     | $-40^\circ\text{C} < T_A < +125^\circ\text{C}$          |            | $\pm 100$    |                              |
| Precision Input Voltage Range     | IVR                      | Guaranteed by CMRR                                                  | $(V-) - 0.1$                                            |            | $(V+) - 4.4$ | V                            |
| Common-Mode Rejection Ratio       | CMRR                     | $(V-) - 0.1$ V $< V_{CM} < (V+) - 4.4$ V, $V_{SY} = \pm 18$ V       | ADA4620-1                                               | 117        | 131          | dB                           |
|                                   |                          |                                                                     | ADA4620-2                                               | 120        | 143          |                              |
|                                   |                          |                                                                     | $-40^\circ\text{C} < T_A < +125^\circ\text{C}$          | 116        | 120          |                              |
| Open-Loop Voltage Gain            | $A_{VOL}$                | $R_L = 10$ k $\Omega$ , $V_{OUT} = \pm 17.8$ V, $V_{SY} = \pm 18$ V |                                                         | 128        | 140          | dB                           |
|                                   |                          |                                                                     | $-40^\circ\text{C} < T_A < +125^\circ\text{C}$          | 124        |              |                              |
|                                   |                          | $R_L = 2$ k $\Omega$ , $V_{OUT} = \pm 17.8$ V, $V_{SY} = \pm 18$ V  |                                                         | 106        | 112          |                              |
|                                   |                          |                                                                     | $-40^\circ\text{C} < T_A < +125^\circ\text{C}$          | 97         |              |                              |
| Input Capacitance                 | $C_{INDM}$               | Differential mode, $V_{SY} = 18$ V, $V_{CM} = 0$ V                  |                                                         | 4.8        |              | $\text{pF}$                  |
|                                   | $C_{INCM}$               | Common mode, $V_{SY} = 18$ V, $V_{CM} = 0$ V                        |                                                         | 7.1        |              |                              |
| Input Resistance                  | $R_{INDM}$               | Differential mode                                                   |                                                         | 200        |              | $\text{G}\Omega$             |
|                                   | $R_{INCM}$               | Common mode                                                         |                                                         | 10         |              | $\text{T}\Omega$             |

(Supply voltage  $V_{SY} = \pm 2.25$  V to  $\pm 18$  V for dual supplies, or 4.5 V to 36 V for single supply; common-mode voltage  $V_{CM} = 0$  V for dual supplies, or  $(V+)/2$  V for single supply;  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

| PARAMETER                                | SYMBOL    | CONDITIONS/COMMENTS                                                                | MIN                                            | TYP   | MAX | UNITS      |
|------------------------------------------|-----------|------------------------------------------------------------------------------------|------------------------------------------------|-------|-----|------------|
| <b>OUTPUT CHARACTERISTICS</b>            |           |                                                                                    |                                                |       |     |            |
| Output Swing High<br>[(V+) - $V_{OUT}$ ] | $V_{OH}$  | $R_L = 10\text{ k}\Omega$ , $V_{SY} = \pm 18$ V, $G = 50$ ,<br>$V_{IN} = 0.37$ V   |                                                | 42    | 60  | mV         |
|                                          |           |                                                                                    | $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ |       | 65  |            |
|                                          |           | $R_L = 2\text{ k}\Omega$ , $V_{SY} = \pm 18$ V, $G = 50$ ,<br>$V_{IN} = 0.37$ V    |                                                | 150   | 175 |            |
|                                          |           |                                                                                    | $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ |       | 215 |            |
|                                          |           | $R_L = 10\text{ k}\Omega$ , $V_{SY} = \pm 2.25$ V, $G = 50$ ,<br>$V_{IN} = 0.37$ V |                                                |       | 30  |            |
|                                          |           | $R_L = 2\text{ k}\Omega$ , $V_{SY} = \pm 2.25$ V, $G = 50$ ,<br>$V_{IN} = 0.37$ V  |                                                |       | 60  |            |
| Output Swing Low<br>[ $V_{OUT} - (V-)$ ] | $V_{OL}$  | $R_L = 10\text{ k}\Omega$ , $V_{SY} = \pm 18$ V, $G = 50$ ,<br>$V_{IN} = 0.37$ V   |                                                | 37    | 50  | mV         |
|                                          |           |                                                                                    | $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ |       | 55  |            |
|                                          |           | $R_L = 2\text{ k}\Omega$ , $V_{SY} = \pm 18$ V, $G = 50$ ,<br>$V_{IN} = 0.37$ V    |                                                | 137   | 160 |            |
|                                          |           |                                                                                    | $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ |       | 190 |            |
|                                          |           | $R_L = 10\text{ k}\Omega$ , $V_{SY} = \pm 2.25$ V, $G = 50$ ,<br>$V_{IN} = 0.37$ V |                                                |       | 20  |            |
|                                          |           | $R_L = 2\text{ k}\Omega$ , $V_{SY} = \pm 2.25$ V, $G = 50$ ,<br>$V_{IN} = 0.37$ V  |                                                |       | 40  |            |
| Short-Circuit Current                    | $I_{SC}$  | $V_{SY} = \pm 5$ V, Sourcing/Sinking                                               |                                                | 55/47 |     | mA         |
|                                          |           | $V_{SY} = \pm 15$ V, Sourcing/Sinking                                              |                                                | 86/58 |     |            |
|                                          |           | $V_{SY} = \pm 18$ V, Sourcing/Sinking                                              |                                                | 94/60 |     |            |
| Closed-Loop Output Impedance             | $Z_{OUT}$ | $f = 1\text{ kHz}$ , $A_V = +1$ , $V_{SY} = \pm 18$ V                              |                                                | 0.65  |     | m $\Omega$ |
|                                          |           | $f = 1\text{ kHz}$ , $A_V = +10$ , $V_{SY} = \pm 18$ V                             |                                                | 4     |     |            |
|                                          |           | $f = 1\text{ kHz}$ , $A_V = +100$ , $V_{SY} = \pm 18$ V                            |                                                | 40    |     |            |
| Open-Loop Output Impedance               | $Z_O$     | $f = 1\text{ MHz}$ , $V_{SY} = \pm 18$ V                                           |                                                | 3.3   |     | $\Omega$   |
| <b>POWER SUPPLY</b>                      |           |                                                                                    |                                                |       |     |            |
| Power Supply Rejection Ratio             | PSRR+     | $V_- = -0.1$ V, $V_{CM} = 0$ V, $V_+$ stepped from 4.4 V to 35.9 V                 |                                                | 114   | 131 | dB         |
|                                          |           |                                                                                    | $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ | 114   |     |            |
|                                          | PSRR-     | $V_+ = 4.4$ V, $V_{CM} = 0$ V, $V_-$ stepped from -31.6 V to -0.1 V                |                                                | 114   | 132 |            |
|                                          |           |                                                                                    | $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ | 114   |     |            |
| Supply Current per Amplifier             | $I_{SY}$  | $I_{OUT} = 0$ mA, $V_{SY} = \pm 18$ V                                              |                                                | 1.3   | 1.4 | mA         |
|                                          |           |                                                                                    | $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ |       | 1.9 |            |

(Supply voltage  $V_{SY} = \pm 2.25\text{ V}$  to  $\pm 18\text{ V}$  for dual supplies, or  $4.5\text{ V}$  to  $36\text{ V}$  for single supply; common-mode voltage  $V_{CM} = 0\text{ V}$  for dual supplies, or  $(V+)/2\text{ V}$  for single supply;  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

| PARAMETER                 | SYMBOL             | CONDITIONS/COMMENTS                                                                                                                                           |                       | MIN | TYP  | MAX | UNITS   |
|---------------------------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|-----|------|-----|---------|
| Operating Range           | V <sub>SY</sub>    | Guaranteed by PSRR                                                                                                                                            |                       | 4.5 |      | 36  | V       |
| DYNAMIC PERFORMANCE       |                    |                                                                                                                                                               |                       |     |      |     |         |
| Slew Rate                 | SR                 | R <sub>L</sub> = 2 kΩ, V <sub>OUT</sub> = ±5 V, A <sub>V</sub> = +1, V <sub>SY</sub> = ±18 V                                                                  | 10% - 90%             |     | 30   |     | V/μs    |
|                           |                    |                                                                                                                                                               | 90% - 10%             |     | 34   |     |         |
|                           |                    | R <sub>L</sub> = 2 kΩ, V <sub>OUT</sub> = ±5 V, A <sub>V</sub> = -1, V <sub>SY</sub> = ±18 V                                                                  | 10% - 90%             |     | 32   |     |         |
|                           |                    |                                                                                                                                                               | 90% - 10%             |     | 32   |     |         |
| Gain Bandwidth Product    | GBP                | R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 50 pF, V <sub>SY</sub> = ±18 V, Measured at 100 kHz                                                                   |                       |     | 16.5 |     | MHz     |
| Unity-Gain Crossover      | UGC                | R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 50 pF, V <sub>SY</sub> = ±18 V                                                                                        |                       |     | 18   |     | MHz     |
| -3 dB Bandwidth           | -3 dB              | R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 50 pF, A <sub>V</sub> = +1, V <sub>SY</sub> = ±18 V                                                                   |                       |     | 51   |     | MHz     |
| Phase Margin              | PM                 | R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 50 pF, V <sub>SY</sub> = ±18 V                                                                                        |                       |     | 57   |     | Degrees |
| Settling Time             | t <sub>s</sub>     | V <sub>OUT</sub> = ±5 V, A <sub>V</sub> = -1, V <sub>SY</sub> = ±18 V, R <sub>F</sub> = R <sub>G</sub> = 1 kΩ, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 50 pF | To ±0.01%             |     | 500  |     | ns      |
|                           |                    |                                                                                                                                                               | To ±0.0122% (12-Bit)  |     | 485  |     |         |
|                           |                    |                                                                                                                                                               | To ±0.00075% (16-Bit) |     | 3.3  |     | μs      |
| Overload Recovery Time    | OLR+               | R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 50 pF, A <sub>V</sub> = -10, V <sub>SY</sub> = ±18 V, Step = 2.2 V                                                    |                       |     | 123  |     | ns      |
|                           | OLR-               | R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 50 pF, A <sub>V</sub> = -10, V <sub>SY</sub> = ±18 V, Step = 2.2 V                                                    |                       |     | 103  |     |         |
| Total Harmonic Distortion | THD                | R <sub>L</sub> = 2 kΩ, V <sub>OUT</sub> = 10 V p-p, A <sub>V</sub> = +1, f = 1 kHz, V <sub>SY</sub> = ±18 V                                                   |                       |     | -148 |     | dB      |
|                           |                    | R <sub>L</sub> = 2 kΩ, V <sub>OUT</sub> = 10 V p-p, A <sub>V</sub> = -1, f = 1 kHz, V <sub>SY</sub> = ±18 V                                                   |                       |     | -147 |     |         |
|                           |                    | R <sub>L</sub> = 2 kΩ, V <sub>OUT</sub> = 10 V p-p, A <sub>V</sub> = +1, f = 100 kHz, V <sub>SY</sub> = ±18 V                                                 |                       |     | -85  |     |         |
|                           |                    | R <sub>L</sub> = 2 kΩ, V <sub>OUT</sub> = 10 V p-p, A <sub>V</sub> = -1, f = 100 kHz, V <sub>SY</sub> = ±18 V                                                 |                       |     | -106 |     |         |
| EMI REJECTION RATIO       |                    |                                                                                                                                                               |                       |     |      |     |         |
| Frequency = 1000 MHz      | EMIRR              | V <sub>IN</sub> = 200 mV p-p                                                                                                                                  |                       |     | 64   |     | dB      |
| Frequency = 2400 MHz      | EMIRR              | V <sub>IN</sub> = 200 mV p-p                                                                                                                                  |                       |     | 80   |     | dB      |
| NOISE PERFORMANCE         |                    |                                                                                                                                                               |                       |     |      |     |         |
| Voltage Noise             | e <sub>n p-p</sub> | 0.1 Hz to 10 Hz, V <sub>CM</sub> = 0 V, V <sub>SY</sub> = ±18 V                                                                                               |                       |     | 225  |     | nV p-p  |
| Voltage Noise Density     | e <sub>n</sub>     | f = 1 Hz, V <sub>CM</sub> = 0 V, V <sub>SY</sub> = ±18 V                                                                                                      |                       |     | 16.9 |     | nV/√Hz  |
|                           |                    | f = 10 Hz, V <sub>CM</sub> = 0 V, V <sub>SY</sub> = ±18 V                                                                                                     |                       |     | 7.4  |     |         |
|                           |                    | f = 100 Hz, V <sub>CM</sub> = 0 V, V <sub>SY</sub> = ±18 V                                                                                                    |                       |     | 5.5  |     |         |
|                           |                    | f = 1 kHz, V <sub>CM</sub> = 0 V, V <sub>SY</sub> = ±18 V                                                                                                     |                       |     | 5.1  |     |         |
|                           |                    | f = 10 kHz, V <sub>CM</sub> = 0 V, V <sub>SY</sub> = ±18 V                                                                                                    |                       |     | 5    |     |         |

(Supply voltage  $V_{SY} = \pm 2.25\text{ V}$  to  $\pm 18\text{ V}$  for dual supplies, or  $4.5\text{ V}$  to  $36\text{ V}$  for single supply; common-mode voltage  $V_{CM} = 0\text{ V}$  for dual supplies, or  $(V+)/2\text{ V}$  for single supply;  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

| PARAMETER                           | SYMBOL               | CONDITIONS/COMMENTS                                                                             |                                 | MIN | TYP   | MAX | UNITS  |
|-------------------------------------|----------------------|-------------------------------------------------------------------------------------------------|---------------------------------|-----|-------|-----|--------|
| Current Noise Density               | I <sub>n</sub>       | f = 10 Hz, V <sub>CM</sub> = 0 V, V <sub>SY</sub> = ±18 V                                       |                                 |     | 0.6   |     | fA/√Hz |
| MATCHING ADA4620-2 - (Ch A – Ch B)  |                      |                                                                                                 |                                 |     |       |     |        |
| Offset Voltage Matching             | V <sub>OS</sub>      | V <sub>SY</sub> = ±18 V                                                                         |                                 |     | ±23.6 |     | μV     |
|                                     |                      |                                                                                                 | −40°C < T <sub>A</sub> < +125°C |     | ±38.4 |     |        |
| Offset Voltage Drift <sup>1</sup>   | ΔV <sub>OS</sub> /ΔT | V <sub>SY</sub> = ±18 V                                                                         | −40°C < T <sub>A</sub> < +125°C |     | ±0.16 |     | μV/°C  |
| Input Bias Current Matching         | I <sub>B</sub>       | V <sub>SY</sub> = ±18 V                                                                         |                                 |     | ±0.06 |     | pA     |
|                                     |                      |                                                                                                 | −40°C < T <sub>A</sub> < +125°C |     | ±7    |     |        |
| CROSSTALK ADA4620-2 - (Ch A – Ch B) |                      |                                                                                                 |                                 |     |       |     |        |
| Crosstalk                           | XTLK                 | Frequency = 1 kHz; R <sub>L</sub> = 2 kΩ, V <sub>OUT</sub> = 4 V p-p, V <sub>SY</sub> = ±18 V   |                                 |     | −152  |     | dB     |
|                                     |                      | Frequency = 10 kHz; R <sub>L</sub> = 2 kΩ, V <sub>OUT</sub> = 4 V p-p, V <sub>SY</sub> = ±18 V  |                                 |     | −133  |     |        |
|                                     |                      | Frequency = 100 kHz; R <sub>L</sub> = 2 kΩ, V <sub>OUT</sub> = 4 V p-p, V <sub>SY</sub> = ±18 V |                                 |     | −113  |     |        |

<sup>1</sup> Calculated using the box method. The box method uses the formula  $(V_{OS,MAX} - V_{OS,MIN})/(T_{MAX} - T_{MIN})$ , where  $V_{OS,MAX}$  and  $V_{OS,MIN}$  are the maximum and minimum offset errors characterized over the full temperature range.

## High Common-Mode Voltage Operation ( $(V+) - 4.4\text{ V} < V_{CM} \leq (V+)$ )

**Table 2. High Common-Mode Voltage Operation**

(Supply voltage  $V_{SY} = \pm 18\text{ V}$  for dual supplies, or  $36\text{ V}$  for single supply; common-mode voltage  $V_{CM} = (V+) - 2\text{ V}$ ;  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

| PARAMETER                    | SYMBOL            | CONDITIONS/COMMENTS                                                       |                                 | MIN   | TYP  | MAX | UNITS |
|------------------------------|-------------------|---------------------------------------------------------------------------|---------------------------------|-------|------|-----|-------|
| INPUT CHARACTERISTICS        |                   |                                                                           |                                 |       |      |     |       |
| Offset Voltage               | V <sub>OS</sub>   |                                                                           |                                 | ±2    | ±15  | mV  |       |
|                              |                   | −40°C < T <sub>A</sub> < +125°C                                           |                                 | ±15   |      |     |       |
|                              |                   | V <sub>CM</sub> = V+                                                      | −40°C < T <sub>A</sub> < +125°C | ±22   | ±120 |     |       |
|                              |                   |                                                                           |                                 | ±120  |      |     |       |
| Input Bias Current           | I <sub>B</sub>    |                                                                           |                                 | ±0.12 | ±10  | pA  |       |
|                              |                   | −40°C < T <sub>A</sub> < +125°C                                           |                                 | ±1.5  |      | nA  |       |
| Input Offset Current         | I <sub>OS</sub>   |                                                                           |                                 | ±0.1  | ±6   | pA  |       |
|                              |                   | −40°C < T <sub>A</sub> < +125°C                                           |                                 | ±125  |      |     |       |
| Common-Mode Rejection Ratio  | CMRR              | (V−) − 0.1 V < V <sub>CM</sub> < V+                                       |                                 | 49    | 66   | dB  |       |
|                              |                   |                                                                           | −40°C < T <sub>A</sub> < +125°C | 50    |      |     |       |
| Open-Loop Voltage Gain       | A <sub>VOL</sub>  | R <sub>L</sub> = 10 kΩ, V <sub>OUT</sub> = ±17.8 V                        |                                 | 100   |      | dB  |       |
|                              |                   | R <sub>L</sub> = 2 kΩ, V <sub>OUT</sub> = ±17.8 V                         |                                 | 67    |      |     |       |
| Input Capacitance            | C <sub>INDM</sub> | Differential mode                                                         |                                 | 5     |      | pF  |       |
|                              | C <sub>INCM</sub> | Common mode                                                               |                                 | 18.2  |      |     |       |
| Input Resistance             | R <sub>INDM</sub> | Differential mode                                                         |                                 | 29    |      | GΩ  |       |
|                              | R <sub>INCM</sub> | Common mode                                                               |                                 | 10    |      | TΩ  |       |
| OUTPUT CHARACTERISTICS       |                   |                                                                           |                                 |       |      |     |       |
| Closed-Loop Output Impedance | Z <sub>OUT</sub>  | f = 1 kHz, A <sub>V</sub> = +1                                            |                                 | 45    |      | mΩ  |       |
|                              |                   | f = 1 kHz, A <sub>V</sub> = +10                                           |                                 | 0.5   |      | Ω   |       |
|                              |                   | f = 1 kHz, A <sub>V</sub> = +100                                          |                                 | 5.5   |      |     |       |
| POWER SUPPLY                 |                   |                                                                           |                                 |       |      |     |       |
| Power Supply Rejection Ratio | PSRR−             | V+ = 4.5 V, V <sub>CM</sub> = (V+) − 2 V, V− stepped from −31.5 V to 0 V  |                                 | 86    | 89   | dB  |       |
|                              |                   |                                                                           | −40°C < T <sub>A</sub> < +125°C | 78    |      |     |       |
| Supply Current per Amplifier | I <sub>SY</sub>   | I <sub>OUT</sub> = 0 mA, V <sub>SY</sub> = ±2.25 V, V <sub>CM</sub> = 0 V |                                 | 1.1   | 1.2  | mA  |       |
|                              |                   |                                                                           | −40°C < T <sub>A</sub> < +125°C |       | 1.6  |     |       |
|                              |                   | I <sub>OUT</sub> = 0 mA, V <sub>SY</sub> = ±18 V                          |                                 | 1.2   | 1.3  |     |       |
|                              |                   |                                                                           | −40°C < T <sub>A</sub> < +125°C |       | 1.7  |     |       |
| Operating Range              | V <sub>SY</sub>   | Guaranteed by PSRR                                                        |                                 | 4.5   | 36   | V   |       |

(Supply voltage  $V_{SY} = \pm 18\text{ V}$  for dual supplies, or  $36\text{ V}$  for single supply; common-mode voltage  $V_{CM} = (V+) - 2\text{ V}$ ;  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

| PARAMETER              | SYMBOL             | CONDITIONS/COMMENTS                                                                                                 |           | MIN | TYP  | MAX     | UNITS |
|------------------------|--------------------|---------------------------------------------------------------------------------------------------------------------|-----------|-----|------|---------|-------|
| DYNAMIC PERFORMANCE    |                    |                                                                                                                     |           |     |      |         |       |
| Slew Rate              | SR                 | R <sub>L</sub> = 2 kΩ, V <sub>OUT</sub> = ±5 V, A <sub>V</sub> = −10, V <sub>IN+</sub> = 16 V                       | 10% - 90% | 5.2 |      | V/μs    |       |
|                        |                    |                                                                                                                     | 90% - 10% | 4.6 |      |         |       |
| Gain Bandwidth Product | GBP                | R <sub>L</sub> = Open, C <sub>L</sub> = 50 pF, Measured at 100 kHz                                                  |           |     | 13   | MHz     |       |
| Unity-Gain Crossover   | UGC                | R <sub>L</sub> = Open, C <sub>L</sub> = 50 pF                                                                       |           |     | 11   | MHz     |       |
| Phase Margin           | PM                 | R <sub>L</sub> = Open, C <sub>L</sub> = 50 pF                                                                       |           |     | 51   | Degrees |       |
| Overload Recovery Time | OLR+               | R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 50 pF, A <sub>V</sub> = −10, Step = +6 V to +16 V, V <sub>CM</sub> = +16 V  |           |     | 1.1  | μs      |       |
|                        | OLR−               | R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 50 pF, A <sub>V</sub> = −10, Step = +26 V to +16 V, V <sub>CM</sub> = +16 V |           |     | 0.17 |         |       |
| NOISE PERFORMANCE      |                    |                                                                                                                     |           |     |      |         |       |
| Voltage Noise          | e <sub>n p-p</sub> | 0.1 Hz to 10 Hz, V <sub>CM</sub> = 0 V                                                                              |           |     | 1.8  | μV p-p  |       |
| Voltage Noise Density  | e <sub>n</sub>     | f = 1 Hz                                                                                                            |           |     | 139  | nV/√Hz  |       |
|                        |                    | f = 10 Hz                                                                                                           |           |     | 50   |         |       |
|                        |                    | f = 100 Hz                                                                                                          |           |     | 26   |         |       |
|                        |                    | f = 1 kHz                                                                                                           |           |     | 21   |         |       |
|                        |                    | f = 10 kHz                                                                                                          |           |     | 20   |         |       |
| Current Noise Density  | I <sub>n</sub>     | f = 10 Hz                                                                                                           |           |     | 1.2  | fA/√Hz  |       |

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$  unless otherwise specified.

**Table 3. Absolute Maximum Ratings**

| PARAMETER                                  | RATING                                        |
|--------------------------------------------|-----------------------------------------------|
| Supply Voltage ( $(V+) - (V-)$ )           | 40 V                                          |
| Input Voltage Single-Ended                 | $(V-) - 0.3\text{ V to } (V+) + 0.3\text{ V}$ |
| Input Voltage Differential                 | $((V+) - (V-)) + 0.6\text{ V}$                |
| Output Voltage ( $V_{OUT}$ )               | $(V-) - 0.3\text{ V to } (V+) + 0.3\text{ V}$ |
| Input Current ( $I_{+IN}$ , $I_{-IN}$ )    | 20 mA                                         |
| Output Short-Circuit Duration <sup>1</sup> | Continuous                                    |
| Storage Temperature                        | $-65^\circ\text{C to } +150^\circ\text{C}$    |
| Operating Temperature                      | $-40^\circ\text{C to } +125^\circ\text{C}$    |
| Junction Temperature                       | $-65^\circ\text{C to } +150^\circ\text{C}$    |
| Lead Temperature Soldering, 10 s           | 300°C                                         |

<sup>1</sup> A heatsink may be required to keep the  $T_J$  below the absolute maximum rating when the output is shorted indefinitely.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## Thermal Characteristics

Thermal performance is directly linked to the PCB design and operating environment. Close attention to PCB thermal design is required.

$\Theta_{JA}$  is the junction-to-ambient thermal resistance.

$\Theta_{JC}$  is the junction-to-case thermal resistance.

**Table 4. Thermal Resistance**

| Package Type     | $\Theta_{JA}$ | $\Theta_{JC}$ | Unit               |
|------------------|---------------|---------------|--------------------|
| <b>ADA4620-1</b> |               |               |                    |
| SOIC_N (R-8)     | 115.5         | 46.3          | $^\circ\text{C/W}$ |
| <b>ADA4620-2</b> |               |               |                    |
| SOIC_N (R-8)     | 110.1         | 47.5          | $^\circ\text{C/W}$ |

## Maximum Power Dissipation

The maximum safe power dissipation in the ADA4620 SOIC-8 package is limited by the associated rise in junction temperature ( $T_J$ ) on the die. The plastic encapsulating the die locally reaches the junction temperature. At approximately  $150^\circ\text{C}$ , which is the glass transition temperature, the plastic changes its properties. Even temporarily

exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4620. Exceeding a junction temperature of 175°C for an extended time can cause changes in the silicon devices, potentially causing failure.

The still air thermal properties of the package and PCB ( $\theta_{JA}$ ), ambient temperature ( $T_A$ ), and total power dissipated in the package ( $P_D$ ) determine the junction temperature of the die. The junction temperature can be calculated by:

$$T_J = T_A + (P_D \times \theta_{JA})$$

The power dissipated in the package ( $P_D$ ) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. In most situations, the package temperature rise is governed by the average power dissipation. The average power dissipation comprises two parts: quiescent power and output stage power. The quiescent power is the voltage between the supply pins ( $V_{SY}$ ) times the quiescent current ( $I_{SY}$ ). The calculation of the output stage power dissipation depends on the output waveforms and load. This calculation also must be broken down into two pieces: the power dissipated when sourcing output current, and the power dissipated when sinking current. Normally, when sourcing current, the current flows from the positive rail,  $V_+$ , into the load. The voltage drop across the output stage is  $(V_+ - V_{OUT})$  and the power dissipation is  $(V_+ - V_{OUT}) \times |I_{LOAD}|$ . Similarly, when sinking current, the voltage drop across the output stage is  $(V_{OUT} - V_-)$  and the power dissipation is  $(V_{OUT} - V_-) \times |I_{LOAD}|$ .

With a sinusoidally-driven resistive load,  $R_L$ , referenced to mid-supply, and driven with a voltage amplitude,  $A$ , the quiescent power dissipation is  $V_{SY} \times I_{SY}$ . The average output power dissipation per cycle when sourcing current is:

$$P_{source} = \frac{1}{T} \int_0^{T/2} \left( \frac{V_{SY}}{2} - A \sin\left(\frac{2\pi t}{T}\right) \right) \left( \frac{A}{R_L} \sin\left(\frac{2\pi t}{T}\right) \right) dt = \frac{A \times V_{SY}}{2\pi R_L} - \frac{A^2}{4R_L}$$

The average output power dissipation per cycle when sinking current is:

$$P_{sink} = \frac{1}{T} \int_{T/2}^T \left( A \sin\left(\frac{2\pi t}{T}\right) + \frac{V_{SY}}{2} \right) \left( -\frac{A}{R_L} \sin\left(\frac{2\pi t}{T}\right) \right) dt = \frac{A \times V_{SY}}{2\pi R_L} - \frac{A^2}{4R_L}$$

The total power dissipation equals the sum of the quiescent power and power dissipated sourcing and sinking:

$$P_{total} = P_{quiescent} + P_{source} + P_{sink}$$

$$P_{total} = V_{SY} \times I_{SY} + \frac{A \times V_{SY}}{\pi R_L} - \frac{A^2}{2R_L}$$

The worst-case power dissipation occurs when  $A = V_{SY}/\pi$  and:

$$P_{total} = V_{SY} \times I_{SY} + \frac{V_{SY}^2}{2\pi^2 R_L}$$

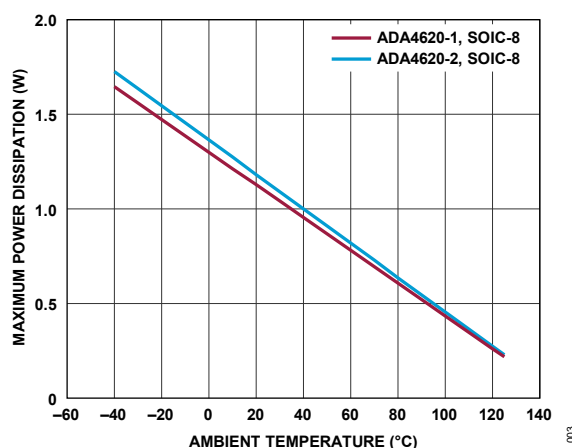


**Figure 3. Maximum Power Dissipation vs. Temperature**

Airflow increases heat dissipation, effectively reducing  $\theta_{JA}$ . Also, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduce the  $\theta_{JA}$ .

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the SOIC-8 (125°C/W) package on a JEDEC standard 4-layer board.  $\theta_{JA}$  values are approximations.

## Electrostatic Discharge (ESD) Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field-induced charged device model (FICDM) and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

## ESD Ratings for AD4620-1

**Table 5. ADA4620-1, 8-Lead SOIC\_N (R-8)**

| ESD Model | Withstand Threshold (V) | Class |
|-----------|-------------------------|-------|
| HBM       | ±1750                   | 1C    |
| FICDM     | ±1000                   | C3    |

## ESD Ratings for AD4620-2

**Table 6. ADA4620-2, 8-Lead SOIC\_N (R-8)**

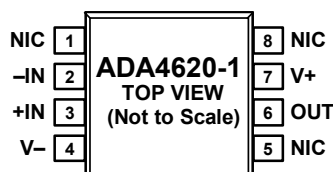
| ESD Model | Withstand Threshold (V) | Class |
|-----------|-------------------------|-------|
| HBM       | ±1500                   | 1C    |
| FICDM     | ±1000                   | C3    |

### ESD Caution



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES  
1. NIC = NOT INTERNALLY CONNECTED. 004

Figure 4. ADA4620-1, 8-Lead SOIC\_N (R-8) Pin Configuration

Table 7. ADA4620-1 Pin Descriptions, 8-Lead SOIC (R-8)

| PIN     | NAME | DESCRIPTION              |
|---------|------|--------------------------|
| 1, 5, 8 | NIC  | Not Internally Connected |
| 2       | -IN  | Inverting Input          |
| 3       | +IN  | Noninverting Input       |
| 4       | V-   | Negative Supply Voltage  |
| 6       | OUT  | Output                   |
| 7       | V+   | Positive Supply Voltage  |

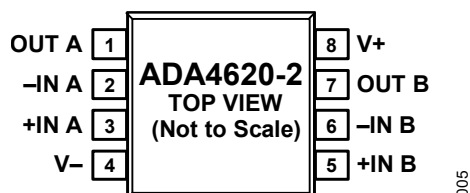


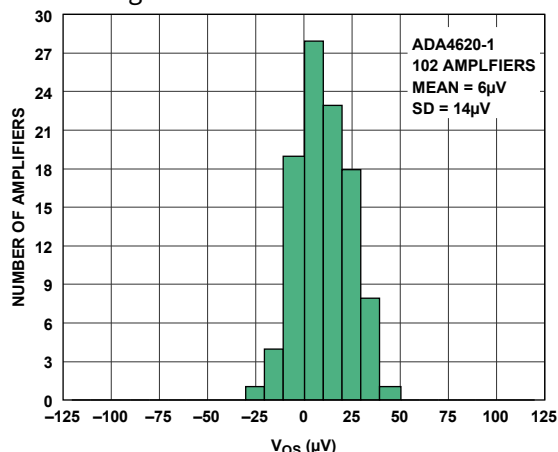
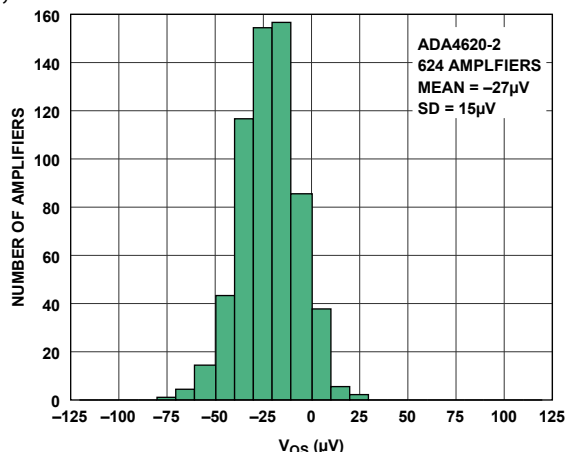
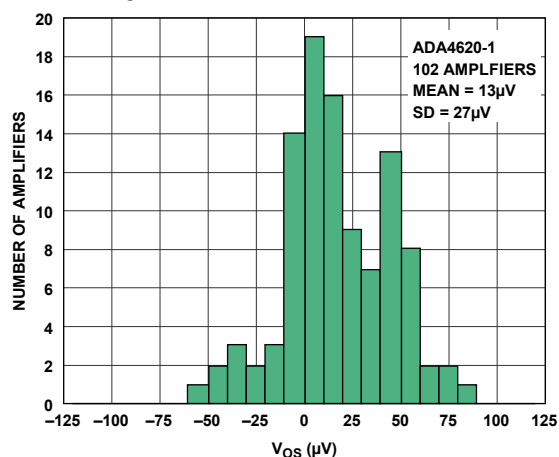
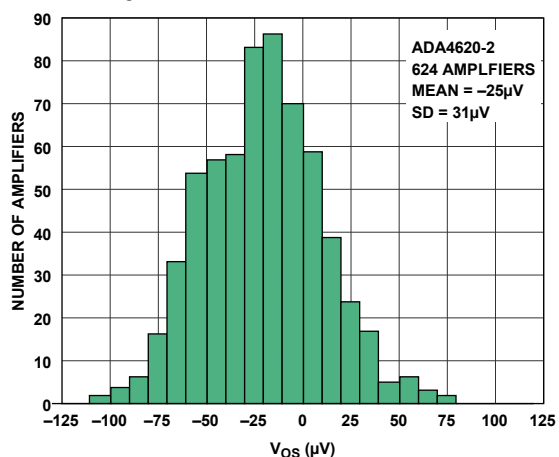
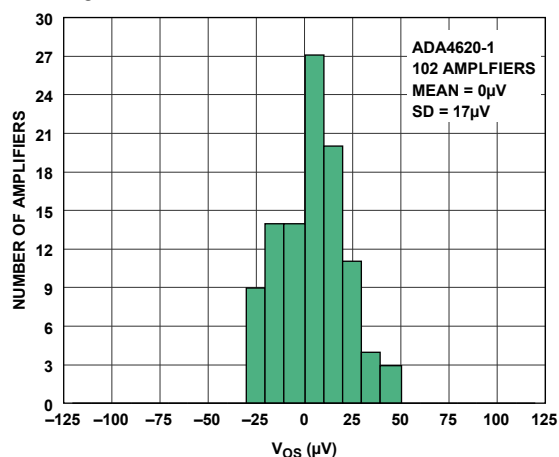
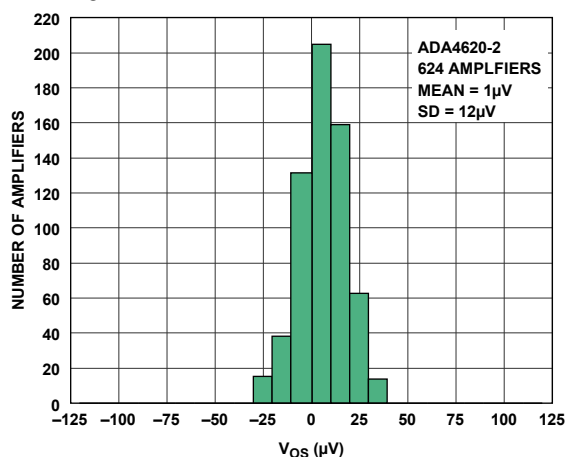
Figure 5. ADA4620-2, 8-Lead SOIC\_N (R-8) Pin Configuration

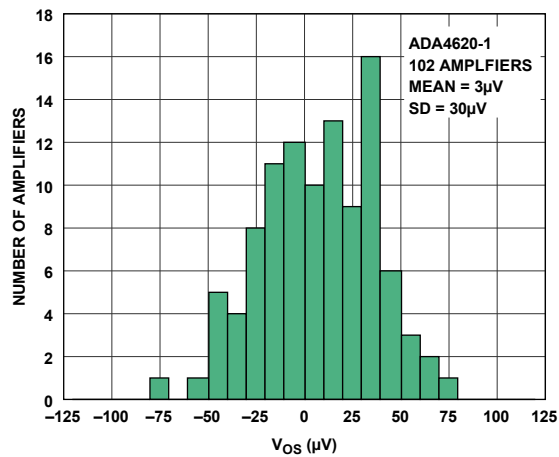
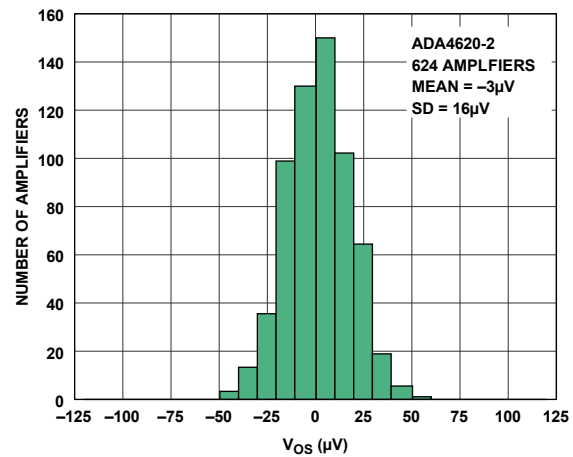
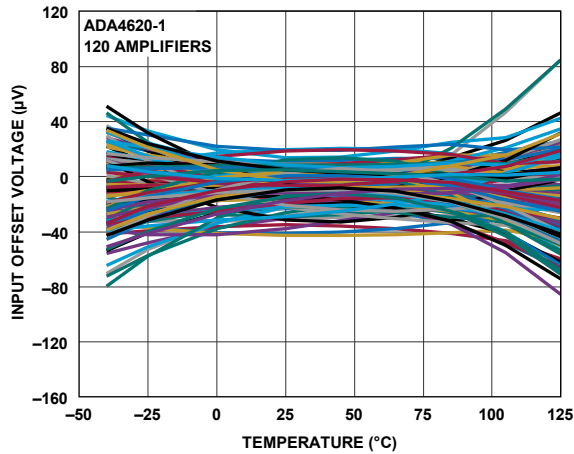
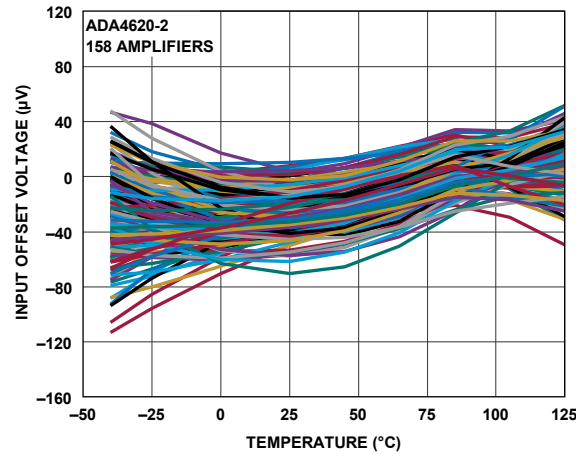
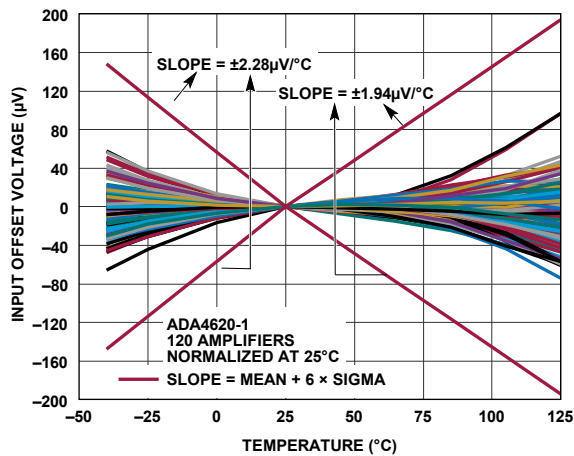
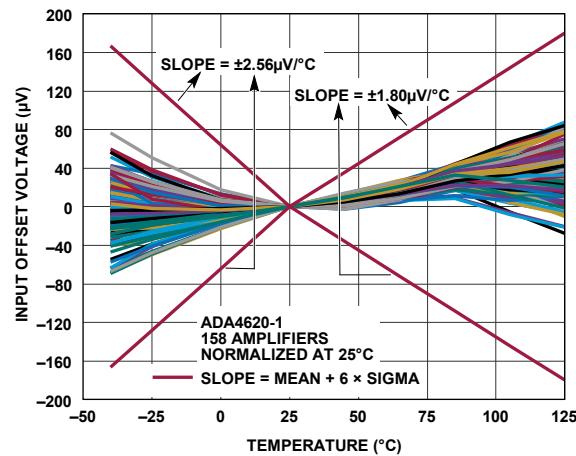
Table 8. ADA4620-2 Pin Descriptions, 8-Lead SOIC (R-8)

| PIN | NAME  | DESCRIPTION                   |
|-----|-------|-------------------------------|
| 1   | OUT A | Output, Channel A             |
| 2   | -IN A | Inverting Input, Channel A    |
| 3   | +IN A | Noninverting Input, Channel A |
| 4   | V-    | Negative Supply Voltage       |
| 5   | +IN B | Noninverting Input, Channel B |
| 6   | -IN B | Inverting Input, Channel B    |
| 7   | OUT B | Output, Channel B             |
| 8   | V+    | Positive Supply Voltage       |

## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{SY} = \pm 18\text{ V}$ ,  $R_L = 2\text{ k}\Omega$ ,  $C_L = 50\text{ pF}$ ; common-mode voltage  $V_{CM} = 0\text{ V}$  for dual supplies, or  $(V+)/2\text{ V}$  for single supply;  $T_A = 25^\circ\text{C}$ . The figures refer to both ADA4620-1 and ADA4620-2, unless otherwise noted.

Figure 6. ADA4620-1  $V_{OS}$  DistributionFigure 7. ADA4620-2  $V_{OS}$  DistributionFigure 8. ADA4620-1  $V_{OS}$  Distribution ( $-40^\circ\text{C}$ )Figure 9. ADA4620-2  $V_{OS}$  Distribution ( $-40^\circ\text{C}$ )Figure 10. ADA4620-1  $V_{OS}$  Distribution ( $+85^\circ\text{C}$ )Figure 11. ADA4620-2  $V_{OS}$  Distribution ( $+85^\circ\text{C}$ )

Figure 12. ADA4620-1  $V_{OS}$  Distribution (+125°C)Figure 13. ADA4620-2  $V_{OS}$  Distribution (+125°C)Figure 14. ADA4620-1  $V_{OS}$  vs. TemperatureFigure 15. ADA4620-2  $V_{OS}$  vs. TemperatureFigure 16. ADA4620-1  $V_{OS}$  vs. Temperature, Bowtie MethodFigure 17. ADA4620-2  $V_{OS}$  vs. Temperature, Bowtie Method

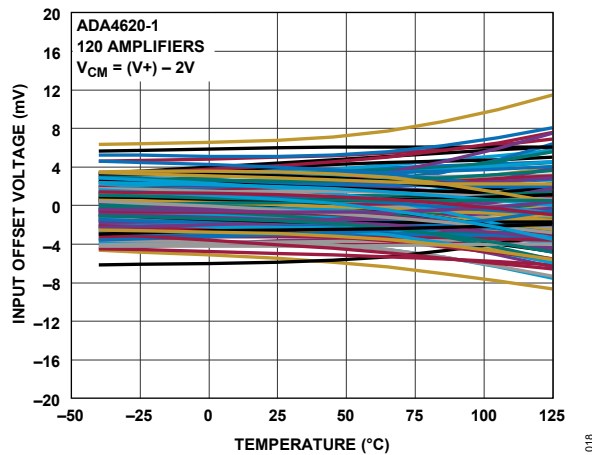


Figure 18. ADA4620-1  $V_{OS}$  vs. Temperature, High  $V_{CM}$  Operation

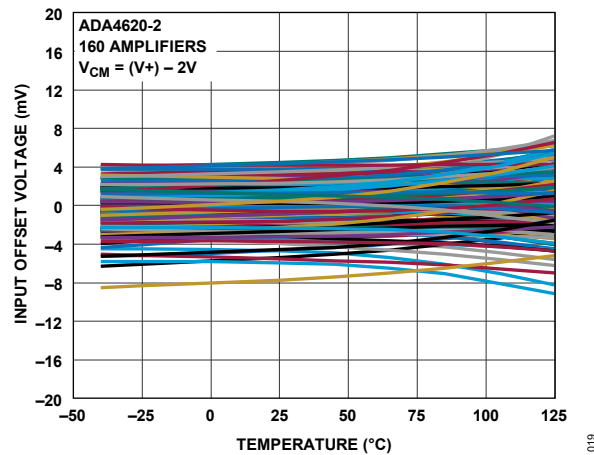


Figure 19. ADA4620-2  $V_{OS}$  vs. Temperature, High  $V_{CM}$  Operation

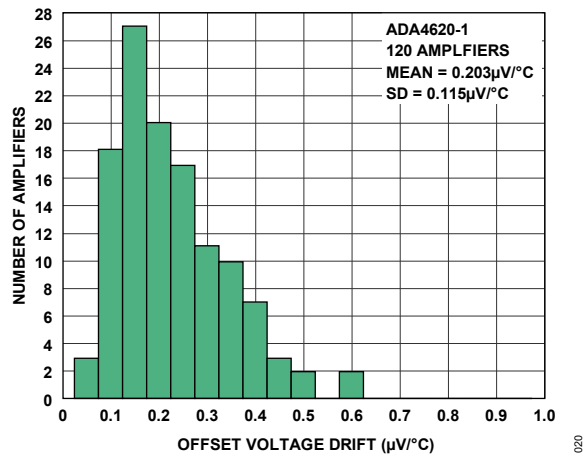


Figure 20. ADA4620-1  $TCV_{OS}$  Distribution (+25°C to +125°C)

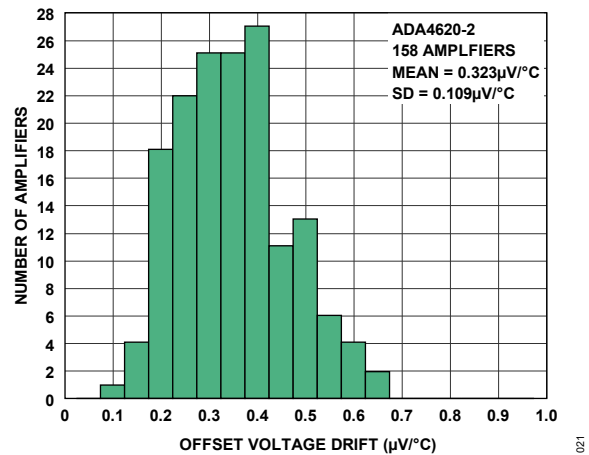


Figure 21. ADA4620-2  $TCV_{OS}$  Distribution (+25°C to +125°C)

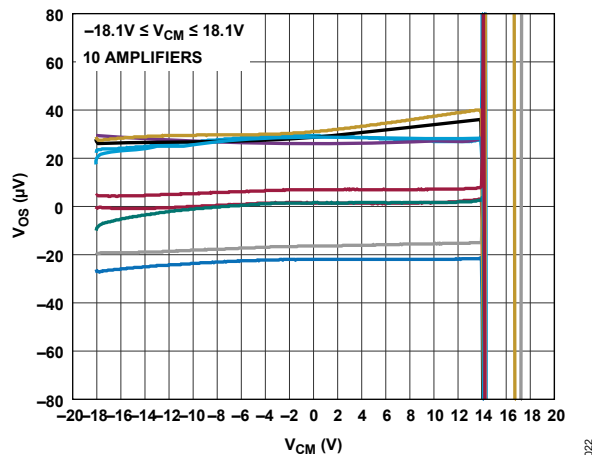


Figure 22.  $V_{OS}$  vs.  $V_{CM}$

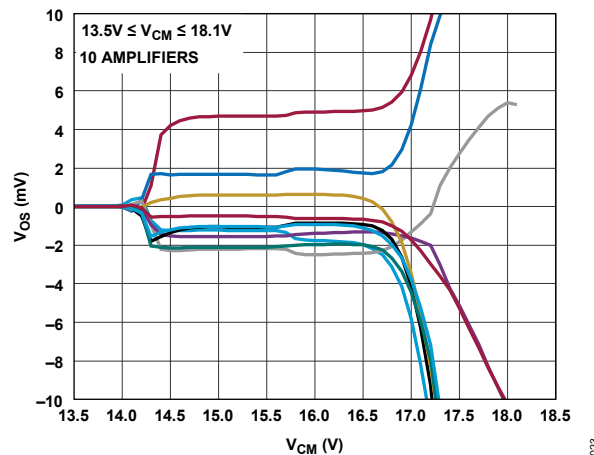
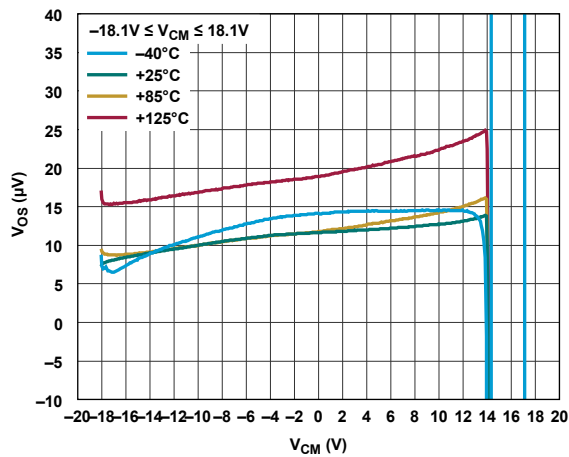
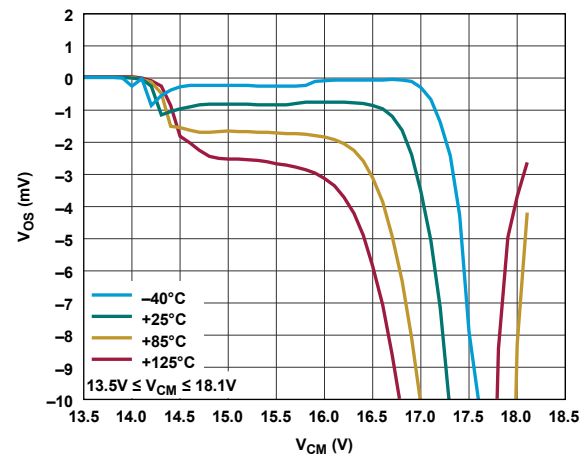
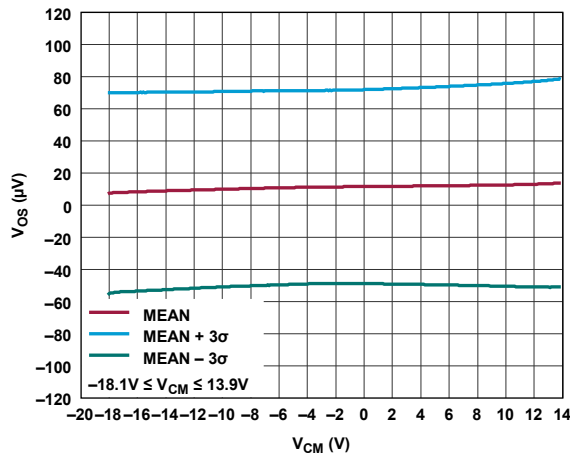
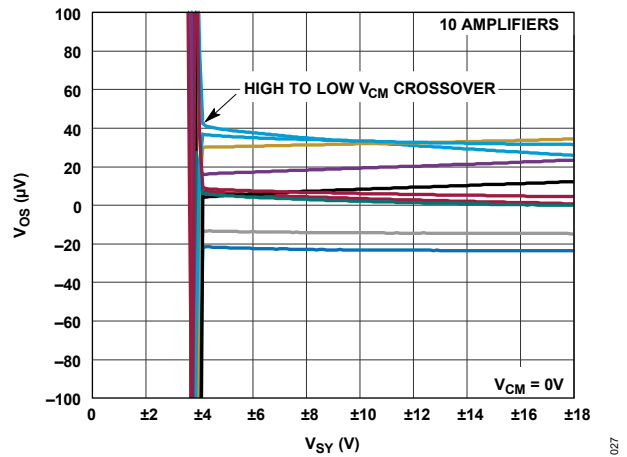
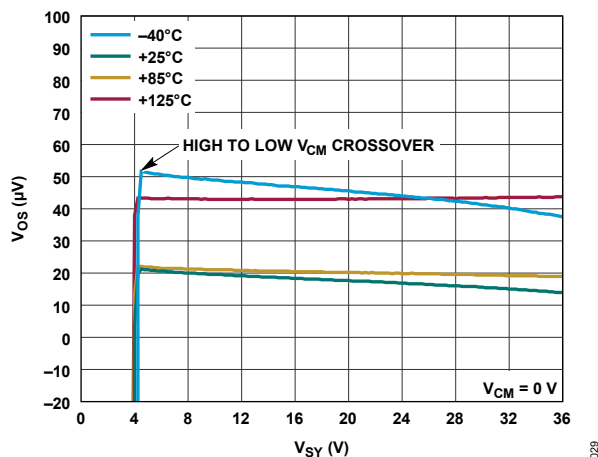
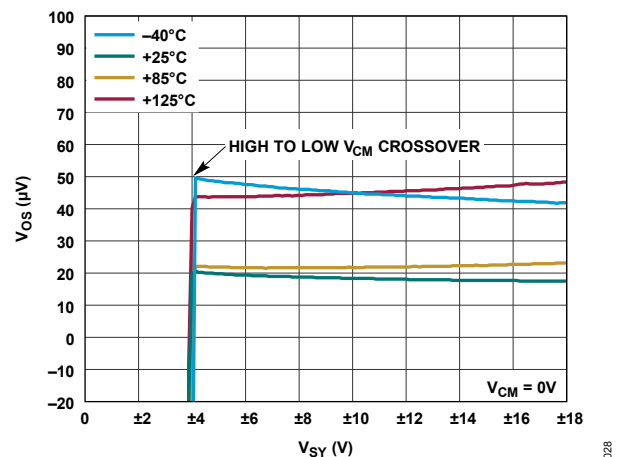
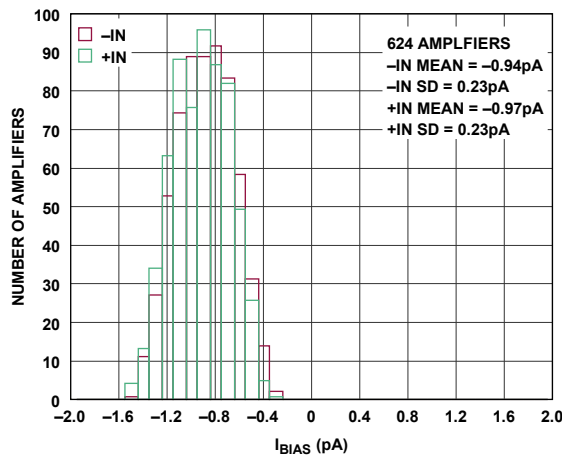
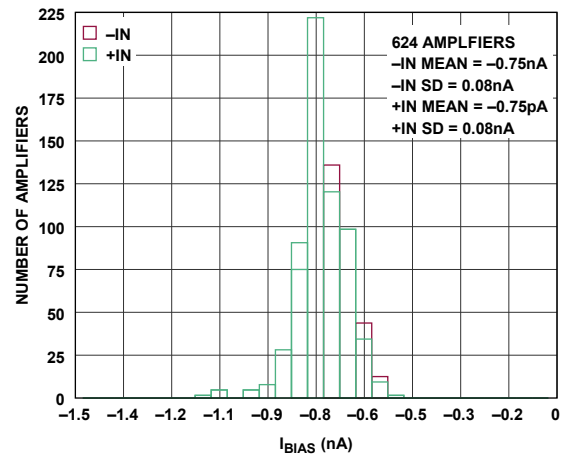
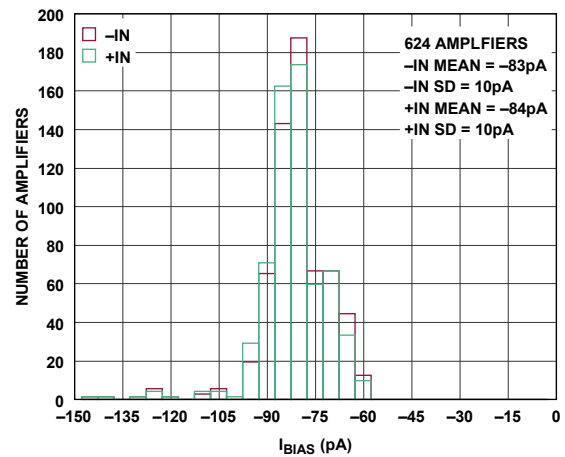
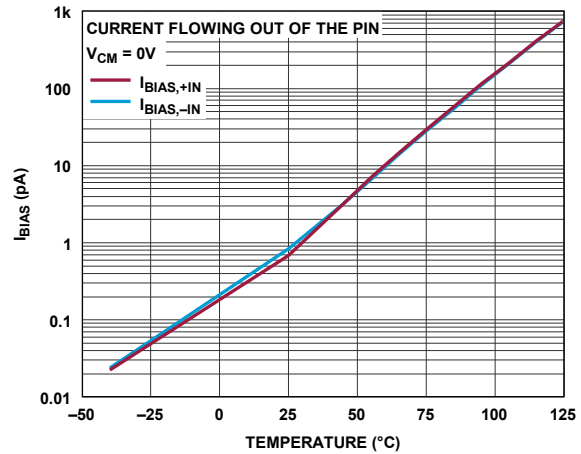
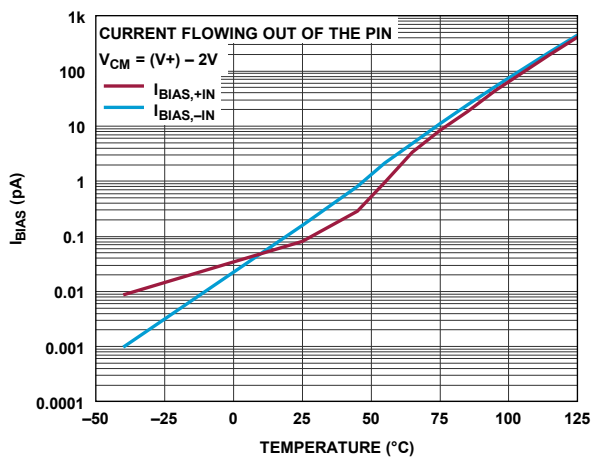
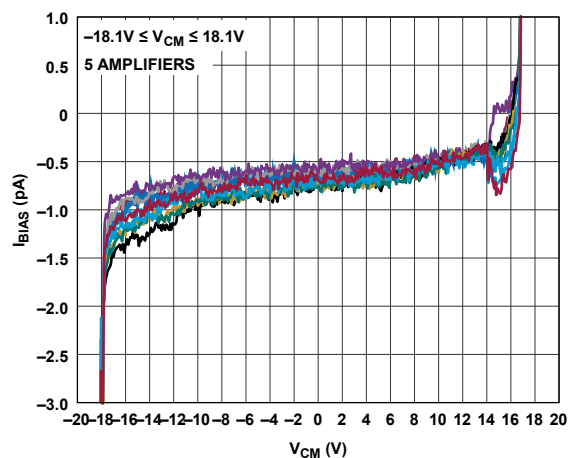
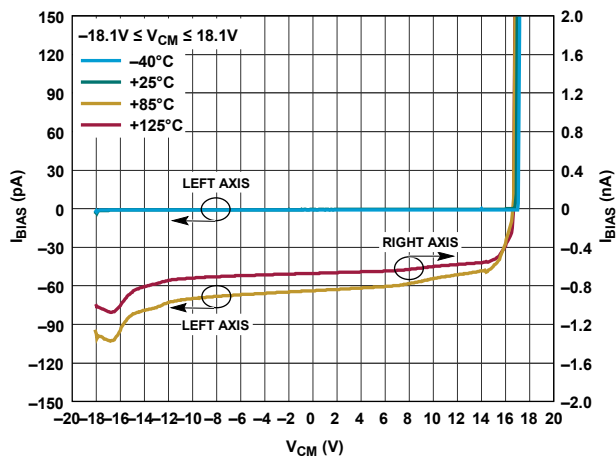
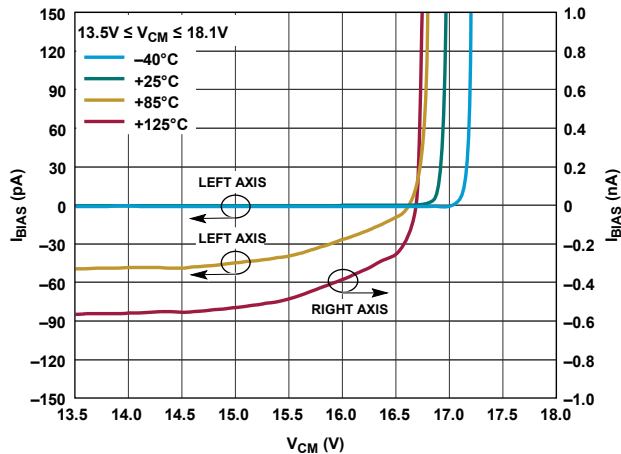
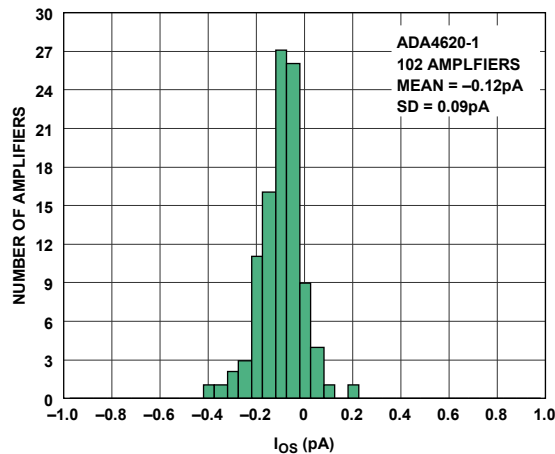
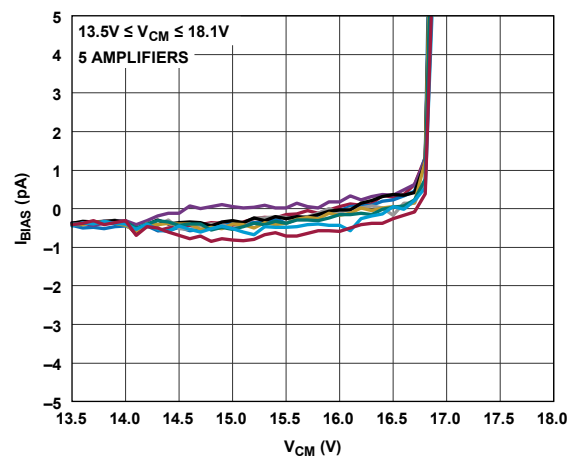
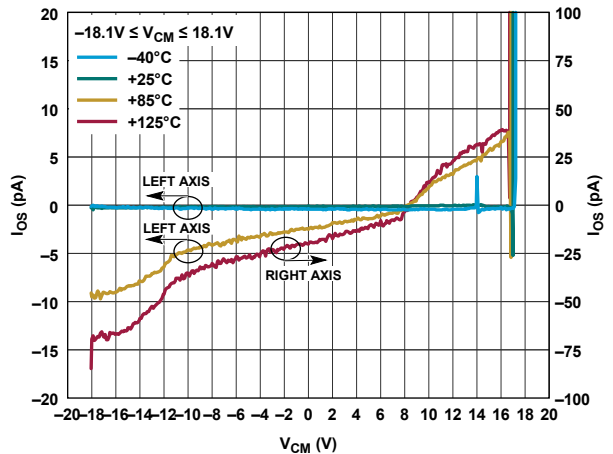
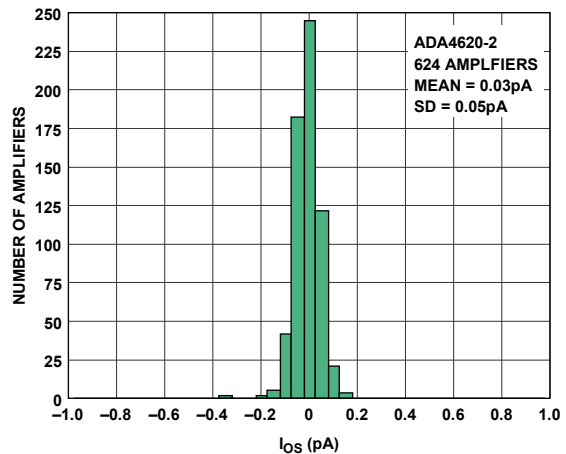
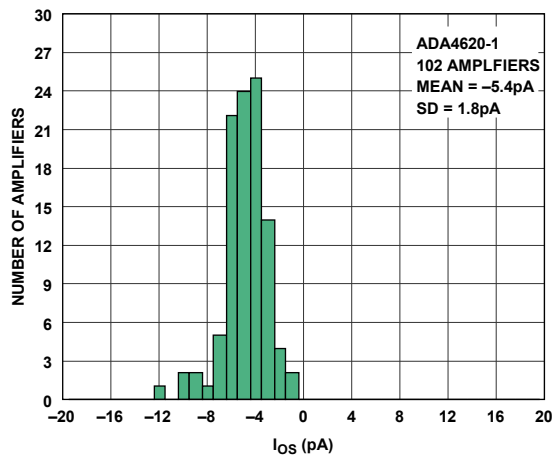
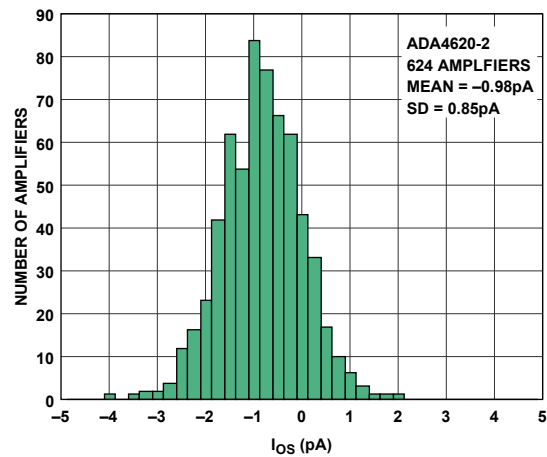
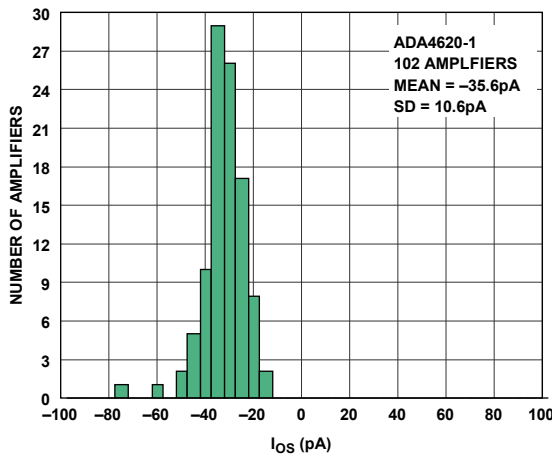
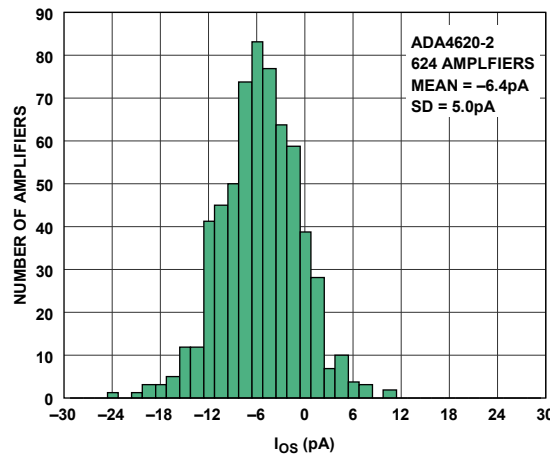
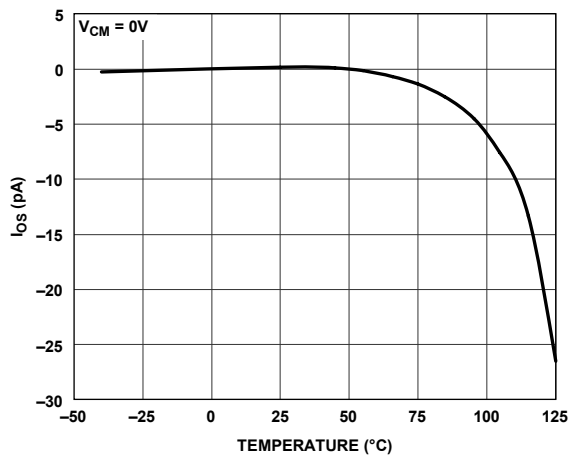
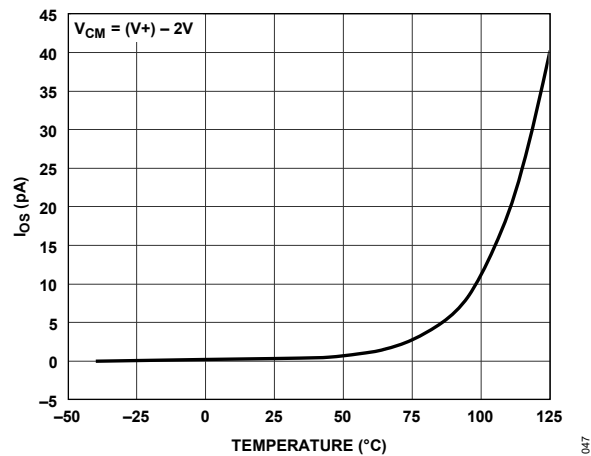


Figure 23.  $V_{OS}$  vs.  $V_{CM}$ , High  $V_{CM}$  Operation

Figure 24.  $V_{OS}$  vs.  $V_{CM}$ , Four TemperaturesFigure 25.  $V_{OS}$  vs.  $V_{CM}$ , High  $V_{CM}$  Operation, Four TemperaturesFigure 26.  $V_{OS}$  vs.  $V_{CM}$ , Mean,  $\pm 3$  SigmaFigure 27.  $V_{OS}$  vs.  $V_{SY}$ , Dual SupplyFigure 28.  $V_{OS}$  vs.  $V_{SY}$ , Single Supply, Four TemperaturesFigure 29.  $V_{OS}$  vs.  $V_{SY}$ , Dual Supply, Four Temperatures

Figure 30.  $I_{BIAS}$  DistributionFigure 32.  $I_{BIAS}$  Distribution (+125°C)Figure 31.  $I_{BIAS}$  Distribution (+85°C)Figure 33.  $I_{BIAS}$  vs. TemperatureFigure 34.  $I_{BIAS}$  vs. Temperature, High  $V_{CM}$  OperationFigure 35.  $I_{BIAS}$  vs.  $V_{CM}$  ( $I_{BIAS+}$  and  $I_{BIAS-}$ )

Figure 36.  $I_{BIAS}$  vs.  $V_{CM}$ , Four TemperaturesFigure 38.  $I_{BIAS}$  vs.  $V_{CM}$ , High  $V_{CM}$  Operation, Four TemperaturesFigure 40. ADA4620-1  $I_{OS}$  DistributionFigure 37.  $I_{BIAS}$  vs.  $V_{CM}$ , High  $V_{CM}$  OperationFigure 39.  $I_{OS}$  vs.  $V_{CM}$ , Four TemperaturesFigure 41. ADA4620-2  $I_{OS}$  Distribution

Figure 42. ADA4620-1  $I_{OS}$  Distribution (+85°C)Figure 43. ADA4620-2  $I_{OS}$  Distribution (+85°C)Figure 44. ADA4620-1  $I_{OS}$  Distribution (+125°C)Figure 45. ADA4620-2  $I_{OS}$  Distribution (+125°C)Figure 46.  $I_{OS}$  vs TemperatureFigure 47.  $I_{OS}$  vs Temperature, High  $V_{CM}$  Operation

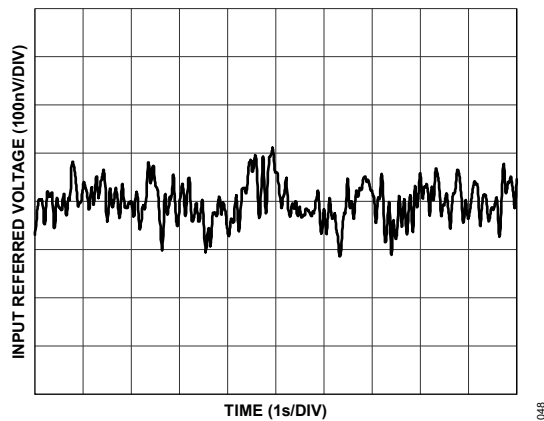


Figure 48. 0.1 Hz to 10 Hz Voltage Noise

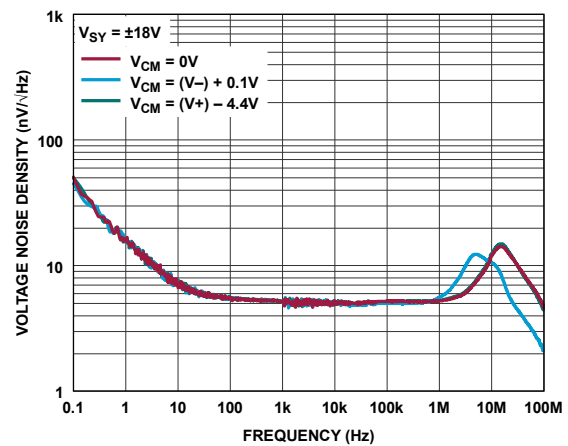


Figure 49. Voltage Noise vs. Frequency

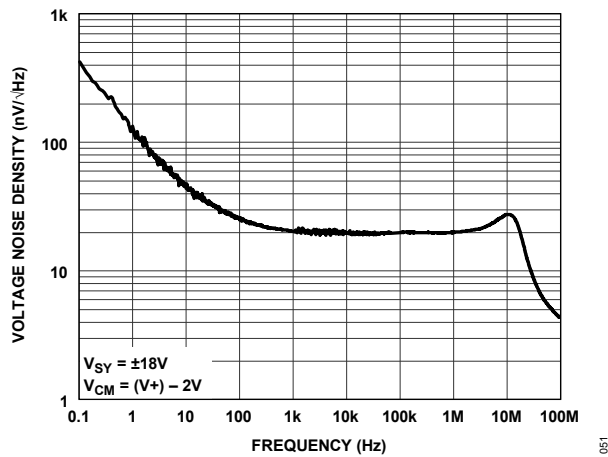
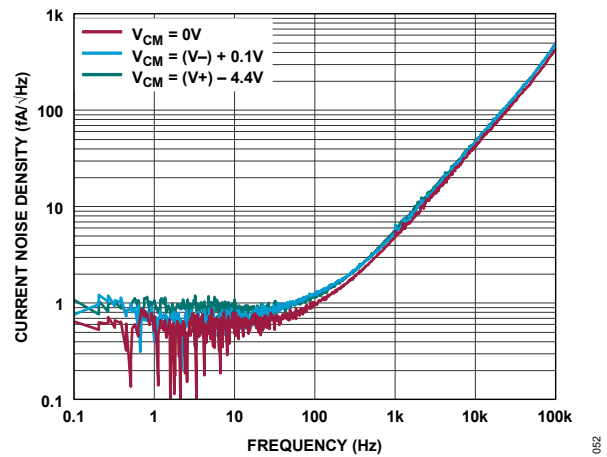
Figure 50. Voltage Noise vs. Frequency, High  $V_{CM}$  Operation

Figure 51. Current Noise vs. Frequency

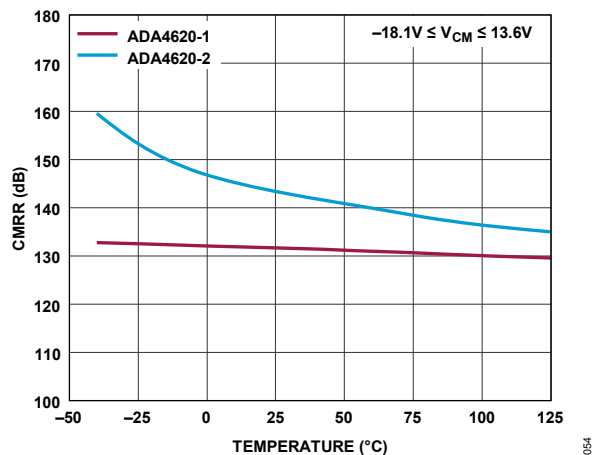


Figure 52. CMRR vs. Temperature

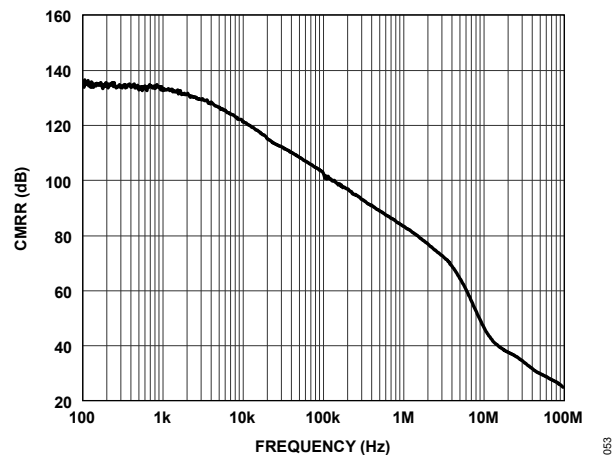


Figure 53. CMRR vs. Frequency

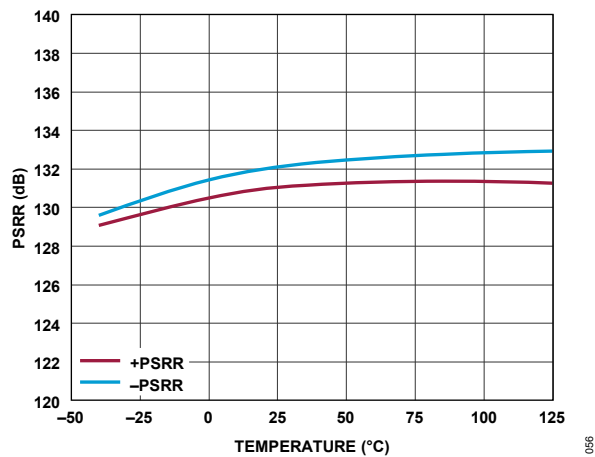


Figure 54. PSRR vs. Temperature

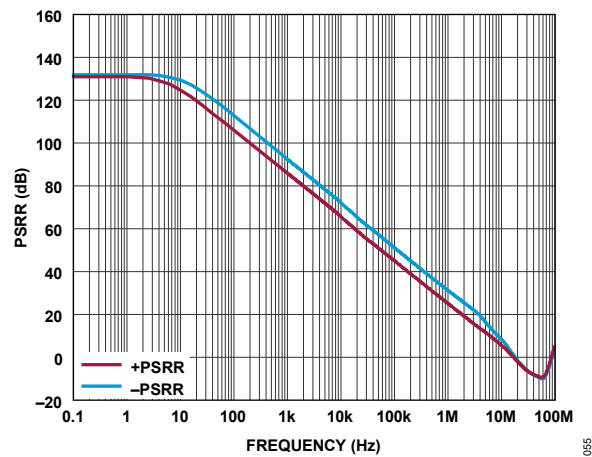
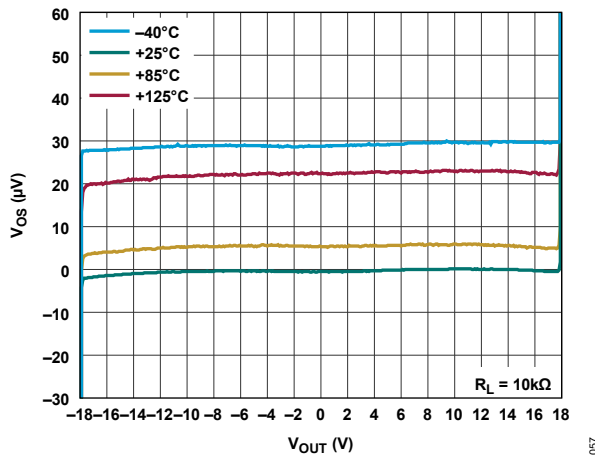
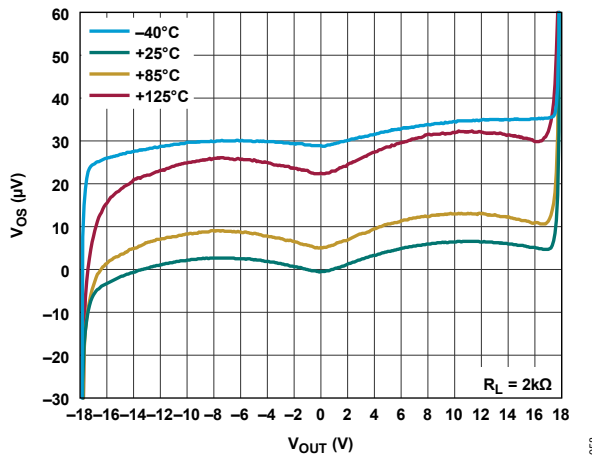
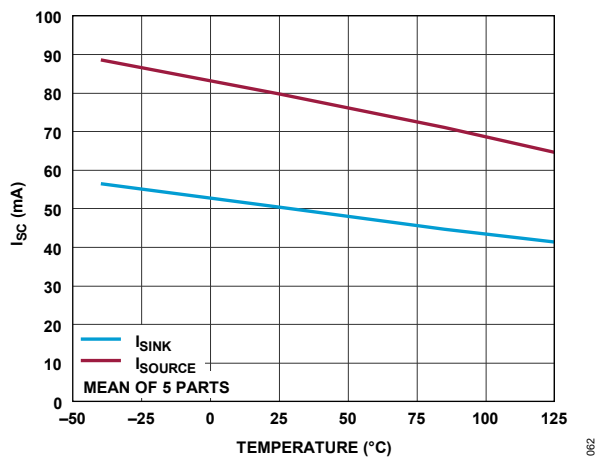
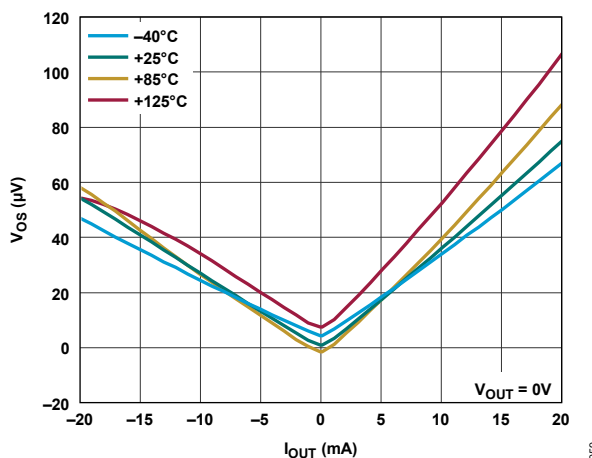


Figure 55. PSRR vs. Frequency

Figure 56.  $V_{OS}$  vs  $V_{OUT}$ , Four Temperatures,  $R_L = 10\text{ k}\Omega$ Figure 57.  $V_{OS}$  vs  $V_{OUT}$ , Four Temperatures,  $R_L = 2\text{ k}\Omega$ Figure 58.  $I_{SC}$  vs. TemperatureFigure 59.  $V_{OS}$  vs.  $I_{OUT}$ , Four Temperatures

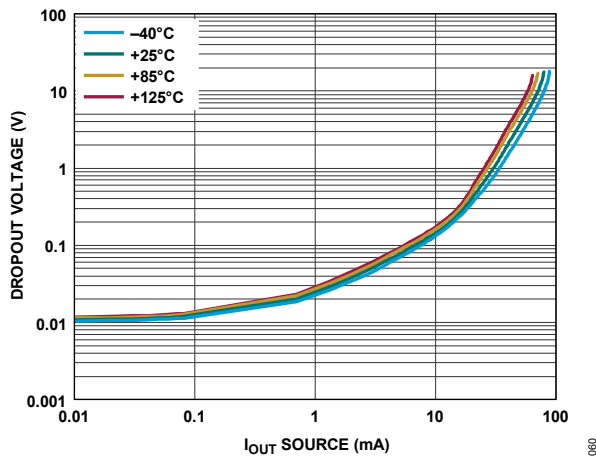
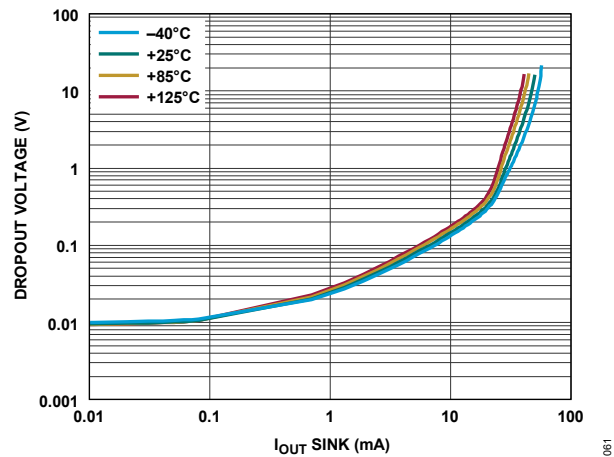
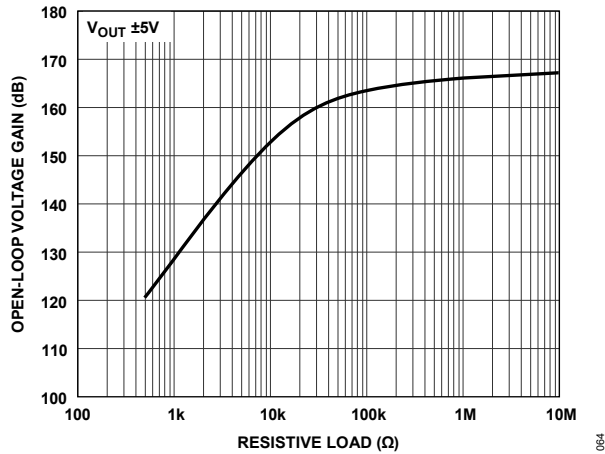
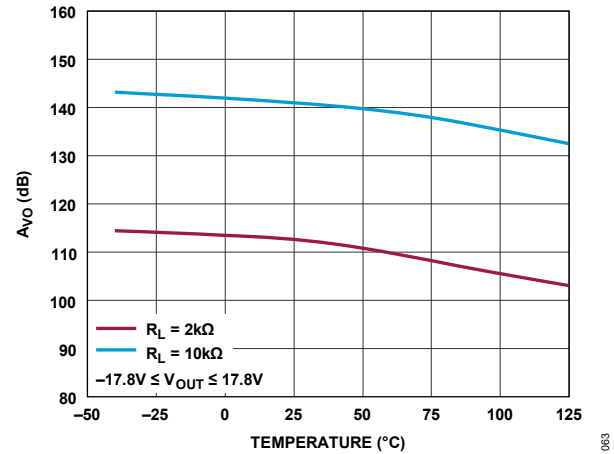
Figure 60. Dropout Voltage ( $V^+ - V_{OUT}$ ) vs.  $I_{OUT}$  SourceFigure 61. Dropout Voltage ( $V_{OUT} - V^-$ ) vs.  $I_{OUT}$  SinkFigure 62. DC Open-Loop Gain vs.  $R_L$ 

Figure 63. DC Open-Loop Gain vs. Temperature

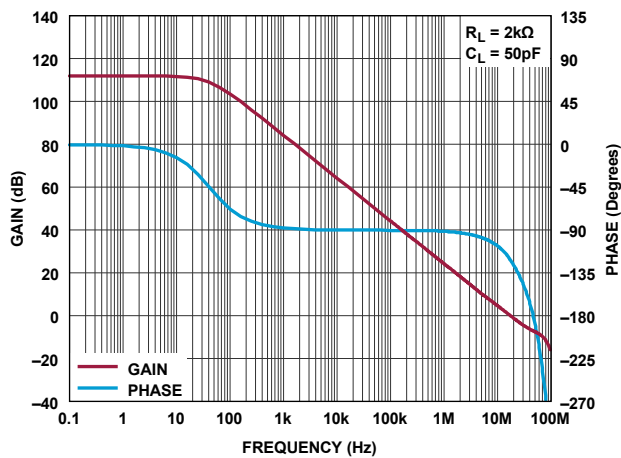


Figure 64. Open-Loop Gain and Phase vs. Frequency (+25°C)

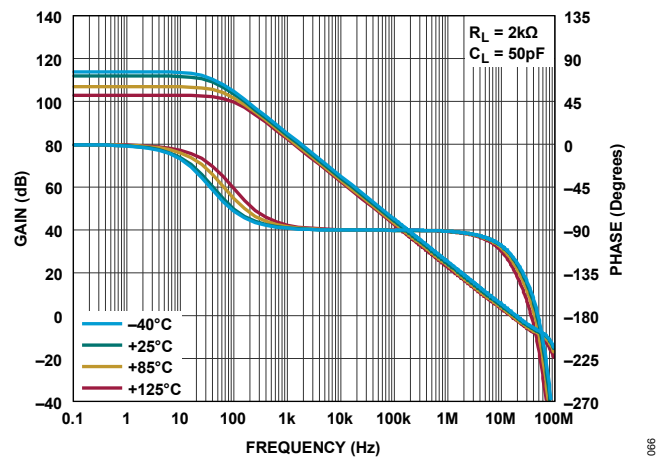


Figure 65. Open-Loop Gain and Phase vs. Frequency and Four Temperatures

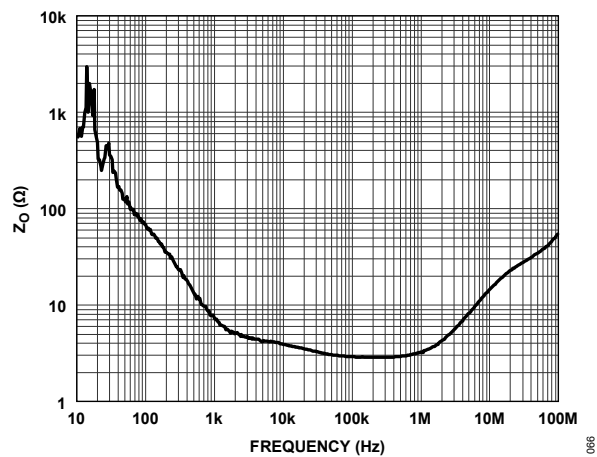


Figure 66. Open-Loop Output Impedance ( $Z_o$ ) vs. Frequency

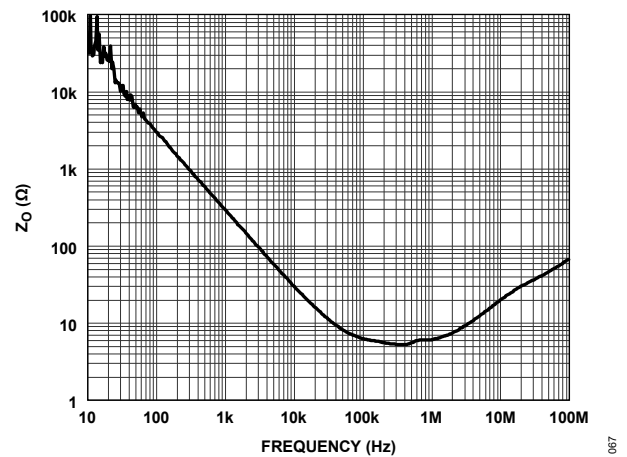


Figure 67. Open-Loop Output Impedance ( $Z_o$ ) vs. Frequency, High  $V_{CM}$  Operation

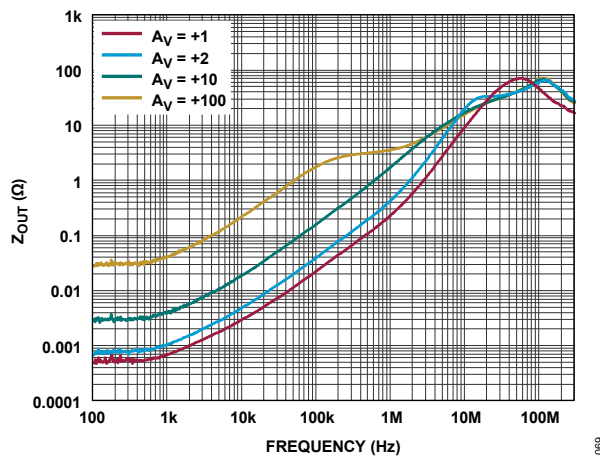


Figure 68. Closed-Loop Output Impedance ( $Z_{OUT}$ ) vs. Frequency

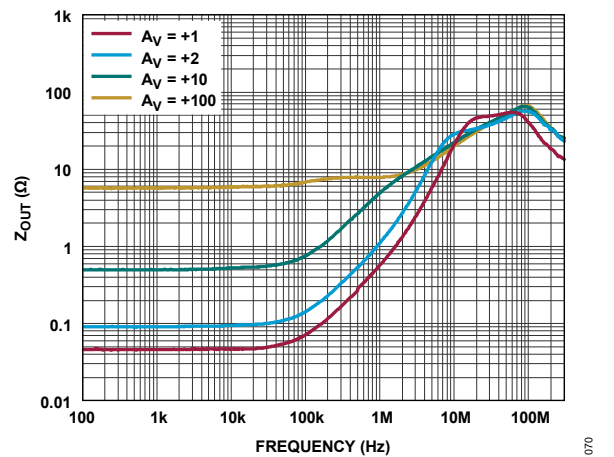


Figure 69. Closed-Loop Output Impedance ( $Z_{OUT}$ ) vs. Frequency, High  $V_{CM}$  Operation

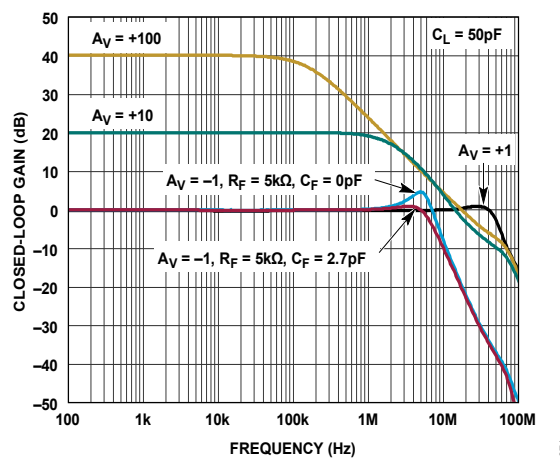


Figure 70. Closed-Loop Gain vs. Frequency

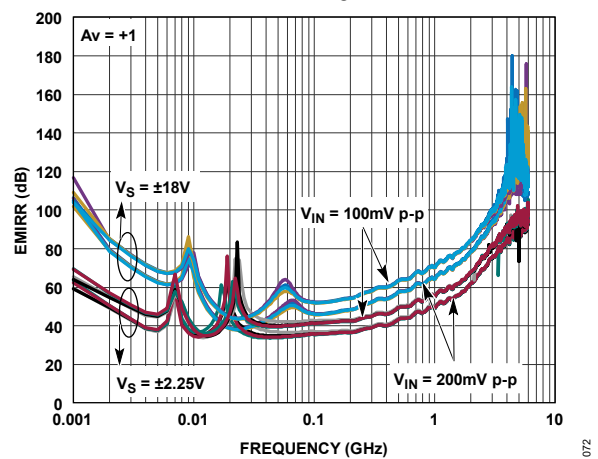


Figure 71. EMIRR vs. Frequency

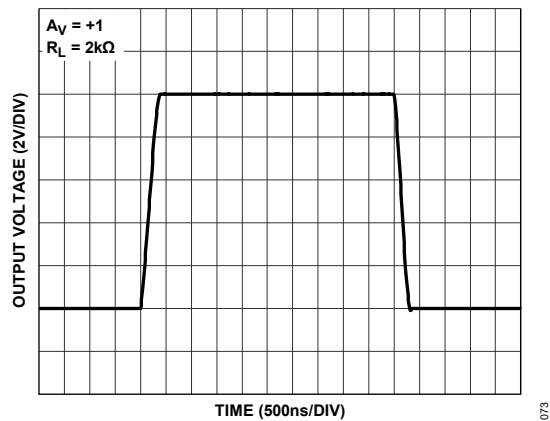


Figure 72. Large Signal Transient Response (10 V Step),  
 $A_V = +1$

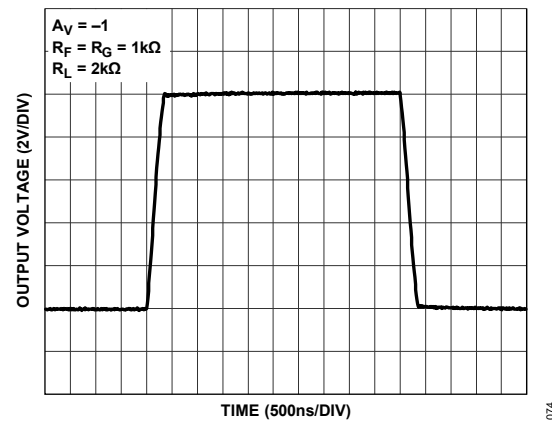


Figure 73. Large Signal Transient Response (10 V Step),  
 $A_V = -1$

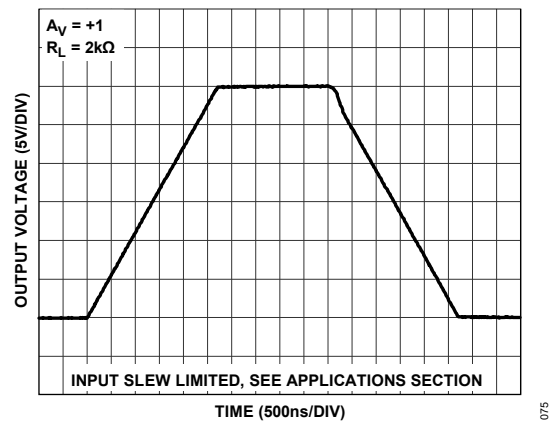


Figure 74. Large Signal Transient Response (30 V Step),  
 $A_V = +1$

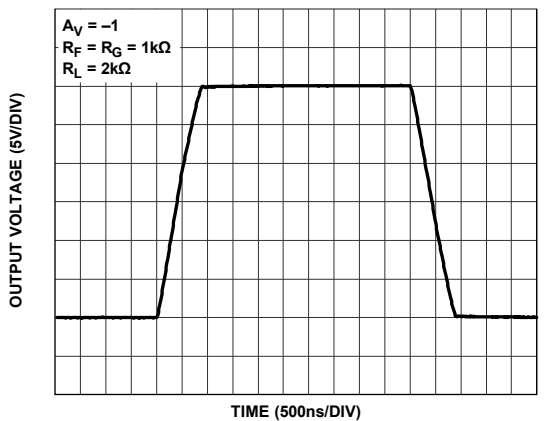


Figure 75. Large Signal Transient Response (30 V Step),  
 $A_V = -1$

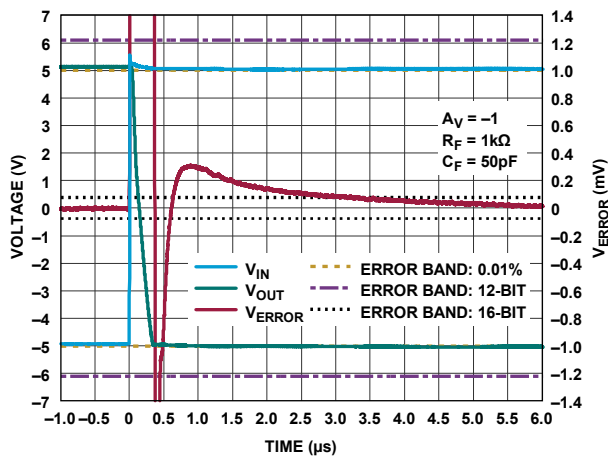


Figure 76. Large Signal Positive Step Settling Time  
(10 V Step)

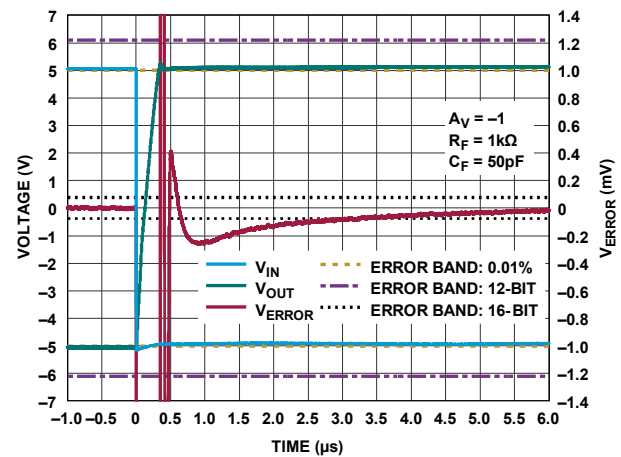


Figure 77. Large Signal Negative Step Settling Time  
(10 V Step)

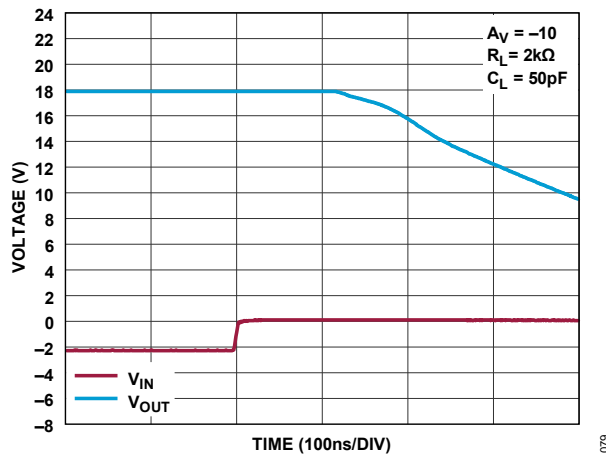


Figure 78. Positive Overload Recovery (Step = 2.2 V)

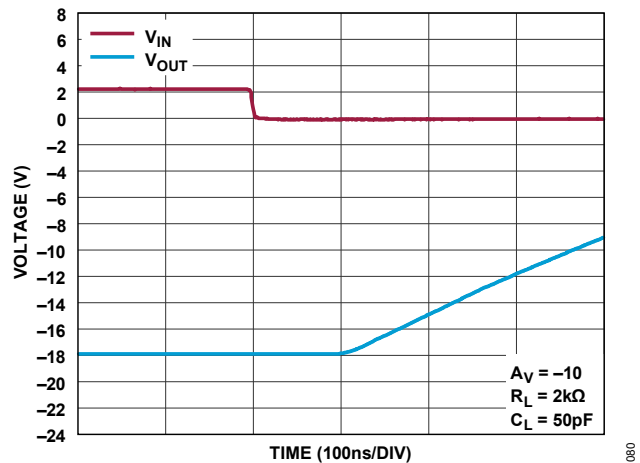


Figure 79. Negative Overload Recovery (Step = 2.2 V)

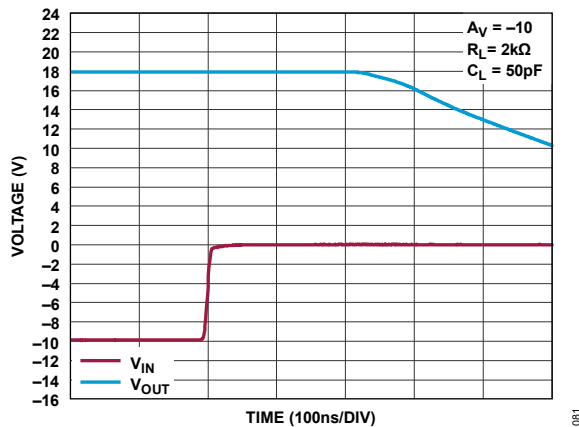


Figure 80. Positive Overload Recovery (Step = 10 V)

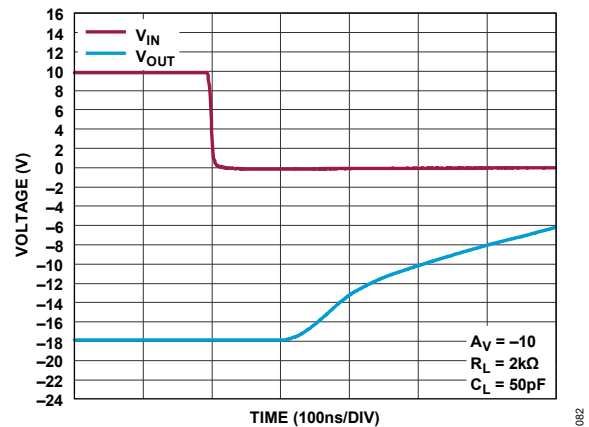
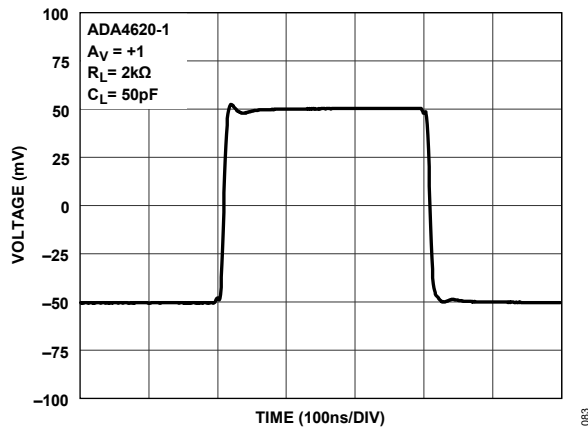
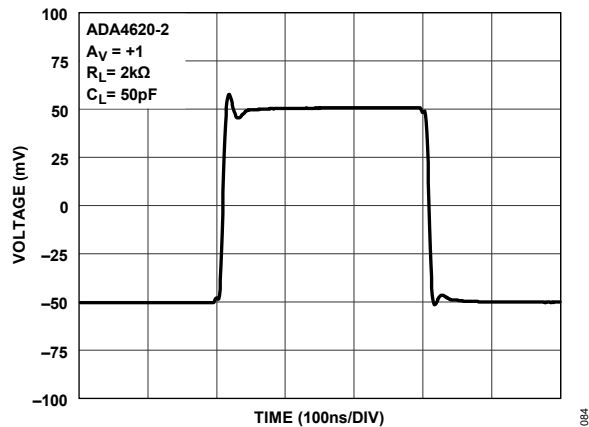


Figure 81. Negative Overload Recovery (Step = 10 V)

Figure 82. ADA4620-1 Small Signal Transient Response (100 mV Step,  $A_V = +1$ )Figure 83. ADA4620-2 Small Signal Transient Response (100 mV Step,  $A_V = +1$ )

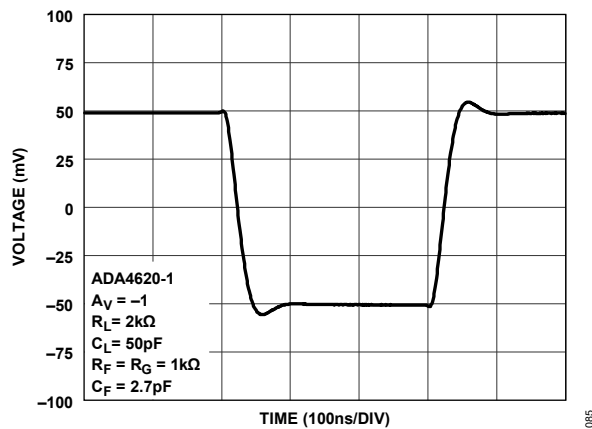


Figure 84. ADA4620-1 Small Signal Transient Response (100 mV Step,  $A_V = -1$ )

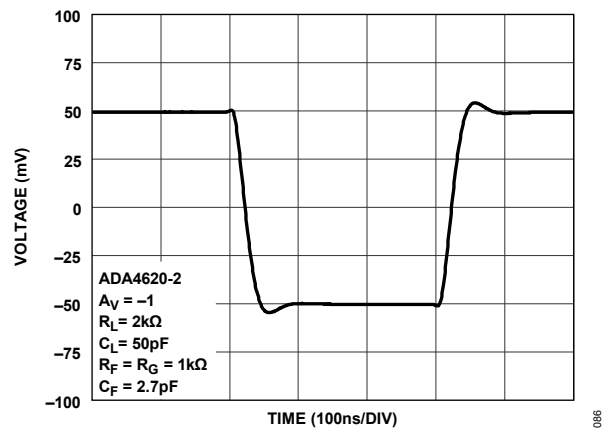


Figure 85. ADA4620-2 Small Signal Transient Response (100 mV Step,  $A_V = -1$ )

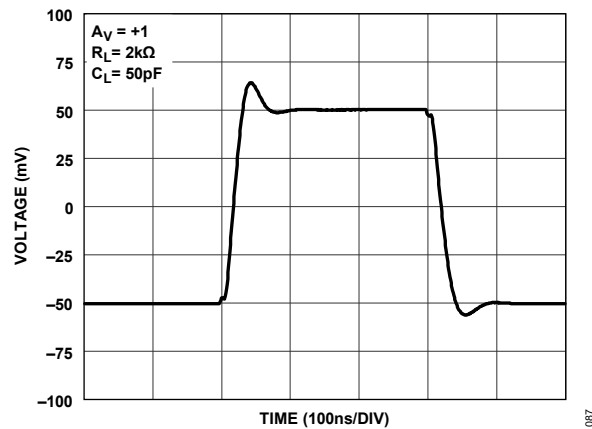


Figure 86. Small Signal Transient Response, High  $V_{CM}$  Operation (100 mV Step,  $A_V = +1$ )

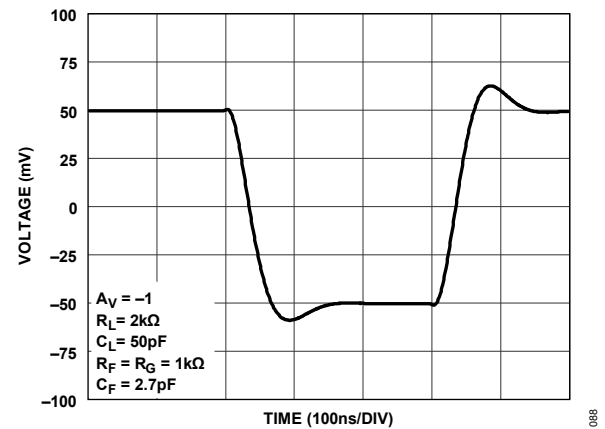


Figure 87. Small Signal Transient Response, High  $V_{CM}$  Operation (100 mV Step,  $A_V = -1$ )

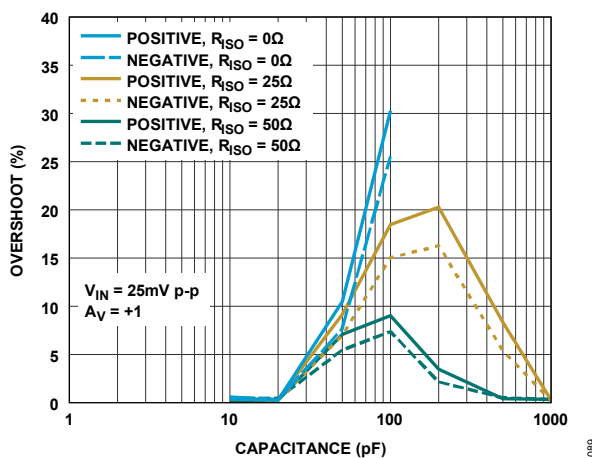


Figure 88. ADA4620-1 Overshoot vs. Load Capacitance ( $A_V = +1$ )

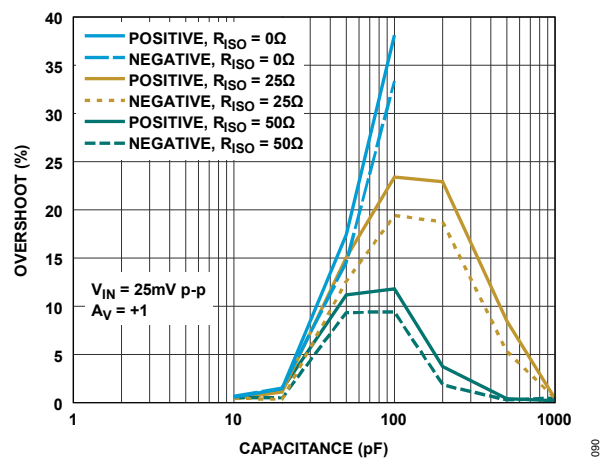


Figure 89. ADA4620-2 Overshoot vs. Load Capacitance ( $A_V = +1$ )

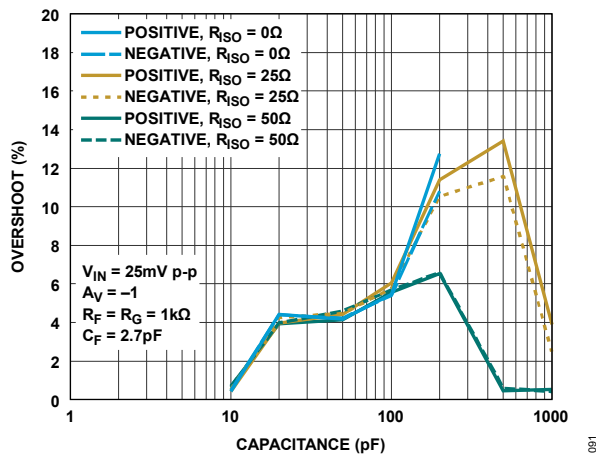


Figure 90. ADA4620-1 Overshoot vs. Load Capacitance ( $A_V = -1$ )

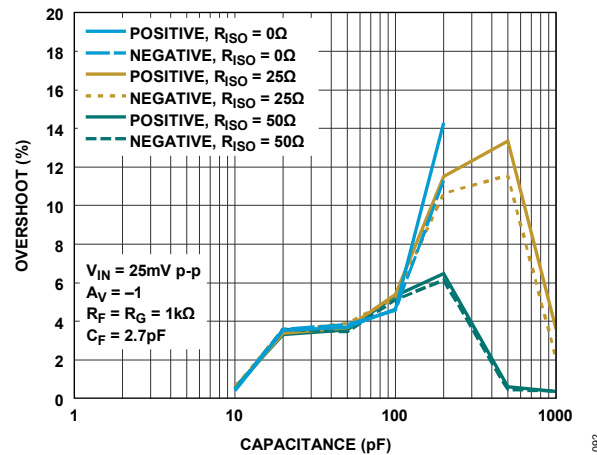


Figure 91. ADA4620-2 Overshoot vs. Load Capacitance ( $A_V = -1$ )

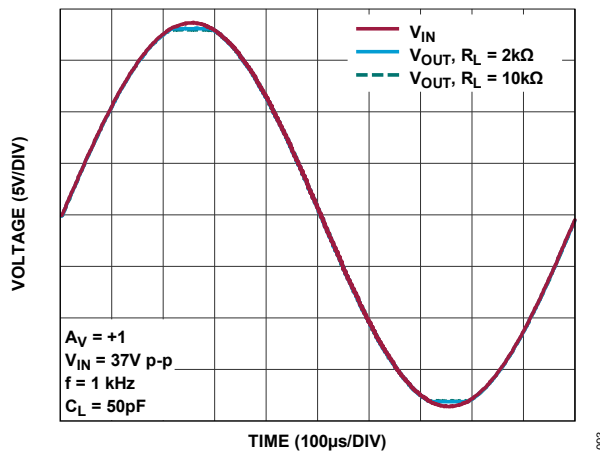


Figure 92. No Phase Reversal (Sine Freq. = 1 kHz)

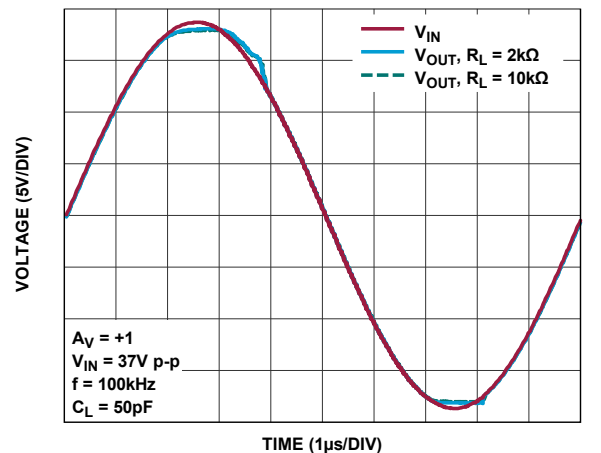


Figure 93. No Phase Reversal (Sine Freq. = 100 kHz)

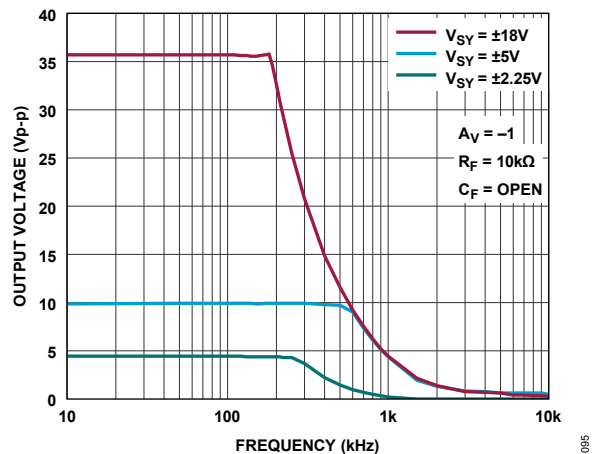


Figure 94. Max. Undistorted Output Swing (THD 1%) vs. Frequency

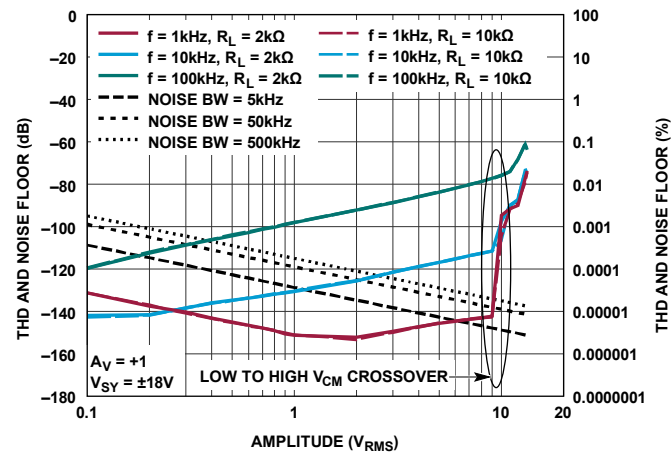
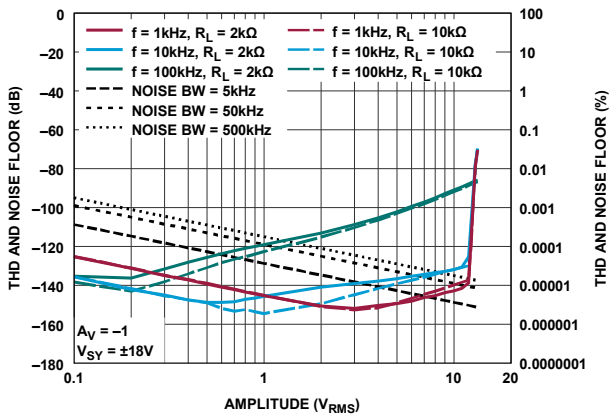
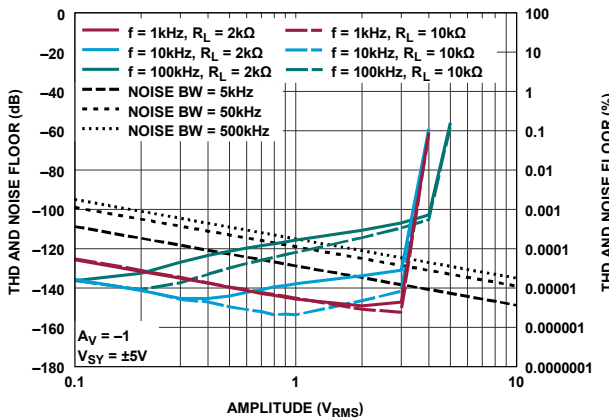
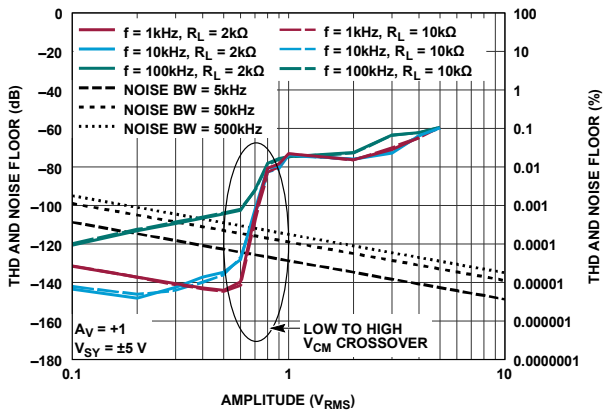
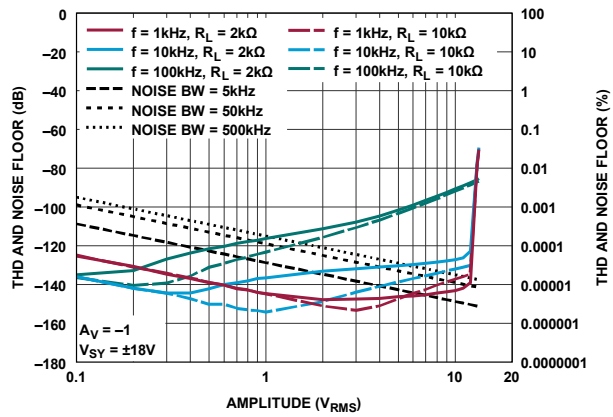
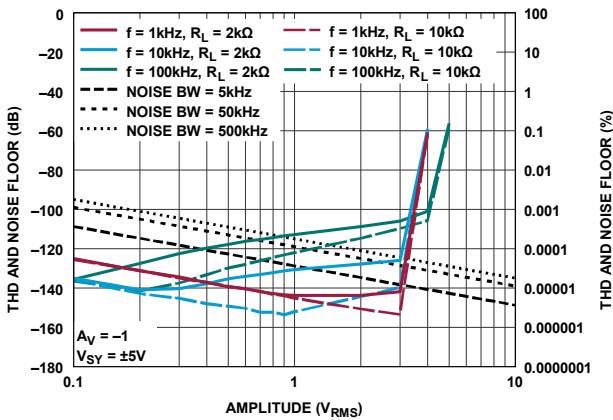
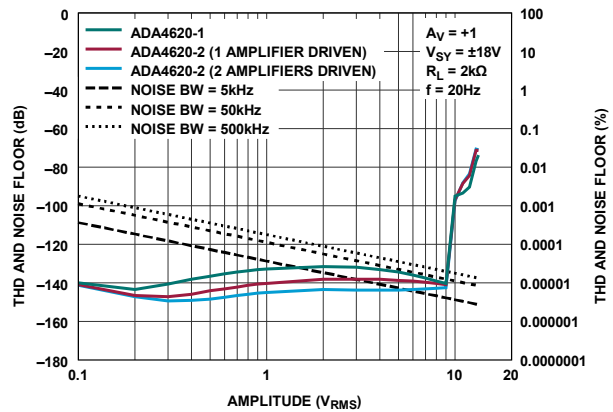


Figure 95. THD vs. Amplitude vs.  $R_L$  ( $A_V = +1$ )

Figure 96. ADA4620-1 THD vs. Amplitude vs.  $R_L$  ( $A_V = -1$ )Figure 98. ADA4620-1 THD vs. Amplitude vs.  $R_L$  ( $A_V = -1$ ,  $V_{SY} = \pm 5V$ )Figure 100. THD vs. Amplitude vs.  $R_L$  ( $A_V = +1$ ,  $V_{SY} = \pm 5V$ )Figure 97. ADA4620-2 THD vs. Amplitude vs.  $R_L$  ( $A_V = -1$ )Figure 99. ADA4620-2 THD vs. Amplitude vs.  $R_L$  ( $A_V = -1$ ,  $V_{SY} = \pm 5V$ )Figure 101. THD vs. Amplitude ( $A_V = +1$ ,  $f = 20\text{ Hz}$ )

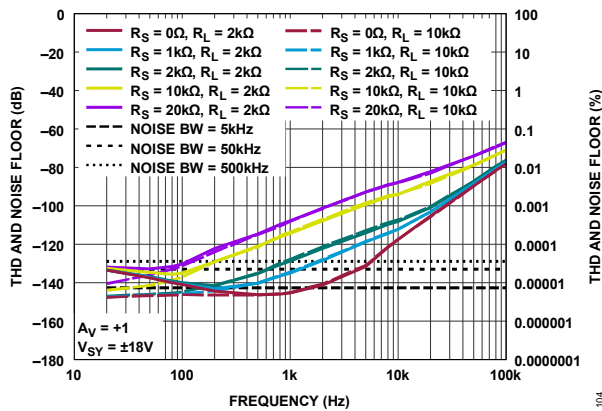


Figure 102. ADA4620-1 THD vs. Frequency for Various Source Impedances

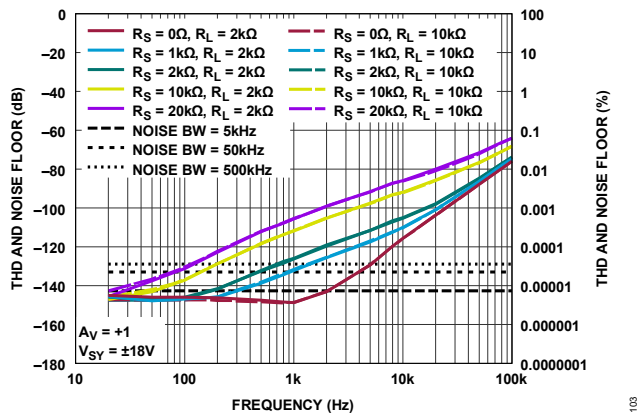


Figure 103. ADA4620-2 THD vs. Frequency for Various Source Impedances

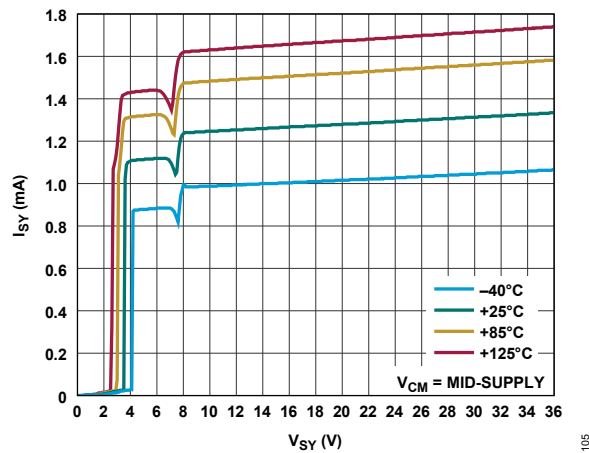


Figure 104.  $I_{SV}$  per Amplifier vs.  $V_{SV}$  (Dual and Single Supplies) at Four Temperatures

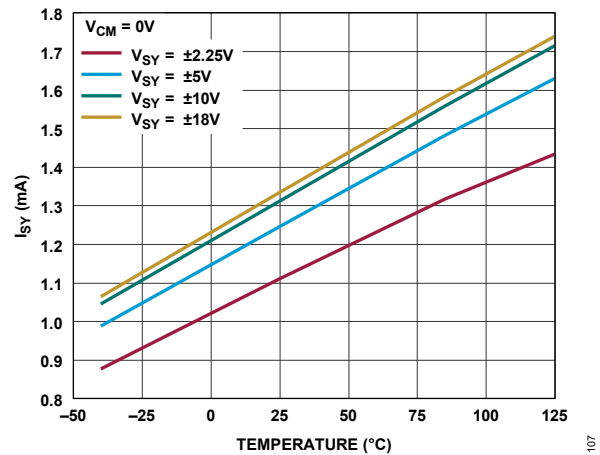


Figure 105.  $I_{SV}$  vs. Temperature for Four Supplies

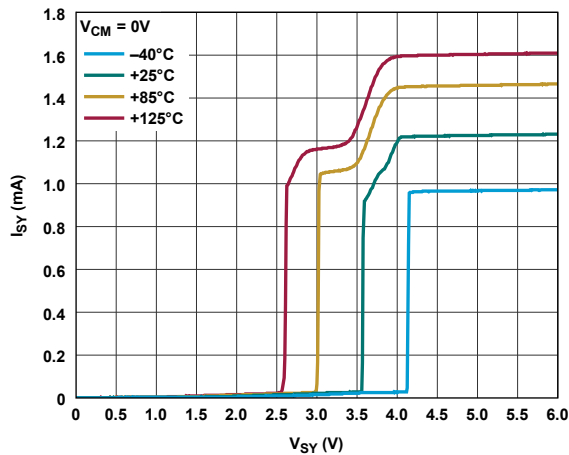


Figure 106.  $I_{SV}$  per Amplifier vs.  $V_{SV}$  (Single Supply) Power on Zoom at Four Temperatures

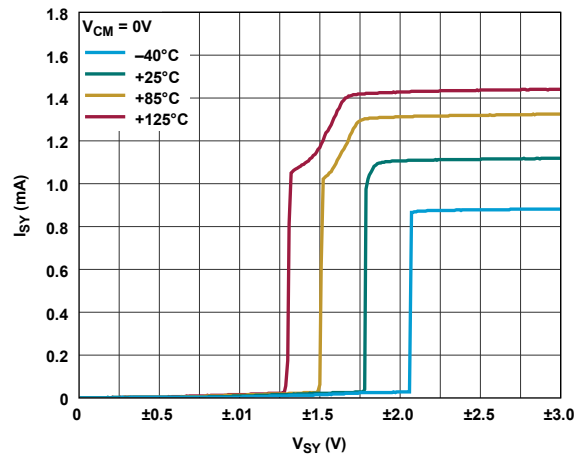


Figure 107.  $I_{SV}$  per Amplifier vs.  $V_{SV}$  (Dual Supply) Power on Zoom at Four Temperatures

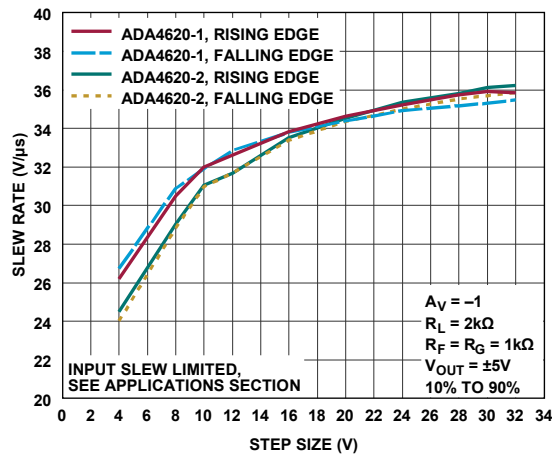
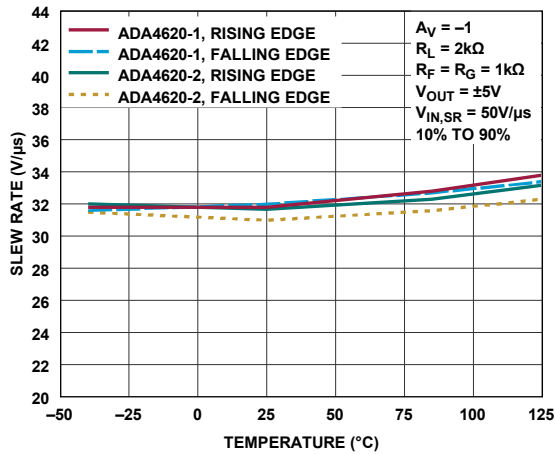
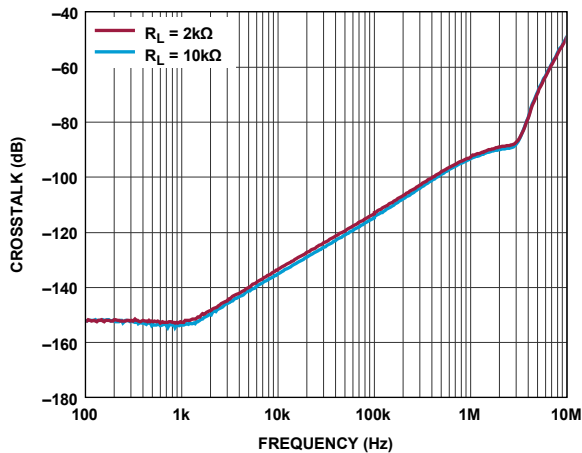
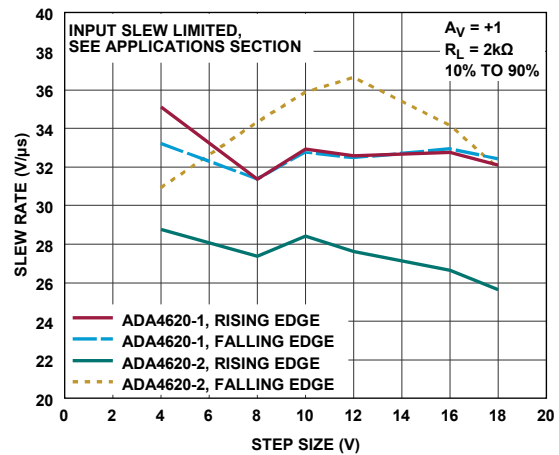
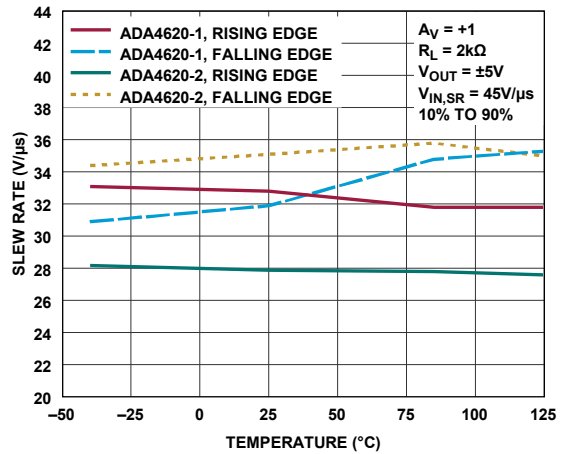
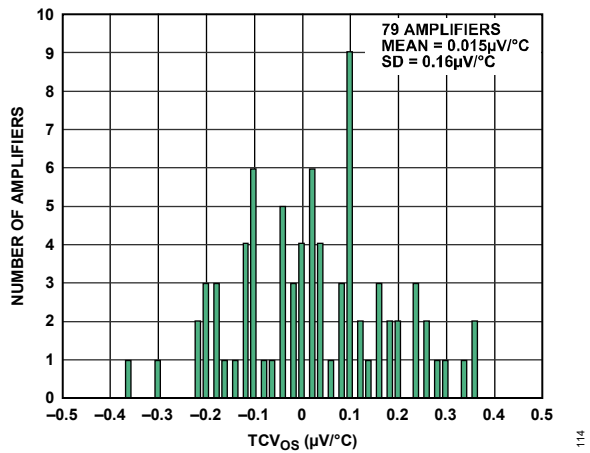
Figure 108. Slew Rate vs. Amplitude ( $A_V = -1$ )Figure 110. Slew Rate vs. Temperature ( $A_V = -1$ )

Figure 112. Crosstalk vs. Frequency

Figure 109. Slew Rate vs. Amplitude ( $A_V = +1$ )Figure 111. Slew Rate vs. Temperature ( $A_V = +1$ )Figure 113. ADA4620-2  $TCV_{OS}$  Match Distribution  
( $-40^{\circ}\text{C} < T_A < 125^{\circ}\text{C}$ )

## THEORY OF OPERATION

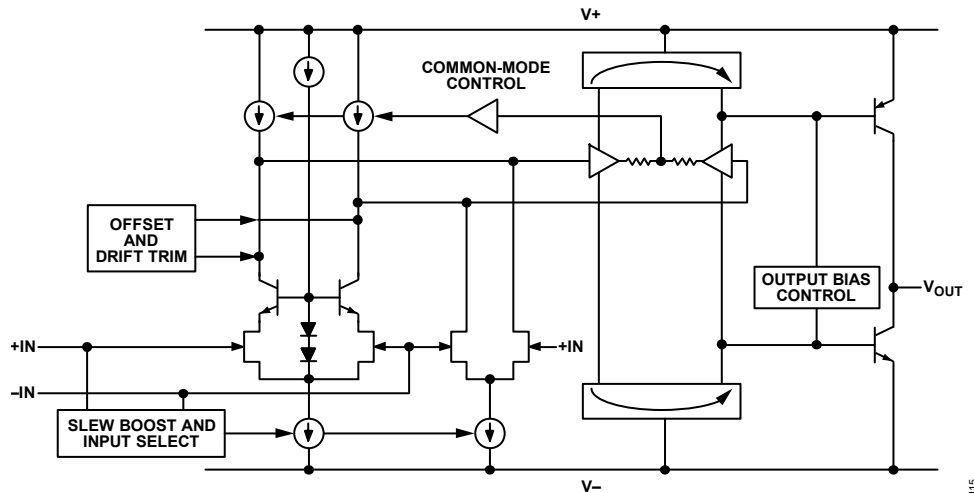


**Figure 114. Simplified Schematic**

The ADA4620 is a wide-input-range, low-power, low-distortion, rail-to-rail output, precision JFET input amplifier that operates over a wide supply voltage range up to a maximum of 36 V. The amplifier employs a two-temperature offset trim to achieve a low offset over a wide temperature range. The amplifier features a secondary input stage to handle input common-mode operation near the positive supply rail. For enhanced slewing, the ADA4620 provides an additional slew-boosting JFET input stage, which operates with large differential input voltages.

### Input and Gain Stages

Figure 114 shows the simplified circuit diagram for the ADA4620. The low-noise architecture provides wide common-mode input range optimized for low noise, low bias current, low offset voltage, and low distortion. The use of a low-noise, offset-trimmed, bootstrapped N-channel JFET-based (nJFET) input stage enables a precision common-mode range starting below the negative supply rail and extending to about 4.4 V below the positive supply rail. The bootstrapping ensures low variation in leakage current versus input common-mode, extremely high common-mode rejection ratio, and reduced harmonic distortion. When the input common-mode voltage rises above about 4.4 V from the positive supply rail, the main input stage shuts off and an alternative nJFET-buffered NPN bipolar differential pair, not shown in the figure, takes control. This alternative input stage maintains low input leakage current and linear operation to within approximately 1 V of the positive rail. The offset voltage of this alternative input stage is not trimmed. Internal clamps prevent phase inversion for signals ranging up to and slightly exceeding the positive supply rail.

Novel slew boosting circuitry provides a high slew rate for fast settling and low distortion without compromising stability. An additional nJFET differential input stage has a bias dependent on the applied differential voltage. During high slew events, the large input differential voltage results in an increase of bias current, which assists the amplifier in tracking rapidly moving signals. The result is a slew rate in excess of 30 V/μs, which improves settling time and reduces distortion.

### Output Stage

The rail-to-rail output stage receives a differential signal from the input stage. This input stage signal is applied across a buffered H-bridge class A/B stage. The buffering ensures the input stage is not significantly loaded and maintains a high gain. The H-bridge is advantageous for providing large slewing currents to the output transistors and output stage compensation. The outputs of this stage are current mirrored to the common-emitter output transistors and compensation. The output stage has no thermal shutdown and the device relies on an inherent

limitation of current drive to the output transistors, along with appropriate user precautions, to maintain a safe operating area (SOA).

## Compensation

The wide gain bandwidth product of 16.5 MHz is achieved through internal compensation ensuring unity-gain stable operation even for capacitive loads larger than 100 pF. Larger capacitive loads can be driven with the assistance of an isolation resistor in series with the load.

An additional aspect of the compensation scheme is that capacitors are coupled to the positive and negative supply rails to improve high-frequency power supply rejection ratio (PSRR).

## No Phase Reversal

The ADA4620 does not suffer from output voltage phase reversal when driven beyond the specified input common-mode range. In JFET amplifiers, phase reversal can happen when the input differential transistors go into their triode region of operation. The input signal then couples directly into the transistors' drains without undergoing the normal inverting gain of the transistors. This is the usual source for phase reversal – a lack of the normal inverting gain at the input. On the ADA4620, the high common-mode output stage is designed in such a way that the amplification does not rely on an inverting gain of the input transistors. This avoids direct coupling into the drain nodes when in the triode region. In this way, the ADA4620 circumvents the phase reversal phenomenon. Additional clamping also ensures that phase reversal does not occur.

## Electrical Overstress Protection

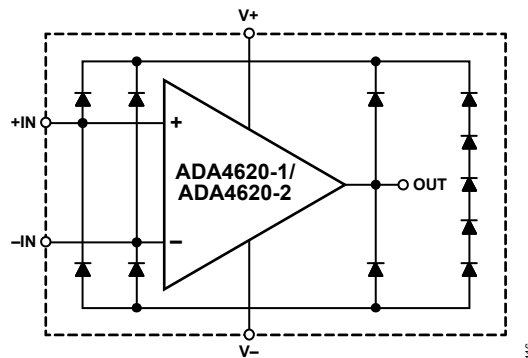


**Figure 115. Electrical Overstress Protection Circuitry**

The ADA4620 is provided with electrical overstress protection, as shown in [Figure 115](#). The diode stack between V+ and V- provides the primary protection against overvoltage stress. The stack of diodes undergoes controlled avalanche breakdown around 47.5 V, well above the absolute maximum rating of 40 V. If the supply voltage exceeds that threshold, significant current begins to flow between the supplies. The series resistance of the diode stack is approximately 11  $\Omega$ , providing some limitation to the current flow.

The signal pins (+IN, -IN, and OUT) of the amplifier are provided with a diode each to V+ and V-. In the case of a pin overvoltage condition (greater than the V+ supply voltage), a diode becomes forward-biased. If the V+ supply is low impedance, current flows from the signal pin to V+. The current is only limited by external resistance. If the V+ supply is high impedance, the pin voltage drags the V+ supply up. This continues until the diode stack breaks down. Similarly, when there is a pin undervoltage condition (less than the V- supply voltage), a diode becomes forward-biased. If the V- supply is low impedance, current flows from V- to the signal pin, again only limited by external resistance. If the V- supply is high impedance, the pin voltage drags down the V- supply until the diode stack

breaks down. In the case where an overvoltage is impressed between signal pins, the protection path is through a diode from the first pin to  $V^+$ , through the diode stack, and through a diode from  $V^-$  to the second pin.

The electrical overstress protection is meant primarily for electrostatic discharge (ESD) protection. Secondly, it is able to handle some amount of signal overdrive, provided adequate current limitation is provided to ensure less than +10 mA flows into the pin, as noted in [Absolute Maximum Ratings](#).

## APPLICATIONS INFORMATION

### Photodiode Preamplifier/Transimpedance Amplifier

The ADA4620 devices are an excellent choice for photodiode preamplifier applications. The low input bias current minimizes the DC error at the output of the preamplifier. In addition, the high gain bandwidth product and low input capacitance maximize the signal bandwidth of the photodiode preamplifier. [Figure 116](#) shows the ADA4620-1/ADA4620-2 as a current to voltage (I to V) converter with an electrical model of a photodiode.

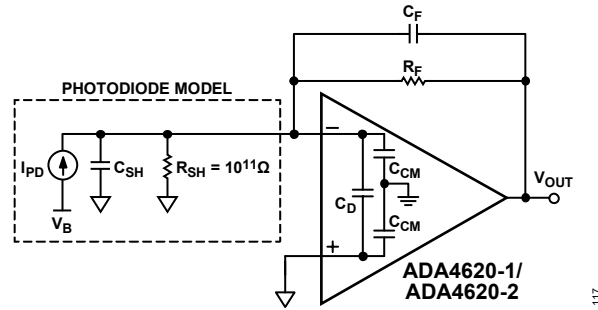


**Figure 116. Equivalent TIA Circuit**

The following basic transfer function describes the transimpedance gain of the photodiode preamplifier:

$$V_{OUT} = \frac{I_{PHOTO} \times R_F}{1 + sC_F R_F} \quad (1)$$

where,  $I_{PHOTO}$  is the output current of the photodiode. The parallel combination of  $R_F$  and  $C_F$  sets the signal bandwidth (see the I to V gain trace in [Figure 117](#)). Note that  $R_F$  must be set so the maximum attainable output voltage corresponds to the maximum diode output current,  $I_{PHOTO}$ , which allows use of the full output swing. The attainable signal bandwidth with this photodiode preamplifier is a function of  $R_F$ , the gain bandwidth product ( $f_{GBP}$ ) of the amplifier, and the total capacitance at the amplifier summing junction, including  $C_{SH}$  and the amplifier input capacitance,  $C_D$  and  $C_{CM}$ .

$$C_S = C_{SH} + C_D + C_{CM} \quad (2)$$

$R_F$  and the total capacitance produce a pole with loop frequency ( $f_p$ ).

$$f_p = \frac{1}{2\pi R_F C_S} \quad (3)$$

With the additional pole from the amplifier open-loop response, the two-pole system results in peaking and instability due to an insufficient phase margin. See [Figure 117](#).

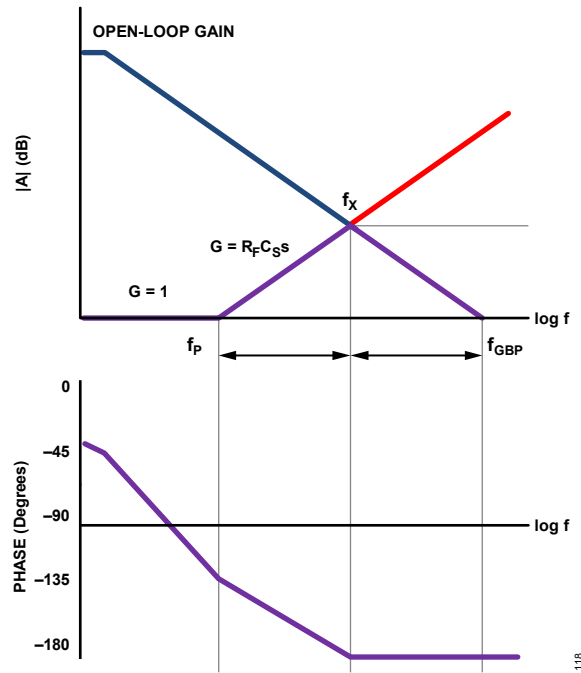


**Figure 117. Gain and Phase Plot of the Transimpedance Amplifier Design, Without Compensation**

Adding  $C_F$  creates a zero in the loop transmission that compensates for the effect of the input pole, which stabilizes the photodiode preamplifier design because of the increased phase margin. Adding  $C_F$  also sets the signal bandwidth (see [Figure 118](#)). The signal bandwidth and the zero frequency are determined by:

$$f_Z = \frac{1}{2\pi R_F C_F} \quad (4)$$

where,  $f_Z$  is the zero frequency. Setting the zero at the  $f_X$  frequency maximizes the signal bandwidth with a  $45^\circ$  phase margin. Because  $f_X$  is the geometric mean of  $f_P$  and  $f_{GBP}$ , it can be calculated by:

$$f_X = \sqrt{f_P \times f_{GBP}} \quad (5)$$

Combining these equations, the  $C_F$  value that produces  $f_X$  is:

$$C_F = \sqrt{\frac{C_S}{2\pi \times R_F \times f_{GBP}}} \quad (6)$$

The frequency response in this case shows approximately 2 dB of peaking and 15% overshoot. Doubling  $C_F$  and halving the bandwidth results in a flat frequency response with approximately 5% transient overshoot. The dominant sources of output noise in the wideband photodiode preamp design are the input voltage noise of the amplifier,  $V_{NOISE}$ , and the resistor noise due to  $R_F$ .

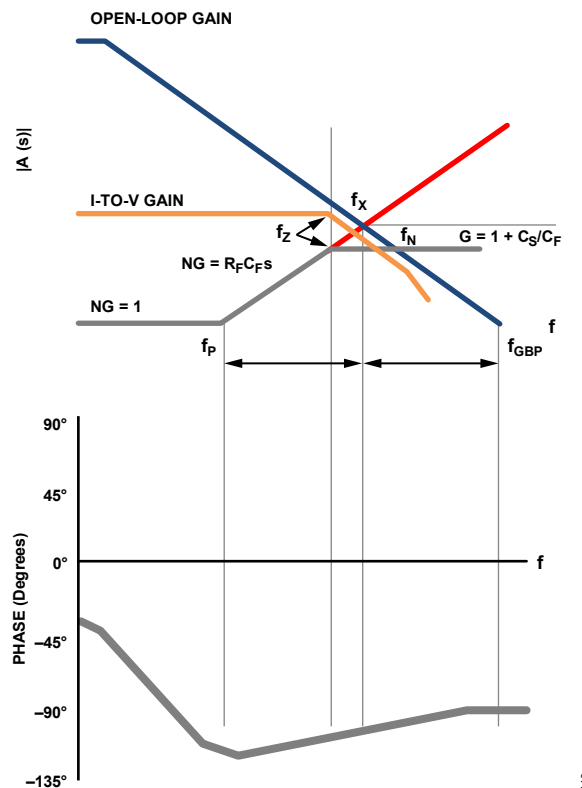


**Figure 118. Ideal Gain and Phase Plot of the Transimpedance Amplifier Design with Compensation**

The gray trace in [Figure 118](#) shows the ideal noise gain over frequencies for the photodiode preamp. Calculate the noise bandwidth at the  $f_N$  frequency by:

$$f_N = \frac{f_{GBP}}{(C_S + C_F)/C_F} \quad (7)$$

In reality, noise gain is limited by the gain bandwidth of the op amp, and rolls off with open-loop gain. The gray trace in [Figure 119](#) shows a more realistic noise gain plot, compared to [Figure 118](#).

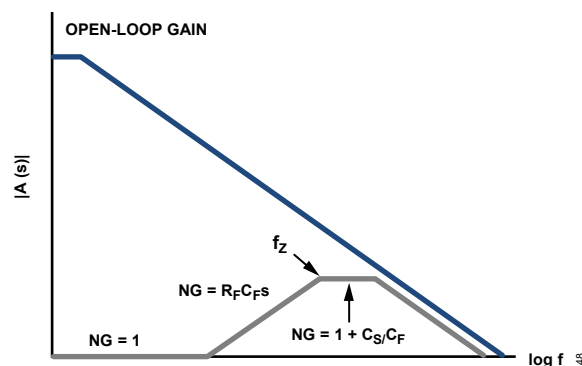


**Figure 119. Attenuated Noise Gain, with Attenuation Following Open-Loop Gain**

Figure 120 shows the ADA4620-1/ADA4620-2 configured as a transimpedance photodiode amplifier. The amplifiers are used in conjunction with a photodiode detector with a shunt capacitance of 3 pF at 5 V of reverse bias (Osram SFH213).

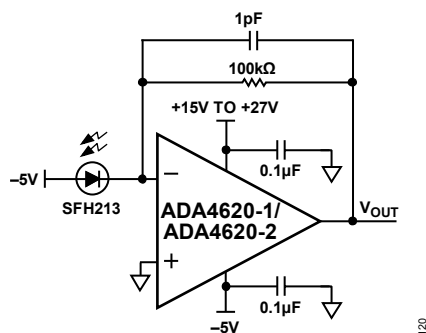


**Figure 120. Transimpedance Photodiode Preamplifier**

Figure 121 shows the transimpedance response of the ADA4620 when  $I_{\text{PHOTO}}$  is 1  $\mu\text{A}$  p-p. The amplifiers have a bandwidth of 2 MHz with no compensation but a lot of peaking. Adding  $C_F$  of 1.5 pF completely eliminates the peaking, and also reduces the bandwidth to 1.1 MHz. See Figure 122.

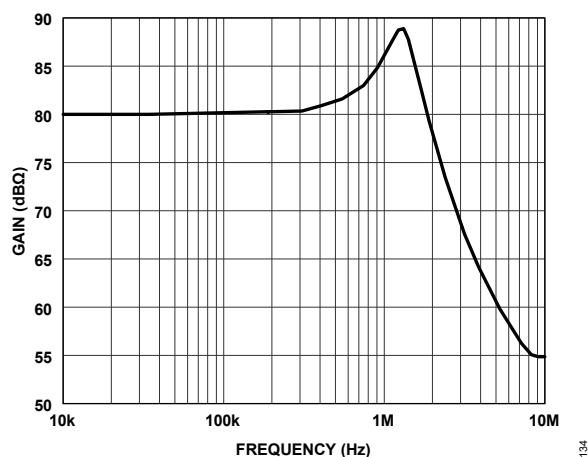


**Figure 121. Initial Photodiode Amplifier Response with Peaking (Undercompensated)**

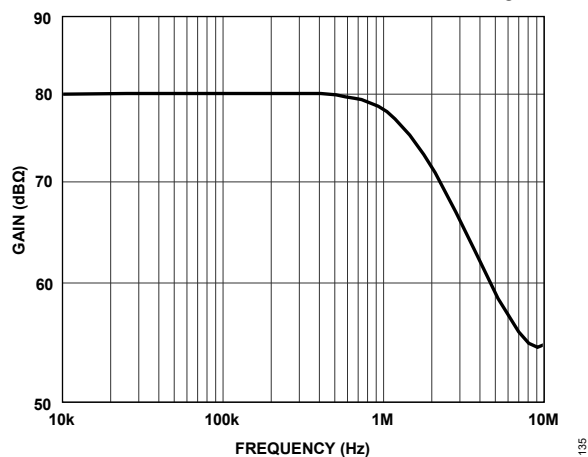


**Figure 122. Photodiode Amplifier Response with  $C_F = 1.5$  pF (Slightly Overcompensated)**

Figure 123 shows the total output noise for the photodiode preamp, where the preamp is configured for slight overcompensation with a feedback capacitor  $C_F = 1.5$  pF. Total output noise is  $520 \mu\text{V}_{\text{RMS}}$  over a 2 MHz measurement bandwidth.

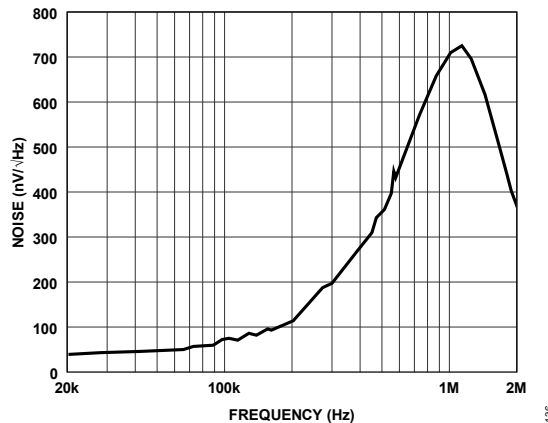


Figure 123. Output Noise Spectrum

For more information, see the KWIK circuit application note: [1 MHz, Single Supply, Photodiode Transimpedance Amplifier \(TIA\) Design](#).

## ADC Driving

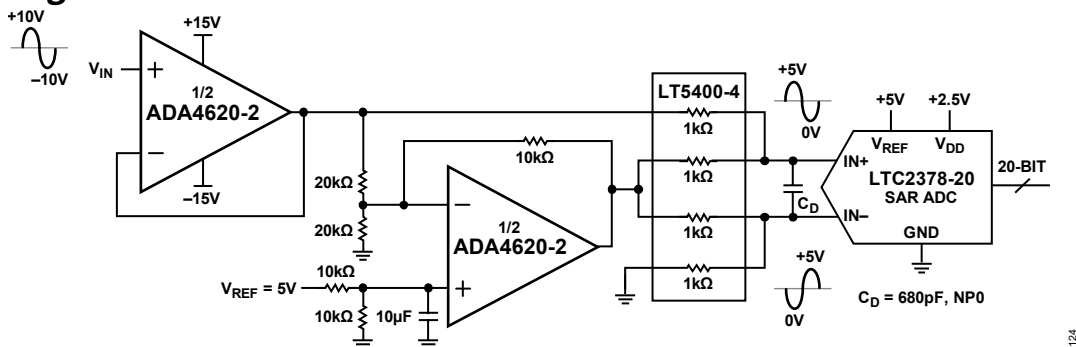


Figure 124. Squeezing a High Voltage High Impedance Signal into a 5 V Precision Differential Input ADC

The ADA4620 has high DC precision and very low bias current. Adding its low distortion, it is suitable for data acquisition systems using high resolution ADCs. When an ADC samples its input, it puts a glitch onto the upstream circuit, such that the upstream circuit must settle back out before the ADC closes its sample window, ending the analog “acquisition” phase. Any unsettled residue from the glitch leads to increased noise and distortion in the sample. Figure 124 shows an ADA4620-2 driving a 20 V p-p single-ended signal into a single-to-differential converting circuit using the other half of the ADA4620-2 and an LT5400. The resulting differential voltages are fed into the LTC2378-20, a 20-bit 1 MSps SAR ADC.

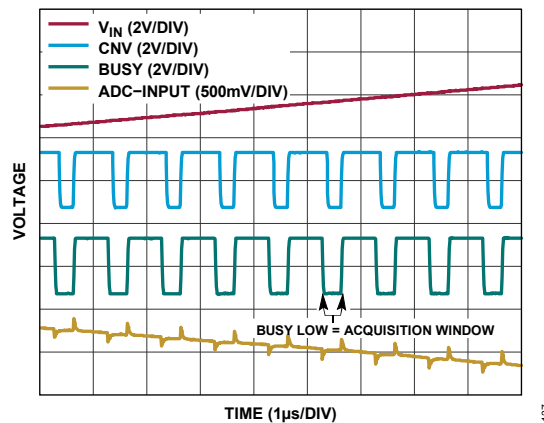


**Figure 125. Analog and Digital Waveforms Associated with the ADA4620 and LTC2378-20, Showing the Sampling Glitches at 1 MSps**

Figure 125 shows the sampling glitches at the IN<sup>-</sup> of the LTC2378-20 at its full rate of 1 MSps. This is with an exact and synchronous 5 kHz input waveform, allowing coherence in the time domain (as shown), but this is incoherent in an FFT (and requires windowing to be intelligible). The red waveform is a piece of the input sinusoid at 5 V/DIV. The blue waveform is the digital CNV signal clocking the ADC, and the green waveform is the BUSY signal from the ADC. While BUSY is low, the sampling capacitor is connected to the upstream circuit, and constitutes the analog acquisition window. The yellow waveform is the actual ADC IN<sup>-</sup>, with the glitches in evidence. Note that with a 1  $\mu$ s sample time, the analog acquisition window is only 300 ns, which is quite a short time for a 16.5 MHz upstream system to try to settle to 20 bits.

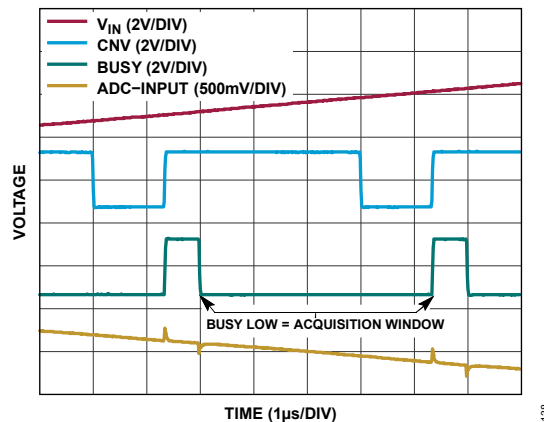


**Figure 126. At a Reduced Sampling Rate of 200 kSps, Giving a Large  $T_s$  of 5  $\mu$ s, Almost All the Extra Time is Allocated to the Sampling Window, Allowing Much Better Settling of the Upstream Circuit**

Figure 126 shows the same system at a reduced sample rate of 200 kSps. Of the now increased sample time of 5  $\mu$ s, the extra 4  $\mu$ s is allocated almost entirely to the analog acquisition time. This gives ample time for the upstream 16.5 MHz GBW circuit to settle to its most precise values.

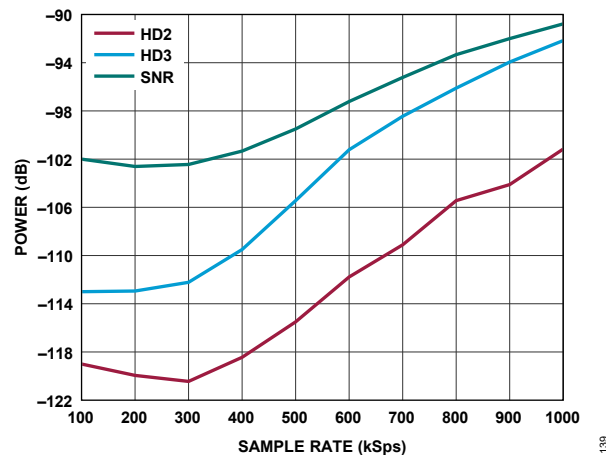


**Figure 127. Distortion and Noise Performance vs. Sample Rate for  $C_d = 680$  pF**

Figure 127 plots various distortion and noise performances achieved with various sample rates and capacitor  $C_d = 680$  pF. Figure 128 is an example FFT.

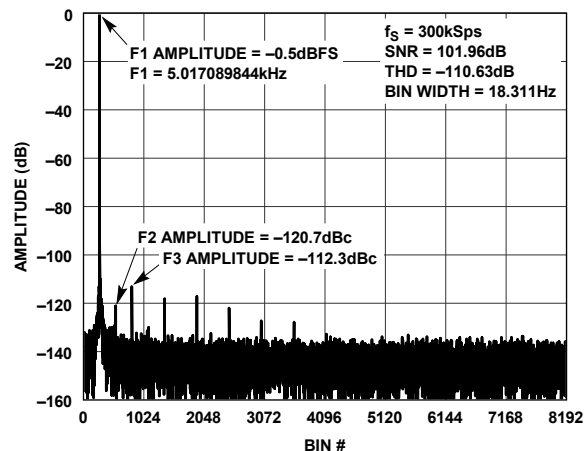


**Figure 128. 8192 Bin FFT Gathered from the Circuit at 300 kSps, -0.5 dBFS, 5.017 kHz Input Sinusoid**

## Multiplexer Compatibility

High-channel-density data-acquisition systems used in medical imaging, industrial process control, and automatic test equipment require numerous ADC channels to acquire data from multiple sensors or analog voltages. This demands significant board space, power, and cost. To address this, a multiplexing technique is employed, allowing signals from many sensors to be routed to a smaller number of ADCs that convert each channel sequentially. This technique reduces the downstream circuitry needed compared to a per-channel design. By using fewer ADCs per system, multiplexing offers substantial savings in power, size, and cost. However, to effectively implement a multiplexing solution, attention must be given to several details, especially when quickly switching between channels, ensuring accurate measurements, and maintaining low power consumption.

In multiplexed data-acquisition (DAQ) systems, an analog multiplexer is used to time-multiplex input analog channels because it allows multiple signals to be routed to a single ADC for conversion. Interfacing the output of the multiplexer to a high input impedance stage before connecting it to the ADC is important because it improves measurement accuracy and settling time. This configuration ensures that the multiplexer can switch channels more quickly and efficiently, enhancing overall signal chain throughput.

Each time the multiplexer switches channels, the multiplexed signal changes value. Even if the input signals are stable, the multiplexed signal varies, requiring downstream circuitry to respond quickly to these transitions. If the output signal does not settle to the target accuracy before reading the next channel, the measured value of a channel can be affected by the previous channel's value, causing channel-to-channel crosstalk. To prevent this, an op amp used as a high impedance stage at the multiplexer's output must respond quickly to its output. The ADA4620 op amp is highly suitable for this purpose due to its low propagation delay and high slew rate, maintaining measurement precision. Although high-speed op amps usually consume a lot of power, the ADA4620 provides a high slew rate while powered with a low supply current, enabling high throughput in multiplexed DAQ systems with lower power consumption. The proprietary circuit topology of this amplifier gives excellent slew rate at low quiescent power dissipation without compromising precision or settling time.

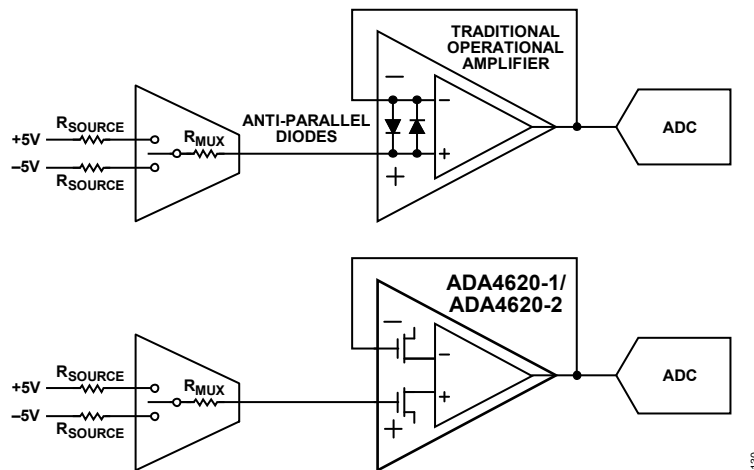


**Figure 129. Multiplexed System and Different Input Structures of Op Amp**

Even if the op amp following the multiplexer is fast enough, another crucial detail often overlooked is the input structure of the operational amplifier. The high impedance stage op amp can be exposed to large differential voltages due to the multiplexer switching between significantly different DC voltages. Therefore, the high impedance stage op amp should be capable to tolerate and measure large step input voltages. The ADA4620 addresses this issue with a robust, mux-compatible architecture that can handle large differential voltages up to the supply rails without relying on differential back-to-back diodes. See [Figure 129](#).

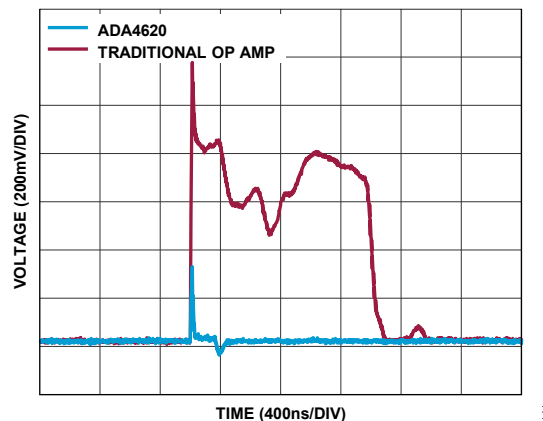


**Figure 130. Traditional Op Amp Inrush Current vs. Small ADA4620 Mux-Compatible Glitch Representing Mux Switching Event**

In a traditional op amp, this large but temporary differential voltage between the input pins results in inrush current due to diode conduction while the op amp output is slewing, as seen in the red trace in [Figure 130](#). This effect causes charge errors to form on upstream RCs, which takes time to settle. This effect can be seen in the red

trace in [Figure 131](#). The mux-compatible JFET inputs of ADA4620 do not need diode protection, and therefore remain very high impedance even with the inputs split by several volts and the output slewing, shown in the blue trace in [Figure 131](#).

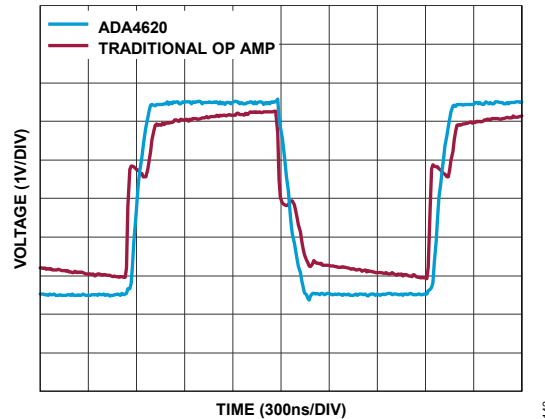


**Figure 131. Output of High Impedance Buffer During Mux Switching (See the [Figure 129 Circuit](#))**

For a more comprehensive discussion of the benefits of mux-compatible op amps, refer to this KWIK circuit application note: [Mux Compatible Analog Front End](#).

### Third-Order Low-Pass Sallen-Key Filter

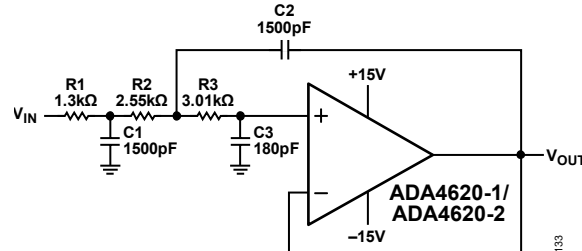


**Figure 132. Third-Order Butterworth Sallen-Key Filter**

A third-order Butterworth filter can be realized without buffering the extra  $s + 1$  term, allowing it to be achieved with a single op amp, as shown in [Figure 132](#). The noninverting Sallen Key approach is chosen over inverting gain multiple feedback to preserve the ultrahigh input  $Z$  at low frequencies. This third-order approach offers a certain important advantage over a second-order approach, which omits  $R_1$  and  $C_1$ . The benefit of having  $R_1$  and  $C_1$  up front is that it has an extremely wide stop band, limited only by the quality of the components and the layout. As a result, it keeps extremely high frequencies from getting to  $R_2$ . If extremely high frequencies are allowed to get to  $R_2$ , the only thing to stop them is  $C_2$ , which can be approximated as a short at high frequencies, and the output impedance of the op amp. But of course, the output impedance of the op amp is not low enough beyond its operating frequency range to arrest those frequencies, and the energy in them essentially makes it past the op-amp output. [Figure 133](#) shows the frequency response of the filter. This design is  $-3$  dB at 100 kHz. Other frequencies can be selected by scaling the passive values. Of course, it is easiest to scale the resistors because they are readily available in finer tolerances. The exact calculated value for  $C_3$  is 200 pF, but the component value is reduced due to the contributing effects of trace capacitance and input capacitance.

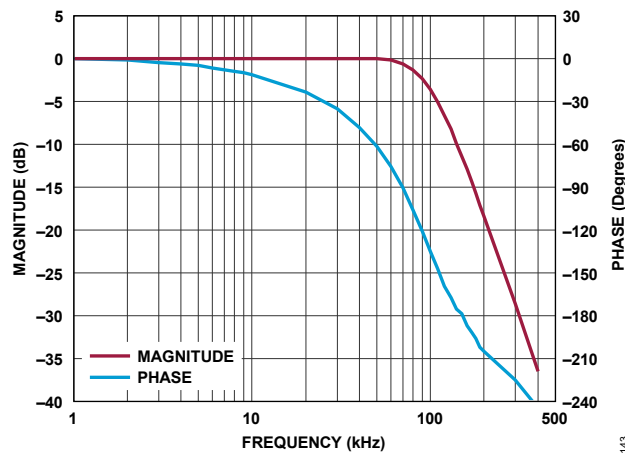


Figure 133. 100 kHz Third-Order Butterworth Filter Frequency Response

## Large Signal Behavior

The ADA4620 is a precision low noise op amp optimized for small signal applications. In the presence of large-signal fast input steps, it does exhibit some less ideal behaviors. For fast steps much larger than 4 V noninverting, and 8 V inverting, the output begins to exhibit some delay. This occurs on the rising edge of the input, in either inverting or noninverting cases. Figure 134 shows the issue in a gain of  $-1$ . The test setup involves a supply voltage of  $\pm 18$  V and up to  $\pm 16$  V input. The output delay time starts out at tens of nanoseconds but can be as high as 500 ns for very large steps. In the noninverting case, shown in Figure 135, steps larger than about 15 V begin to show an extended overshoot on the output, with amplitude 1.4 V, and output delay times extending into the low microseconds. Figure 134 and Figure 135 show the behaviors all the way up to a 32 V step. In these two figures, the dashed lines represent the input step signal, and the solid line that overlays the flat portion of each dotted line is the corresponding output for that input signal.

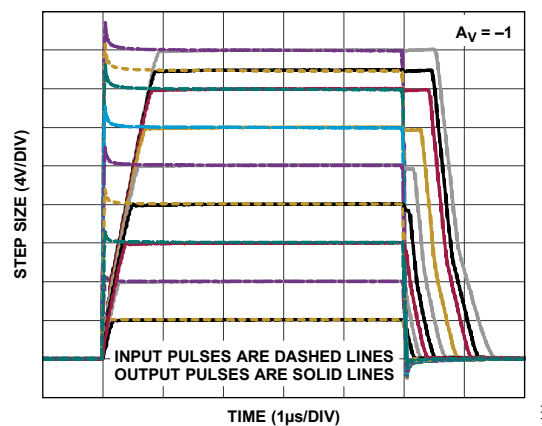


Figure 134. Large Signal Inverting Output Behavior, Without Feedback C, Input Signals Shown Inverted



**Figure 135. Large Signal Noninverting Output Behavior, Without Input RC**

The inverting case is relatively easy to improve, as it simply involves adding a feedback C that most designs include anyway. [Figure 136](#) shows results from an  $A_V = -1$  case with 1 k $\Omega$ :1 k $\Omega$  resistors and a feedback capacitor of 270 pF. The behavior is very cleanly independent of step size. Of course, to reduce power consumption, higher value resistors can be used, in which case the feedback capacitor value can be reduced.

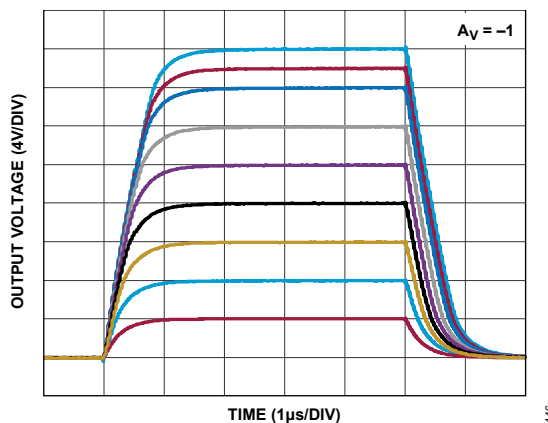


**Figure 136. Inverting Step Responses With 1 k $\Omega$ :1 k $\Omega$  Gain Resistors and Feedback Capacitance of 270 pF**

For the noninverting case, this output behavior can be mitigated by slowing the input drive slew and/or adding a small RC before the IN+ pin. See [Figure 137](#), where the ramp rate is reduced to 80 V/ $\mu$ s and goes into a 330  $\Omega$ , 330 pF RC before the ADA4620.

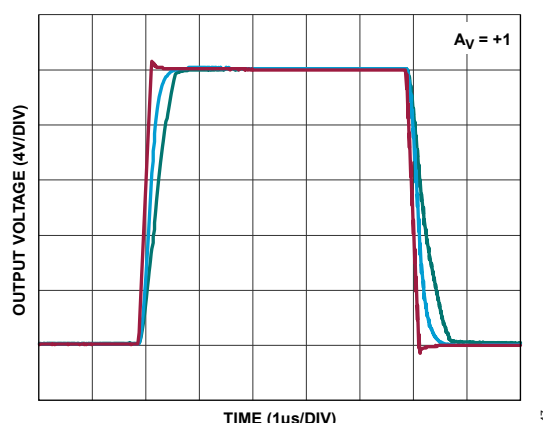


**Figure 137.** 20 V Step into ADA4620 in  $A_V = +1$ . Red is 80 V/μs Input Pulse, Blue is After 330 Ω, 330 pF RC into the +IN Pin, Green is Well-Behaved Output

## Recommended Power Solution

Analog Devices has a wide range of power management products that meet the requirements of most high-performance signal chains. For a dual-supply application, the ADA4620 may need as high as a  $\pm 18$  V supply. Low dropout (LDO) linear regulators such as the LT3042 for the positive supply and the LT3093 for the negative supply help improve the PSRR at high frequency and generate a low noise power rail. In addition, if a negative supply is not available, the ADP5070 can generate the negative supply from a positive supply. [Table 9](#) shows the list of the recommended power management devices for ADA4620.

**Table 9. Recommended Power Management Devices**

| Product                 | Description                                                                 |
|-------------------------|-----------------------------------------------------------------------------|
| <a href="#">ADP5070</a> | DC-to-DC switching regulator with independent positive and negative outputs |
| <a href="#">LT3032</a>  | Dual 150 mA positive/negative low noise LDO linear regulator                |
| <a href="#">LT3093</a>  | -20 V, 200 mA, ultralow noise, ultrahigh PSRR negative linear regulator     |
| <a href="#">LT3042</a>  | 20 V, 200 mA, ultralow noise, ultrahigh PSRR RF linear regulator            |

It is recommended to use a low ESR 0.1 μF bypass capacitor close to each power supply pin of the ADA4620 and ground to reduce errors coupling in from the power supplies. For noisy power supplies, place an additional 10 μF capacitor in parallel with the 0.1 μF for better performance.

## Layout Guidelines

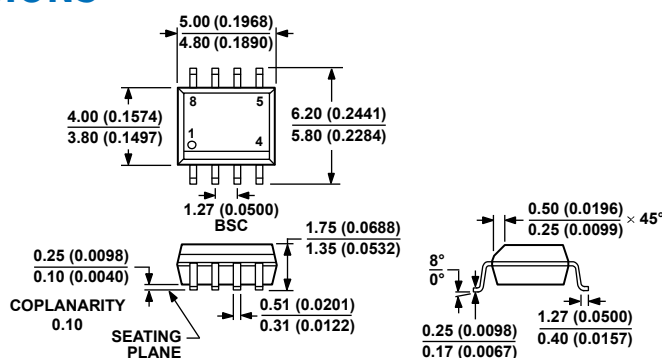
The ADA4620 has extremely high impedance inputs. Shunt impedances from leakage resistance and parasitic capacitance in the PCB layout can severely degrade the performance of the low bias input in the presence of high impedance sources. Protect against parasitic leakage currents with guarding techniques to reduce the voltage gradient seen by the input node. Physically, a guard is a low impedance conductor that surrounds a high impedance node and is driven to the voltage of that node. It buffers leakage by diverting the leakage from the sensitive node and into the low impedance guard. Remove the solder mask from the guard traces and leave the metal exposed so it can shunt rogue surface charges to itself rather than allow them to pass over and reach sensitive nodes. For more information on guarding techniques, refer to [Layout For Precision Op Amps](#).

Depending on the application circuit, the ADA4620-1 (single) or the ADA4620-2 (dual) may be easier to lay out. For example, for noninverting applications, the dual has a +IN at pin 5 on the corner, easily protected by the adjacent

–IN. Where the high-impedance application is inverting, the single has the –IN on pin 2, adjacent to the “Not Internally Connected” pin 1 and the equipotential +IN on pin 3. Place any input resistors close to the ADA4620 inputs to avoid interaction with trace parasitics.

If one of the channels is not in use, connect the +IN pin to a voltage within the linear range of the channel to avoid overdrive conditions that can interfere with other channels, and leave the output unconnected except to the –IN pin. Place decoupling capacitors, such as 0.1  $\mu\text{F}$ , near the ADA4620. Larger capacitors, such as 10  $\mu\text{F}$ , can be used farther away from the op amp.

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA  
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

**Figure 138.8-Lead Standard Small Outline Package [SOIC\_N]  
Narrow Body  
(R-8)**  
Dimensions shown in millimeters and (inches)

## ORDERING GUIDE

**Table 10. Ordering Guide**

| Model <sup>1</sup> | Temperature Range | Package Description                            | Packing Quantity | Package Option |
|--------------------|-------------------|------------------------------------------------|------------------|----------------|
| ADA4620-1ARZ       | −40°C to +125°C   | 8-Lead Standard Small Outline Package [SOIC_N] | Tube, 98         | R-8            |
| ADA4620-1ARZ-R7    | −40°C to +125°C   | 8-Lead Standard Small Outline Package [SOIC_N] | Reel, 1000       | R-8            |
| ADA4620-1ARZ-RL    | −40°C to +125°C   | 8-Lead Standard Small Outline Package [SOIC_N] | Reel, 2500       | R-8            |
| EVAL-ADA4620-1ARZ  |                   | Evaluation Board                               |                  |                |
| ADA4620-2ARZ       | −40°C to +125°C   | 8-Lead Standard Small Outline Package [SOIC_N] | Tube, 98         | R-8            |
| ADA4620-2ARZ-R7    | −40°C to +125°C   | 8-Lead Standard Small Outline Package [SOIC_N] | Reel, 1000       | R-8            |
| ADA4620-2ARZ-RL    | −40°C to +125°C   | 8-Lead Standard Small Outline Package [SOIC_N] | Reel, 2500       | R-8            |
| EVAL-ADA4620-2ARZ  |                   | Evaluation Board                               |                  |                |

<sup>1</sup> Z = RoHS Compliant Part

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