

CoolGaN™
CoolGaN™ Transistor 100 V G3

PG-VSON-6

Features

- Ultra fast switching and high efficiency
- Space saving and highly robust package
- No reverse recovery charge
- Ultra low gate charge and output charge
- Moisture rating MSL1
- Industrial grade 3x5 package

Potential applications

- Telecom & Datacenter 48V IBC
- Sync Rectification for AC-DC and DC-DC converters
- Robotics and drones
- Battery powered tools
- 48V servo drive
- e-Mobility, UAVs
- Class D Audio
- Solar & Energy storage systems
- Point of Load Converters

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22 and J-STD-020.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on)}$	2.4	mΩ
I_D	76	A
Q_{oss}	43	nC
Q_G	11	nC
Q_{rr}	0	nC

Part number	Package	Marking	Related links
IGC033S101	PG-VSON-6	33SA1	see Appendix A

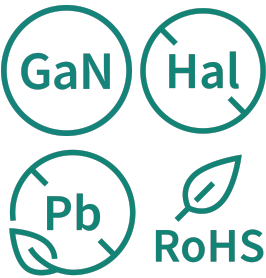
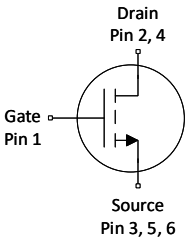
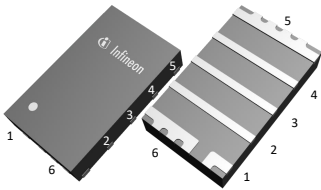




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1 Maximum ratings

at $T_j = 25\text{ °C}$, unless otherwise specified. Stresses beyond max ratings may cause permanent damage to the device. For optimum lifetime and reliability, Infineon recommends operating conditions that do not continuously exceed 80 % of the maximum ratings stated (unless otherwise explicitly stated). For further information, contact your local Infineon sales office.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain-source voltage	V_{DS}	-	-	100	V	$V_{GS}=0\text{ V}$
Pulsed drain-source voltage ¹⁾	$V_{DS, pulse}$	-	-	120	V	$V_{GS}=0\text{ V}$, 1 h total time
Continuous drain current	I_D	-	-	76	A	$V_{GS}=5\text{ V}$, $T_C=25\text{ °C}$
				21		$V_{GS}=5\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=38\text{ °C/W}$ ²⁾
Pulsed drain current ³⁾	$I_{D, pulse}$	-	-	700	A	$T_j=25\text{ °C}$
				330		$T_j=150\text{ °C}$
Pulsed gate-source voltage ¹⁾	V_{GS}	-6.5	-	6.5	V	Pulsed 100 h total time
Power dissipation	P_{tot}	-	-	45	W	$T_C=25\text{ °C}$
				3.3		$T_A=25\text{ °C}$, $R_{thJA}=38\text{ °C/W}$ ²⁾
Storage temperature	T_{stg}	-55	-	150	°C	-
Junction temperature	T_j	-40				

¹⁾ Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation.

²⁾ Device on 4-layer FR4 PCB, vertical in still air.

³⁾ Pulse current limited by transfer characteristic.

2 Recommended operating conditions

Table 3 Recommended operating conditions

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate-source voltage	V_{GS}	-4.0	5.0	5.5	V	-

3 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, top	R_{thJC}	-	15	18	°C/W	-
Thermal resistance, junction - case, bottom			1.9	2.8		
Thermal resistance, junction - ambient 1s0p	R_{thJA}	-	60	-	°C/W	On 1 layer PCB, vertical in still air.
Thermal resistance, junction - ambient 2s2p	R_{thJA}	-	38	-	°C/W	With vias on 4 layer PCB, vertical in still air.

4 Electrical Characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.2	1.9	2.9	V	$V_{DS}=V_{GS}$, $I_D=8.0\text{ mA}$
Drain-source leakage current	I_{DSS}	-	0.3	1.5	μA	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$
			6.0	50		$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	16	250	μA	$V_{GS}=5\text{ V}$, $T_j=25\text{ °C}$
			0.01	0.1		$V_{GS}=-4\text{ V}$, $T_j=25\text{ °C}$
			120	1100		$V_{GS}=5\text{ V}$, $T_j=125\text{ °C}$
			0.01	0.1		$V_{GS}=-4\text{ V}$, $T_j=125\text{ °C}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.4	3.3	$\text{m}\Omega$	$V_{GS}=5\text{ V}$, $I_D=20\text{ A}$
Gate resistance ⁴⁾	R_G	-	0.5	-	Ω	-

⁴⁾ Defined by design. Not subject to production test.

Table 6 Capacitance characteristics ⁵⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1200	1400	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}		540	590		
Reverse transfer capacitance	C_{rss}		6.1	8.0		

⁵⁾ Defined by design. Not subject to production test.

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	2.8	-	nC	$V_{DS}=50\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$		2.1	-	nC	
Gate to drain charge ⁶⁾	Q_{gd}		2.6	-	nC	
Switching charge	Q_{sw}		3.3	-	nC	
Gate charge total ⁶⁾	Q_g		11	14	nC	
Gate plateau voltage	$V_{plateau}$		2.6	-	V	
Output charge ⁶⁾	Q_{oss}	-	43	47	nC	$V_{DS}=50\text{ V}$, $V_{GS}=0\text{ V}$

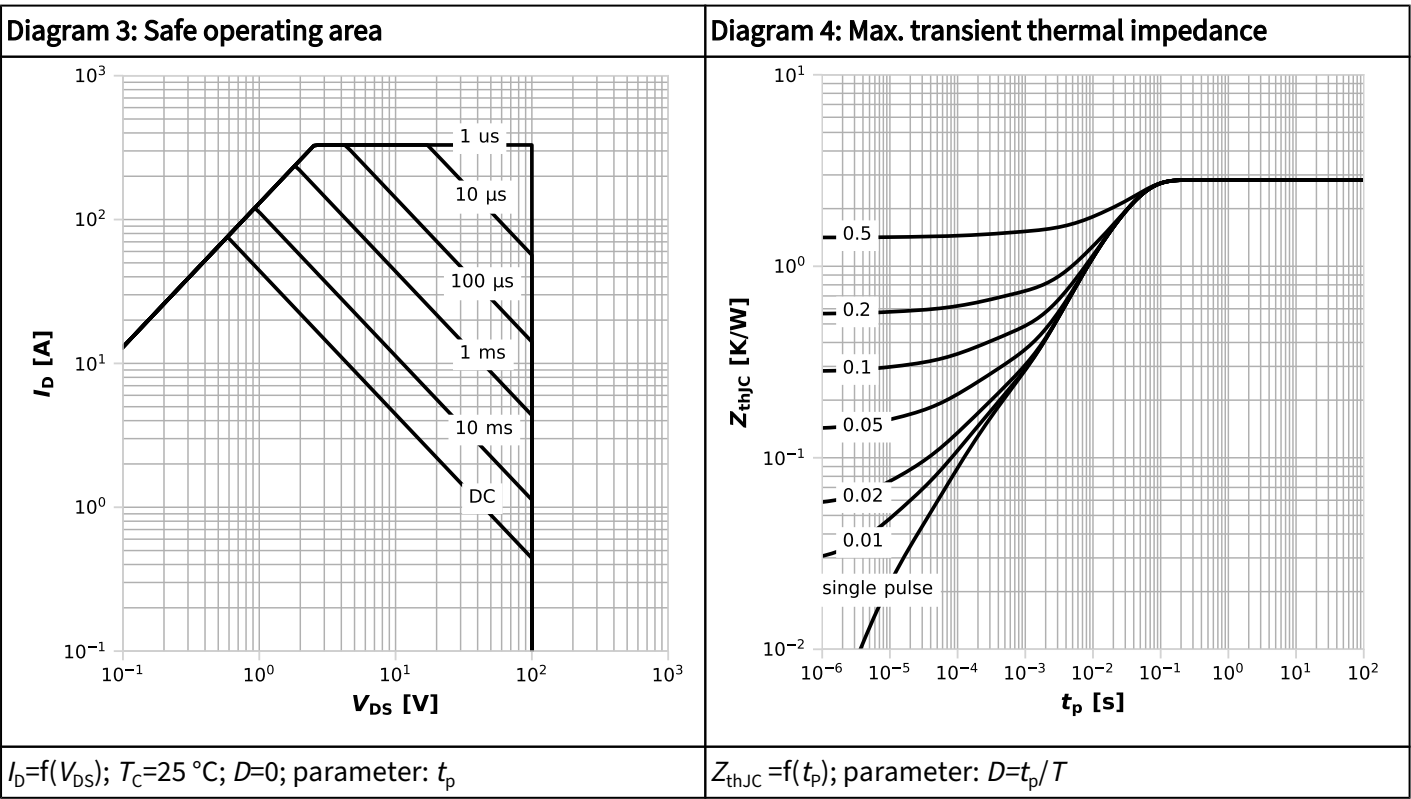
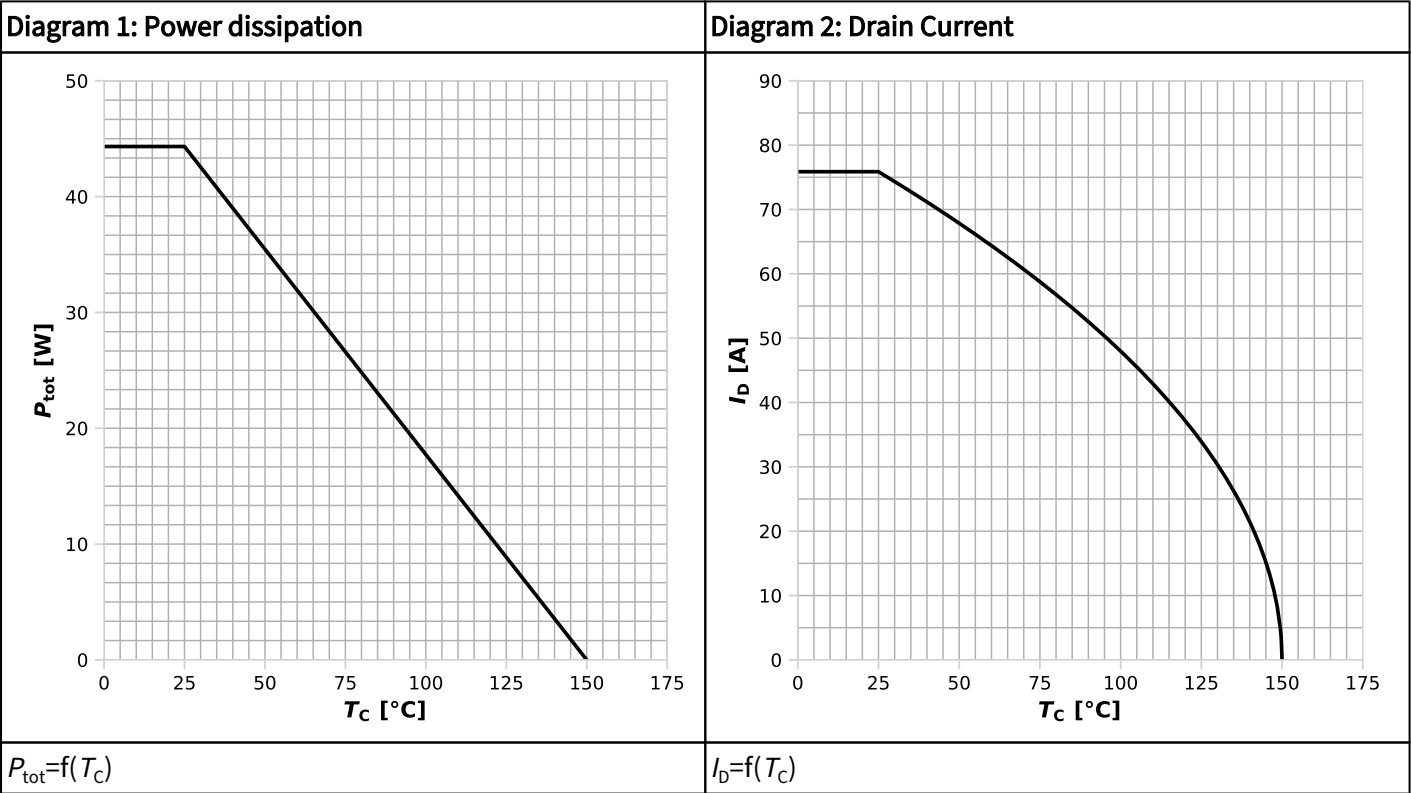
⁶⁾ Defined by design. Not subject to production test.

Table 8 Reverse operation

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Reverse continuous current	I_S	-	-	16	A	$T_C=25\text{ °C}$
Pulsed current, reverse	$I_{S,pulse}$			304		
Source-Drain reverse voltage	V_{SD}	-	2.4	3.1	V	$V_{GS}=0\text{ V}, I_{S,pulse}=20\text{ A}, T_j=25\text{ °C}$
			2.0	-		$V_{GS}=0\text{ V}, I_{S,pulse}=0.5\text{ A}, T_j=25\text{ °C}$
Reverse recovery charge ⁷⁾	Q_{rr}	-	0	-	nC	$V_R=50\text{ V}, I_{S,pulse}=20\text{ A}, di_{S,pulse}/dt=100\text{ A}/\mu\text{s}$

⁷⁾ Defined by design. Not subject to production test.

5 Electrical characteristics diagrams



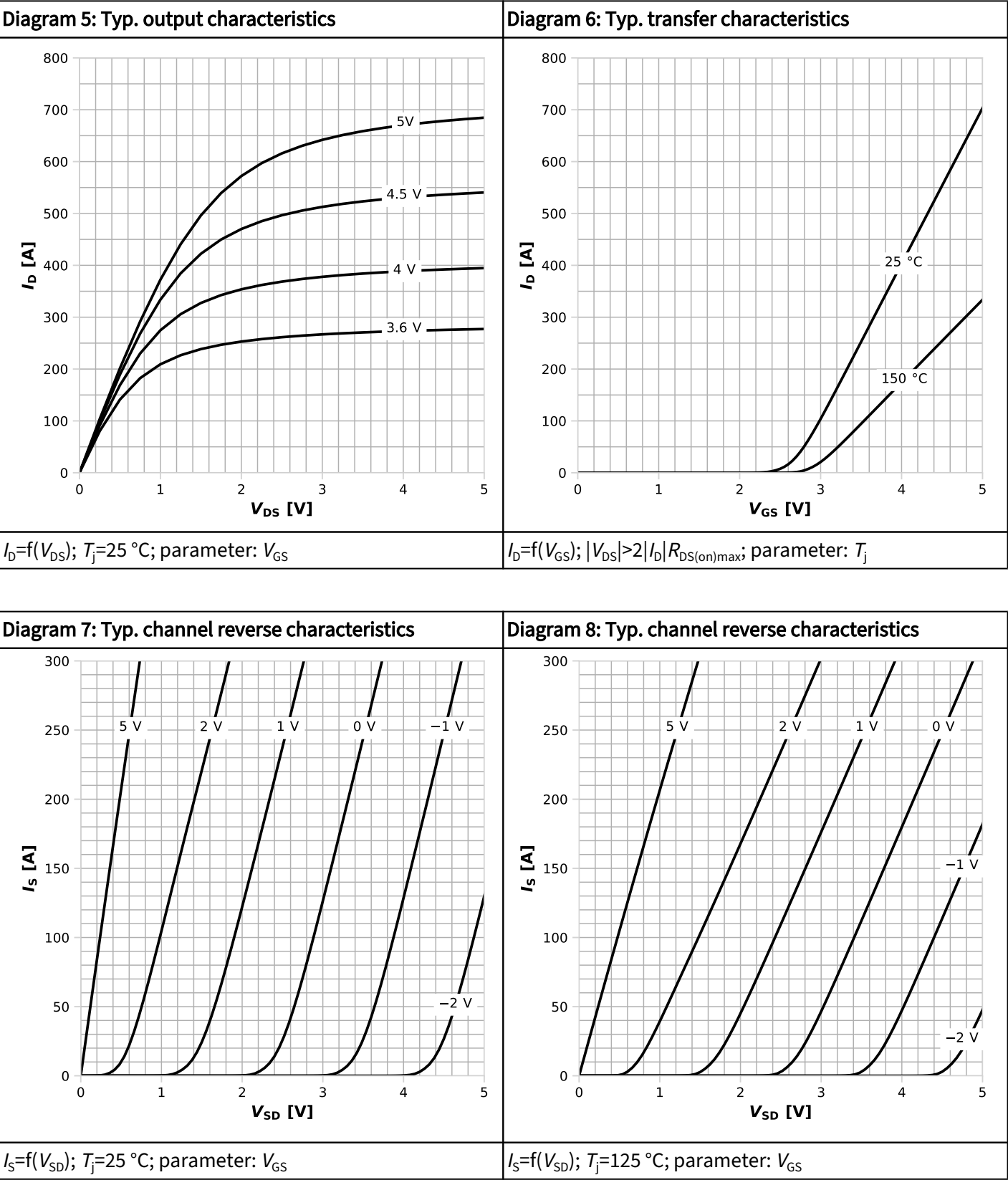
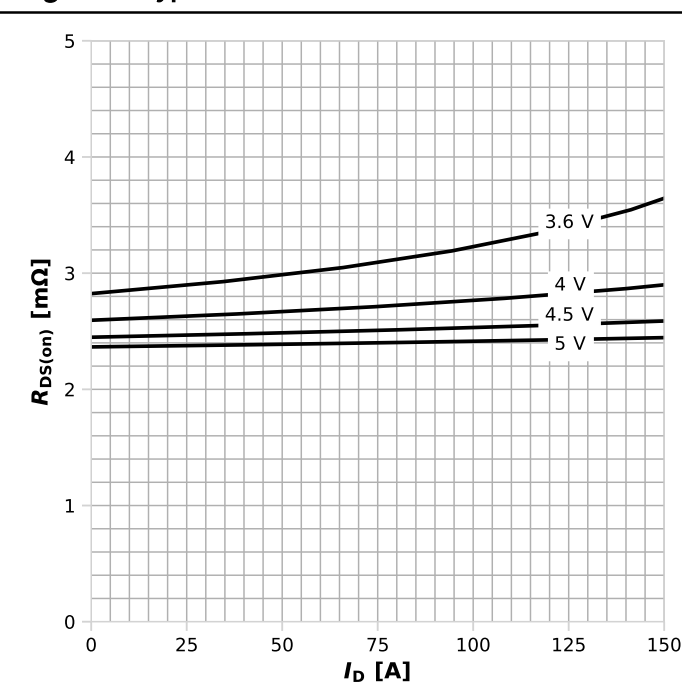
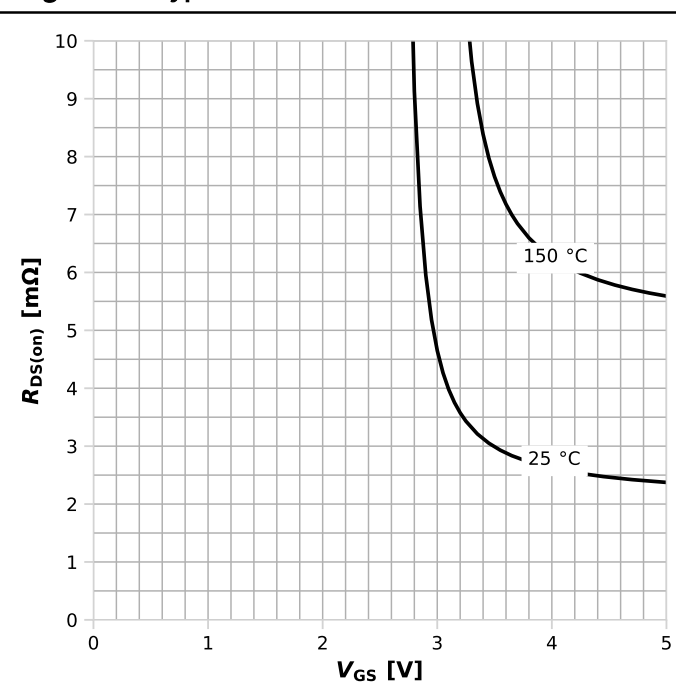


Diagram 9: Typ. drain-source on-state resistance



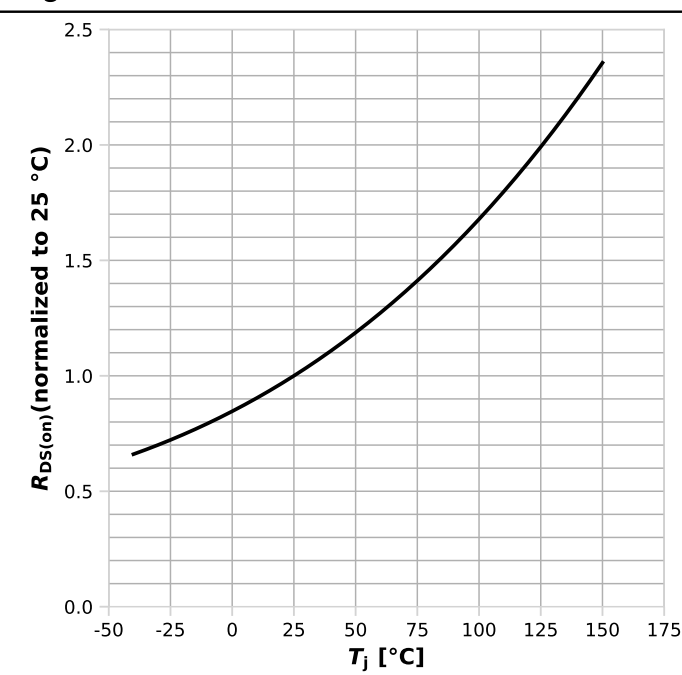
$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 10: Typ. Drain-source on-state resistance



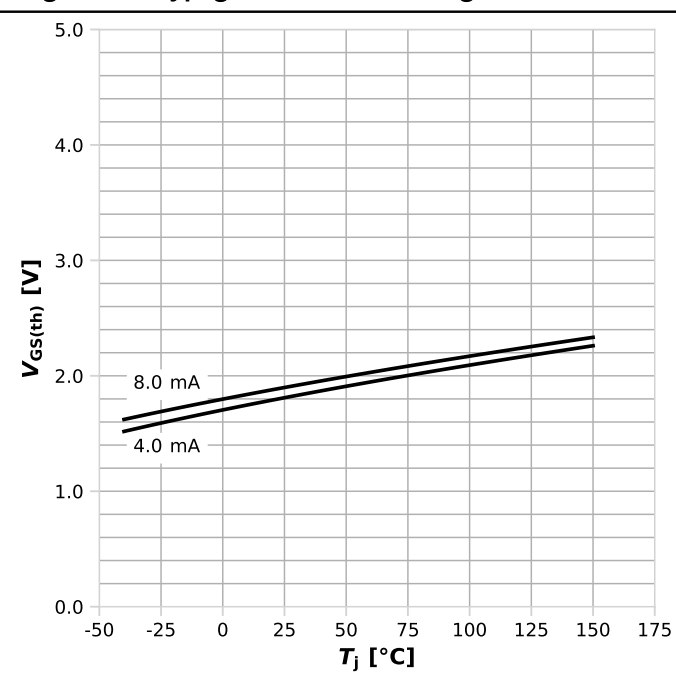
$R_{DS(on)} = f(V_{GS}); I_D = 20 \text{ A}; \text{parameter: } T_j$

Diagram 11: Drain-source on-state resistance



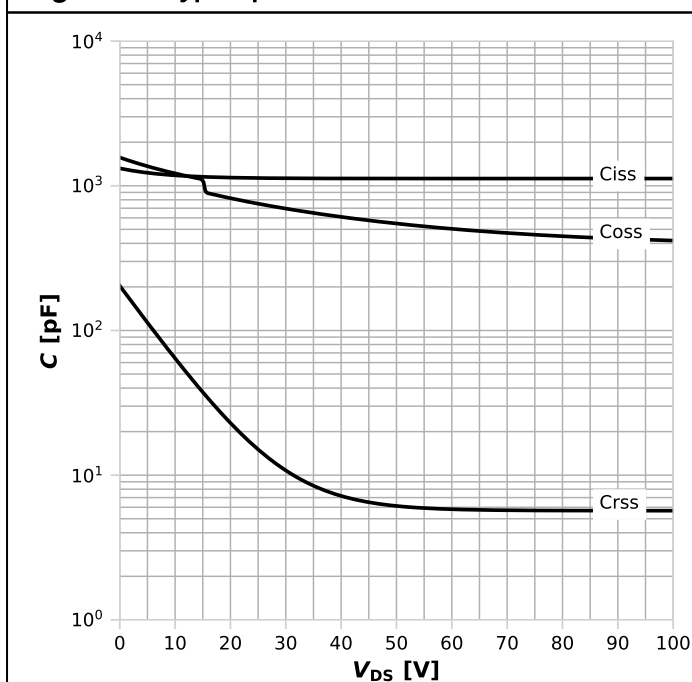
$R_{DS(on)} = f(T_j); I_D = 20 \text{ A}, V_{GS} = 5 \text{ V}$

Diagram 12: Typ. gate threshold voltage



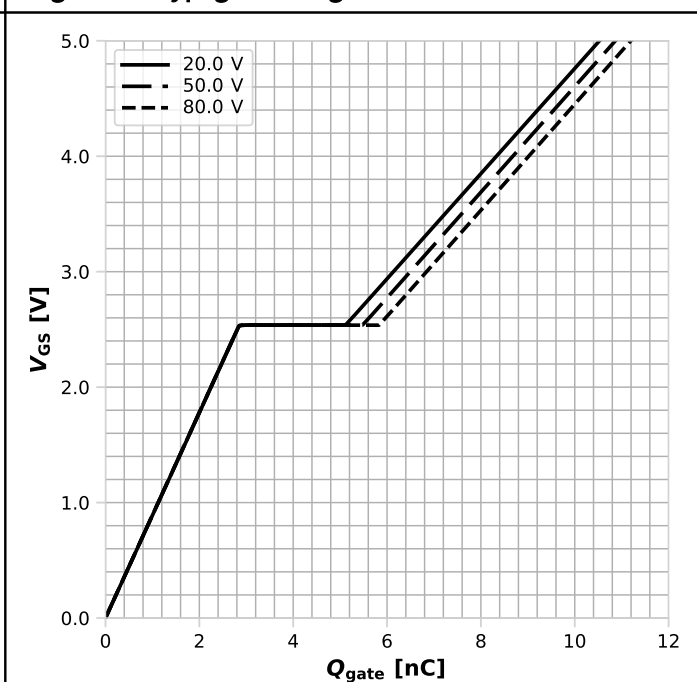
$V_{GS(th)} = f(T_j), V_{GS} = V_{DS}; \text{parameter: } I_D$

Diagram 13: Typ. capacitances



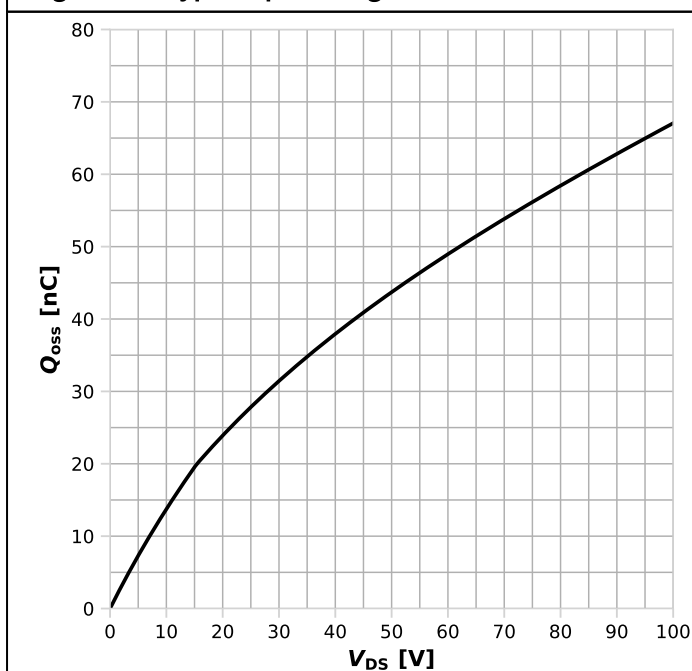
$$C=f(V_{DS}); V_{GS}=0\text{ V}$$

Diagram 14 Typ. gate charge



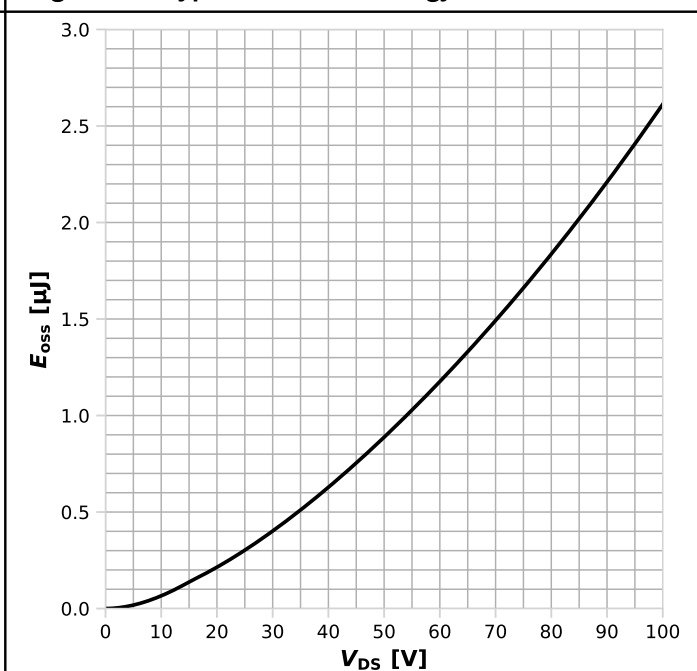
$$V_{GS}=f(Q_{gate}); I_D=20\text{ A pulsed; parameter: }V_{DS}$$

Diagram 15: Typ. output charge



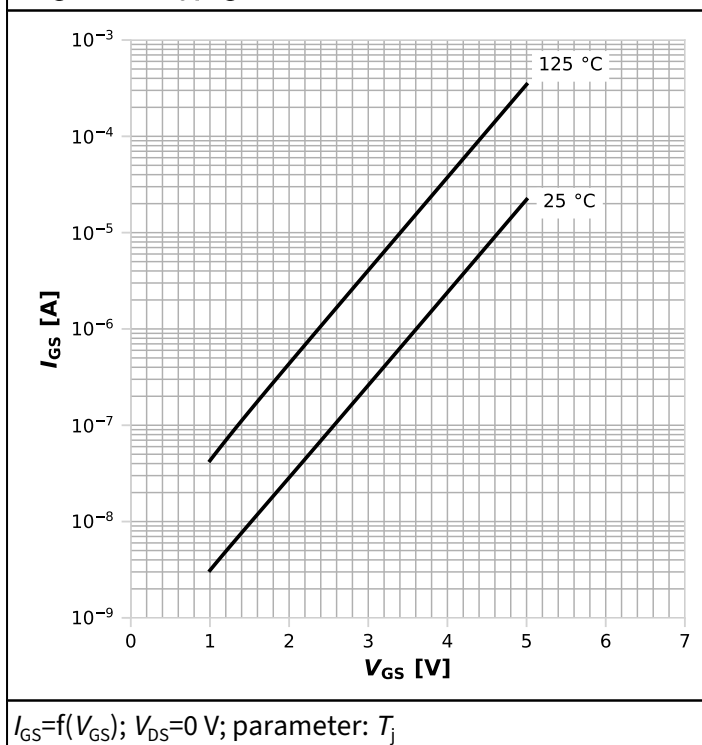
$$Q_{oss}=f(V_{DS}), V_{GS}=0\text{ V}$$

Diagram 16: Typ. Coss stored Energy

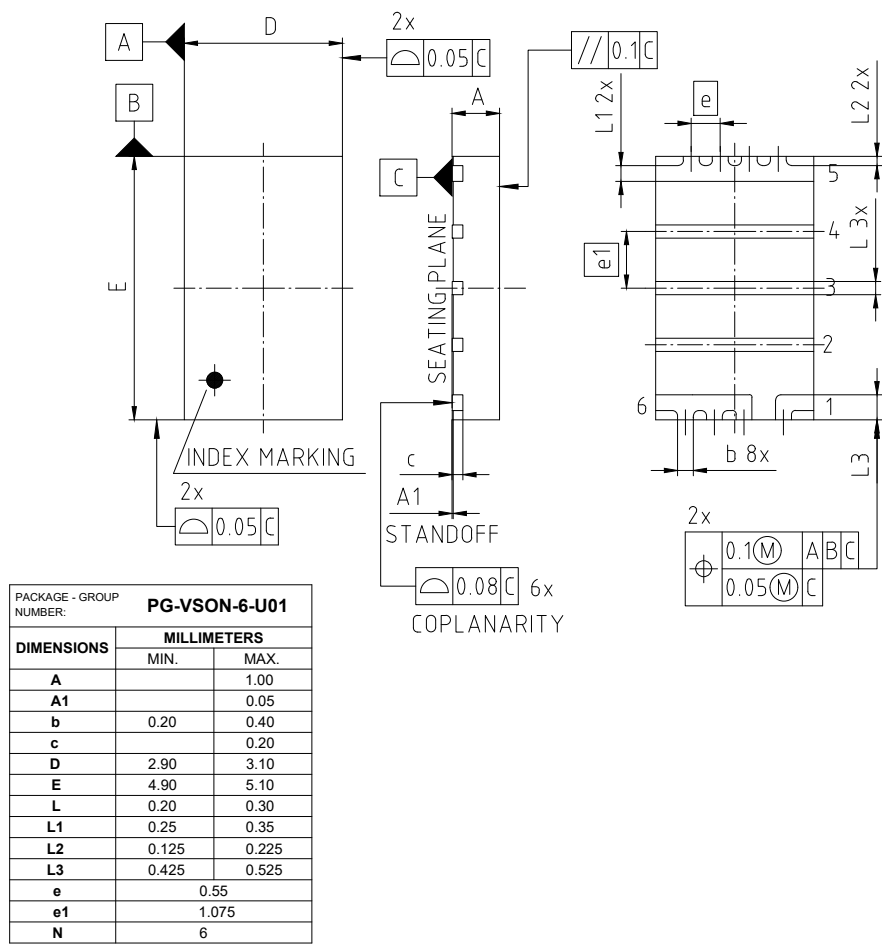


$$E_{oss}=f(V_{DS}), V_{GS}=0\text{ V}$$

Diagram 17: Typ. gate characteristics forward



6 Package outlines



NOTE:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-VSON-6, dimensions in mm

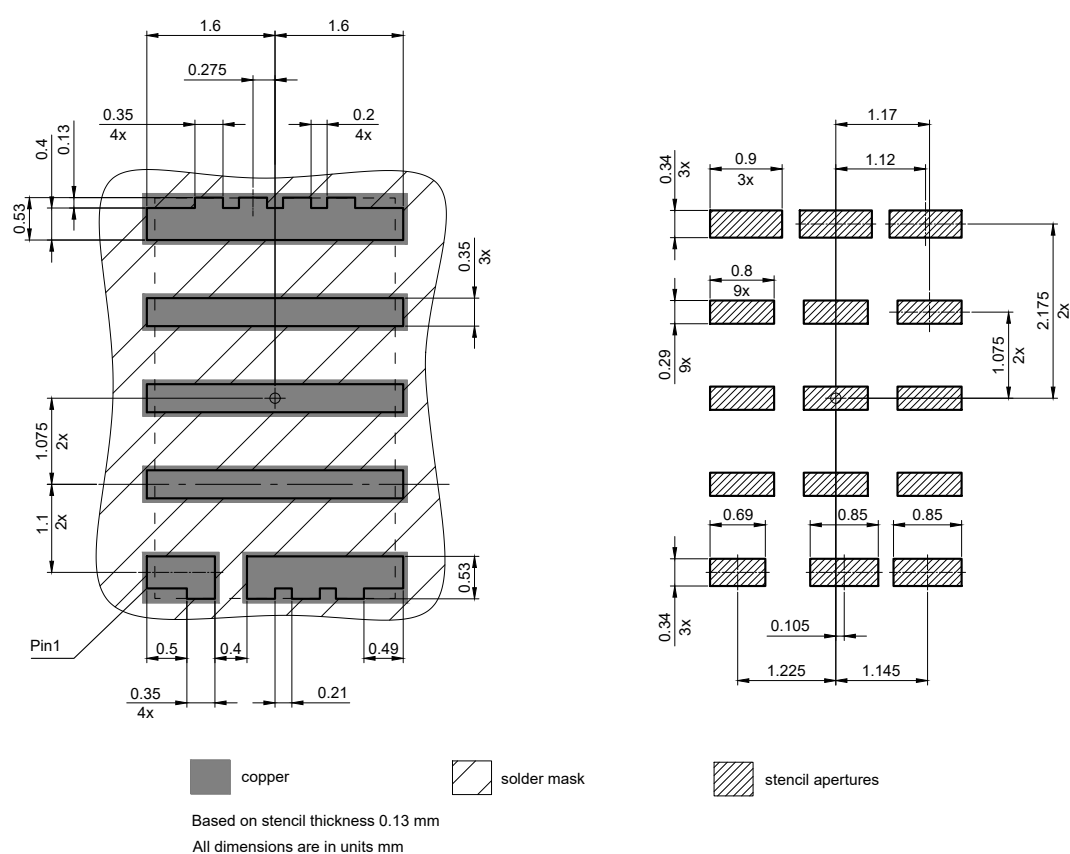
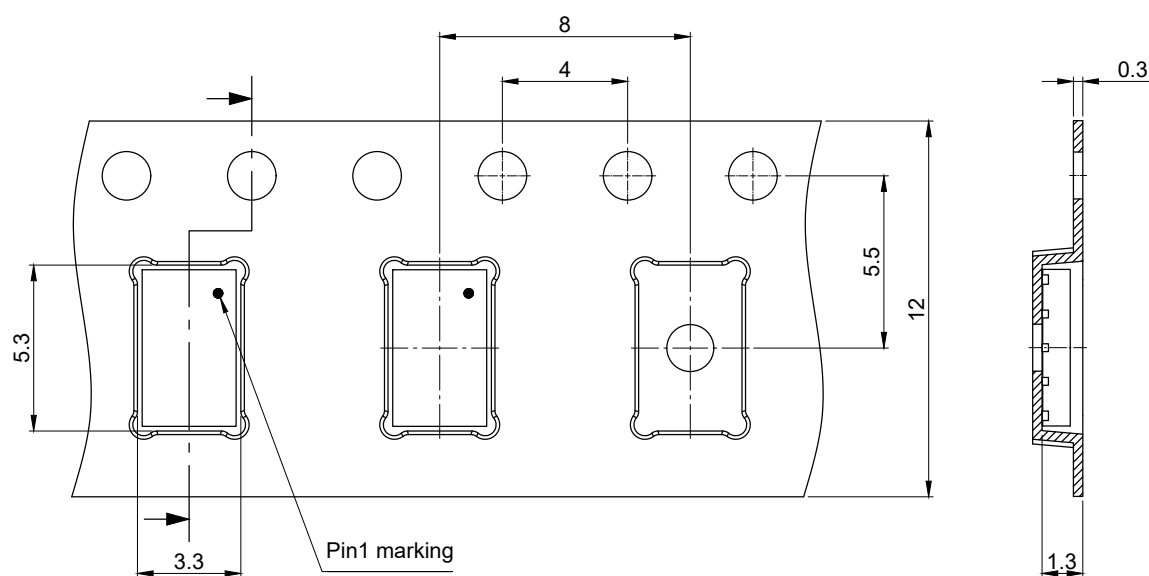


Figure 2 Footprint drawing PG-VSON-6, dimensions in mm



All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 3 Packaging variant PG-VSON-6, dimensions in mm

7 Appendix A

Table 9 **Related links**

- [IFX CoolGaN™ GaN webpage](#)
- [IFX CoolGaN™ reliability white paper](#)
- [IFX CoolGaN™ gate driver application note](#)
- [IFX CoolGaN™ Evaluation Boards](#)
- [IFX Packages Description-PG-VSON-6-3](#)

Revision history

IGC033S101

Revision 2025-04-22, Rev. 1.2

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2024-12-10	Release of final
1.1	2024-12-12	Updated Features
1.2	2025-04-22	Updated static IGSS characteristics

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