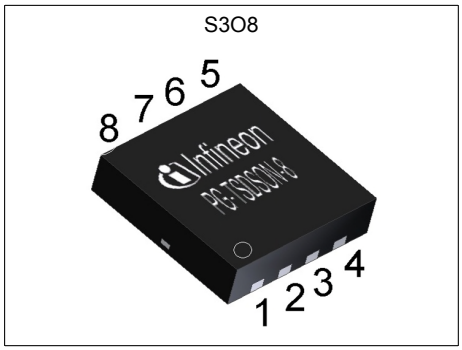
MOSFET

OptiMOS™3 M-Series Power-MOSFET, 30 V



Features

- Optimized for 5V driver application (Notebook, VGA, POL)
- Low FOM_{SW} for High Frequency SMPS
- 100% avalanche tested
- N-channel
- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Qualified according to JEDEC[1] for target applications
- Superior thermal resistance
- Pb-free plating; RoHS compliant
- Halogen free according to IEC61249-2-21

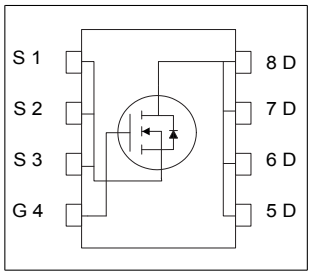


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	30	V
$R_{DS(on),max}$, V_{GS}=10 V	8	mΩ
$R_{DS(on),max}$, V_{GS}=4.5 V	9.7	mΩ
I_D	50	A

Type / Ordering Code	Package	Marking	Related Links
BSZ088N03MS G	PG-TSDSON-8	088N03M	-

[1] J-STD20 and JESD22

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1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- - - - -	- - - - -	50 32 45 29 11	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=4.5 V, T_C=25 °C V_{GS}=4.5 V, T_C=100 °C V_{GS}=4.5 V, T_A=25 °C, R_{thJA}=60 K/W[2]
Pulsed drain current[3]	$I_{D,pulse}$	-	-	200	A	T_C=25 °C
Avalanche current, single pulse[4]	I_{AS}	-	-	20	A	T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	25	mJ	I_D=20 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	35 2.1	W	T_C=25 °C T_A=25 °C, R_{thJA}=60 K/W[2]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.6	K/W	-
Device on PCB, 6 cm^2 cooling area[2]	R_{thJA}	-	-	60	K/W	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[3] See Diagram 3 for more detailed information
[4] See Diagram 13 for more detailed information

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3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1	-	2	V	V_{DS}=V_{GS}, I_D=250 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=30 V, V_{GS}=0 V, T_j=25 °C V_{DS}=30 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=16 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	8.2 6.7	9.7 8.0	mΩ	V_{GS}=4.5 V, I_D=20 A V_{GS}=10 V, I_D=20 A
Gate resistance	R_G	0.5	1	1.8	Ω	-
Transconductance	g_{fs}	28	57	-	S	|V_{DS}|>2|I_D|$R_{DS(on)max}$, I_D=30 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1)]	C_{iss}	-	1600	2100	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Output capacitance[1)]	C_{oss}	-	510	680	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	33	-	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	4.3	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, R_G=1.6 Ω
Rise time	t_r	-	3.0	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, R_G=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	18	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, R_G=1.6 Ω
Fall time	t_f	-	2.4	-	ns	V_{DD}=15 V, V_{GS}=10 V, I_D=30 A, R_G=1.6 Ω

Table 6 Gate charge characteristics[2)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge[1)]	Q_{gs}	-	5.0	6.7	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge at threshold[1)]	$Q_{g(th)}$	-	2.5	3.4	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate to drain charge[1)]	Q_{gd}	-	2.3	3.8	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Switching charge[1)]	Q_{sw}	-	4.8	7.2	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge total[1)]	Q_g	-	9.9	13	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	3.2	-	V	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge total[1)]	Q_g	-	21	27	-	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET[1)]	$Q_{g(sync)}$	-	8.6	11	nC	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V
Output charge[1)]	Q_{oss}	-	13	18	-	V_{DD}=15 V, V_{GS}=0 V

[1)] Defined by design. Not subject to production test
[2)] See ″Gate charge waveforms″ for parameter definition

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Table 7 Reverse diode

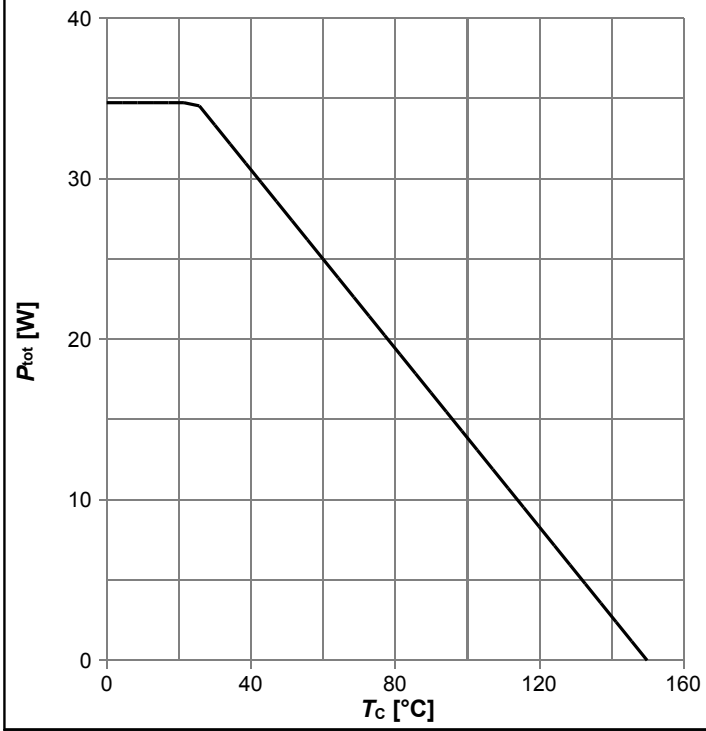
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	31	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	200	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.87	1.1	V	V_{GS}=0 V, I_F=20 A, T_j=25 °C
Reverse recovery charge[1)]	Q_{rr}	-	-	10	nC	V_R=15 V, I_F=I_S, di_F/dt=400 A/µs

[1)] Defined by design. Not subject to production test

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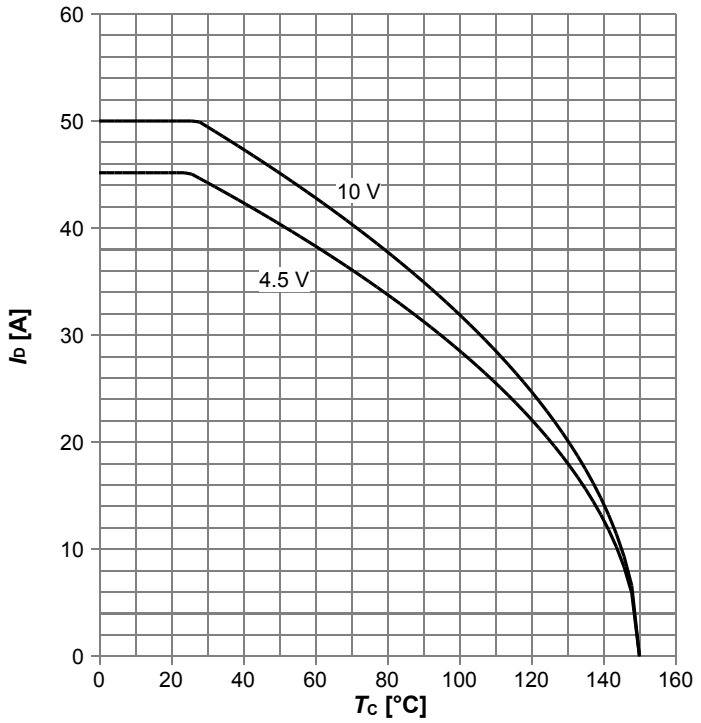
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



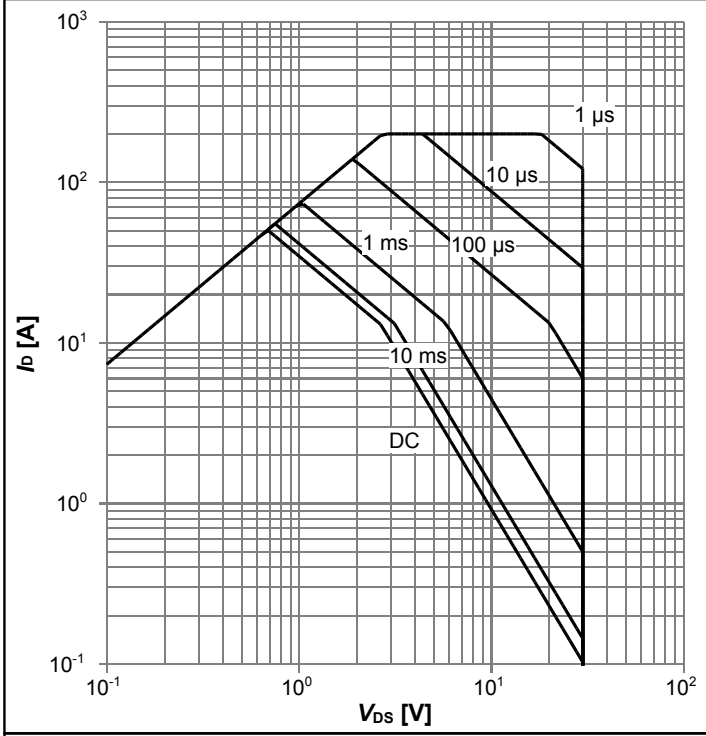
$P_{tot}=f(T_C)$

Diagram 2: Drain current



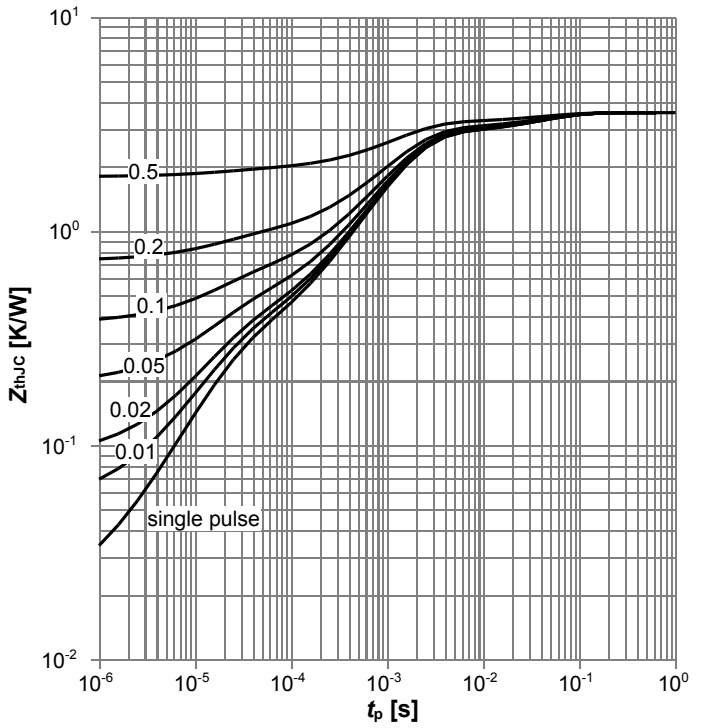
$I_D=f(T_C)$; parameter: V_{GS}

Diagram 3: Safe operating area



$I_D=f(V_{DS})$; T_C=25 °C; D=0; parameter: t_p

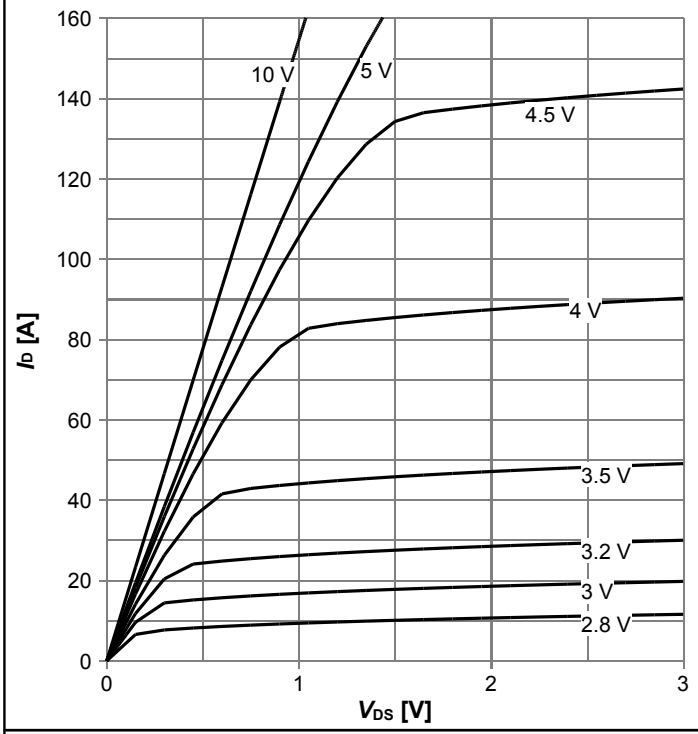
Diagram 4: Max. transient thermal impedance



$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

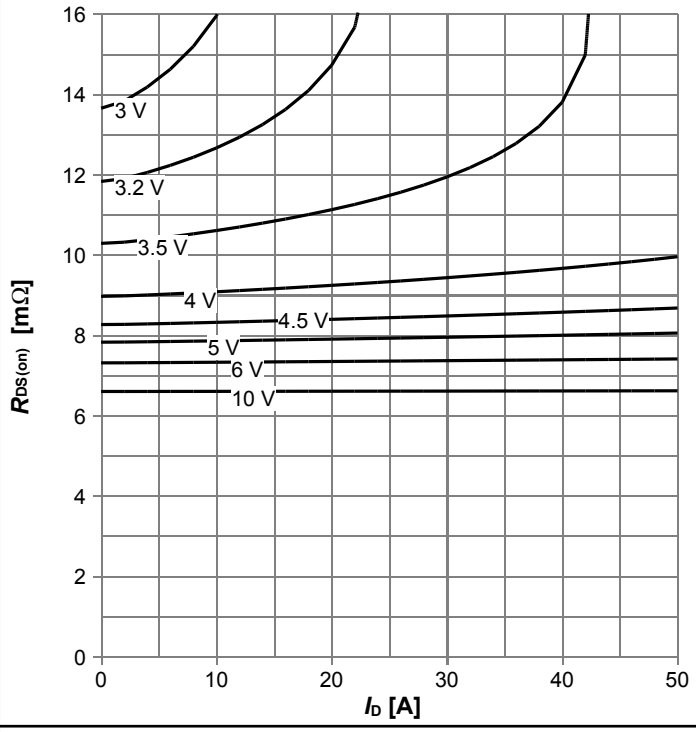
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Diagram 5: Typ. output characteristics



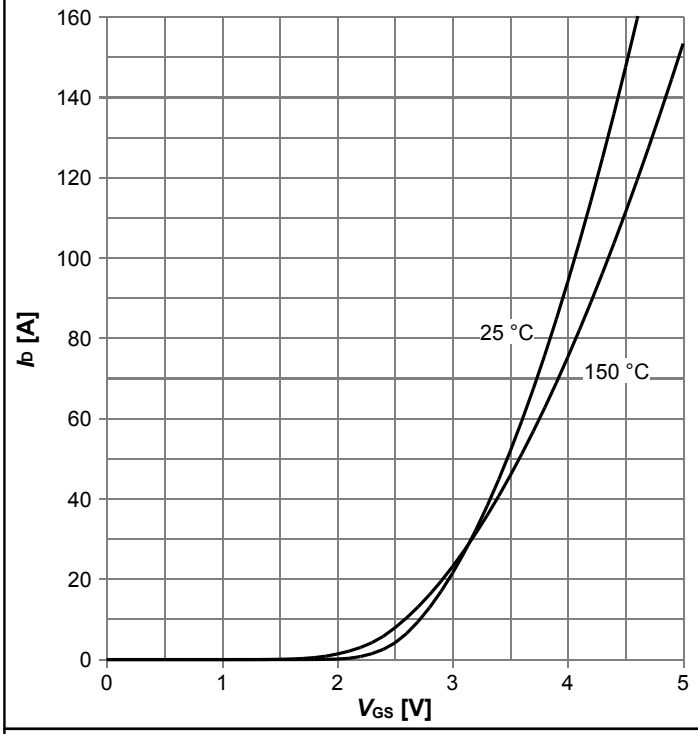
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



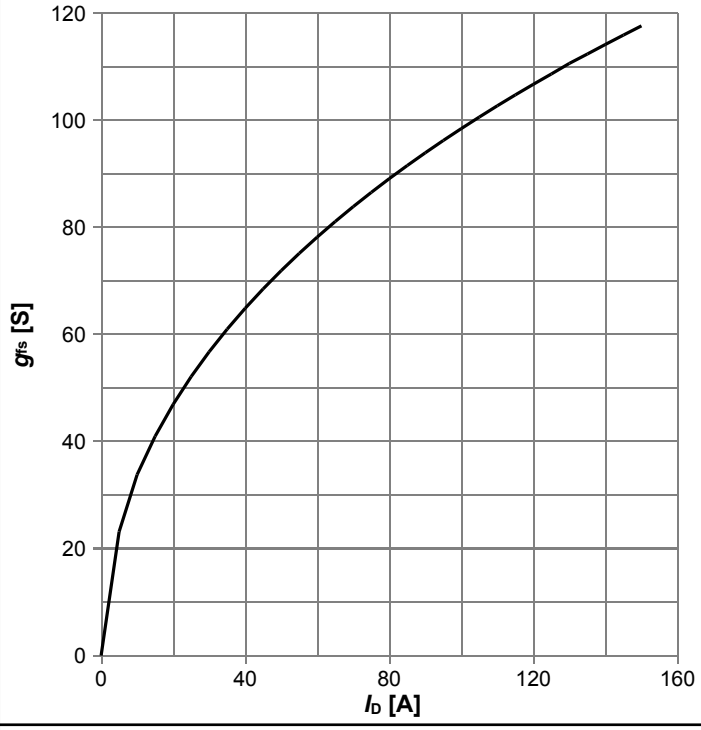
$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

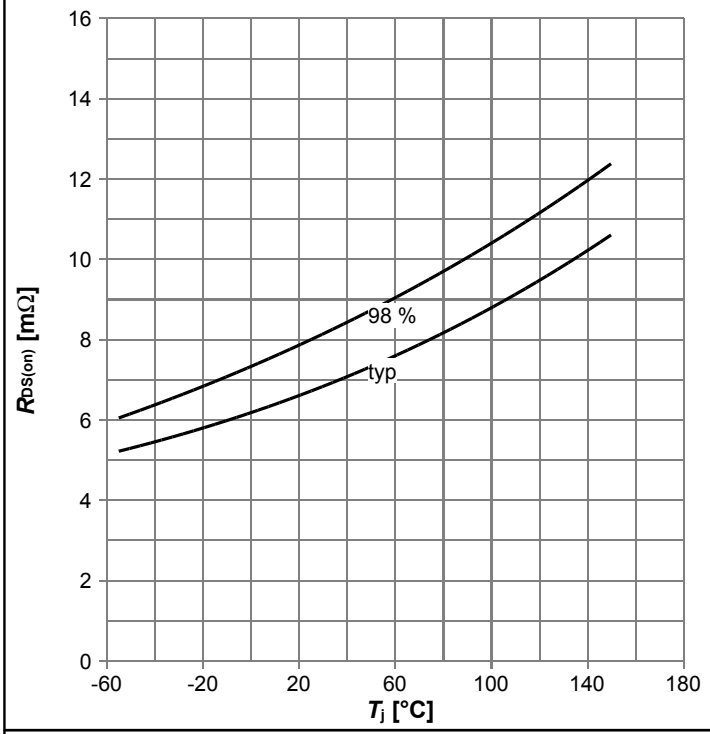
Diagram 8: Typ. forward transconductance



g_{fs}=f(I_D); T_j=25 °C

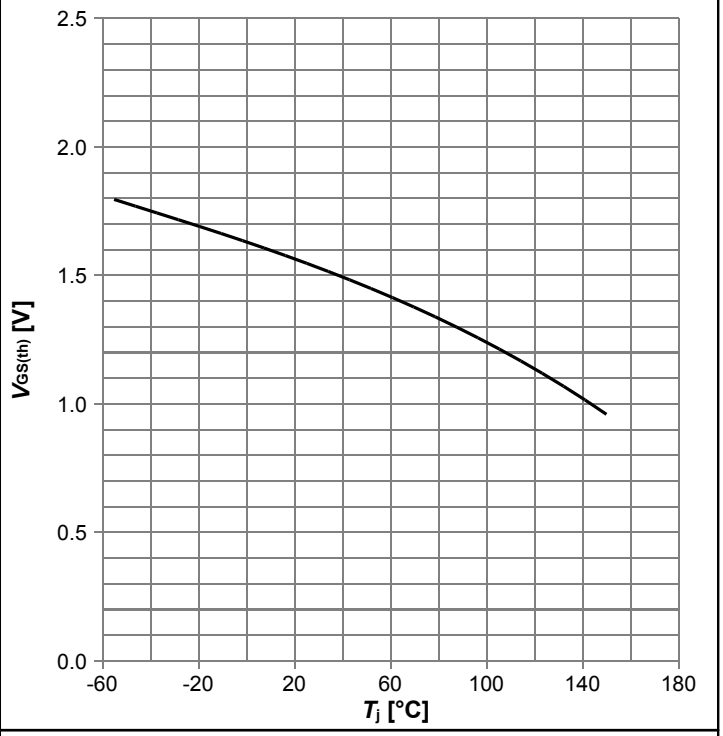
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Diagram 9: Drain-source on-state resistance



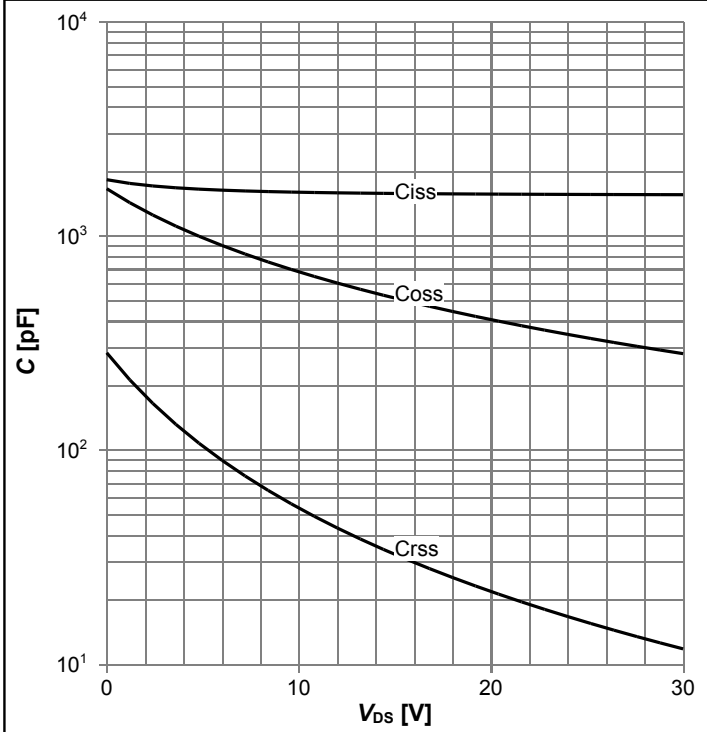
$R_{DS(on)}$=f(T_j); I_D=20 A; V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



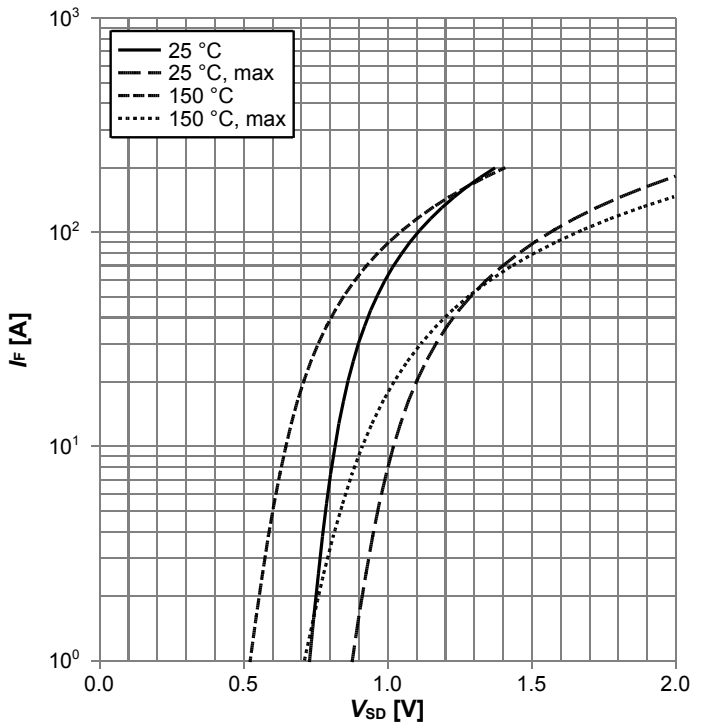
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=250 µA

Diagram 11: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

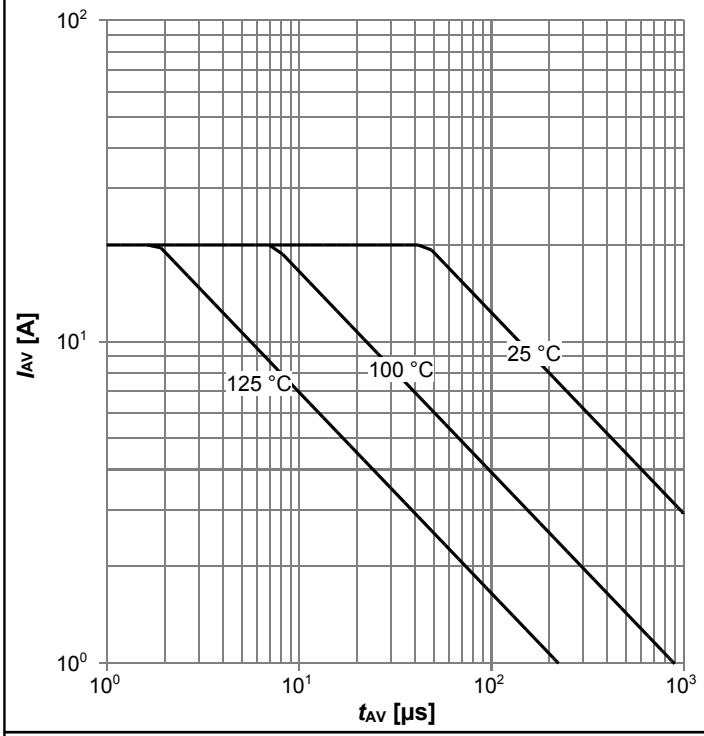
Diagram 12: Forward characteristics of reverse diode



I_F=f(V_{SD}); parameter: T_j

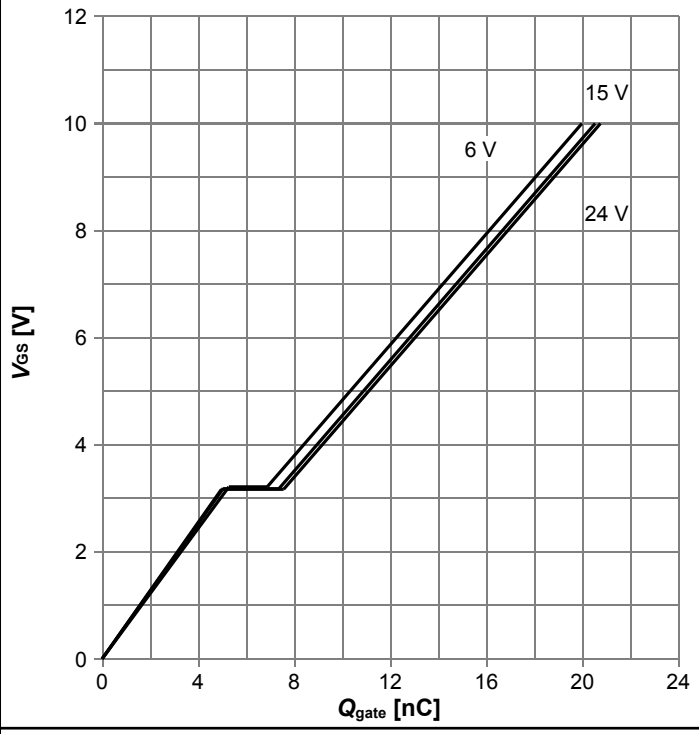
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Diagram 13: Avalanche characteristics



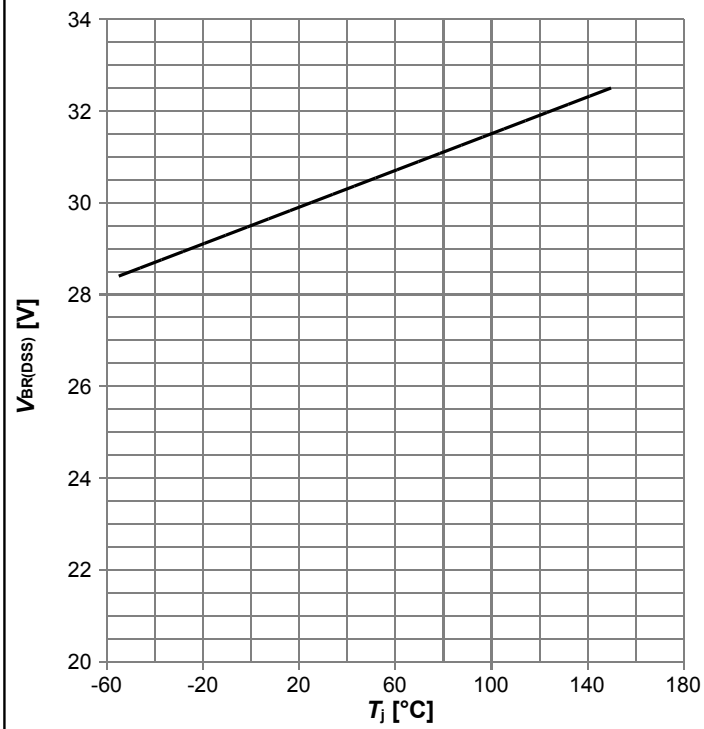
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



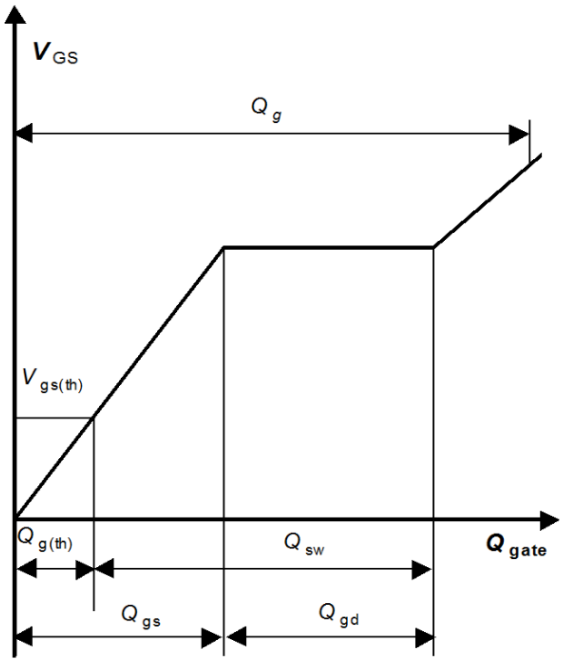
V_{GS}=f(Q_{gate}); I_D=30 A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



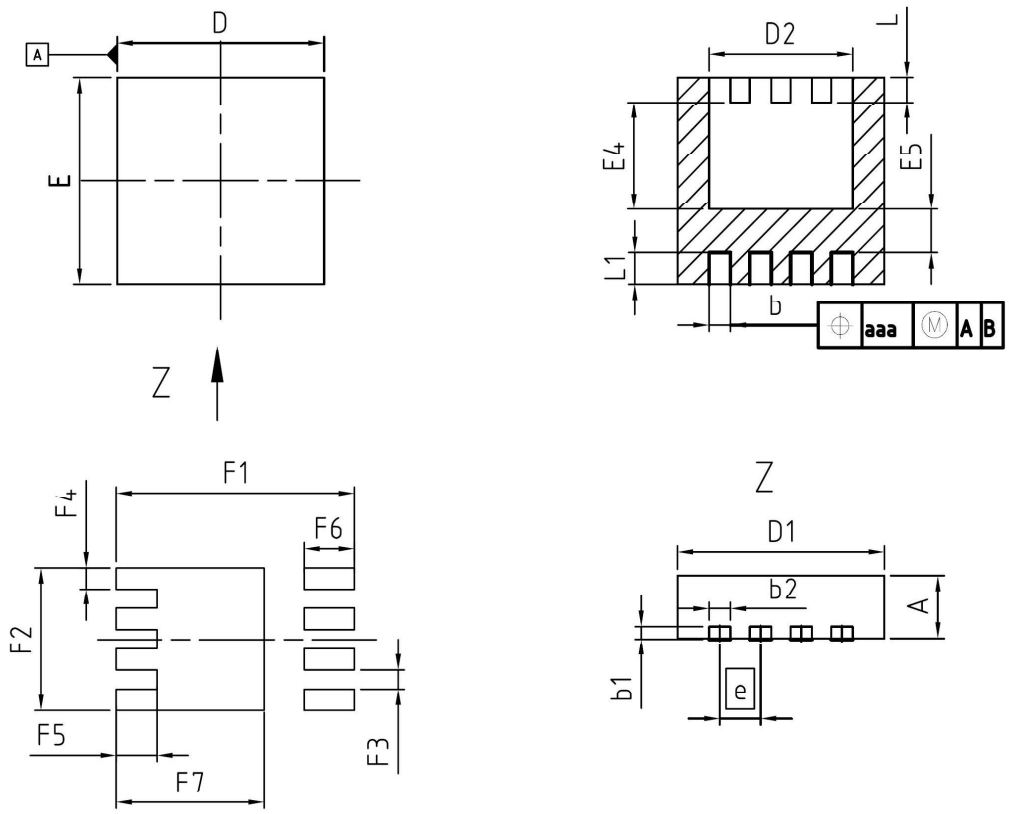
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram Gate charge waveforms



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5 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.24	0.44	0.009	0.017
b1	0.10	0.30	0.004	0.012
b2	0.20	0.44	0.008	0.017
D=D1	3.20	3.40	0.126	0.134
D2	2.15	2.45	0.085	0.096
E	3.20	3.40	0.126	0.134
E4	1.60	1.81	0.063	0.071
E5	0.59	0.86	0.023	0.034
e	0.65		0.026	
N	8		8	
L	0.30	0.56	0.012	0.022
L1	0.33	0.60	0.013	0.024
aaa	0.25		0.010	
F1	3.80		0.150	
F2	2.29		0.090	
F3	0.31		0.012	
F4	0.34		0.013	
F5	0.65		0.026	
F6	0.80		0.031	
F7	2.36		0.093	

DOCUMENT NO.
Z8B00131645

SCALE 0 2.5 0 2.5 5mm

EUROPEAN PROJECTION

ISSUE DATE
17-09-2008

REVISION
02

Figure 1 Outline PG-TSDSON-8, dimensions in mm/inches

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Revision History

BSZ088N03MS G

Revision: 2020-07-27, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.1	2020-07-27	Update current rating and footnotes

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