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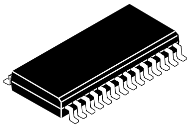
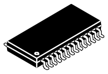
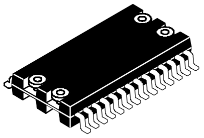




bq4802Y
bq4802LY

SLUS464C – AUGUST 2000 – REVISED JUNE 2002

PARALLEL REAL-TIME CLOCK WITH CPU SUPERVISOR AND EXTERNAL SRAM NONVOLATILE MEMORY BACKUP

FEATURES

- **Real-Time Clock Counts Seconds Through Centuries in BCD Format**
  - **bq4802Y: 5-V Operation**
  - **bq4802LY: 3.3-V Operation**
- **On-Chip Battery-Backup Switchover Circuit With Nonvolatile Control for External SRAM**
- **Less Than 500 nA of Clock Operation Current in Backup Mode**
- **Microprocessor Reset With Push-Button Override**
- **Independent Watchdog Timer With Programmable Time-Out Period**
- **Power-Fail Interrupt Warning**
- **Programmable Clock Alarm Interrupt Active in Battery-Backup Mode**
- **Programmable Periodic Interrupt**
- **Battery-Low Warning**
- **28-pin SOIC, TSSOP, and SNAPHAT Package Options**

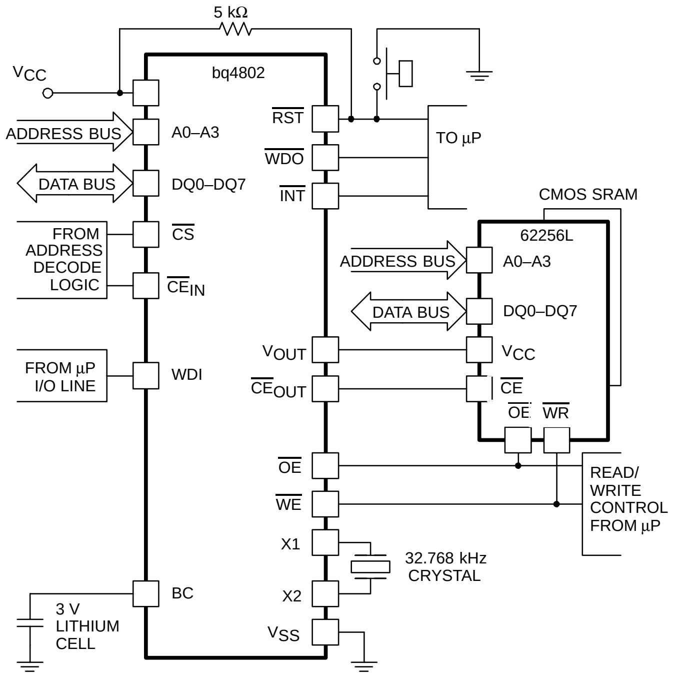
APPLICATIONS

- **Telecommunications Base Stations**
- **Servers**
- **Handheld Data Collection Equipment**
- **Medical Equipment**
- **Handheld Instrumentation**
- **Test Equipment**

DESCRIPTION

The bq4802Y/bq4802LY real-time clock is a low-power microprocessor peripheral that integrates a time-of-day clock, a century-based calendar, and a CPU supervisor, with package options including a 28-pin SOIC, TSSOP, or SNAPHAT that requires the bq48SH-28x6 to complete the two-piece module. The bq4802Y/bq4802LY is ideal for fax machines, copiers, industrial control systems, point-of-sale terminals, data loggers, and computers.

TYPICAL APPLICATION



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The bq4802Y/bq4802LY provides direct connections for a 32.768-kHz quartz crystal and a 3-V backup battery. Through the use of the conditional chip enable output ($\overline{CE}_{OUT}$) and battery voltage output (V_{OUT}) pins, the bq4802Y/bq4802LY can write-protect and make non- volatile external SRAMs. The backup cell powers the real-time clock and maintains SRAM information in the absence of system voltage. The crystal and battery are contained within the modules for a more integrated solution.

The bq4802Y/bq4802LY contains a temperature-compensated reference and comparator circuit that monitors the status of its voltage supply. When the bq4802Y/bq4802LY detects an out-of-tolerance condition, it generates an interrupt warning and subsequently a microprocessor reset. The reset stays active for 200 ms after V_{CC} rises within tolerance, to allow for power supply and processor stabilization. The reset function also allows for an external push-button override.

ORDERING INFORMATION

T_A	OPERATION	DEVICES			SYMBOL
		SOIC(1) (DW)	**TSSOP(1) (PW)**	**SNAPHAT(1)(2)(3) (DSH)**	
0°C to +70°C	5 V	bq4802YDW	bq4802YPW	bq4802YDSH	bq4802Y
	3.3 V	bq4802LYDW	bq4802LYPW	bq4802LYDSH	bq4802LY

(1) The DW, PW and DSH packages are available taped and reeled. Add an R suffix to the device type (i.e., bq4802YDWR).
(2) The DSH package is available taped only.
(3) The bq48SH–28x6 should be ordered to complete the SNAPHAT module and is the same part number for both 3.3-V and 5-V modules.

CAUTION: Wave soldering of DSH package may cause damage to SNAPHAT sockets.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	bq4802Y bq4802LY
Input voltage range, VCC, V_T ($V_T \leq$ VCC +0.3)	–0.3 V to 6.0 V
Operating temperature range, T_J	0°C to 70°C
Storage temperature range, T_{stg}	–55°C to 125°C
Temperature under bias, T_{Jbias}	–40°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	300°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage, V_{CC}	bq4802Y	4.5	5.5	V
	bq4802LY	2.7	3.6	
Input low voltage, V_{IL}		–0.3	0.8	V
Input high voltage, V_{IH}		2.2	V_{CC} + 0.3	V
Backup cell voltage, V_{BC}		2.4	4.0	V
Push button reset input low, V_{BC}		–0.3	0.4	V
Push button reset input high, V_{PBRH}		2.2	V_{CC} + 0.3	V

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, $V_{CC(min)} \leq V_{CC} \leq V_{CC(max)}$ unless otherwise noted)

INPUT SUPPLY

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current		100% Minimum duty cycle, $\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA		5	9	mA
I_{SB1}	Standby supply current		$\overline{CS}$ = V_{IH}		3		mA
			$\overline{CS}$ = V_{CC} – 0.2 V, 0 V ≤ V_{IN} ≤ 0.2 V or V_{IN} = V_{CC} – 0.2 V		1.5		
I_{CCB}	Battery operation supply current		V_{BC} = 3 V, T_A = 25°C, No load at V_{OUT} or $\overline{CE}_{OUT}$, $I_{I/O}$ = 0 mA		0.3	0.5	µA
I_{LI}	Input leakage current		V_{IN} = V_{SS} to V_{CC}	–1		1	µA
I_{LO}	Output leakage current		$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}	–1		1	µA
$V_{OUT(1)}$	Output voltage		I_{OUT} = 80 mA, V_{CC} > V_{BC}	V_{CC}-0.3			V
$V_{OUT(2)}$			I_{OUT} = 100 µA, V_{CC} < V_{BC}	V_{BC}-0.3			
V_{PFD}	Power fail detect voltage	bq4802Y		4.30	4.37	4.5	V
		bq4802LY		2.4	2.53	2.65	
V_{SO}	Supply switch over voltage		V_{BC} > $V_{(PFD)}$		V_{PFD}		V
			V_{BC} < $V_{(PFD)}$		V_{BC}		
$V_{\overline{RST}}$	RST output voltage(1)		$I_{(RST)}$ = 4 mA			0.4	V
$V_{\overline{INT}}$	INT output voltage(1)		$I_{(INT)}$ = 4 mA			0.4	V

(1) $\overline{RST}$ and $\overline{INT}$ are open drain outputs.

WATCHDOG

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(WDIL)}$	Low-level watchdog input current		–50	–10		µA
$I_{(WDIH)}$	High-level watchdog input current			20	50	
$V_{(WDO)}$	$\overline{WDO}$ output voltage	I_{SINK} = 4 mA			0.4	V
		I_{SOURCE} = 2 mA	2.4			

CRYSTAL SPECIFICATIONS (DT-26) OR EQUIVALENT)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_O	Oscillation frequency			32.768		kHz
C_L	Load capacitance			6		pF
T_P	Temperature turnover point		20	25	30	°C
k	Parabolic curvature constant				–0.042	ppm/°C
Q	Quality factor		40,000	70,000		
R_1	Series resistance				45	kΩ
C_0	Shunt capacitance			1.1	1.8	pF
C_0/C_1	Capacitance ratio			430	600	
D_L	Drive level				1	µW
$\Delta f/f_0$	Aging (first year at 25°C)			1	–	ppm

CAPACITANCE

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{I/O}$	Input/output capacitance	V_{Out} = 0 V			7	pF
C_I	Input capacitance	V = 0 V			5	

AC TEST CONDITIONS, INPUT PULSE LEVELS V_I = 0 V to 3.0 V, t_R = t_F = 5 NS, VREF = 1.5 V

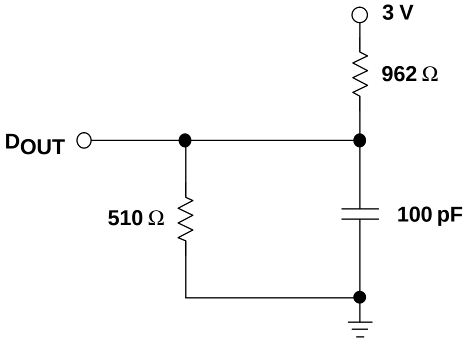


Figure 1. Output Load A

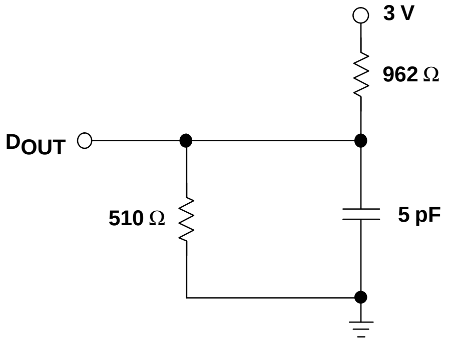


Figure 2. Output Load B

OPERATING CHARACTERISTICS

READ CYCLE (T_A = T_{OPR}, V_{CC} = 5 V)

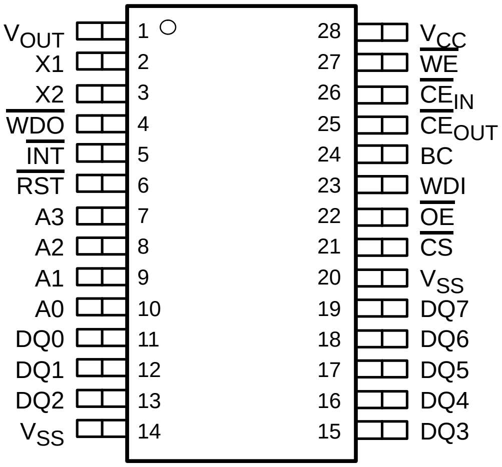
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{RC}	Read cycle time		200		ns
t_{AA}	Address access time	Output load A		100	ns
t_{ACS}	Chip select access time	Output load A		100	ns
t_{OE}	Output enable to output valid	Output load A		100	ns
t_{CLZ}	Chip select to output low Z	Output load B	8		ns
t_{OLZ}	Output enable until output low Z	Output load B	0		ns
t_{CHZ}	Output enable until output high Z	Output load B	0	45	ns
t_{OHZ}	Output disable until output high Z	Output load B	0	45	ns
t_{OH}	Output hold from address change	Output load A	10		ns

READ CYCLE (T_A = T_{OPR}, V_{CC} = 3.3 V)

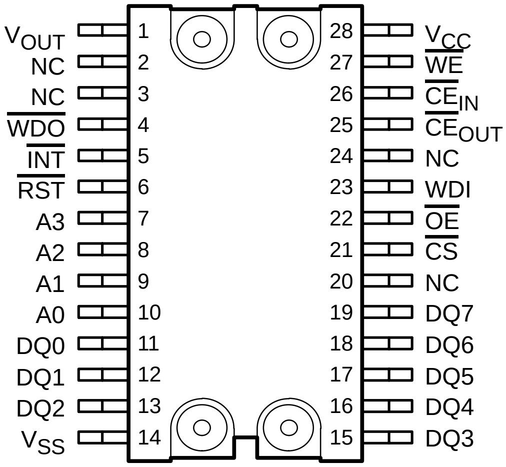
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{RC}	Read cycle time		300		ns
t_{AA}	Address access time	Output load A		150	ns
t_{ACS}	Chip select access time	Output load A		150	ns
t_{OE}	Output enable to output valid	Output load A		150	ns
t_{CLZ}	Chip select to output low Z	Output load B	15		ns
t_{OHL}	Output enable until output low Z	Output load B	0		ns
t_{CLH}	Output enable until output high Z	Output load B	0	60	ns
t_{OLZ}	Output disable until output high Z	Output load B	0	60	ns
t_{OH}	Output hold from address change	Output load A	18		ns

PIN ASSIGNMENTS

DW OR PW PACKAGE
(TOP VIEW)



DSH PACKAGE
(TOP VIEW)



NC – No internal connection

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
A0	10		A0 – A3 allow access to the 16 bytes of real-time clock and control registers.
A1	9		
A2	8		
A3	7		
BC	24(1)		BC should be connected to a 3-V backup cell. A voltage within the V_{BC} range on the BC pin should be present upon power up to provide proper oscillator start-up. Not accessible in module packages.
$\overline{CE}_{IN}$	26		Input to the chip-enable gating circuit
$\overline{CE}_{OUT}$	25		$\overline{CE}_{OUT}$ goes low only when $\overline{CE}_{IN}$ is low and V_{CC} is above the power fail threshold. If $\overline{CE}_{IN}$ is low, and power fail occurs, $\overline{CE}_{OUT}$ stays low for 100 µs or until $\overline{CE}_{IN}$ goes high, whichever occurs first.
$\overline{CS}$	21	I	Chip-select input
DQ0	11	I	DQ0–DQ7 provide x8 data for real-time clock information. These pins connect to the memory data bus.
DQ1	12	I	
DQ2	13	I	
DQ3	15	I	
DQ4	16	I	
DQ5	17	I	
DQ6	18	I	
DQ7	19	I	
$\overline{INT}$	5		$\overline{INT}$ goes low when a power fail, periodic, or alarm condition occurs. $\overline{INT}$ is an open-drain output.
$\overline{OE}$	22		$\overline{OE}$ provides the read control for the RTC memory locations.
$\overline{RST}$	6		$\overline{RST}$ goes low whenever V_{CC} falls below the power fail threshold. $\overline{RST}$ remains low for 200 ms (typical) after V_{CC} crosses the threshold on power-up. The bq4802Y/bq4802LY also enters the reset cycle when $\overline{RST}$ is released from being pulled low for more than 1 µs.
V_{CC}	28	I	5-V or 3.3-V input
V_{OUT}	1	O	V_{OUT} provides the higher of V_{CC} or V_{BC}, switched internally, to supply external RAM.
V_{SS}	14		Ground
	20(1)		

(1) This pin should be left unconnected (NC) when using the SNAPHAT (DSH) package.

Terminal Functions (Continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
WDI	23	I	WDI is a three-level input. If WDI remains either high or low for longer than the watchdog time-out period (1.5-s default), WDO goes low. WDO remains low until the next transition at WDI. Leaving WDI unconnected disables the watchdog function. WDI connects to an internal voltage divider between V_{OUT} and V_{SS}, which sets it to mid-supply when left unconnected.
$\overline{\text{WDO}}$	4		$\overline{\text{WDO}}$ goes low if WDI remains either high or low longer than the watchdog time-out period. $\overline{\text{WDO}}$ returns high on the next transition at WDI. WDO remains high if WDI is unconnected.
$\overline{\text{WE}}$	27		$\overline{\text{WE}}$ provides the write control for the RTC memory locations.
X1	2(1)		Crystal connection
X2	3(1)		

FUNCTIONAL BLOCK DIAGRAM

Figure 3 is a block diagram of the bq4802Y/bq4802LY. The following sections describe the bq4802Y/bq4802LY functional operation including clock interface, data-retention modes, power-on reset timing, watchdog timer activation, and interrupt generation.

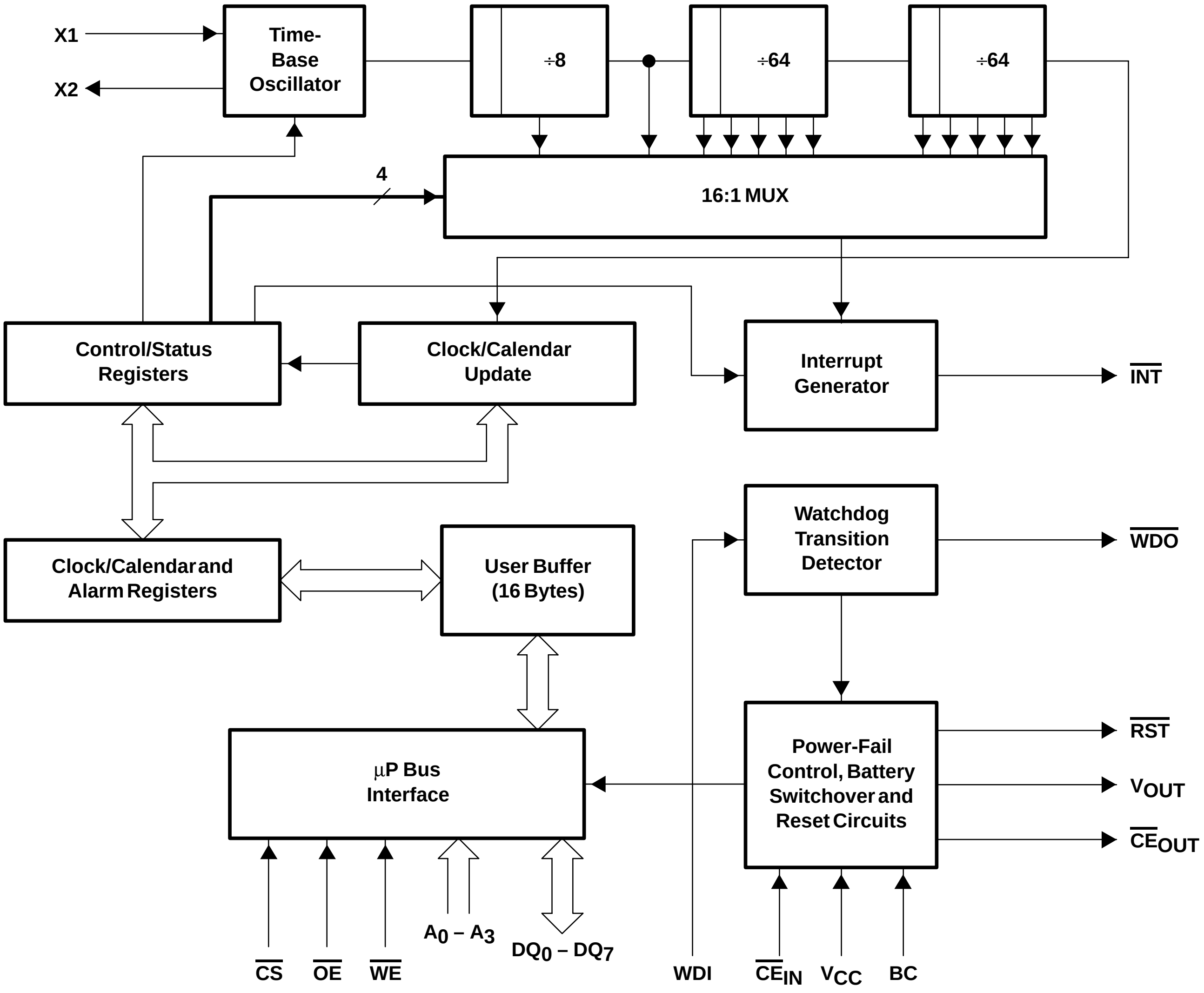
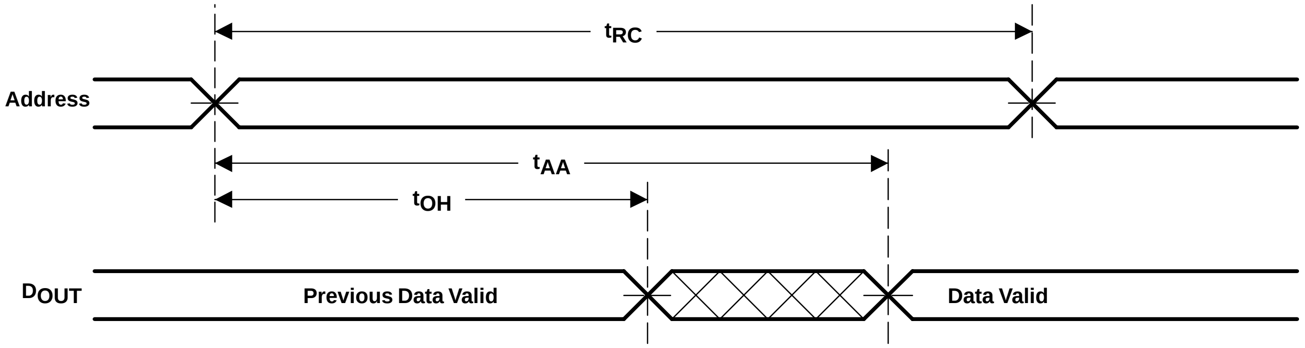


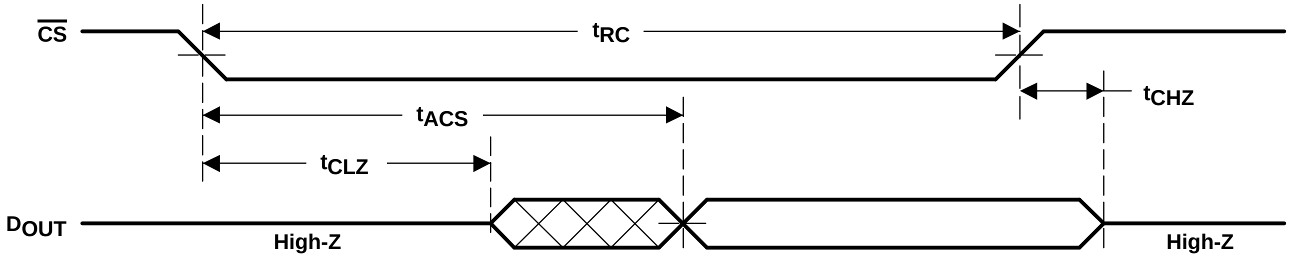
Figure 3. Block Diagram

READ CYCLE TIMING DIAGRAMS



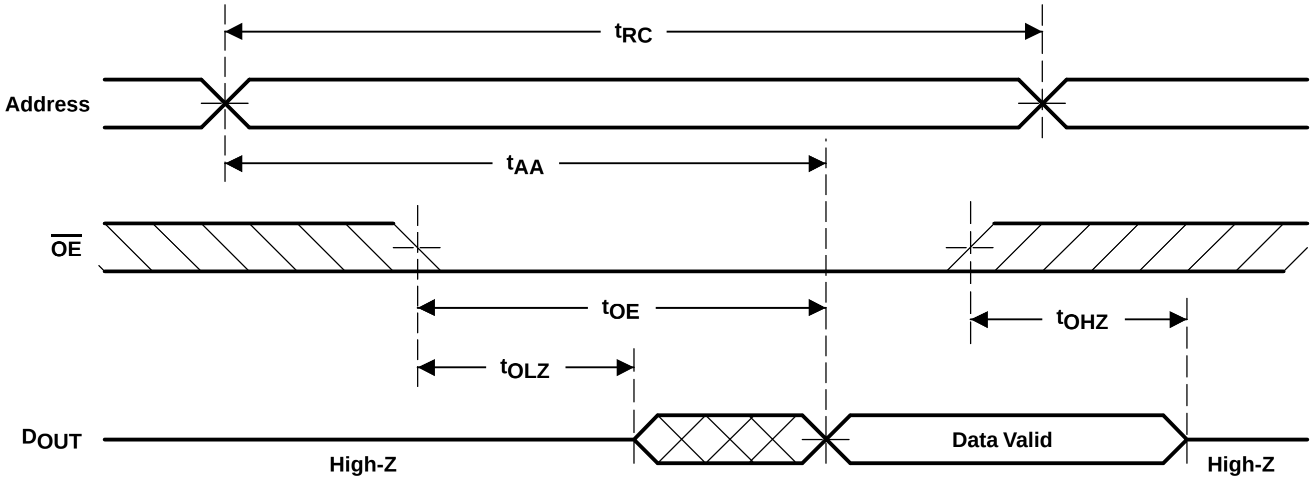
NOTES: A. $\overline{\text{WE}}$ is held high for a read cycle.
B. Device is continuously selected: $\overline{\text{CS}}$ = $\overline{\text{OE}}$ = V_{IL}.

Figure 4. Read Cycle No. 1 – Address Access



NOTES: A. $\overline{\text{WE}}$ is held high for a read cycle.
B. Device is continuously selected: $\overline{\text{CS}}$ = $\overline{\text{OE}}$ = V_{IL}.
C. $\overline{\text{OE}}$ = V_{IL}.

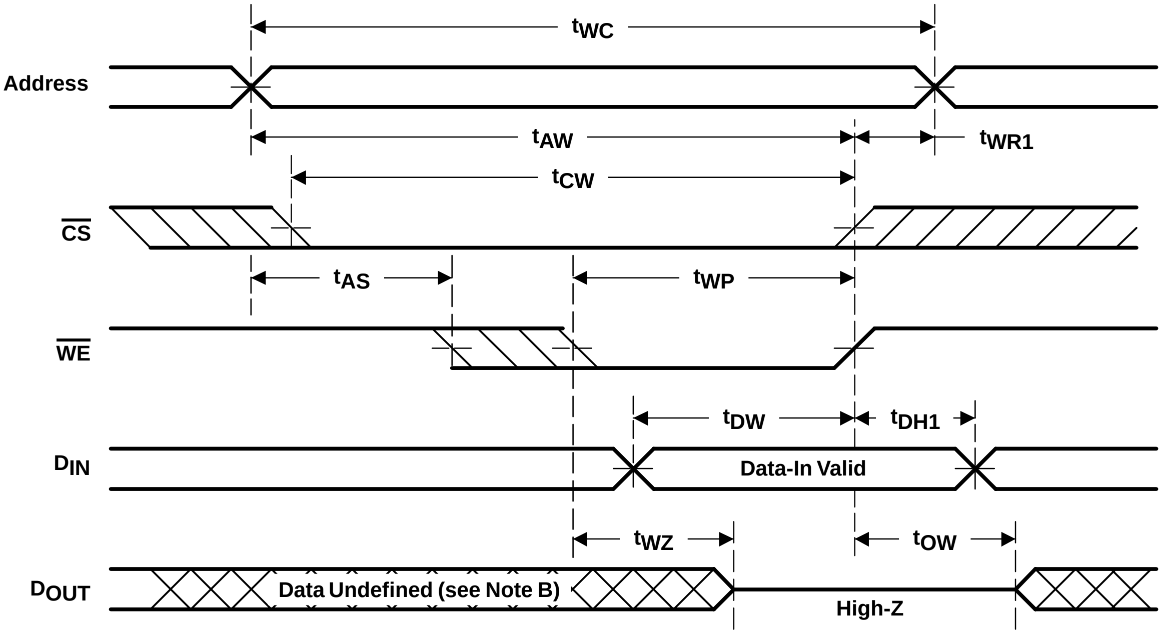
Figure 5. Read Cycle No. 2 – $\overline{\text{CS}}$ Access



NOTES: A. $\overline{\text{WE}}$ is held high for a read cycle.
B. $\overline{\text{CS}}$ = V_{IL}.

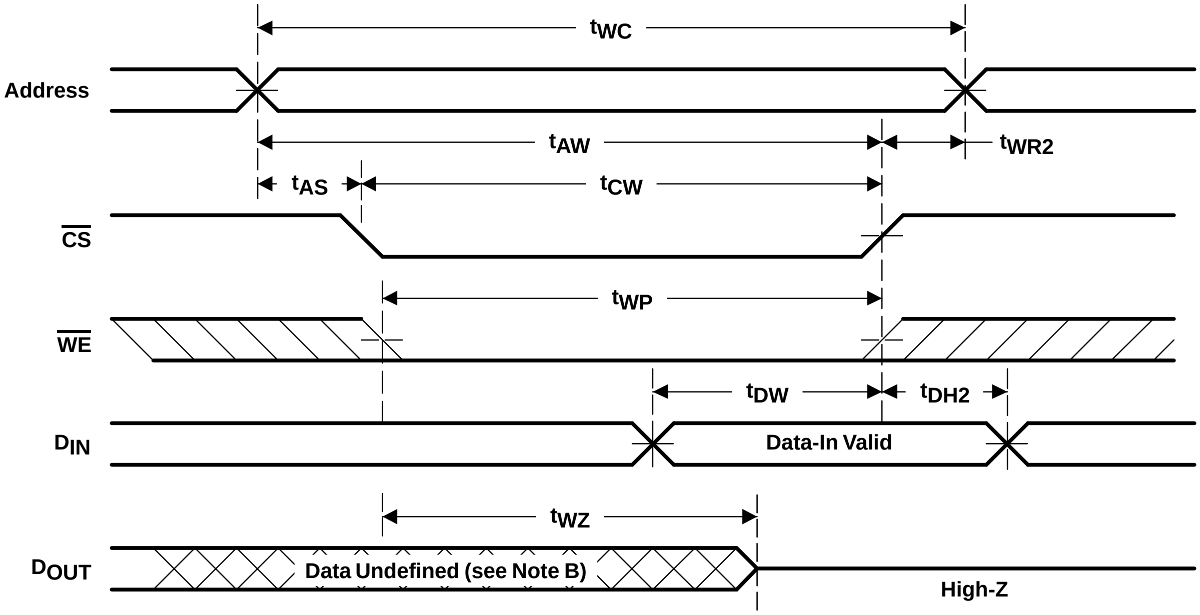
Figure 6. Read Cycle No. 3 – $\overline{\text{OE}}$ Access

WRITE CYCLE TIMING DIAGRAMS



NOTES:
- A. $\overline{\text{WE}}$ or $\overline{\text{CS}}$ must be held high during address transition.
- B. Because I/O may be active ($\overline{\text{OE}}$ low) during the period, data input signals of opposite polarity to the outputs must be applied.
- C. If $\overline{\text{OE}}$ is high, the I/O pins remain in a state of high impedance.

Figure 7. Write Cycle No. 1 – $\overline{\text{WE}}$ Controlled



NOTES:
- A. $\overline{\text{WE}}$ or $\overline{\text{CS}}$ must be held high during address transition.
- B. Because I/O may be active ($\overline{\text{OE}}$ low) during the period, data input signals of opposite polarity to the outputs must be applied.
- C. If $\overline{\text{OE}}$ is high, the I/O pins remain in a state of high impedance.
- D. Either t_{WR1} or t_{WR2} must be met.
- E. Either t_{DH1} or t_{DH2} must be met.

Figure 8. Write Cycle No. 2 – $\overline{\text{CS}}$ Controlled

WRITE CYCLE ($T_A = T_{OPR}$, V_{CC} = 5 V)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{WC}	Write cycle time		200		ns
t_{CW}	Chip select to end of write	See Note 1	195		ns
t_{AW}	Address valid to end of write	See Note 1	195		ns
t_{AS}	Address setup time	Measured from address valid to beginning of write(2)	30		ns
t_{WP}	Write pulse width	Measured from beginning of write to end of write(1)	165		ns
t_{WR1}	Write recovery time (write cycle 1)	Measured from $\overline{WE}$ going high to end of write cycle(3)	5		ns
t_{WR2}	Write recovery time (write cycle 2)	Measured from $\overline{CS}$ going high to end of write cycle(3)	15		ns
t_{DW}	Data valid to end of write	Measured to first low-to-high transition of either $\overline{CS}$ or $\overline{WE}$	50		ns
t_{DH1}	Data hold time (write cycle 1)	Measured from $\overline{WE}$ going high to end of write cycle(4)	0		ns
t_{DH2}	Data hold time (write cycle 2)	Measured from $\overline{CS}$ going high to end of write cycle(4)	10		ns
t_{WZ}	Write enable to output high Z	I/O pins are in output state.(5)	0	45	ns
t_{OW}	Output active from end of write	I/O pins are in output state.(5)	0		ns

(1) A write cycle ends at the earlier transition of $\overline{CS}$ going high and $\overline{WE}$ going high.
(2) A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write cycle begins at the later transition of $\overline{CS}$ going low or $\overline{WE}$ going low.
(3) Either t_{WR1} or t_{WR2} must be met.
(4) Either t_{DH1} or t_{DH2} must be met.
(5) If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high Z state.

WRITE CYCLE ($T_A = T_{OPR}$, V_{CC} = 3.3 V)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{WC}	Write cycle time		300		ns
t_{CW}	Chip select to end of write	See Note 1	250		ns
t_{AW}	Address valid to end of write	See Note 1	250		ns
t_{AS}	Address setup time	Measured from address valid to beginning of write(2)	56		ns
t_{WP}	Write pulse width	Measured from beginning of write to end of write(1)	280		ns
t_{WR1}	Write recovery time (write cycle 1)	Measured from $\overline{WE}$ going high to end of write cycle(3)	8		ns
t_{WR2}	Write recovery time (write cycle 2)	Measured from $\overline{CS}$ going high to end of write cycle(3)	25		ns
t_{DW}	Data valid to end of write	Measured to first low-to-high transition of either $\overline{CS}$ or $\overline{WE}$	80		ns
t_{DH1}	Data hold time (write cycle 1)	Measured from $\overline{WE}$ going high to end of write cycle(4)	0		ns
t_{DH2}	Data hold time (write cycle 2)	Measured from $\overline{CS}$ going high to end of write cycle(4)	15		ns
t_{WZ}	Write enable to output high Z	I/O pins are in output state.(5)	0	60	ns
t_{OW}	Output active from end of write	I/O pins are in output state.(5)	0		ns

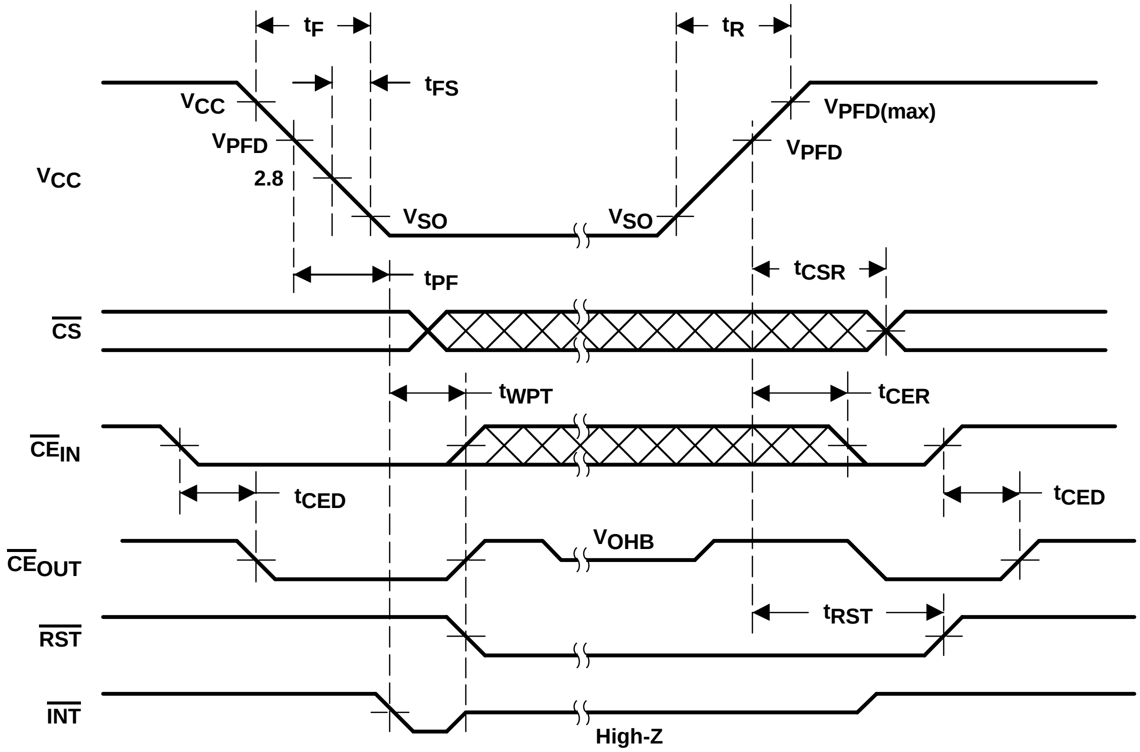
(1) A write cycle ends at the earlier transition of $\overline{CS}$ going high and $\overline{WE}$ going high.
(2) A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write cycle begins at the later transition of $\overline{CS}$ going low or $\overline{WE}$ going low.
(3) Either t_{WR1} or t_{WR2} must be met.
(4) Either t_{DH1} or t_{DH2} must be met.
(5) If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high Z state.

POWER-DOWN/POWER-UP TIMING ($T_A = T_{OPR}$)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_F	V_{CC} slew rate fall time		3.0 V to 0 V	300			µs
t_R	V_{CC} slew rate rise time		V_{SO} to $V_{PDF(max)}$	100			
t_{PF}	Interrupt delay time from V_{PFD}	bq4802Y		6		24	
		bq4802LY		10		40	
t_{WPT}	Write-protect time for external SRAM	bq4802Y	See Note 1	90	100	125	
		bq4802LY	See Note 1	150	170	210	
t_{CSR}	$\overline{CS}$ at V_{HI} after power-up	bq4802Y	See Note 2	100	200	300	ms
		bq4802LY	See Note 2	170	330	500	
t_{RST}	V_{PFD} to $\overline{RST}$ active (reset active time-out period)			t_{CSR}		t_{CSR}	
t_{CER}	Device enable recovery time		See Note 3	t_{CSR}		t_{CSR}	
t_{CED}	Device enable propagation delay time to external SRAM	bq4802Y	Output load A		9	15	ns
		bq4802LY			15	25	
t_{PBL}	Push-button low time			1			µs

(1) Delay after V_{CC} slews down past V_{PFD} before SRAM is write protected and $\overline{RST}$ activated.
(2) Internal write-protection period after V_{CC} passes V_{PFD} on power up.
(3) Time during which external SRAM is write protected after V_{CC} passes V_{PFD} on power up.

CAUTION:NEGATIVE UNDERSHOOTS BELOW THE ABSOLUTE MAXIMUM RATING OF –0.3 V IN BATTERY-BACKUP MODE MAY AFFECT DATA INTEGRITY.



NOTES: A. PWRIE set to 1 to enable power fail interrupt.
B. $\overline{RST}$ and $\overline{INT}$ are open drain and require and external pullup resistor.

Figure 9. Power-Down/Power-Up Timing Diagram

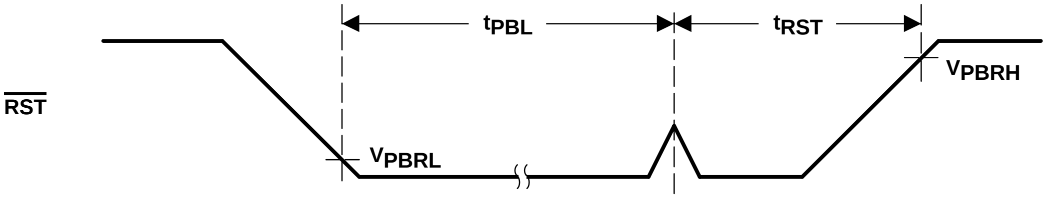


Figure 10. Push-Button Reset Timing

FUNCTIONAL DESCRIPTION

The following sections describe the bq4802Y/bq4802LY functional operation including clock interface, data-retention modes, power-on reset timing, watchdog timer activation, and interrupt generation.

Table 1. Operational Truth Table

V_{CC}	$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{CE}}_{OUT}$	V_{OUT}	MODE	DQ	POWER
$< V_{CC(MAX)}$	V_{IH}	X	X	$\overline{\text{CE}}_{IN}$	V_{OUT1}	Deselect	High Z	Standby
	V_{IL}	X	V_{IL}	$\overline{\text{CE}}_{IN}$	V_{OUT1}	Write	D_{IN}	Active
$> V_{CC(MIN)}$	V_{IL}	V_{IL}	V_{IH}	$\overline{\text{CE}}_{IN}$	V_{OUT1}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	$\overline{\text{CE}}_{IN}$	V_{OUT1}	Read	High-Z	Active
$<V_{PFD(MIN}>V_{SO}$	X	X	X	V_{OH}	V_{OUT1}	Deselect	High-Z	CMOS standby
$\leq V_{SO}$	X	X	X	V_{OHB}	V_{OUT2}	Deselect	High-Z	Battery-backup mode

ADDRESS MAP

The bq4802Y/bq4802LY provides 16 bytes of clock and control status registers. Table 1 is a map of the bq4802Y/bq4802LY registers, and Table 2 describes the register bits.

Table 2. Clock and Control Register Map

Addr (h)	D7	D6	D5	D4	D3	D2	D1	D0	Range (h)	Register
0	0	10-second digit			1-second digit				00–59	Seconds
1	ALM1	ALM0			1-second digit				00–59	Seconds alarm
		10-second digit								
2	0	10-minute digit			1-minute digit				00–59	Minutes
3	ALM1	ALM0			1-minute digit				00–59	Minutes alarm
		10-minute digit								
4	PM/AM	0	10-hour digit		1-hour digit				01–12AM 81–92PM	Hours
5	ALM1	ALM0	10-hour digit		1-hour digit				01–12AM 81–92PM	Hours alarm
	PM/AM									
6	0	0	10-day digit		1-day digit				01–31	Day
7	ALM1	ALM0	10-day digit		1-day digit				01–31	Day alarm
8	0	0	0	0	0	day of week digit			01–07	Day of Week
9	0	0	0	10 mo.	1-month digit				01–12	Month
A	10-year digit				1-year digit				00–99	Year
B	(1)	WD2	WD1	WD0	RS3	RS2	RS1	RS0	–	Rates
C	(1)	(1)	(1)	(1)	AIE	PIE	PWRIE	ABE	–	Enables
D	(1)	(1)	(1)	(1)	AF	PF	PWRF	BVF	–	Flags
E	(1)	(1)	(1)	(1)	UTI	$\overline{\text{STOP}}$	24/12	DSE	–	Control
F	10-century digit				1-century digit				00–99	Century

(1) Unused bits; cannot be written to and read as 0.
(2) Internal write-protection period after V_{CC} passes V_{PFD} on power up.
(3) Clock calendar data in BCD. Automatic leap year adjustment up to year 2100.
(4) PM/AM = 1 for PM and 0 for AM.
(5) DSE = 1 to enable daylight savings adjustment.
(6) 24/12 = 1 to enable 24–hour data representation and 0 for 12–hour data representation.
(7) Day of week coded as Sunday = 1 through Saturday = 7
(8) $\overline{\text{BVF}}$ = 1 for valid BC input
(9) $\overline{\text{STOP}}$ = 1 to turn the RTC on and 0 stops the RTC in battery-backup mode

Table 3. Clock and Control Register Map

BIT	DESCRIPTION
24/12	24- or 12-hour data representation
ABE	Alarm interrupt enable in battery-backup mode
AF	Alarm interrupt flag
AIE	Alarm interrupt enable
ALM0–ALM1	Alarm mask bits
BVF	Battery-valid flag
DSE	Daylight savings enable
PF	Periodic interrupt flag
PIE	Periodic interrupt enable
PM/AM	PM or AM indication
PWRF	Power-fail interrupt flag
PWRIE	Power-fail interrupt enable
RS0–RS3	Periodic interrupt rate
$\overline{\text{STOP}}$	Oscillator stop and start
UTI	Update transfer inhibit
WD0–WD2	Watchdog time-out rate

CLOCK MEMORY INTERFACE

The bq4802Y/bq4802LY has the same interface for clock/calendar and control information as standard SRAM. To read and write to these locations, the user must put the bq4802Y/bq4802LY in the proper mode and meet the timing requirements.

READ MODE

The bq4802Y/bq4802LY is in read mode whenever $\overline{\text{OE}}$ (output enable) is low and $\overline{\text{CS}}$ (chip select) is low. The unique address, specified by the four address inputs, defines which one of the 16 clock/calendar bytes is to be accessed. The bq4802Y/bq4802LY makes valid data available at the data I/O pins within t_{AA} (address access time). This occurs after the last address input signal is stable, and providing the $\overline{\text{CS}}$ and $\overline{\text{OE}}$ (output enable) access times are met. If the $\overline{\text{CS}}$ and $\overline{\text{OE}}$ access times are not met, valid data is available after the latter of chip select access time (t_{ACS}) or output enable access time (t_{OE}).

$\overline{\text{CS}}$ and $\overline{\text{OE}}$ control the state of the eight three-state data I/O signals. If the outputs are activated before t_{AA}, the data lines are driven to an indeterminate state until t_{AA}. If the address inputs are changed while $\overline{\text{CS}}$ and $\overline{\text{OE}}$ remain low, output data remains valid for t_{OH} (output data hold time), but goes indeterminate until the next address access.

WRITE MODE

The bq4802Y/bq4802LY is in write mode whenever $\overline{\text{WE}}$ and $\overline{\text{CS}}$ are active. The start of a write is referenced from the latter-occurring falling edge of $\overline{\text{WE}}$ or $\overline{\text{CS}}$. A write is terminated by the earlier rising edge of $\overline{\text{WE}}$ or $\overline{\text{CS}}$. The addresses must be held valid throughout the cycle. $\overline{\text{CS}}$ or $\overline{\text{WE}}$ must return high for a minimum of t_{WR2} from $\overline{\text{CS}}$ or t_{WR1} from $\overline{\text{WE}}$ prior to the initiation of another read or write cycle.

Data-in must be valid t_{DW} prior to the end of write and remain valid for t_{DH1} or t_{DH2} afterward. $\overline{\text{OE}}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{\text{CS}}$ and $\overline{\text{OE}}$, a low on $\overline{\text{WE}}$ disables the outputs t_{WZ} after $\overline{\text{WE}}$ falls.

READING THE CLOCK

Once every second, the user-accessible clock/calendar locations are updated simultaneously from the internal real-time counters. To prevent reading data in transition, updates to the bq4802Y/bq4802LY clock registers should be halted. Updating is halted by setting the update transfer inhibit (UTI) bit D3 of the control register E. As long as the UTI bit is 1, updates to user-accessible clock locations are inhibited. Once the frozen clock information is retrieved by reading the appropriate clock memory locations, the UTI bit should be reset to 0 in order to allow updates to occur from the internal counters. Because the internal counters are not halted by setting the UTI bit, reading the clock locations has no effect on clock accuracy. Once the UTI bit is reset to 0, the internal registers update within one second the user-accessible registers with the correct time. A halt command issued during a clock update allows the update to occur before freezing the data.

SETTING THE CLOCK

The UTI bit must also be used to set the bq4802Y/bq4802LY clock. Once set, the locations can be written with the desired information in BCD format. Resetting the UTI bit to 0 causes the written values to be transferred to the internal clock counters and allows updates to the user-accessible registers to resume within one second.

STOPPING AND STARTING THE CLOCK OSCILLATOR

The bq4802Y/bq4802LY clock can be programmed to turn off when the part goes into battery back-up mode by setting $\overline{\text{STOP}}$ to 0 prior to power down. If the board using the bq4802Y/bq4802LY is to spend a significant period of time in storage, the $\overline{\text{STOP}}$ bit can be used to preserve some battery capacity. $\overline{\text{STOP}}$ set to 1 keeps the clock running when V_{CC} drops below V_{SO}. With V_{CC} greater than V_{SO}, the bq4802Y/bq4802LY clock runs regardless of the state of $\overline{\text{STOP}}$.

POWER-DOWN/POWER-UP CYCLE

The bq4802Y/bq4802LY continuously monitors V_{CC} for out-of-tolerance. During a power failure, when V_{CC} falls below V_{PFD}, the bq4802Y/bq4802LY write-protects the clock and storage registers. The power source is switched to BC when V_{CC} is less than V_{PFD} and BC is greater than V_{PFD}, or when V_{CC} is less than V_{BC} and V_{BC} is less than

V_{PFD}. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{PFD}, the power source is V_{CC}. Write-protection continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

An external CMOS static RAM is battery-backed using the V_{OUT} and chip enable output pins from the bq4802Y/bq4802LY. As the voltage input V_{CC} slews down during a power failure, the chip enable output, $\overline{CE}_{OUT}$, is forced inactive independent of the chip enable input $\overline{CE}_{IN}$.

This activity unconditionally write-protects the external SRAM as V_{CC} falls below V_{PFD}. If a memory access is in progress to the external SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT}, the chip enable output is unconditionally driven high, write-protecting the controlled SRAM.

As the supply continues to fall past V_{PFD}, an internal switching device forces V_{OUT} to the external backup energy source. $\overline{CE}_{OUT}$ is held high by the V_{OUT} energy source.

During power up, V_{OUT} is switched back to the main supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. If $V_{PFD} < V_{BC}$ on the bq4802Y/bq4802LY the switch to the main supply occurs at V_{PFD}. $_{CEOUT}$ is held inactive for time t_{CER} (200-ms maximum) after the power supply has reached V_{PFD}, independent of the $\overline{CE}_{IN}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{CE}_{IN}$ input is passed through to the $\overline{CE}_{OUT}$ output with a propagation delay of less than 12 ns. Figure 2 shows the hardware hookup for the external RAM, battery, and crystal.

A primary backup energy source input is provided on the bq4802Y/bq4802LY. The BC input accepts a 3-V primary battery, typically some type of lithium chemistry. Since the bq4802Y/bq4802LY provides for reverse battery charging protection, no diode or current limiting resistor is needed in series with the cell. To prevent battery drain when there is no valid data to retain, V_{OUT} and $\overline{CE}_{OUT}$ are internally isolated from BC by the initial connection of a battery. Following the first application of V_{CC} above V_{PFD}, this isolation is broken, and the backup cell provides power to V_{OUT} and $\overline{CE}_{OUT}$ for the external SRAM. The crystal should be located as close to X1 and X2 as possible and meet the specifications in the *crystal specifications* section of the electrical characteristics tables. With the specified crystal, the bq4802Y/bq4802LY RTC is accurate to within one minute per month at room temperature. In the absence of a crystal, a 32.768-kHz waveform can be fed into X1 with X2 grounded. The power source and crystal are integrated into the SNAPHAT modules.

Power-On Reset

The bq4802Y/bq4802LY provides a power-on reset, which pulls the RST pin low on power down and remains low on power up for t_{RST} after V_{CC} passes V_{PFD}. With valid battery voltage on BC, RST remains valid for $V_{CC} = V_{SS}$.

Push-Button Reset

The bq4802Y/bq4802LY also provides a push-button override to the reset when the device is not already in a reset cycle. When the RST pin is released after being pulled low for 1 µs then the RST stays low for 200 ms (typical).

WATCHDOG TIMER

The watchdog monitors microprocessor activity through the watchdog input (WDI). To use the watchdog function, connect WDI to a bus line or a microprocessor I/O line. If WDI remains high or low for longer than the watchdog time-out period (1.5 seconds default), the bq4802Y/bq4802LY asserts WDO and RST.

Watchdog Input

The bq4802Y/bq4802LY resets the watchdog timer if a change of state (high-to-low, low-to-high, or a minimum 100 ns pulse) occurs at the watchdog input (WDI) during the watchdog period. The watchdog time-out is set by WD0 – WD2 in register B. The bq4802Y/bq4802LY maintains the watchdog time-out programming through power cycles. The default state (no valid battery power) of WD0 – WD2 is 000 or 1.5 s on power up. Table 3 shows the programmable watchdog time-out rates. The watchdog time-out period immediately after a reset is equal to the programmed watchdog time-out.

To disable the watchdog function, leave WDI floating. An internal resistor network (100-kΩ equivalent impedance at WDI) biases WDI to approximately 1.6 V. Internal comparators detect this level and disable the watchdog timer. When V_{CC} is below the power-fail threshold, the bq4802Y/bq4802LY disables the watchdog function and disconnects WDI from its internal resistor network, thus making it high impedance.

Watchdog Output

The watchdog output ($\overline{WDO}$) remains high if there is a transition or pulse at WDI during the watchdog timeout period. The bq4802Y/bq4802LY disables the watchdog function and $\overline{WDO}$ is a logic high when V_{CC} is below the power fail threshold, battery-backup mode is enabled, or WDI is an open circuit. In watchdog mode, if no transition occurs at WDI during the watchdog time-out period, the bq4802Y/bq4802LY asserts $\overline{RST}$ for the reset time-out period t1. WDO goes low and remains low until the next transition at WDI. If WDI is held high or low indefinitely, $\overline{RST}$ generates pulses (t1 seconds wide) every t3 seconds. Figure 11 shows the watchdog timing.

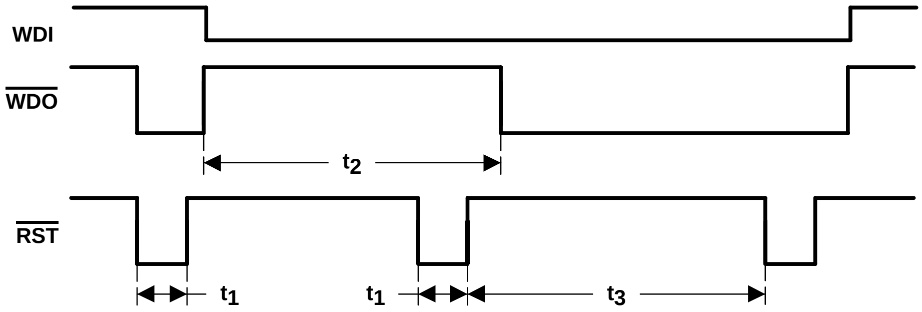


Figure 11. Watchdog Time-Out Period and Reset Active Time

Table 4. Watchdog and Reset Timeout Rates

WD2	WD1	WD0	WATCHDOG TIMEOUT PERIOD	RESET TIMEOUT PERIOD
0	0	0	1.50 s	0.25 ms
0	0	1	23.4375 ms	3.9063 ms
0	1	0	46.875 ms	7.8125 ms
0	1	1	93.750 ms	15.625 ms
1	0	0	187.5 ms	31.25 ms
1	0	1	375 ms	62.5 ms
1	1	0	750 ms	125 ms
1	1	1	3.0 s	0.5 s

INTERRUPTS

The bq4802Y/bq4802LY allows three individually selected interrupt events to generate an interrupt request on the $\overline{\text{INT}}$ pin. These three interrupt events are:

- The periodic interrupt, programmable to occur once every 30.5 µs to 500 ms.
- The alarm interrupt, programmable to occur once per second to once per month.
- The power-fail interrupt, which can be enabled to be asserted when the bq4802Y/bq4802LY detects a power failure.

An individual interrupt-enable bit in register C, the interrupts register, enables the periodic, alarm and power-fail interrupts. When an event occurs, its event flag bit in the flags register, register D, is set. If the corresponding event enable bit is also set, then an interrupt request is generated. Reading the flags register clears all flag bits and makes $\overline{\text{INT}}$ high impedance. To reset the flag register, the bq4802Y/bq4802LY addresses must be held stable at register D for at least 50 ns to avoid inadvertent resets.

Periodic Interrupt

Bits RS3 – RS0 in the interrupt register program the rate for the periodic interrupt. The user can interpret the interrupt in two ways, either by polling the flags register for PF assertion or by setting PIE so that $\overline{\text{INT}}$ goes active when the bq4802Y/bq4802LY sets the periodic flag. Reading the flags register resets the PF bit and returns $\overline{\text{INT}}$ to the high-impedance state. Table 5 shows the periodic rates.

Table 5. Periodic Interrupt Rates

REGISTER BITS				PERIODIC INTERRUPT PERIOD
RS3	RS2	RS1	RS0	
0	0	0	0	NONE
0	0	0	1	30.5175 µs
0	0	1	0	61.035 µs
0	0	1	1	122.070 µs
0	1	0	0	244.141 µs
0	1	0	1	488.281 µs
0	1	1	0	976.5625 µs
0	1	1	1	1.95315 ms
1	0	0	0	3.90625 ms
1	0	0	1	7.8125 ms
1	0	1	0	15.625 ms
1	0	1	1	31.25 ms
1	1	0	0	62.5 ms
1	1	0	1	125 ms
1	1	1	0	250 ms
1	1	1	1	500 ms

ALARM INTERRUPT

Registers 1, 3, 5, and 7 program the real-time clock alarm. During each update cycle, the bq4802Y/bq4802LY compares the date, hours, minutes, and seconds in the clock registers with the corresponding alarm registers. If a match between all the corresponding bytes is found, the alarm flag AF in the flags register is set. If the alarm interrupt is enabled with AIE, an interrupt request is generated on $\overline{\text{INT}}$. The alarm condition is cleared by a read to the flags register. ALM1 – ALM0 in the alarm registers, mask each alarm compare byte. Setting ALM1 (D7) and ALM0 (D6) to 1 masks an alarm byte. Alarm byte masking can be used to select the frequency of the alarm interrupt, according to Table 6. The alarm interrupt can be made active while the bq4802Y/bq4802LY is in the battery-backup mode by setting ABE in the interrupts register. Normally, the $\overline{\text{INT}}$ pin goes high-impedance during battery backup. With ABE set, $\overline{\text{INT}}$ is driven low if an alarm condition occurs and the AIE bit is set.

Table 6. Alarm Frequency

1h	3h	5h	7h	ALARM FREQUENCY
ALM1–ALM0	ALM1–ALM0	ALM1–ALM0	ALM1–ALM0	
1	1	1	1	Once per second
0	1	1	1	Once per minute when seconds match
0	0	1	1	Once per hour, when minutes and seconds match
0	0	0	1	Once per day, when hours, minutes and seconds match
0	0	0	0	When date, hours minutes and seconds match

POWER–FAIL INTERRUPT

When V_{CC} falls to the power-fail-detect point, the power-fail flag PWRF is set. If the power-fail interrupt enable bit (PWRIE) is also set, then $\overline{\text{INT}}$ is asserted low. The power-fail interrupt occurs t_{WPT} before the bq4802Y/bq4802LY generates a reset and deselects.

BATTERY–LOW WARNING

The bq4802Y/bq4802LY checks the battery on power-up. When the battery voltage is approximately 2.1 V, the battery valid flag BVF in the flags register is set to a 0 indicating that clock and RAM data may be invalid.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ4802LYDW	ACTIVE	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4802LYDW	Samples
BQ4802LYDWR	ACTIVE	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4802LYDW	Samples
BQ4802LYDWRG4	ACTIVE	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4802LYDW	Samples
BQ4802LYPW	ACTIVE	TSSOP	PW	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4802LYPW	Samples
BQ4802LYPWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4802LYPW	Samples
BQ4802YDW	ACTIVE	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4802YDW	Samples
BQ4802YDWR	ACTIVE	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4802YDW	Samples
BQ4802YPW	ACTIVE	TSSOP	PW	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4802YPW	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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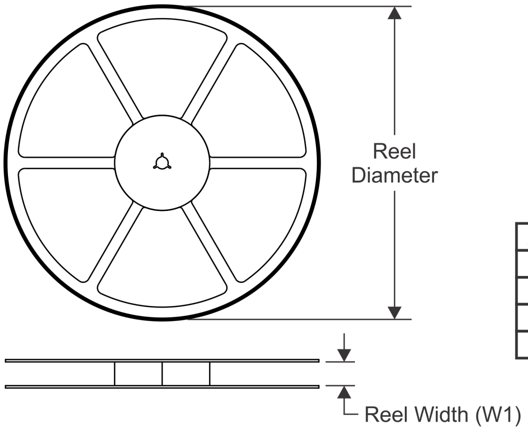
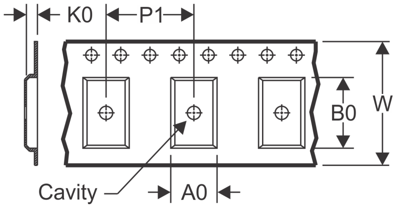
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

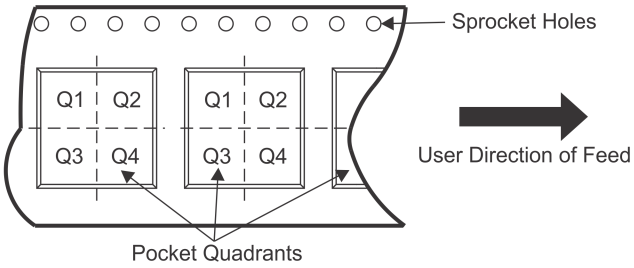


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

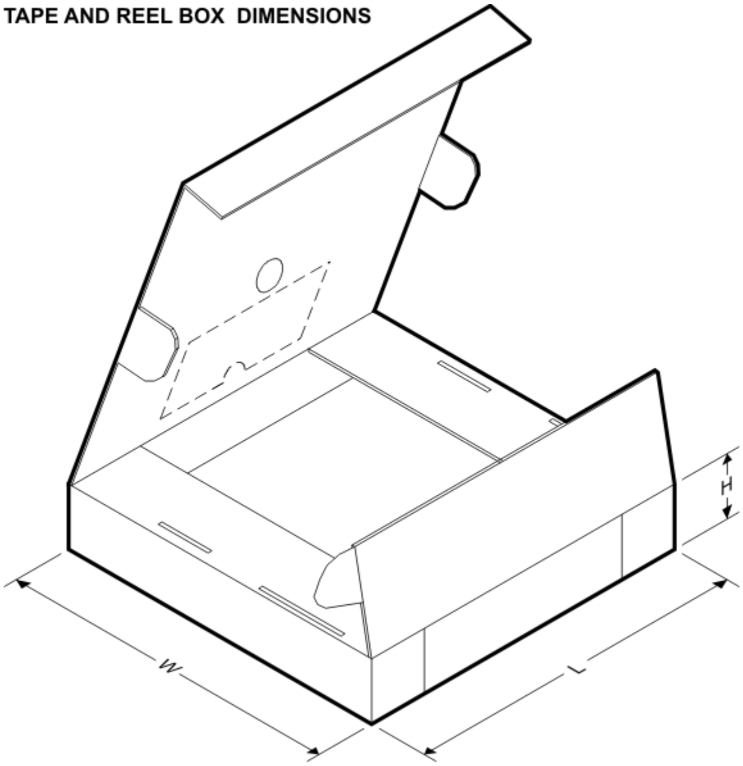
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ4802LYDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
BQ4802LYPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
BQ4802YDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

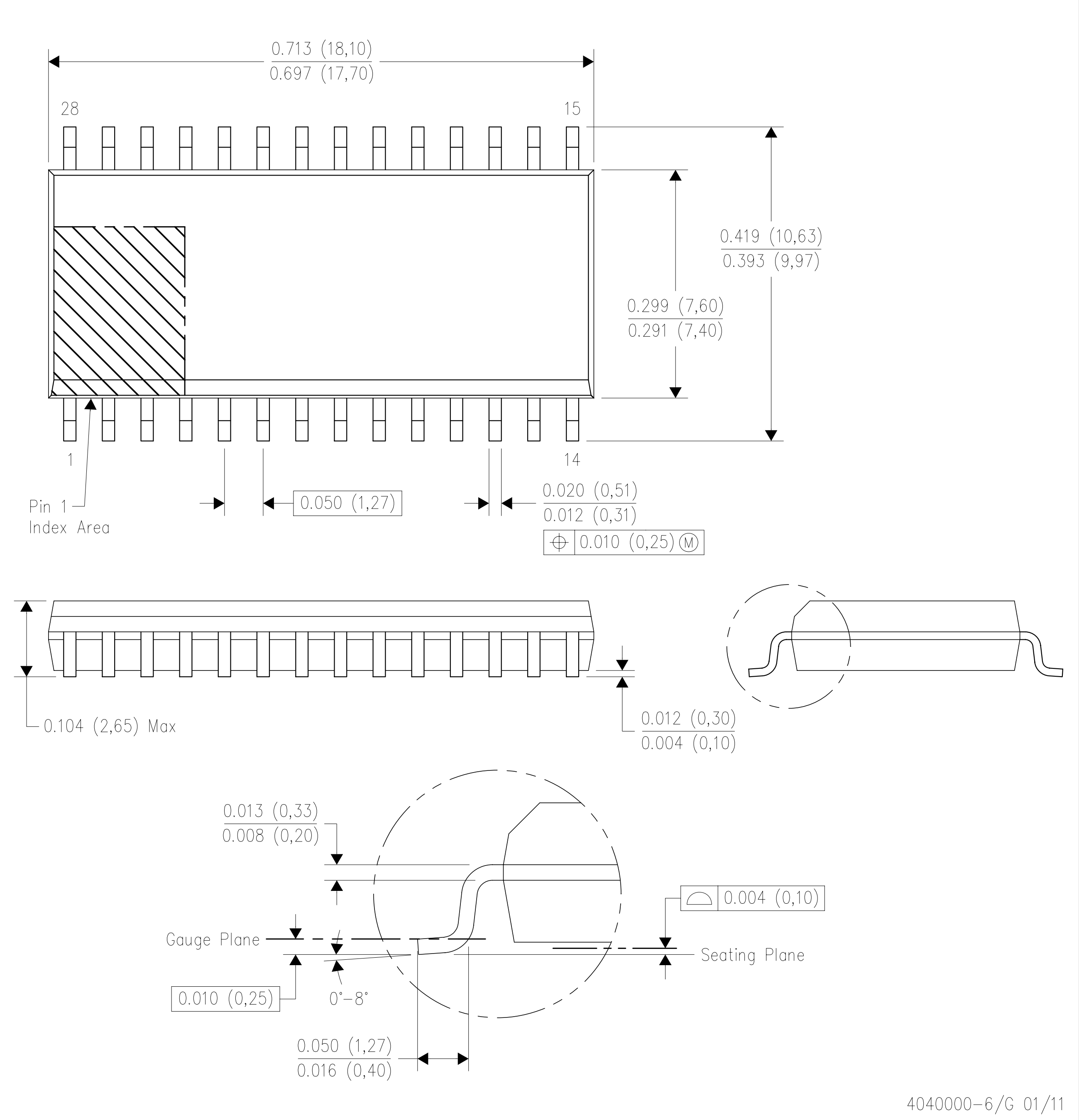
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

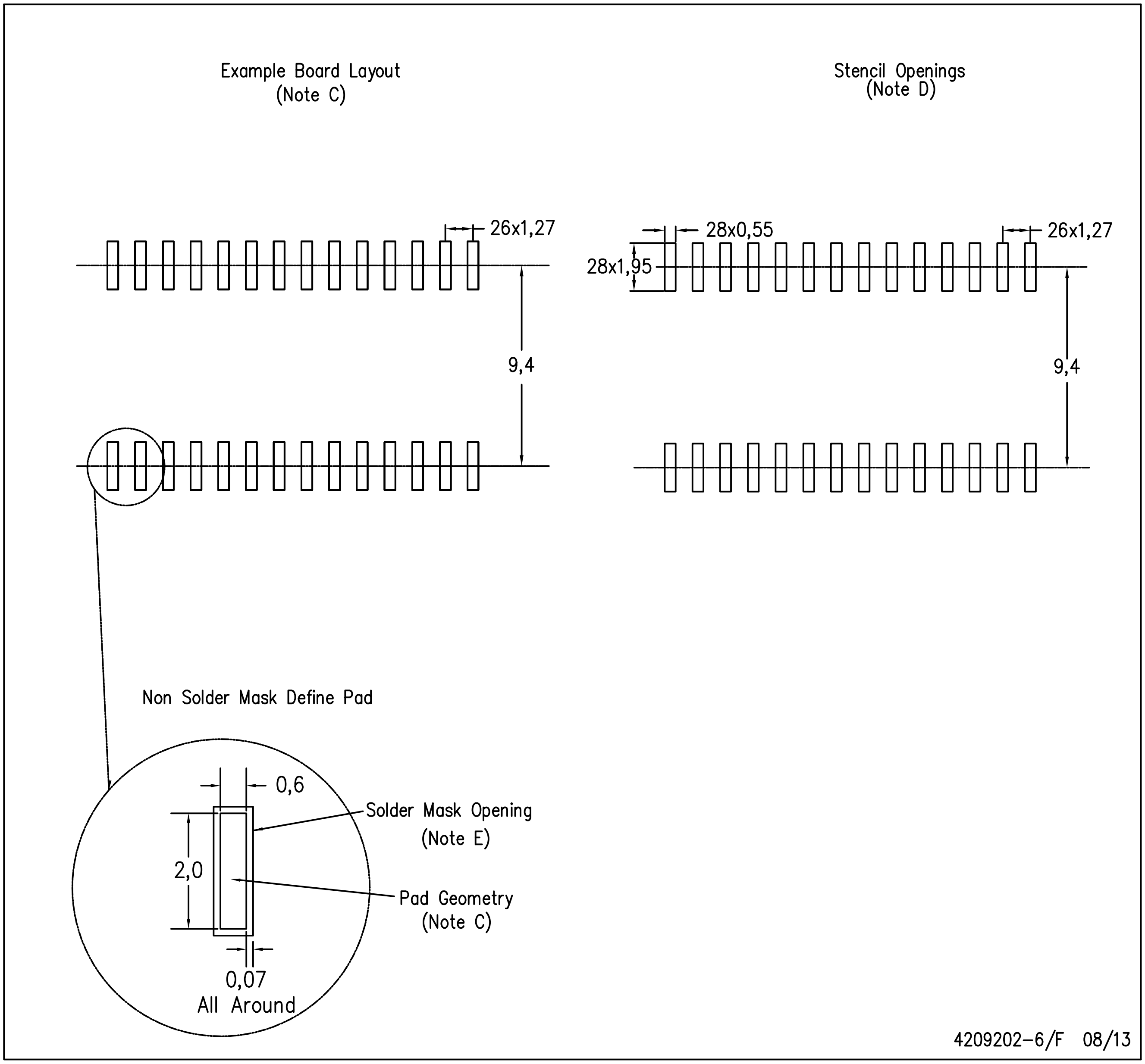
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ4802LYDWR	SOIC	DW	28	1000	367.0	367.0	55.0
BQ4802LYPWR	TSSOP	PW	28	2000	853.0	449.0	35.0
BQ4802YDWR	SOIC	DW	28	1000	367.0	367.0	55.0

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



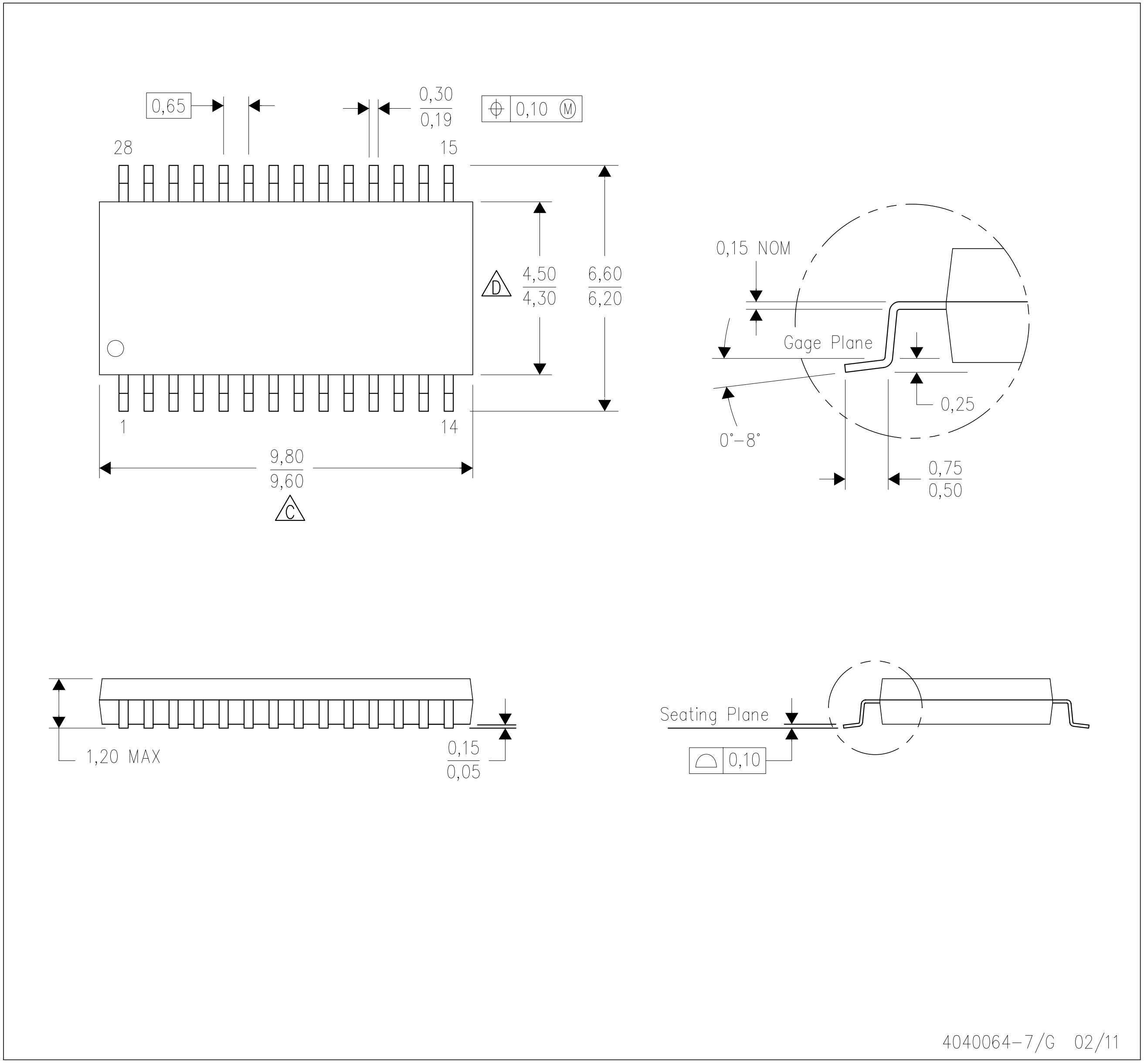
NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AE.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



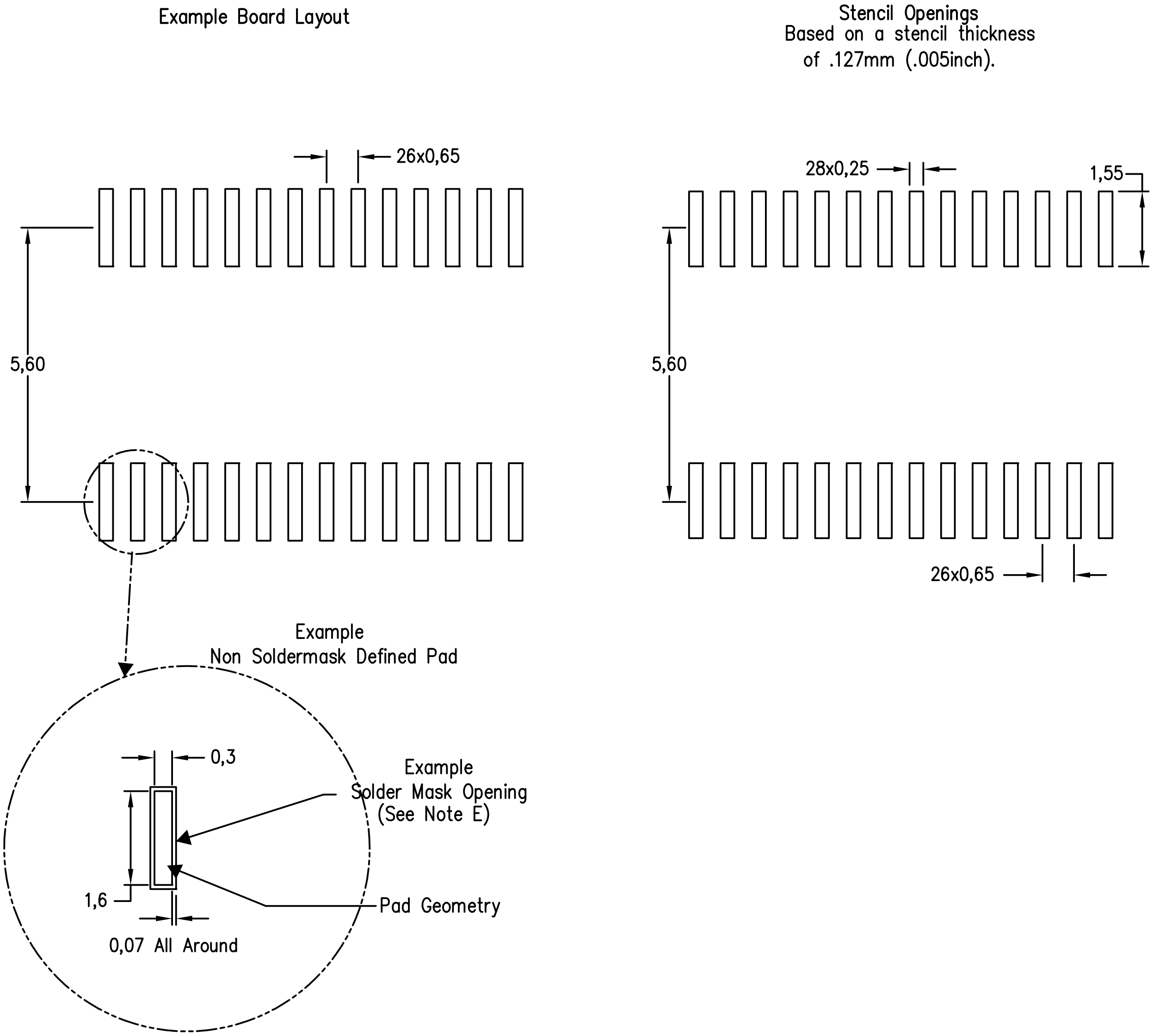
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R-PDSO-G28) PLASTIC SMALL OUTLINE



4211284-6/G 08/15

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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