Lattice CertusPro-NX FPGA and ADI's Secure Ethernet Connectivity based development kit

Product Brief

Document History

Version	Author		Description of Changes
	Name	Date	
1.0	eInfochips	31st Mar '26	Internal review changes.

License Agreement

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Pre-requisites

Anti-Static Handling Procedure

This device has exposed PCB and chips. Accordingly, proper anti-static precautions should be employed when handling the SoM, including:

- Use a grounded anti-static mat.
- Use a grounded wrist or foot strap.

Motor Control Board based on Lattice CertusPro-NX with ADI PHYs!

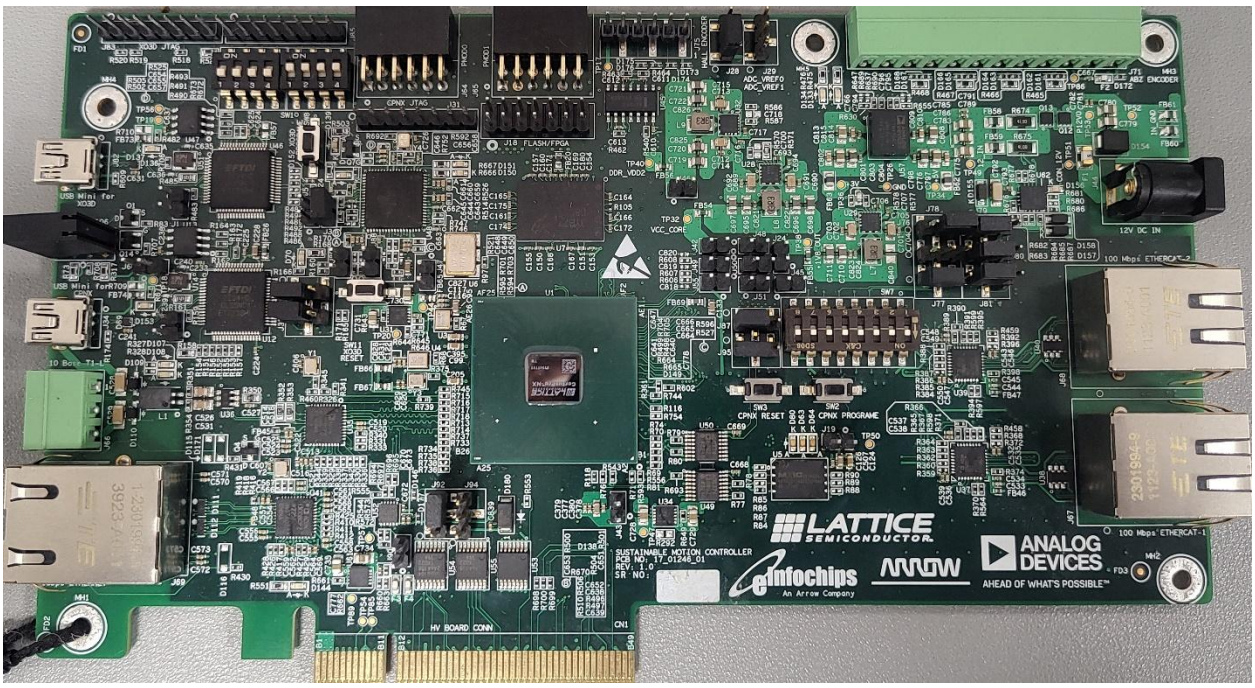

Figure 1 Motion Control Board

Kit Contents:

- Motion Control Board based on Lattice CertusPro-NX with ADI PHYs.
- 12V DC/2A Adapter.
- USB Cable for Programming via PC (USB-A to Mini-B).
- Copy of Quick Start Guide.

Product Information:

The Lattice CertusPro-NX FPGA based development kit is designed to enable motion-control use cases, support rapid prototyping, and facilitate testing of systems with an integrated RISC-V processor and peripheral IPs.

- The **Motion Control Board based on Lattice CertusPro-NX with ADI PHYs** features the CertusPro-NX FPGA in the LFG672 package which is built on Lattice Nexus™ FPGA platform using low power 28 nm FD-SOI technology and ADI's Secure Ethernet Connectivity. The board has the ability to expand the usability of the CertusPro-NX FPGA with 1xABZ Encoder, 1xHALL Encoder, 1xPCI connector, 2xPMOD connectors, ADI PHYs such as 1xADIN1100 over RGMII, 2xADIN1200 over MII, 1xADIN1300 over RGMII interface. Easy-to-use board resources of the jumper, LED indicator, push button and switch are available for user-defined applications.
- Embedded system solutions play an important role in FPGA system design, allowing you to develop software for a processor in an FPGA device. It provides the flexibility for you to control various peripherals from a system bus.
- To develop an embedded system on an FPGA, you need to design the System-on-Chip (SoC) with an embedded processor and develop system software on the processor. Lattice Propel helps you develop your system with a RISC-V processor, peripheral IP, and a set of tools.
- The features of the Motion Control Board can assist engineers with the rapid prototyping and testing of their specific designs.
- One of the Motion control board controls and monitoring the Motor in closed loop with ethernet commands.

Features:

- CertusPro-NX FPGA (LFCPNX-100-9LFG672I)
- Root port configuration
- 2×RJ45 100 Mbps EtherCAT (ADIN1200 PHY)
- 1×RJ45 1Gbps RGMII (ADIN1300 PHY)
- 1×10 Base T1-L 10Mbps (ADIN1100 PHY)
- LPDDR4 DRAM Memory
- On-board Boot Flash – 128 Mb Serial Peripheral Interface (SPI) Flash, with Quad read feature
- USB-B connection for CPNX device programming and Inter-Integrated Circuit Bus (I2C) utility
- USB-B connection for MACHXO3D device programming and Inter-Integrated Circuit Bus (I2C) utility
- 2 x PMOD Connector
- 4 input DIP switches for CPNX & 4 input DIP switches for MACHXO3D, 4 push buttons, 2 status LEDs for CPNX & 2 status LEDs for MACHXO3D.
- MAXQ1065 Cryptographic controller
- Lattice Radiant® software programming support.
- Multiple reference clock sources
- ADI Compatible HV Board.
- ABZ (part no: 1803374) and HALL (part no: TSM-106-02-T-SV) Encoder.
- Motor Control Driver IC Compatible.

Product Details:

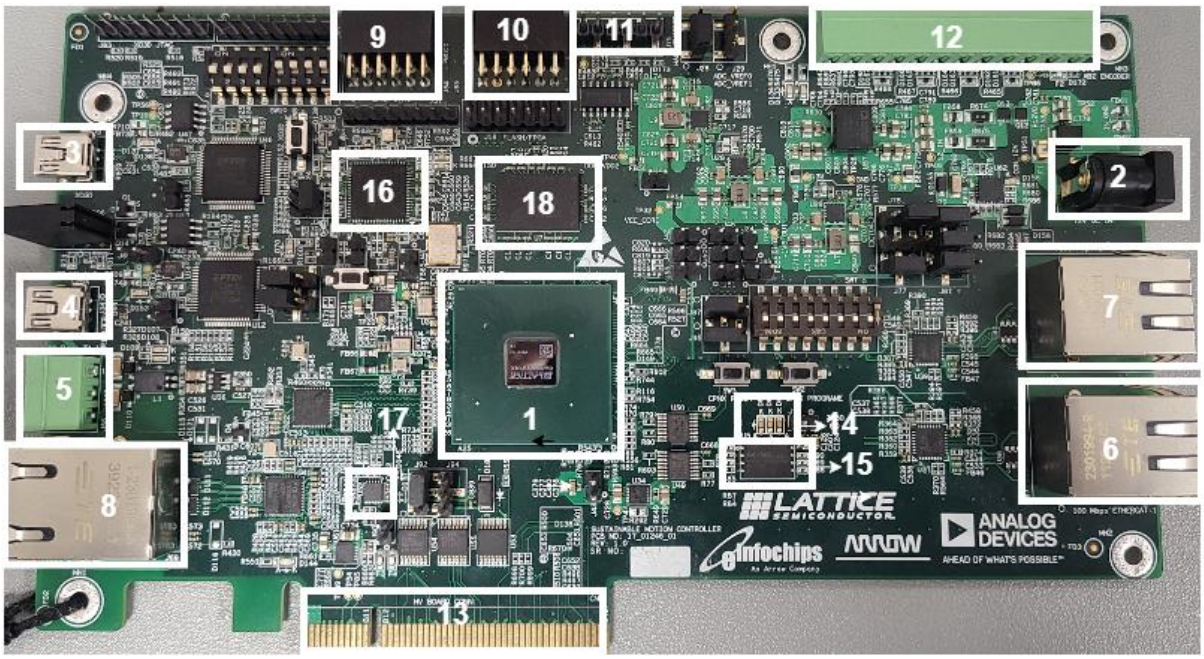

Figure 2 Detailed View of MCB

Sr. No.	Components
1	Lattice CertusPro-NX FPGA
2	12V DC/2A Power Adapter jack
3	Mini-USB port for MachXO3D
4	Mini-USB port for CertusPro-NX
5	10BaseTL port for ADIN1100
6	RJ45 Ethernet port for ADIN1200_1
7	RJ45 Ethernet port for ADIN1200_2

8	RJ45 Ethernet port for ADIN1300
9	PMOD0
10	PMOD1
11	HALL Encoder connector
12	ABZY Encoder connector
13	PCIe Connector for HV Board
14	Debug LEDs
15	Winbond QSPI
16	Lattice MachXO3D FPGA
17	MAXQ1065
18	LPDDR4

Table 1 Components Details

LED Representation of Motion Control Board based on
Lattice CertusPro-NX with ADI PHYs:

REFDES	LED Name	Colour	LED Status	Function
D63	Debug LED	Green	On	Debug LED0 for Certus-Pro
D64	Debug LED	Green	On	Debug LED1 for Certus-Pro
D70	Status LED	Green	On	Status LED for FTDI chip of Certus-pro
D80	Initialize LED	Green	On	Certus-pro initialization state
D106-1	DONE LED	Green	On	Certus-pro configuration completed
D106-2	Power LED	Green	On	12V to 5V Power Supply is healthy
D106-3	Status LED	Green	On	Status LED for Certus-Pro
D133	Status LED	Green	On	ABZ Encoder Functionality
D134	Status LED	Green	On	ABZ Encoder Functionality
D136	Power LED	Green	On	Power in from USB 2.0 Mini for MachXO3D FTDI
D138	Initialize LED	Green	On	MACHXO3D initialization state
D139	Power LED	Green	On	MACHXO3D configuration completed
D144	Power LED	Green	On	HV board Power is healthy
D145	Power LED	Green	On	5V to 1V_VCC_CORE Power Supply is healthy
D147	Power LED	Green	On	5V to 1.8V Power Supply is healthy
D148	Power LED	Green	On	5V to 1.1V Power Supply is healthy
D150	Debug LED	Green	On	Debug LED0 for MACHXO3D
D151	Debug LED	Green	On	Debug LED1 for MACHXO3D
D153	Power LED	Green	On	Power in from USB 2.0 Mini for Certus-Pro FTDI
D156	Fault LED	Yellow	On	Fault at MAX16141AAAF/VY+

Table 2 various LEDs of Motion Control Board

Detailed Specifications:

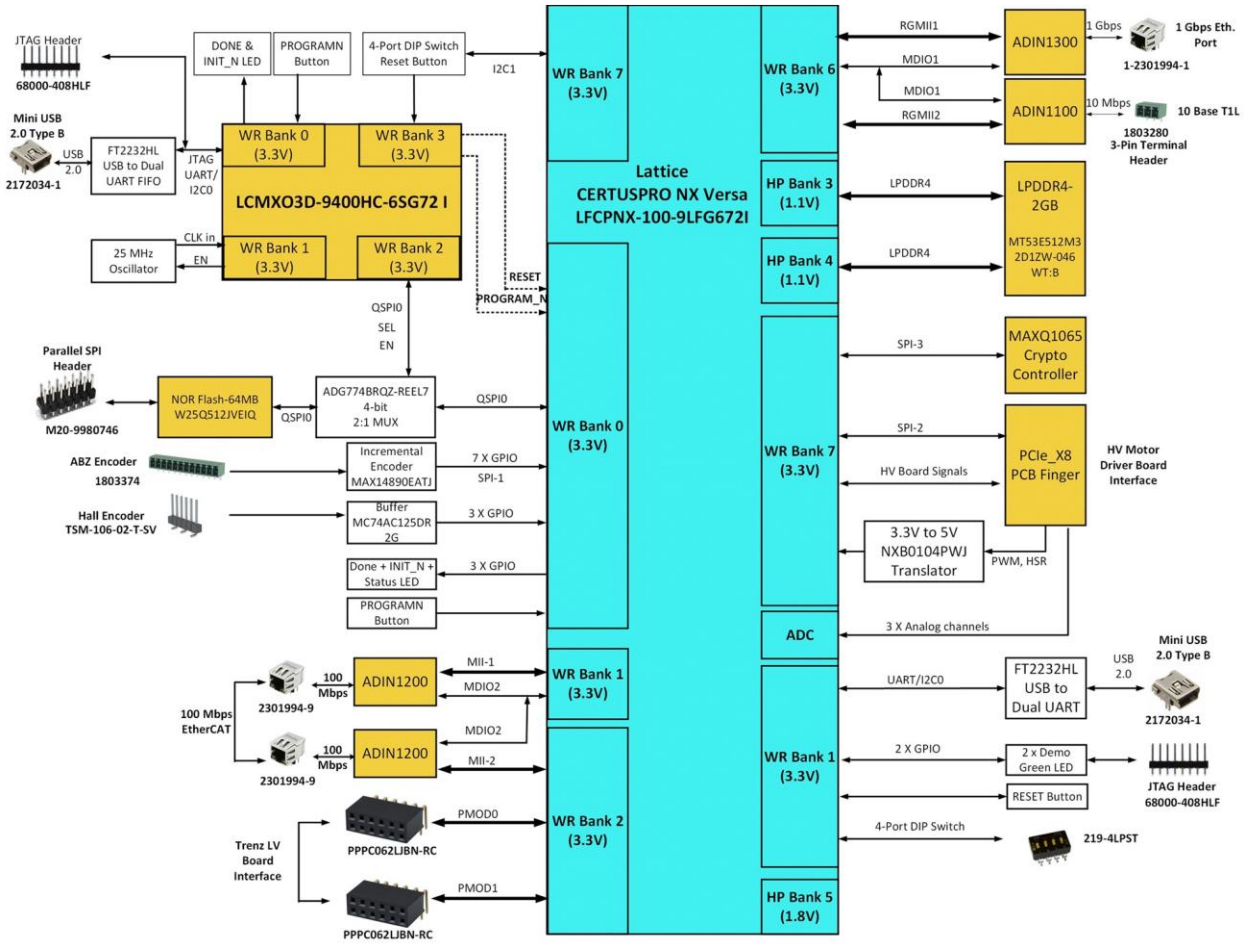

Figure 3 Block Diagram of Motion Control Board

The block diagram illustrates the design of the **Motion Control Board based on Lattice CertusPro-NX with ADI PHYs**. The diagram provides an understanding of the various components on the board and their connections. For application-specific developments, the Hardware packages, Firmware packages and FPGA packages are all available on GitHub.

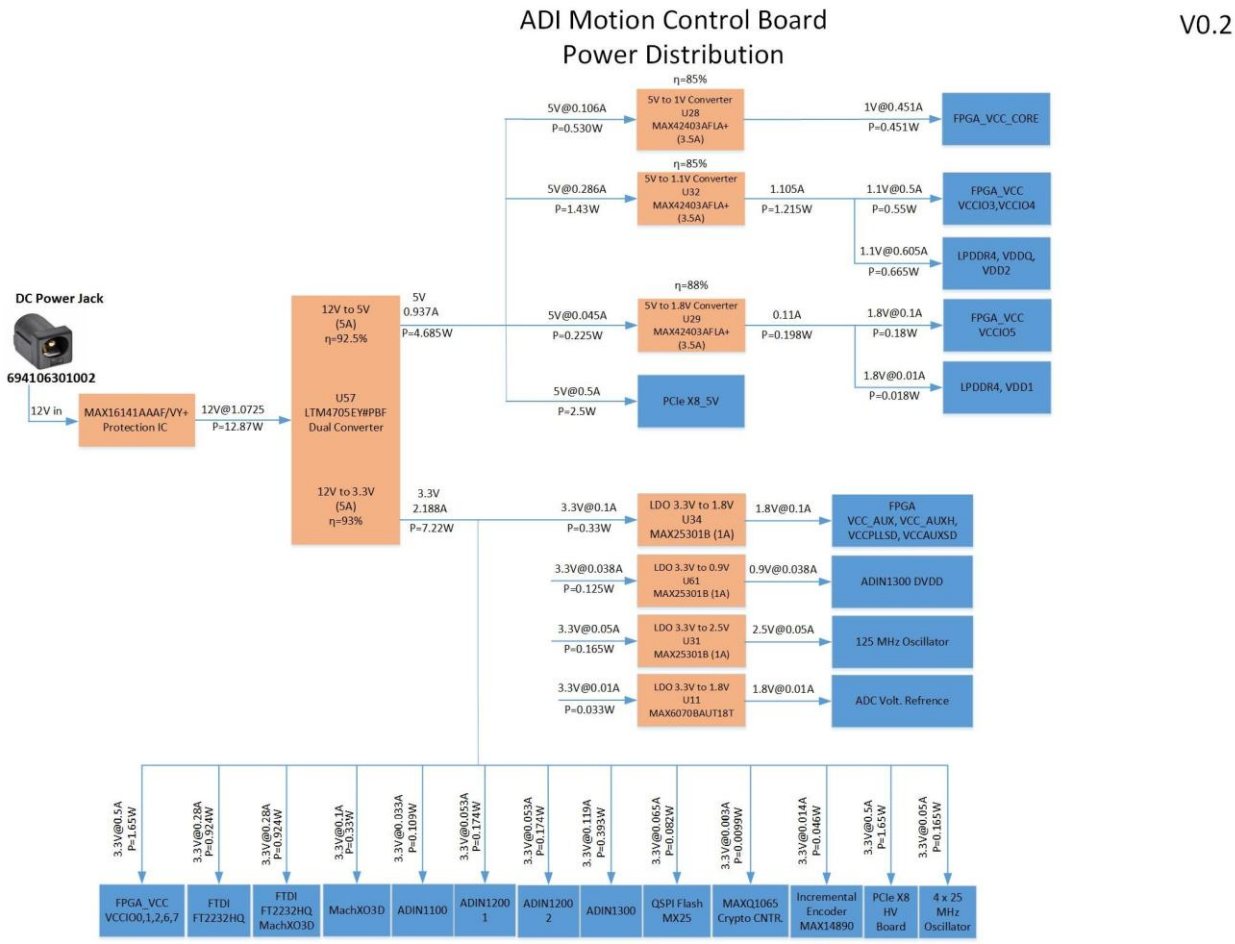

Figure 4 Power Connection of Motion Control Board

The diagram provides an understanding of the signal and power chain for the **Motion Control Board based on Lattice CertusPro-NX with ADI PHYs**.

Featured Products:

CertusPro-NX FPGA (LFCPNX-100-9LFG672I)

- Up to 100K logic cells, 7.3 Mb of embedded memory blocks (EBR, LRAM), 156 18 x 18 multipliers, 299 programmable I/O, 8 SERDES supporting up to 10.3 Gbps per lane and supporting popular protocols (10 Gig Ethernet, PCIe Gen 3, DisplayPort, SLVS-EC and CoaXPress).
- Packages as small as 9x9 mm, and in ball-pitch options of 0.5, 0.8 and 1.0 mm.
- Power modes – User selectable Low Power vs. High Performance modes, enabled by FD-SOI programmable back-bias.
- Design security – ECDSA bitstream authentication, coupled with robust AES-256 encryption.
- Fast configuration – I/O configures in 4 ms, and full-device in under 30 ms in 100K LC device.
- Available in Commercial, Industrial and Automotive (AEC-Q100 qualified) temperature grades.
- Datasheet

ADIN1100

- ADIN1100 communicates over RGMII interface.

- ADIN1100 is configured over Clause-22/Clause-45 MDIO
- Auto-negotiation mode speed as 10 Mbps, Voltage level as 2.4 V pk-pk and full-duplex mode.
- Due to support of 10BaseTL, long range communication is possible.
- It has PHY address 0x01.
- Datasheet

ADIN1200

- IEEE 802.3 compliant with support for 10BASE-Te/100BASE-TX interfaces.
- ADIN1200 is configured over Clause-22 MDIO.
- ADIN1200 communicates over MII interface.
- Programmable RGMII timing delay and drive current.
- Auto-negotiation mode, speed as 10Mbps/100Mbps and supports half-duplex/full-duplex mode.
- It supports EtherCAT.
- Supports Time-Sensitive Networking (TSN).
- Wide range of EMC test standards compliance, including surge, EFT, ESD, conducted immunity, radiated emissions, and conducted emissions (Class A).
- PHY address of ADIN1200-1 is 0x02 and ADIN1200-2 is 0x03.
- Datasheet

ADIN1300

- IEEE 802.3 compliant with support for 10BASE-Te/100BASE-TX/1000BASE-T interfaces.
- ADIN1300 is configured over Clause-22 MDIO.
- Programmable RGMII timing delay and drive current.
- Auto negotiation support of 10/100/1000Mbps speed.
- ADIN1300 communicates over RGMII interface.
- Supports Time-Sensitive Networking (TSN).
- Wide range of EMC test standards compliance, including surge, EFT, ESD, conducted immunity, radiated emissions, and conducted emissions (Class A).
- It has PHY address 0x04.
- Datasheet

Lattice MachXO3D

- Simplifies implementation of hardware security by integrating Root-of-Trust in your platform's first on, last off device.
- Supports security throughout the product lifecycle including device manufacturing and transport, platform manufacturing, installation, operation, and decommissioning.
- Enables comprehensive protection against a variety of threats by providing data security, equipment security, data authentication, design security and brand protection.
- Programmable logic combined with secure dual boot configuration block provides flexibility during design implementation and enables secure updates after equipment deployment.
- Delivers robust security and pre-verified cryptographic functions compliant with NIST SP 800-193 PFR and CAVP guidelines to protect non-volatile memory, detect malicious code, and recover in case of corruption.
- Datasheet

ADI_MAXQ1065

- Support for various cryptographic algorithms and protocols including ECC Compute Engine using Curve NIST P-256, FIPS-186 ECDSA, NIST SP800-56Ar3 Key Exchange, and SHA-2 Compute Engine.
- Comprehensive AES Compute Engine capabilities with support for key sizes of 128 and 256 bits, along with various cipher modes including ECB, CBC, CCM, and GCM.

- Secure communication features such as TLS/DTLS 1.2 Handshake and Record Layer, ECDSA Authentication, ECDHE Key Exchange, AES-GCM or CCM Record Layer, and X.509 v3 Certificate Support.
- Onboard True Random Number Generator (TRNG) compliant with NIST SP800-90A/C, along with NIST SP800-90B Entropy Source, ensuring strong cryptographic operations and secure key generation.
- Enhanced security features including Tamper Input for detecting system-level intrusion, Secure Factory Provisioning Service, and unique, unalterable Factory-Programmed ID Number, providing robust protection against various attacks, and ensuring device integrity.
- It will verify firmware using Secure Hash Algorithm 256-bit.
- Datasheet

Winbond_QSPI

- W25Q512JV: 512M-bit Flash.
- It Supports Standard SPI: CLK, /CS, DI, DO
  Dual SPI: CLK, /CS, IO_0, IO_1,
  Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
- Highest Performance Serial Flash
- Efficient “Continuous Read”
- Flexible Architecture with 4KB sectors
- Advanced Security Features
- Datasheet

HALL Encoder

- Outputs Source/Sink
- It has TTL Compatible Inputs.
- These are Pb−Free Devices.
- It takes PWM signals as input.
- IC processes the signals and gives the phase angle of the PWM signals.
- Datasheet

ABZ Encoder

- High flexibility with support for all encoder types: RS-422, HTL, TTL, and DI.
- RS-422 switching rates up to 35Mbps, TTL switching rates up to 5MHz, and HTL switching rates up to 400kHz.
- SPI or pin-controlled operation with SPI interface for per-receiver configuration.
- It takes differential signal as input using RS 485 HF.
- IC processes the differential signal and converts it into a single ended signal.
- Datasheet

LPDDR4

- For technical support login to micron_technology website and search for datasheet and other relevant documents.

Design your own Motion Control Board Application:

Why not integrate **Motion Control Board based on Lattice CertusPro-NX with ADI PHYs** to develop your new product or custom prototype?

The **Motion Control Board based on Lattice CertusPro-NX with ADI PHYs** is provided with complete hardware development package to support a quick, simple, and low-risk **Motion Control Board** design. Provided is a proven, tested, and verified reference design which includes.

For Motion Control Board based on Lattice CertusPro-NX with ADI PHYs

- Hardware Package for Development of a device.
- FW Code for Motion Control Board Device.

FPGA Integration:

- Contact Lattice Semiconductor for the IPs for creating a SoC project.

Schematic Capture Integration:
The schematic for Motion Control Board is available in .pdf for review at Schematics. It is also available in OrCAD compatible format and can be copied and pasted directly into your own design assuming the format is compatible.

The Gerber file is available at Gerber Files. The layout can also be copied and pasted into your own design.

Important Points to be kept in mind:

- Using EtherCAT,
  For MII1 R359 & R458 should be DNP
  For MII2 R384 & R459 should be DNP

Software Integration:

There are three PHY drivers to be configured with Lattice CertusPro-NX FPGA (LFCPNX-100-9LFG672I)

1. ADIN1100_Phy_Config.c: The driver implements control to the PHY via MDIO clause-22 and clause-45 and it configures PHY to auto-negotiation, full-duplex mode, and at 10Mbps speed.

- All three drivers are configured over MDIO via TSEMAC layer.
- LwIP stack 2.2.0 is ported, and created application demo code is running on TCP echo server client application. For various other applications refer to LwIP website.

Example firmware for the Motion Control Board is available at FW_Package.

For more information and manuals related to **Motion Control Board based on Lattice CertusPro-NX with ADI PHYs** please refer to GitHub Link given below: Motion Control Board GitHub

7 Ordering Information

Product name	Part number	Description
LSCC-ARW-MCB	LSCC-ARW-MCB	*A Lattice CertusPro-NX FPGA and ADI's Secure Ethernet Connectivity based development kit designed to enable motion-control use cases, support rapid prototyping, and facilitate testing of systems with an integrated RISC-V processor and peripheral IPs.*

About eInfochips

eInfochips, an Arrow company, is a leading global provider of product engineering and semiconductor design services.

Contact Information:

Corporate Headquarters:	**USA Office:**
eInfochips Ltd. Aryan Park complex, Nr. Shilaj railway crossing, Thaltej – 380054 Ahmedabad Tel +91-79-67128700/500 Fax +91-79-26882222	eInfochips, Inc. 2025 Gateway Place, Suite 270 San Jose, CA 95110 USA Tel +1-408-496-1882 Fax +1-801-650-1480
Technical Assistance:	eInfochips support portal (https://supportcenter.einfochips.com)
Sales Support:	sales.support@einfochips.com

Table 3 : Contact Details of EIC.