Document Number: AFT23S170−13S
Rev. 0, 6/2013

RoHS

RF Power LDMOS Transistor

N−Channel Enhancement−Mode Lateral MOSFET

This 45 watt RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 2300 to 2400 MHz.

- Typical Single−Carrier W−CDMA Performance: V_{DD} = 28 Volts, I_{DQ} = 1100 mA, P_{out} = 45 Watts Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

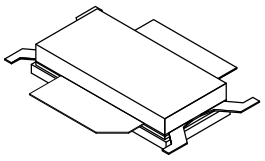
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2300 MHz	18.3	33.8	6.9	−34.4	−13
2350 MHz	18.6	33.8	6.9	−34.3	−16
2400 MHz	18.8	33.9	6.8	−33.9	−13

Features

- Greater Negative Gate−Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications
- In Tape and Reel. R3 Suffix = 250 Units, 44 mm Tape Width, 13−inch Reel.

AFT23S170−13SR3

2300−2400 MHz, 45 W AVG., 28 V



NI−780S−2L4S

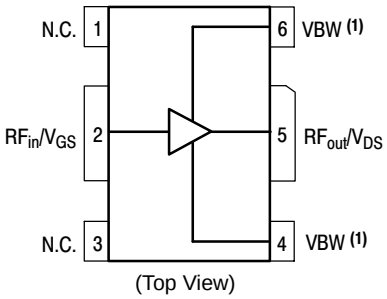


Figure 1. Pin Connections

1. Device can operate with the V_{DD} current supplied through pin 4 and pin 6 at a reduced RF output power level. Refer to CW operation data in the Maximum Ratings table.

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Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain−Source Voltage	V_{DSS}	−0.5, +65	Vdc
Gate−Source Voltage	V_{GS}	−6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Case Operating Temperature Range	T_C	−40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	−40 to +225	°C
CW Operation @ T_C = 25°C when DC current is fed through pin 4 and pin 6 Derate above 25°C	CW	94 0.44	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 78°C, 45 W CW, 28 Vdc, I_{DQ} = 1100 mA, 2350 MHz	$R_{\theta JC}$	0.42	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22−A114)	2
Machine Model (per EIA/JESD22−A115)	B
Charge Device Model (per JESD22−C101)	IV

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate−Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 219 μAdc)	$V_{GS(th)}$	0.9	1.3	1.7	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 1100 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.4	1.8	2.2	Vdc
Drain−Source On−Voltage (V_{GS} = 6 Vdc, I_D = 2.19 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc
Functional Tests (4) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1100 mA, P_{out} = 45 W Avg., f = 2400 MHz, Single−Carrier W−CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	17.5	18.8	20.0	dB
Drain Efficiency	η_D	32.0	33.9	—	%
Output Peak−to−Average Ratio @ 0.01% Probability on CCDF	PAR	6.3	6.8	—	dB
Adjacent Channel Power Ratio	ACPR	—	−33.9	−32.0	dBc
Input Return Loss	IRL	—	−13	−9	dB

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes − AN1955.
4. Part internally matched both on input and output.

(continued)

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Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Load Mismatch (In Freescale Test Fixture, 50 ohm system) I_{DQ} = 1100 mA, f = 2350 MHz					
VSWR 10:1 at 32 Vdc, 230 W CW Output Power (3 dB Input Overdrive from 178 W CW Rated Power)	No Device Degradation				
Typical Performance (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1100 mA, 2300−2400 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	147	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2300−2400 MHz bandwidth)	Φ	—	–14.3	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	95	—	MHz
Gain Flatness in 100 MHz Bandwidth @ P_{out} = 45 W Avg.	G_F	—	0.5	—	dB
Gain Variation over Temperature (−30°C to +85°C)	ΔG	—	0.015	—	dB/°C
Output Power Variation over Temperature (−30°C to +85°C)	ΔP1dB	—	0.006	—	dB/°C

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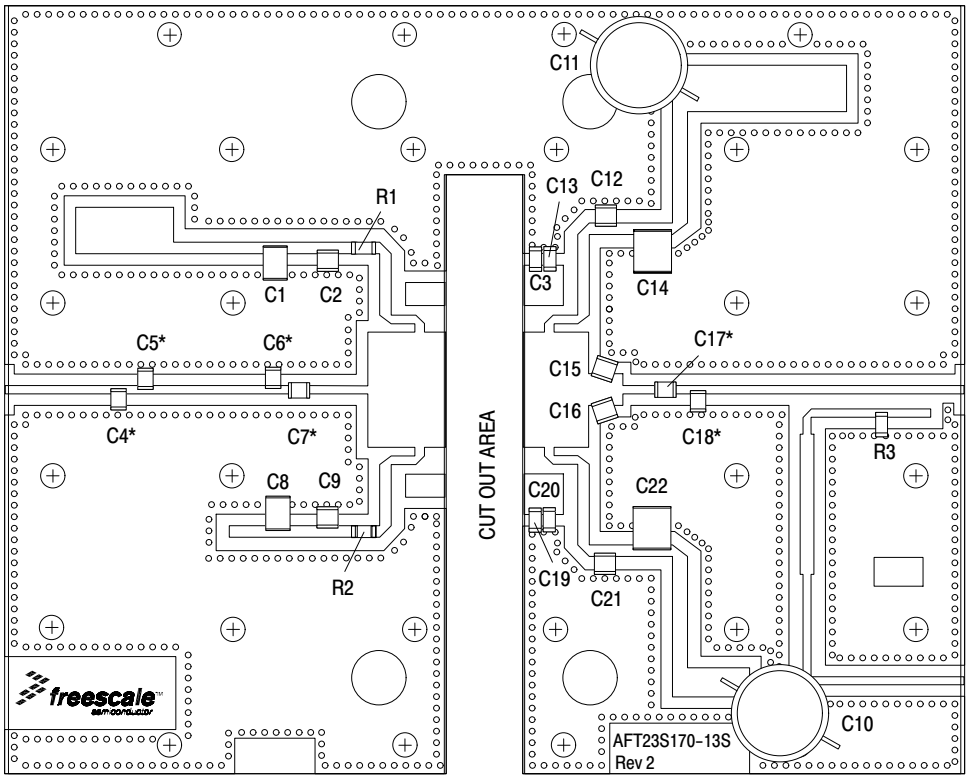

*C4, C5, C6, C7, C17 and C18 are mounted vertically.

Figure 2. AFT23S170−13SR3 Test Circuit Component Layout

Table 5. AFT23S170−13SR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C8	2.2 µF, 100 V Chip Capacitors	C3225X7R1H225KT	TDK
C2, C7, C9, C12, C17, C21	4.7 pF Chip Capacitors	ATC100B4R7BT500XT	ATC
C3, C13, C19, C20	1000 nF Chip Capacitors	12065G105AT2A	AVX
C4, C5, C18	0.3 pF Chip Capacitors	ATC100B0R3BT500XT	ATC
C6	1.0 pF Chip Capacitor	ATC100B1R0BT500XT	ATC
C10, C11	470 µF Electrolytic Capacitors	B41858C8477M000	EPCOS
C14, C22	10 µF, 100 V Chip Capacitors	C5750X7S2A106KT	TDK
C15, C16	0.2 pF Chip Capacitors	ATC100B0R2BT500XT	ATC
R1, R2	4.7 Ω, 1/4 W Chip Resistors	WCR1206-4R7FI	Welwyn
R3	0 Ω, 2 A Chip Resistor	WCR1206-R005J	Welwyn
PCB	0.020″, ε_r = 3.5	RO4350B	Rogers

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TYPICAL CHARACTERISTICS

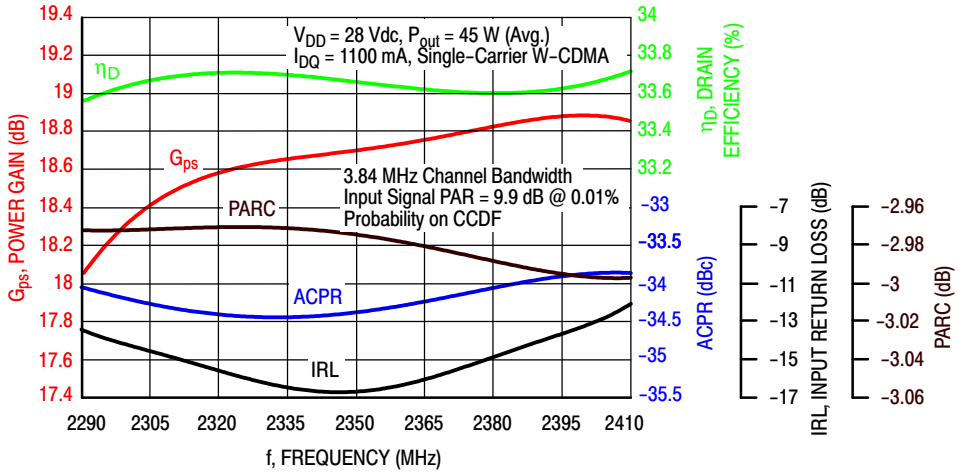

Figure 3. Single−Carrier Output Peak−to−Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 45 Watts Avg.

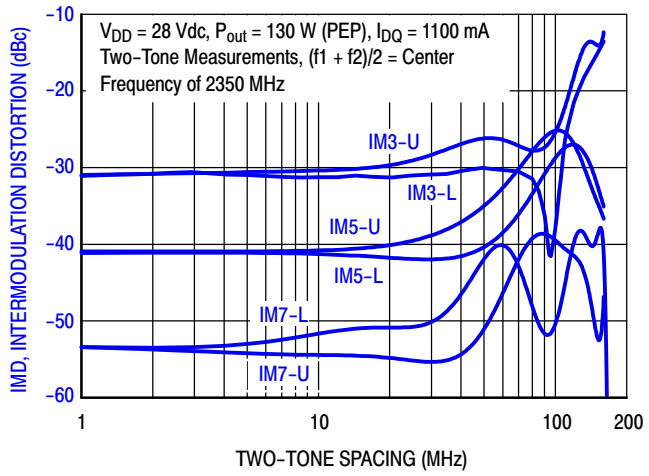

Figure 4. Intermodulation Distortion Products versus Two−Tone Spacing

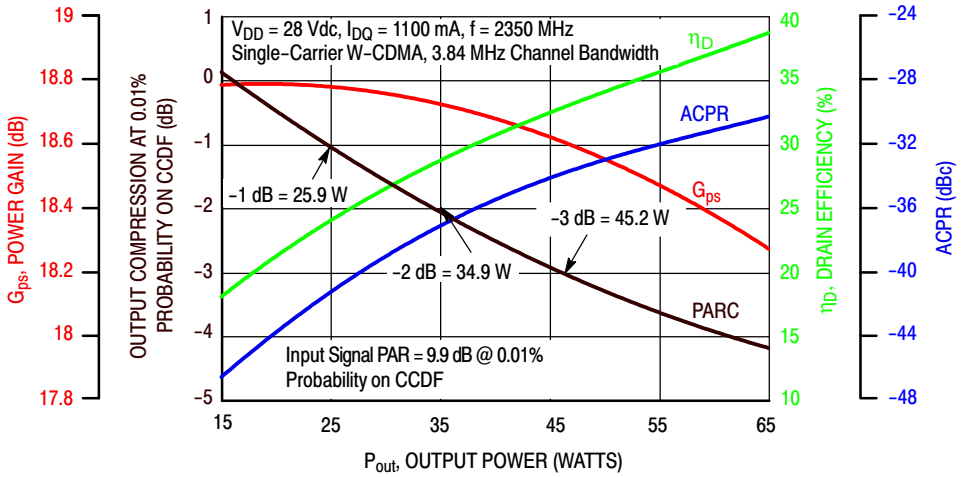

Figure 5. Output Peak−to−Average Ratio Compression (PARC) versus Output Power

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TYPICAL CHARACTERISTICS

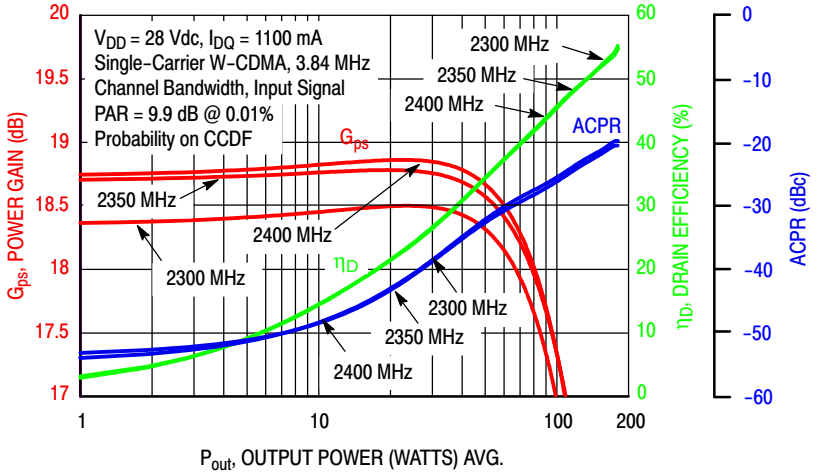

Figure 6. Single−Carrier W−CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

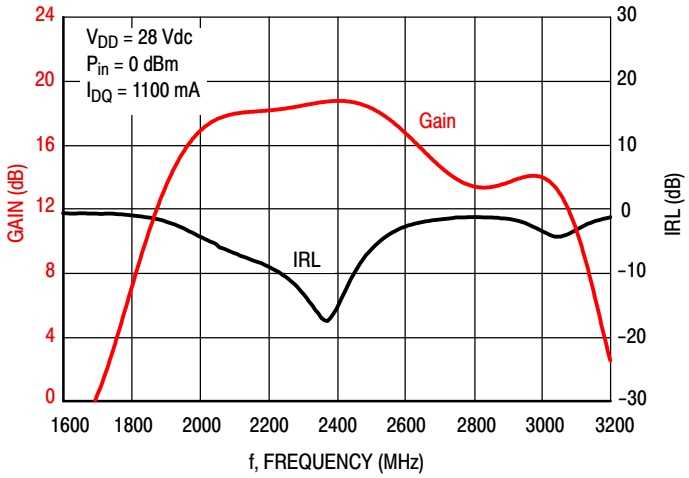

Figure 7. Broadband Frequency Response

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V_{DD} = 28 Vdc, I_{DQ} = 1161 mA, Pulsed CW, 10 µsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	3.46 – j9.07	3.45 + j8.51	2.09 – j4.35	18.2	53.2	210	51.5	–11
2350	5.27 – j10.0	4.90 + j8.90	2.11 – j4.50	18.0	53.3	213	51.8	–11
2400	8.84 – j10.7	7.40 + j10.2	2.06 – j4.47	18.5	53.2	211	52.4	–12

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	3.46 – j9.07	3.53 + j8.93	2.09 – j4.54	16.0	54.2	260	54.3	–16
2350	5.27 – j10.0	5.22 + j9.48	2.15 – j4.69	15.9	54.2	260	54.3	–17
2400	8.84 – j10.7	8.20 + j10.7	2.18 – j4.77	16.3	54.1	258	54.7	–17

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 8. Load Pull Performance — Maximum Power Tuning

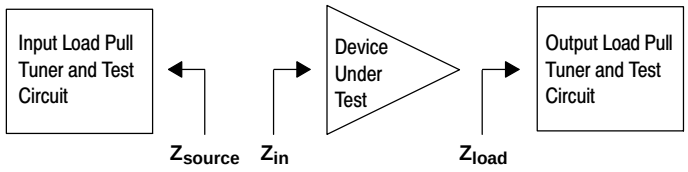
V_{DD} = 28 Vdc, I_{DQ} = 1161 mA, Pulsed CW, 10 µsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	3.46 – j9.07	3.56 + j8.75	3.81 – j2.63	20.3	51.8	152	60.4	–14
2350	5.27 – j10.0	5.04 + j9.29	3.29 – j2.43	20.2	51.8	152	61.1	–16
2400	8.84 – j10.7	7.80 + j10.4	2.95 – j2.60	20.5	51.9	154	61.5	–16

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	3.46 – j9.07	3.59 + j9.10	3.67 – j2.84	18.1	52.9	193	62.7	–20
2350	5.27 – j10.0	5.26 + j9.74	3.29 – j2.76	18.0	52.9	193	63.0	–22
2400	8.84 – j10.7	8.48 + j10.9	3.06 – j2.82	18.4	52.8	192	63.0	–23

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 9. Load Pull Performance — Maximum Drain Efficiency Tuning



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P1dB − TYPICAL LOAD PULL CONTOURS — 2350 MHz

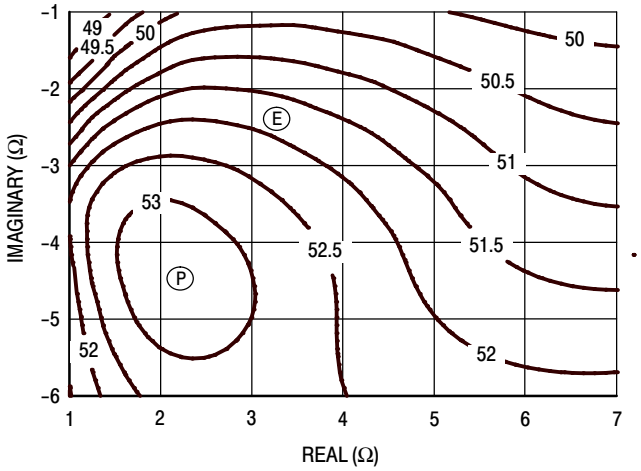

Figure 10. P1dB Load Pull Output Power Contours (dBm)

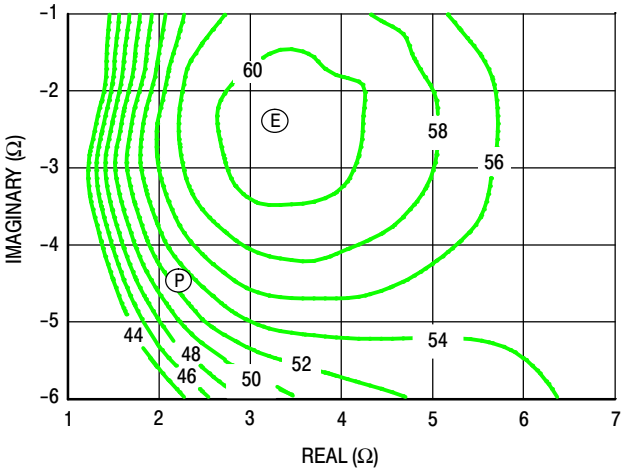

Figure 11. P1dB Load Pull Efficiency Contours (%)

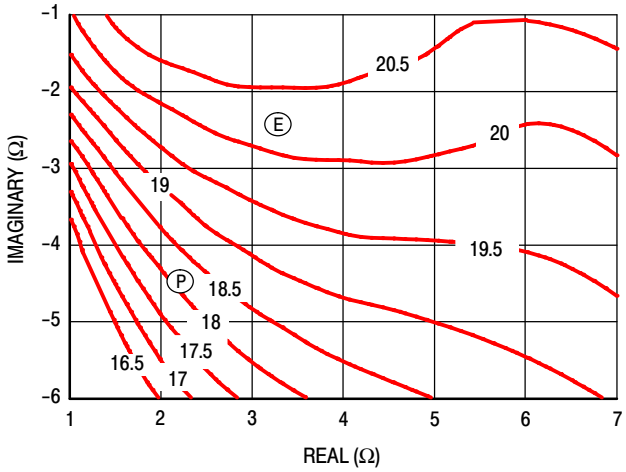

Figure 12. P1dB Load Pull Gain Contours (dB)

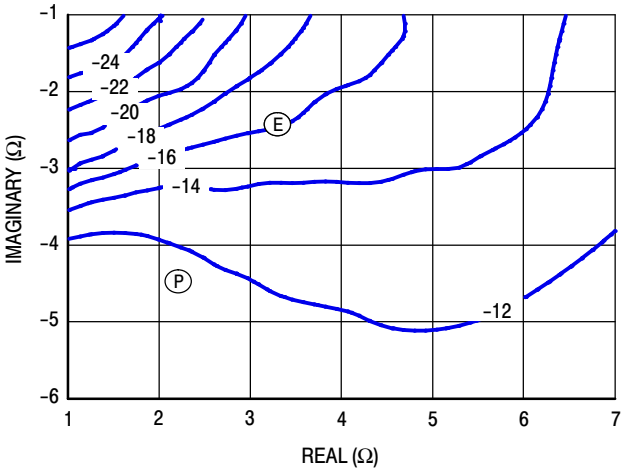

Figure 13. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Power Gain
Drain Efficiency
Linearity
Output Power

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P3dB − TYPICAL LOAD PULL CONTOURS — 2350 MHz

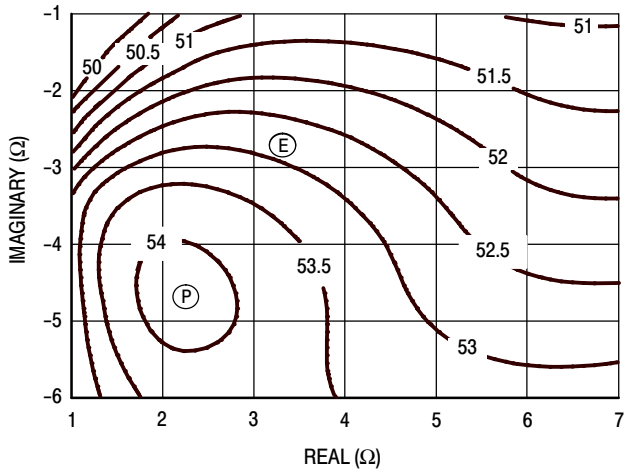

Figure 14. P3dB Load Pull Output Power Contours (dBm)

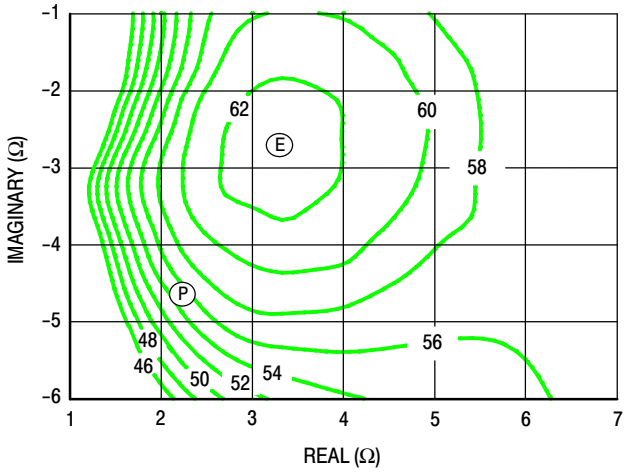

Figure 15. P3dB Load Pull Efficiency Contours (%)

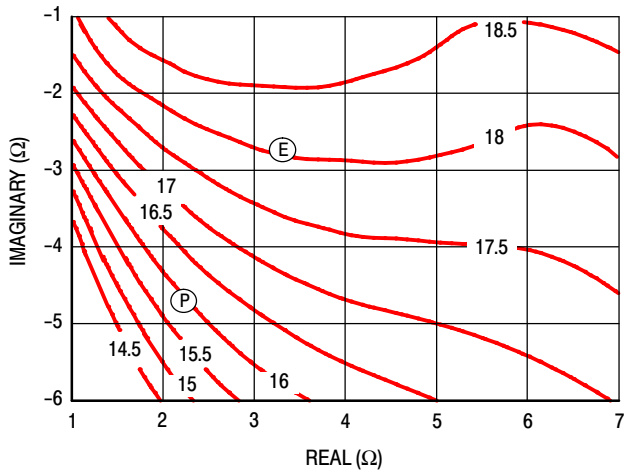

Figure 16. P3dB Load Pull Gain Contours (dB)

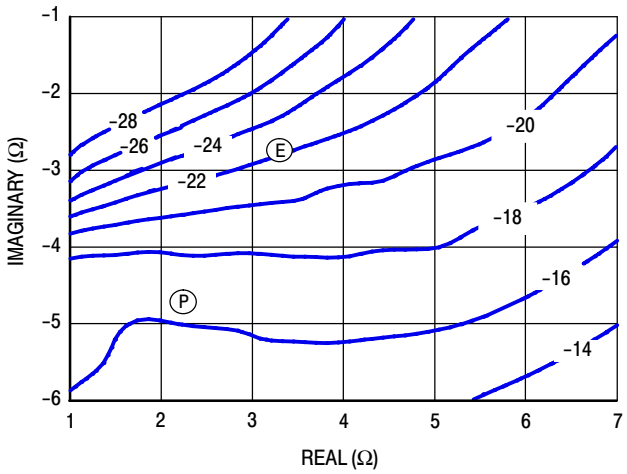

Figure 17. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓔ = Maximum Output Power
Ⓟ = Maximum Drain Efficiency

Power Gain
Drain Efficiency
Linearity
Output Power

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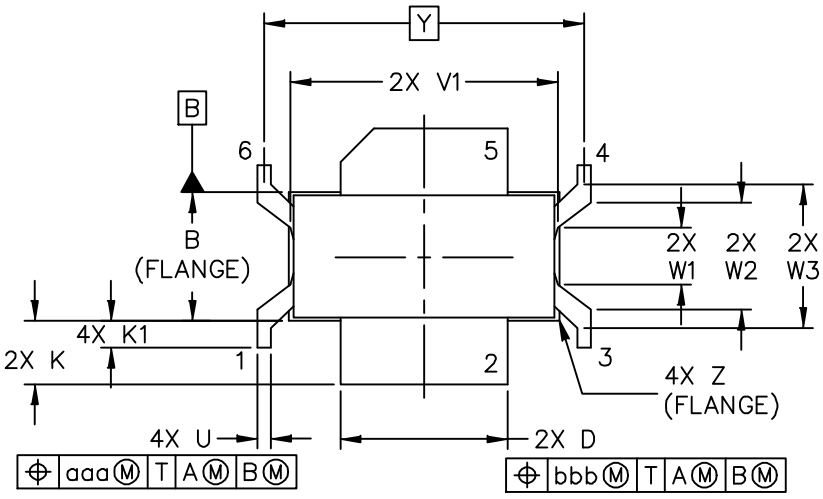
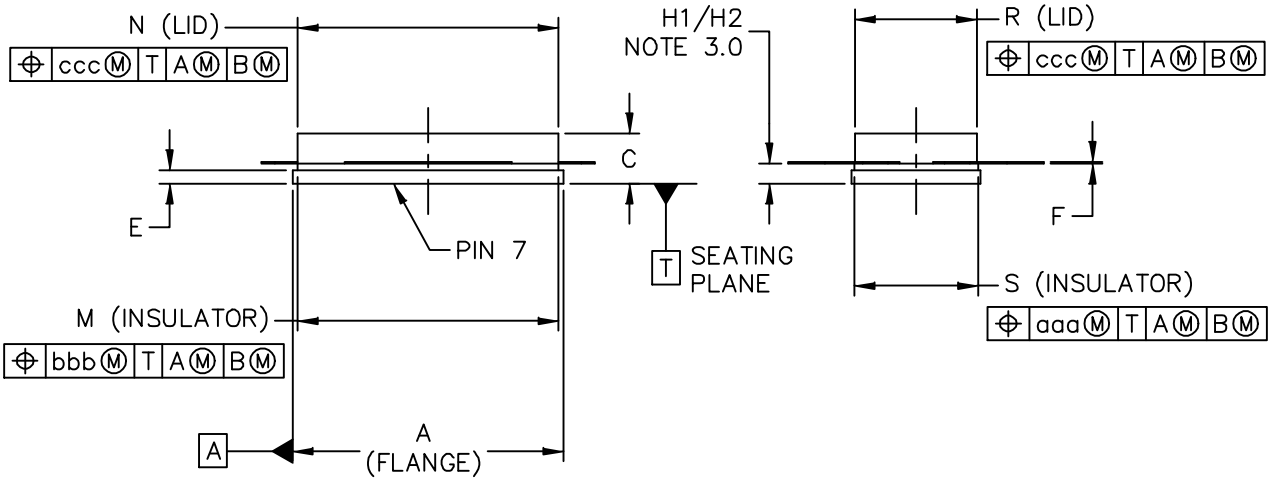
PACKAGE DIMENSIONS





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	CASE NUMBER: 2268-02	24 MAY 2012
	STANDARD: NON-JEDEC	

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NOTES:

1.0 CONTROLLING DIMENSION: INCH.

2.0 INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3.0 DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 2 & 5. H2 APPLIES TO PINS 1, 3, 4 & 6.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.805	.815	20.45	20.70	R	.365	.375	9.27	9.53
B	.380	.390	9.65	9.91	S	.365	.375	9.27	9.53
C	.125	.170	3.18	4.32	U	.035	.045	0.89	1.14
D	.495	.505	12.57	12.83	V1	.795	.805	20.19	20.45
E	.035	.045	0.89	1.14	W1	.165	.175	4.19	4.45
F	.004	.007	0.10	0.18	W2	.315	.325	8.00	8.26
H1	.057	.067	1.45	1.70	W3	.425	.435	10.80	11.05
H2	.054	.070	1.37	1.78	Y	.956 BSC		24.28 BSC	
K	.170	.210	4.32	5.33	Z	R.000	R.040	R.00	R1.02
K1	.070	.090	1.78	2.29	aaa	–	.005	–	0.127
M	.774	.786	19.66	19.96	bbb	–	.010	–	0.254
N	.772	.788	19.61	20.02	ccc	–	.015	–	0.381

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NI–780S–6	CASE NUMBER: 2268–02	24 MAY 2012
	STANDARD: NON–JEDEC	

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	June 2013	• Initial Release of Data Sheet

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