

512K x 8 HIGH-SPEED CMOS STATIC RAM

APRIL 2005

FEATURES

- High-speed access times:
10, 12 ns
- High-performance, low-power CMOS process
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ options
- $\overline{\text{CE}}$ power-down
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 3.3V power supply
- Packages available:
 - 36-pin 400-mil SOJ
 - 36-pin miniBGA
 - 44-pin TSOP (Type II)
- Lead-free available

DESCRIPTION

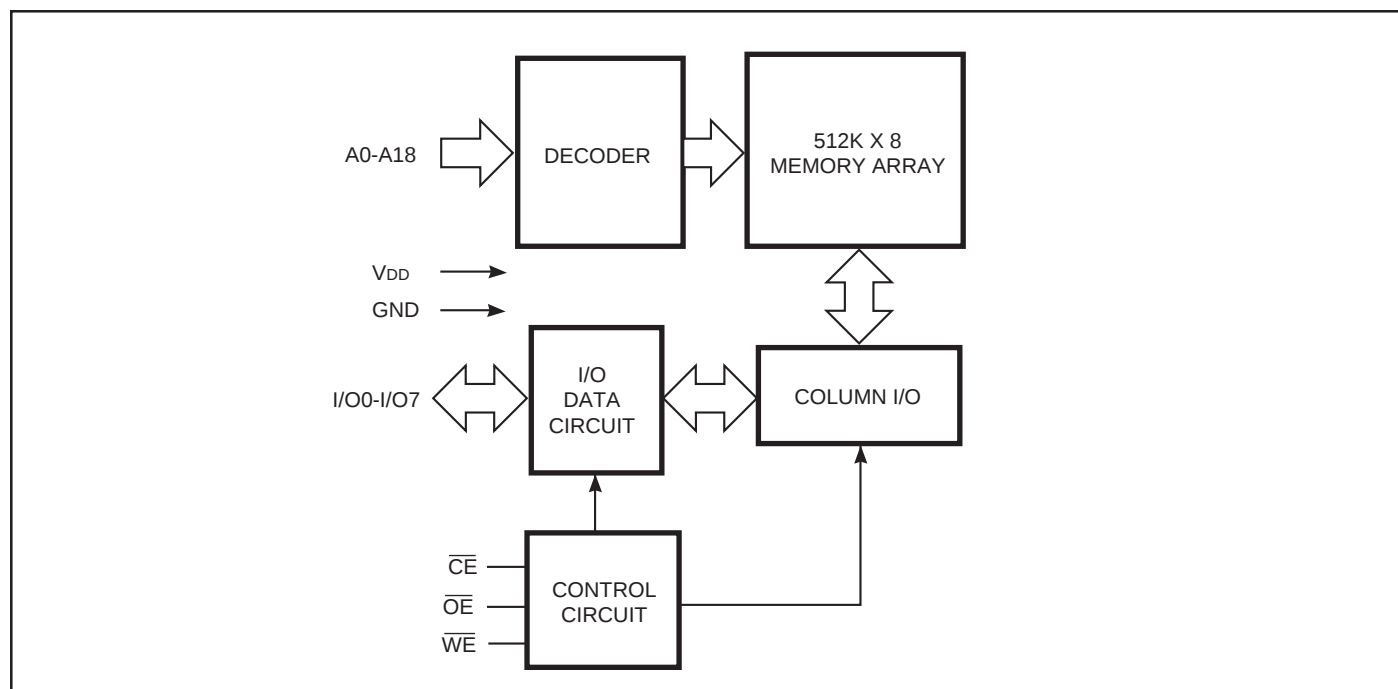
The *ISSI* IS61LV5128AL is a very high-speed, low power, 524,288-word by 8-bit CMOS static RAM. The IS61LV5128AL is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When $\overline{\text{CE}}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 250 μW (typical) with CMOS input levels.

The IS61LV5128AL operates from a single 3.3V power supply and all inputs are TTL-compatible.

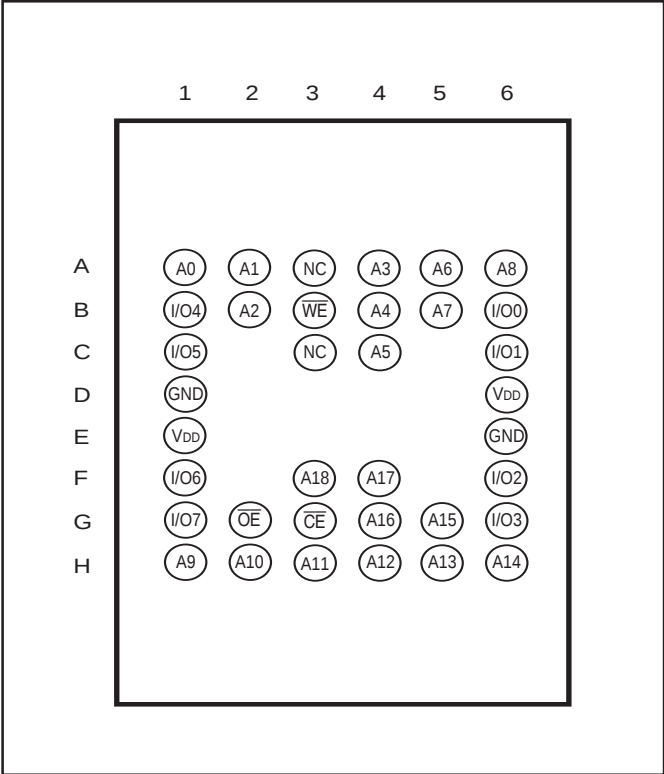
The IS61LV5128AL is available in 36-pin 400-mil SOJ, 36-pin mini BGA, and 44-pin TSOP (Type II) packages.

FUNCTIONAL BLOCK DIAGRAM

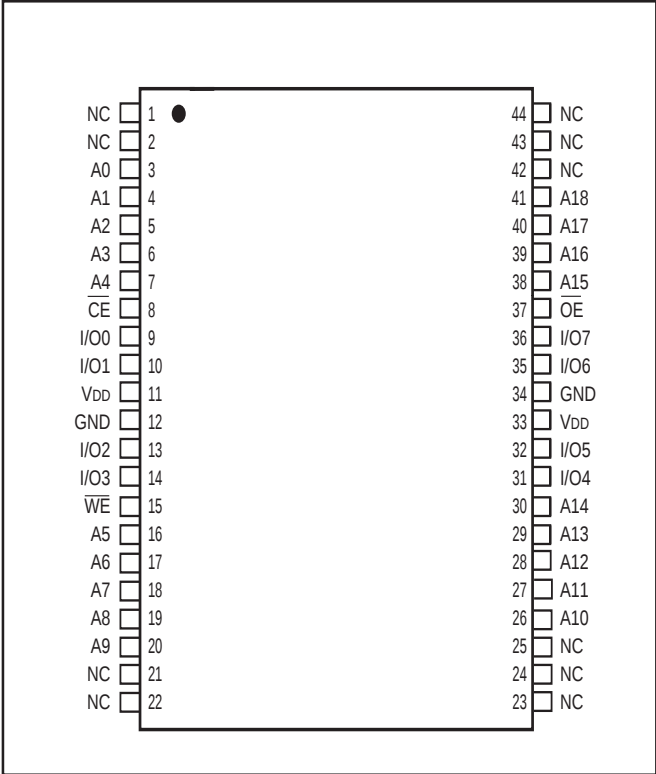


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PIN CONFIGURATION
36 mini BGA



44-Pin TSOP (Type II)



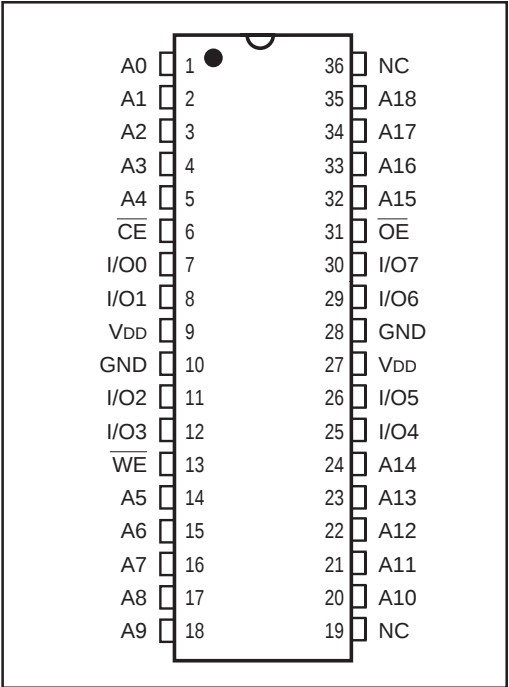
PIN DESCRIPTIONS

A0-A18	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Bidirectional Ports
V _{DD}	Power
GND	Ground
NC	No Connection

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	V _{DD} Current
Not Selected (Power-down)	X	H	X	High-Z	I _{SB1} , I _{SB2}
Output Disabled	H	L	H	High-Z	I _{CC}
Read	H	L	L	D _{OUT}	I _{CC}
Write	L	L	X	D _{IN}	I _{CC}

36-Pin SOJ



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to V _{DD} + 0.5	V
T _{STG}	Storage Temperature	-65 to +150	°C
P _T	Power Dissipation	1.0	W

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	V _{DD}	
		10ns	12ns
Commercial	0°C to +70°C	3.3V +10%, -5%	3.3V ±10%
Industrial	-40°C to +85°C	3.3V +10%, -5%	3.3V ±10%

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{I/O}	Input/Output Capacitance	V _{OUT} = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{DD} = Min., I _{OH} = -4.0 mA	2.4	—	V
V _{OL}	Output LOW Voltage	V _{DD} = Min., I _{OL} = 8.0 mA	—	0.4	V
V _{IH}	Input HIGH Voltage		2.0	V _{DD} + 0.3	V
V _{IL}	Input LOW Voltage ⁽¹⁾		-0.3	0.8	V
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{DD}	Com. Ind.	-2 5	2 μA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{DD} , Outputs Disabled	Com. Ind.	-2 5	2 μA

Note:

1. V_{IL} = -3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions	-10		-12		Unit
			Min.	Max.	Min.	Max.	
I _{CC}	V _{DD} Dynamic Operating Supply Current	V _{DD} = Max., I _{OUT} = 0 mA, f = f _{MAX}	Com. Ind.	— 90 95	— 85 90	— 85 90	mA
I _{SB}	TTL Standby Current (TTL Inputs)	V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} $\overline{CE} \geq V_{IH}$, f = f _{MAX} .	Com. Ind.	— 40 45	— 35 40	— 35 40	mA
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} $\overline{CE} \geq V_{IH}$, f = 0	Com. Ind.	— 20 25	— 20 25	— 20 25	mA
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} = Max., $\overline{CE} \geq V_{DD} - 0.2V$, V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V, f = 0	Com. Ind.	— 15 20	— 15 20	— 15 20	mA

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	-10		-12		Unit
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	10	—	12	—	ns
t_{AA}	Address Access Time	—	10	—	12	ns
t_{OH}	Output Hold Time	2	—	2	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	10	—	12	ns
t_{DOE}	$\overline{OE}$ Access Time	—	4	—	5	ns
$t_{HZOE}^{(2)}$	$\overline{OE}$ to High-Z Output	—	4	—	5	ns
$t_{LZOE}^{(2)}$	$\overline{OE}$ to Low-Z Output	0	—	0	—	ns
$t_{HZCE}^{(2)}$	$\overline{CE}$ to High-Z Output	0	4	0	6	ns
$t_{LZCE}^{(2)}$	$\overline{CE}$ to Low-Z Output	3	—	3	—	ns
t_{PU}	Power Up Time	0	—	0	—	ns
t_{PD}	Power Down Time	—	10	—	12	ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

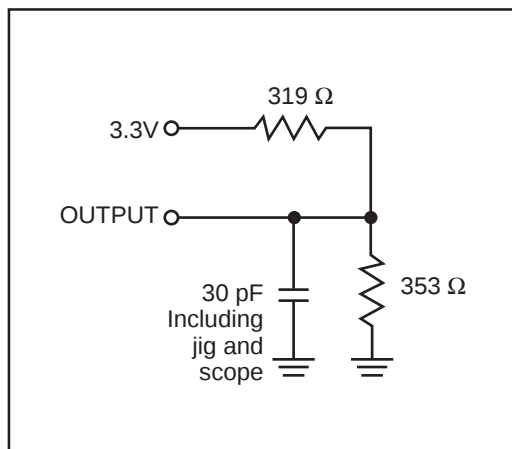


Figure 1

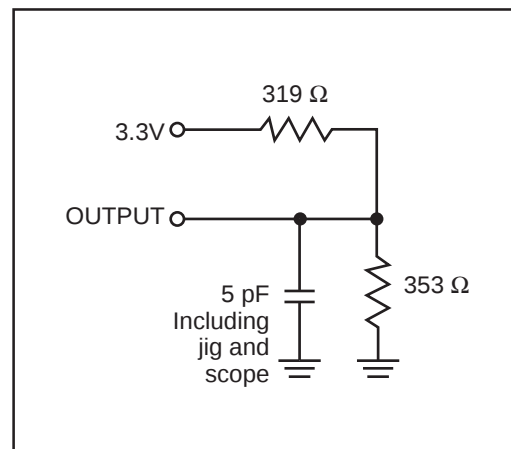
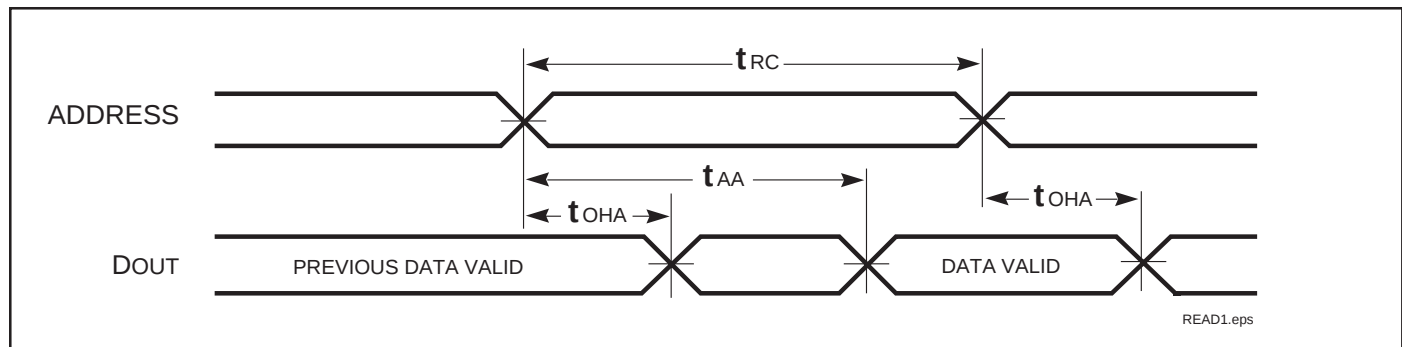
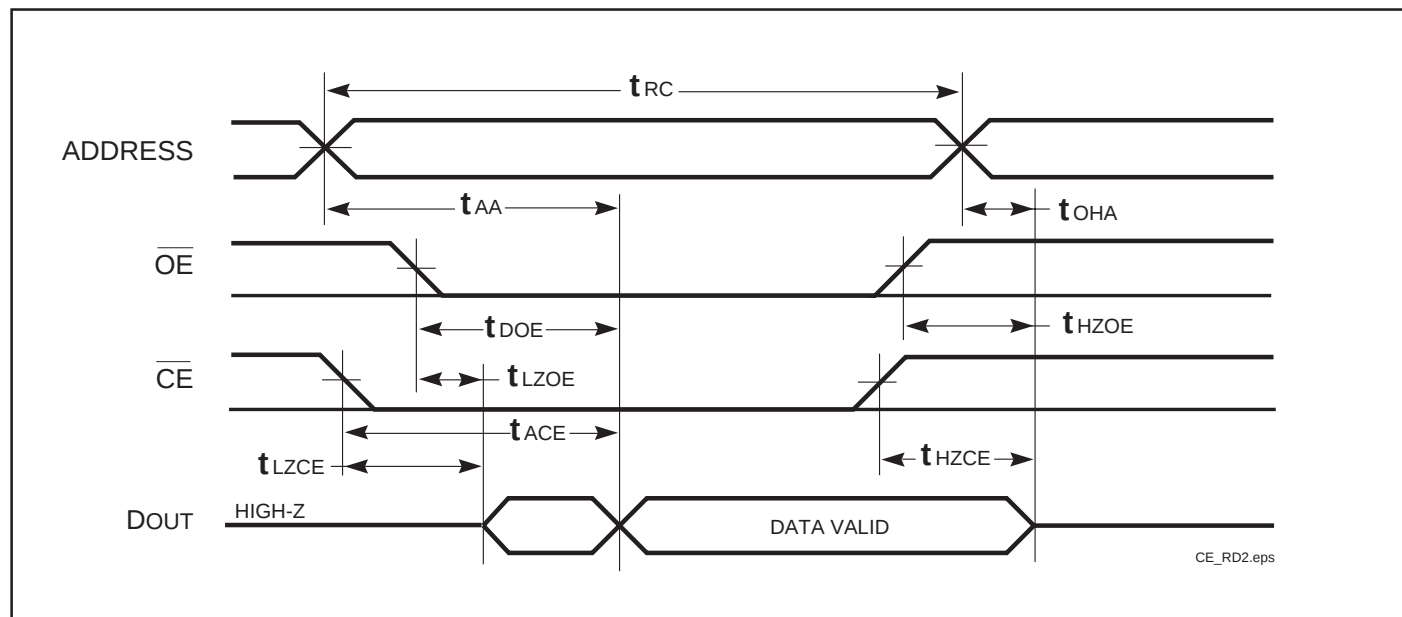


Figure 2

AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$)READ CYCLE NO. 2^(1,3) ($\overline{CE}$ and $\overline{OE}$ Controlled)

Notes:

1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

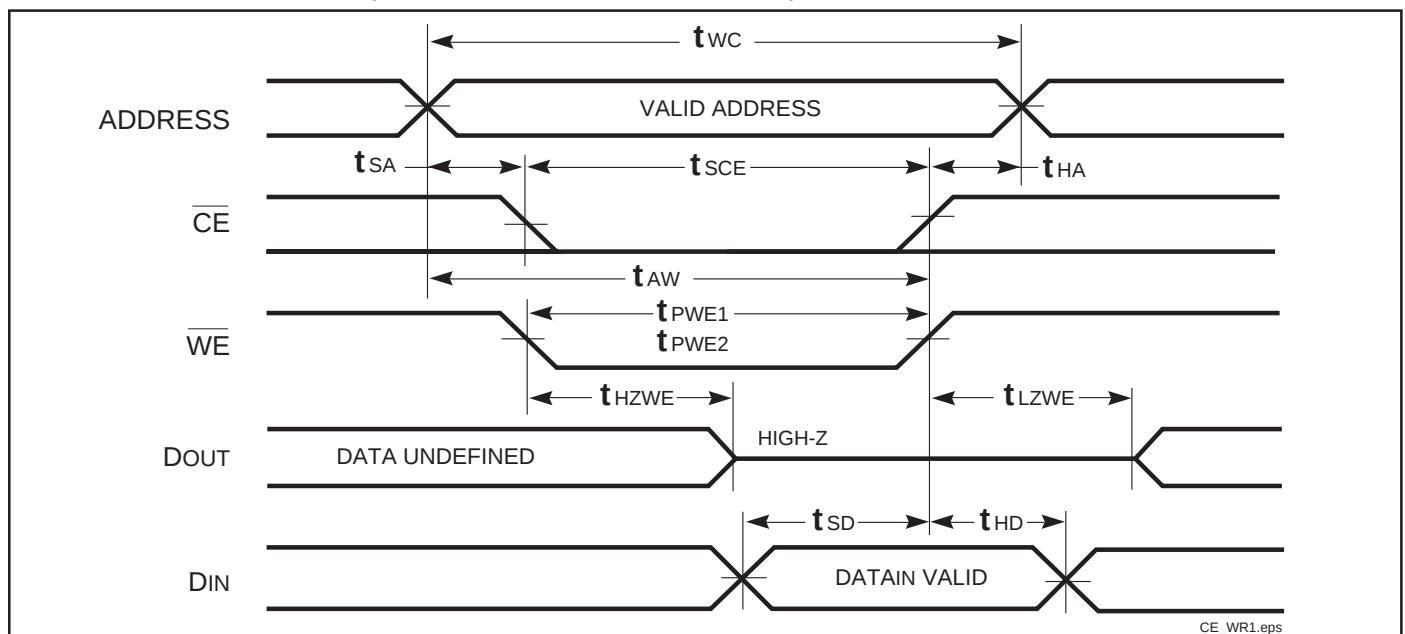
WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

Symbol	Parameter	-10		-12		Unit
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	10	—	12	—	ns
t_{SCE}	$\overline{CE}$ to Write End	8	—	8	—	ns
t_{AW}	Address Setup Time to Write End	8	—	8	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width	8	—	8	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	10	—	12	—	ns
t_{SD}	Data Setup to Write End	6	—	6	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
$t_{HZWE}^{(2)}$	$\overline{WE}$ LOW to High-Z Output	—	5	—	6	ns
$t_{LZWE}^{(2)}$	$\overline{WE}$ HIGH to Low-Z Output	2	—	2	—	ns

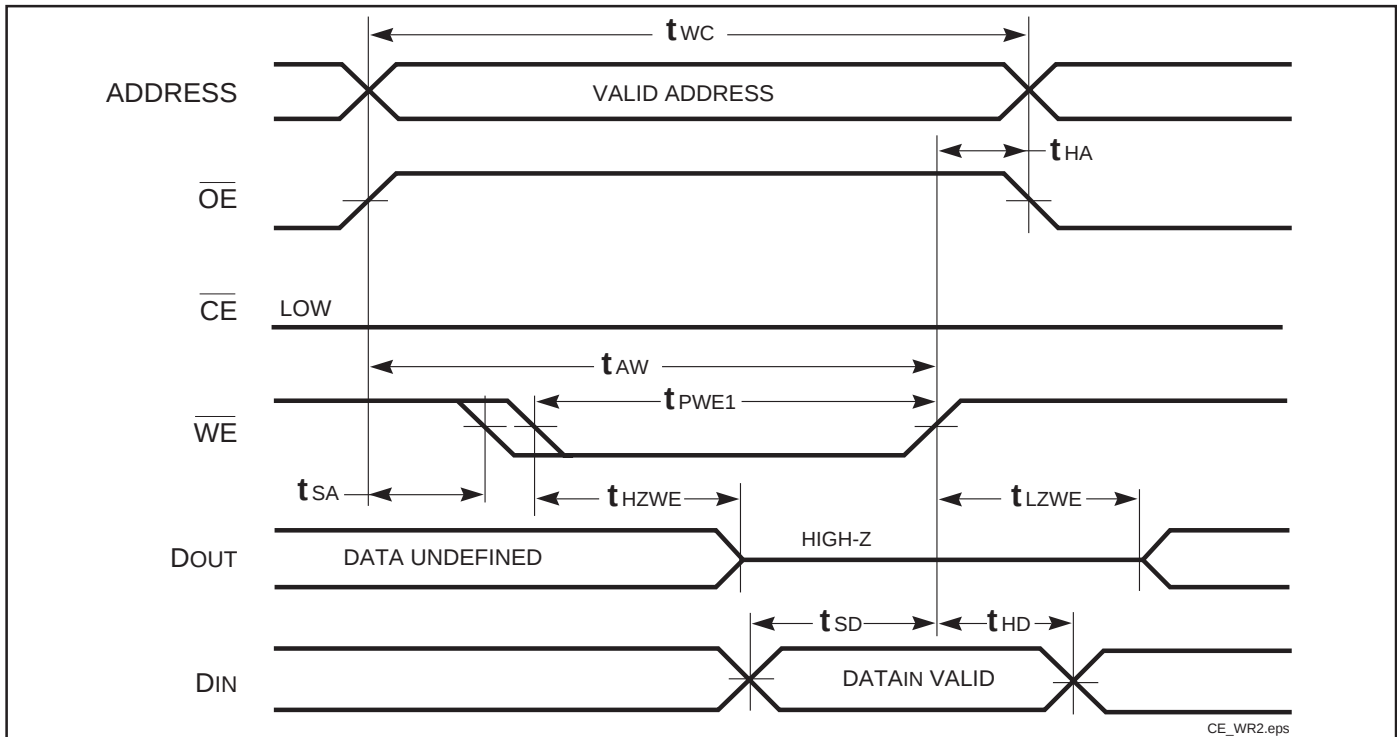
Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

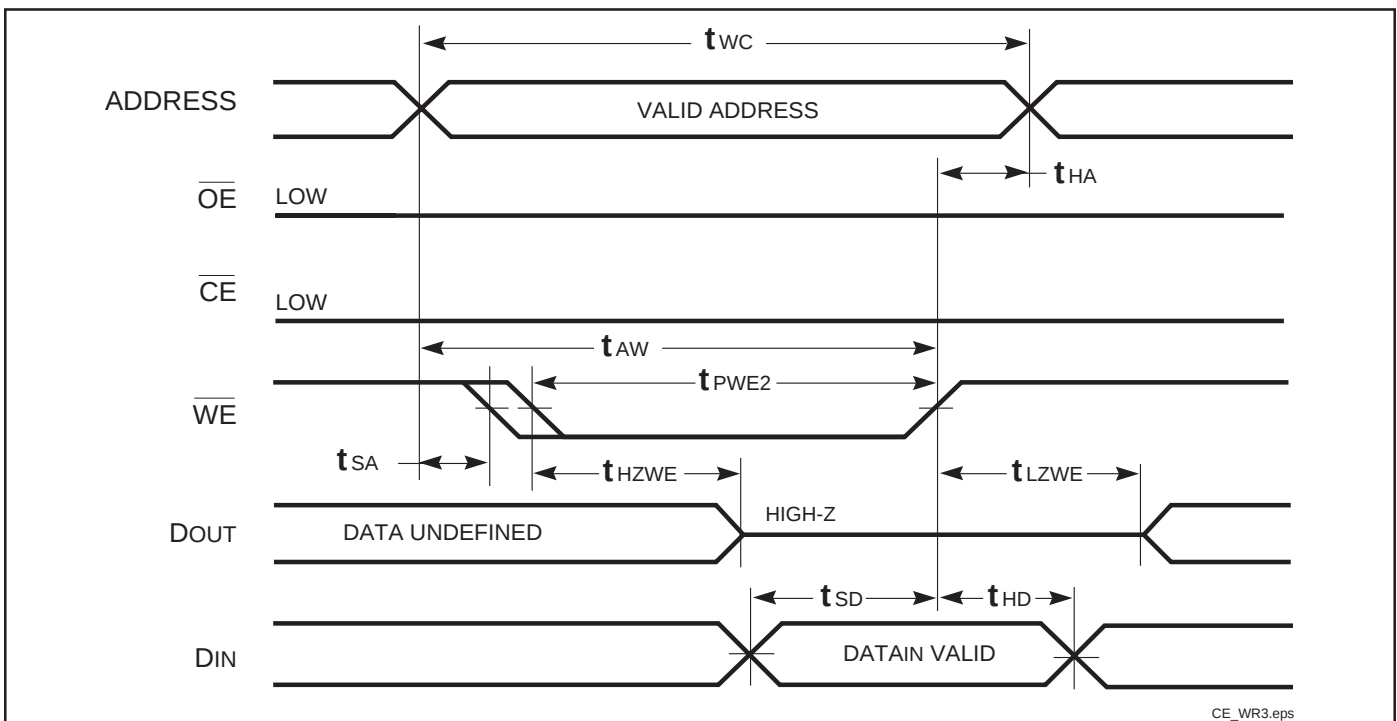
AC WAVEFORMS

WRITE CYCLE NO. 1^(1,2) ($\overline{CE}$ Controlled, $\overline{OE}$ = HIGH or LOW)

CE_WR1.eps

WRITE CYCLE NO. 2^(1,2) ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)**Notes:**

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} > V_{IH}$.

WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)

ORDERING INFORMATION**Commercial Range: 0°C to +70°C**

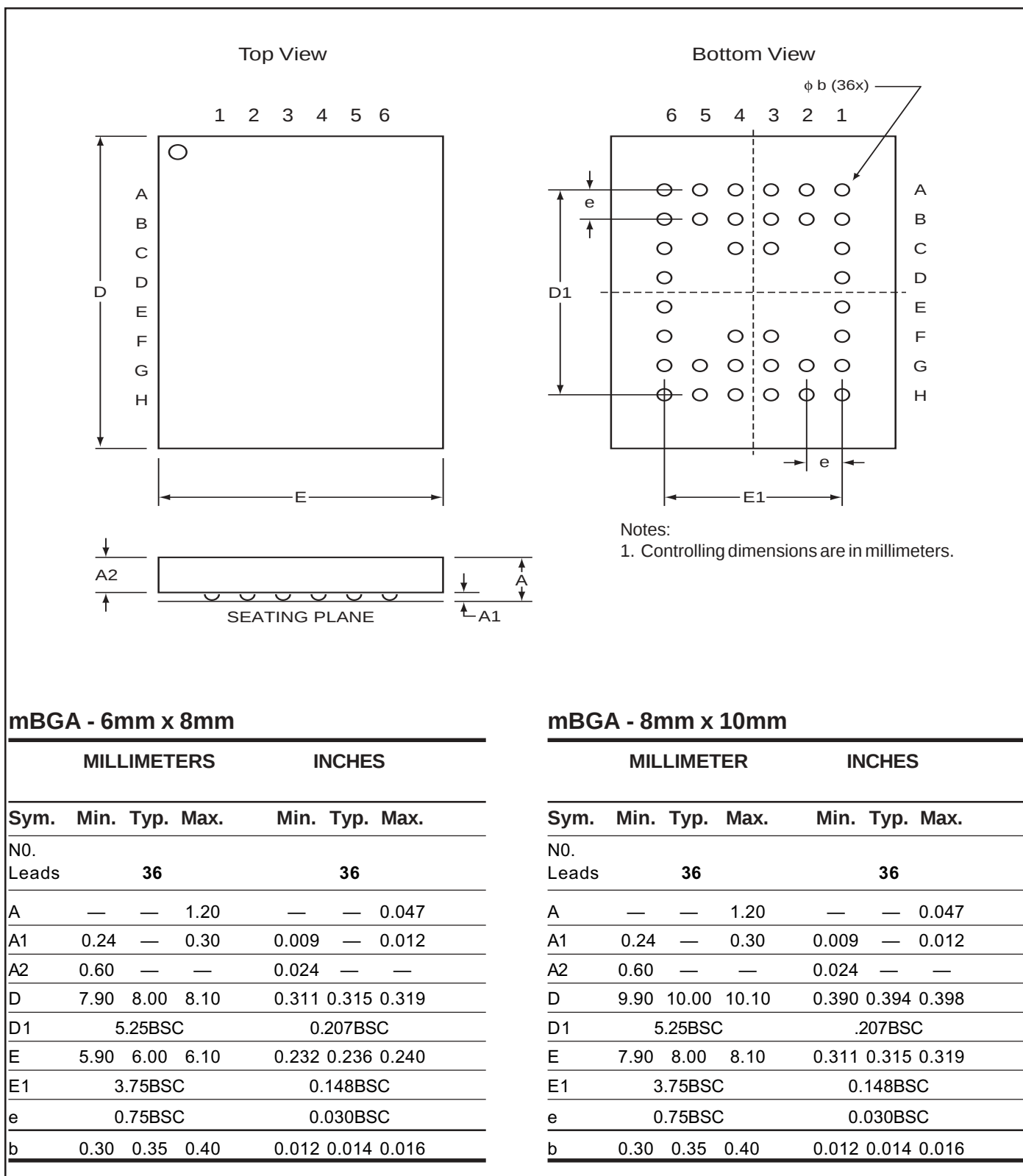
Speed (ns)	Order Part No.	Package
10	IS61LV5128AL-10K	400-mil Plastic SOJ
10	IS61LV5128AL-10T	TSOP (Type II)
12	IS61LV5128AL-12K	400-mil Plastic SOJ
12	IS61LV5128AL-12T	TSOP (Type II)

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
10	IS61LV5128AL-10KI	400-mil Plastic SOJ
10	IS61LV5128AL-10KLI	400-mil Plastic SOJ, Lead-free
10	IS61LV5128AL-10TI	TSOP (Type II)
10	IS61LV5128AL-10TLI	TSOP (Type II), Lead-free
10	IS61LV5128AL-10BI	mini BGA (8mmx10mm)
10	IS61LV5128AL-10BLI	mini BGA (8mmx10mm), Lead-free
12	IS61LV5128AL-12TI	TSOP (Type II)

PACKAGING INFORMATION

Mini Ball Grid Array Package Code: B (36-pin)



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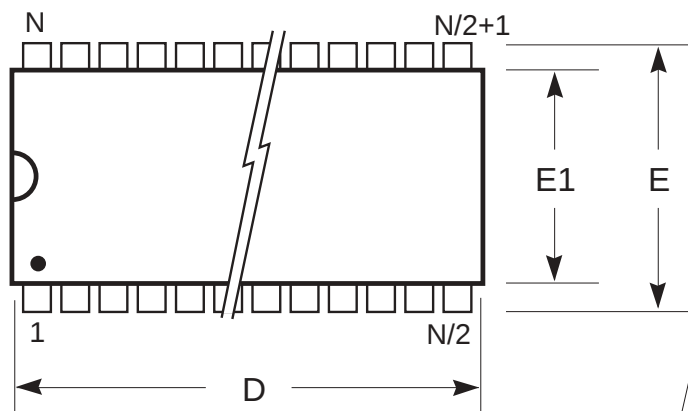
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Rev. E
01/15/03

PACKAGING INFORMATION

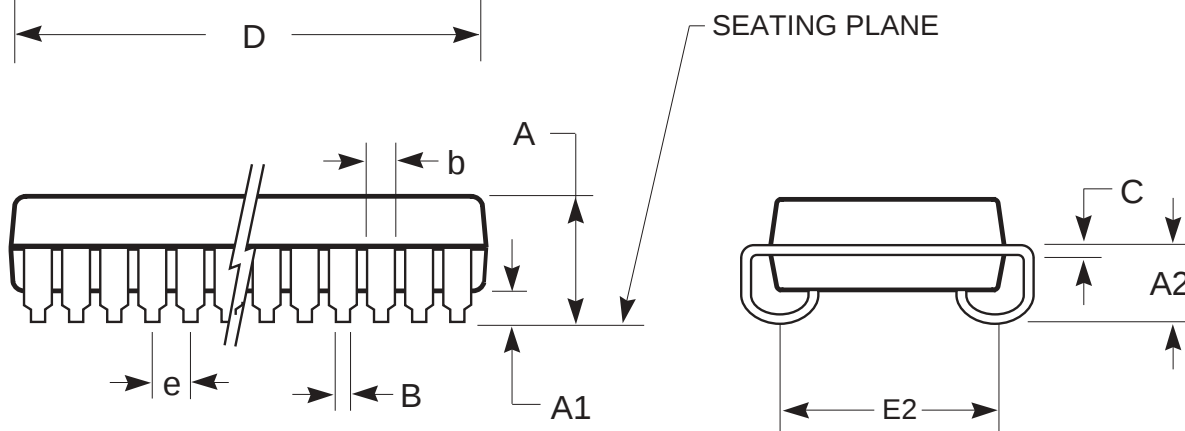
400-mil Plastic SOJ

Package Code: K



Notes:

1. Controlling dimension: millimeters.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Reference document: JEDEC MS-027.



Symbol	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
No. Leads (N)	28				32				36			
A	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148
A1	0.64	—	0.025	—	0.64	—	0.025	—	0.64	—	0.025	—
A2	2.08	—	0.082	—	2.08	—	0.082	—	2.08	—	0.082	—
B	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020
b	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032
C	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013
D	18.29	18.54	0.720	0.730	20.82	21.08	0.820	0.830	23.37	23.62	0.920	0.930
E	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445
E1	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E2	9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC	
e	1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC	

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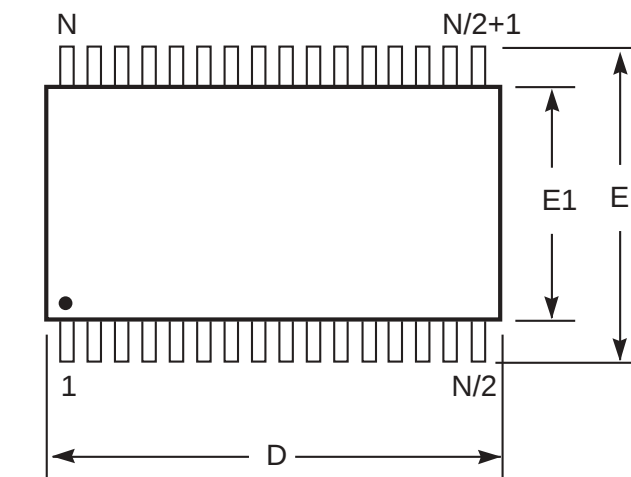
Symbol	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
No. Leads (N)	40				42				44			
A	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148
A1	0.64	—	0.025	—	0.64	—	0.025	—	0.64	—	0.025	—
A2	2.08	—	0.082	—	2.08	—	0.082	—	2.08	—	0.082	—
B	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020
b	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032
C	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013
D	25.91	26.16	1.020	1.030	27.18	27.43	1.070	1.080	28.45	28.70	1.120	1.130
E	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445
E1	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E2	9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC		9.40 BSC		0.370 BSC	
e	1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC		1.27 BSC		0.050 BSC	

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PACKAGING INFORMATION

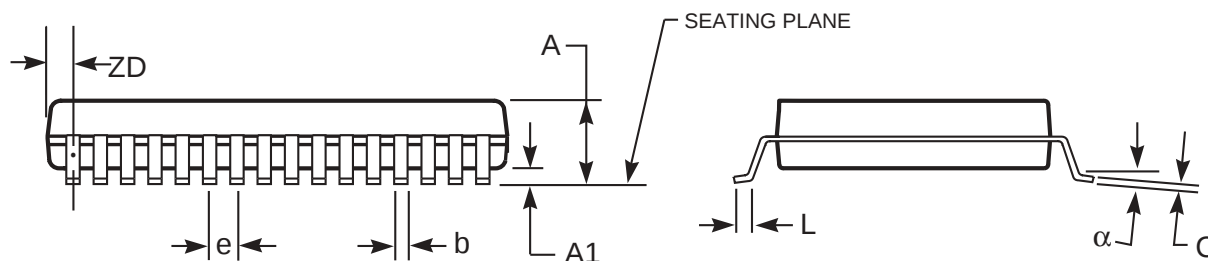
Plastic TSOP

Package Code: T (Type II)



Notes:

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.



Plastic TSOP (T - Type II)

Symbol	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Ref. Std.												
No. Leads (N)	32				44				50			
A	—	1.20	—	0.047	—	1.20	—	0.047	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006
b	0.30	0.52	0.012	0.020	0.30	0.45	0.012	0.018	0.30	0.45	0.012	0.018
C	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008
D	20.82	21.08	0.820	0.830	18.31	18.52	0.721	0.729	20.82	21.08	0.820	0.830
E1	10.03	10.29	0.391	0.400	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E	11.56	11.96	0.451	0.466	11.56	11.96	0.455	0.471	11.56	11.96	0.455	0.471
e	1.27 BSC		0.050 BSC		0.80 BSC		0.032 BSC		0.80 BSC		0.031 BSC	
L	0.40	0.60	0.016	0.024	0.41	0.60	0.016	0.024	0.40	0.60	0.016	0.024
ZD	0.95 REF		0.037 REF		0.81 REF		0.032 REF		0.88 REF		0.035 REF	
α	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°

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