FP0705

High frequency, high current power inductors

Product description

- High current carrying capacity
- Low core loss
- Inductance Range from 72 nH to 220 nH
- Current range from 20 A to 65 A
- 7.0 mm x 7.0 mm footprint surface mount package in a 4.95 mm height
- Ferrite core material
- Halogen free, lead free, RoHS compliant

Applications

- Multi-phase and Vcore regulators
- Voltage Regulator Modules (VRMs)
  - Server and desktop
  - Central processing unit (CPU)
  - Graphics processing unit (GPU)
  - Application specific integrated circuit (ASIC)
  - High power density
- Data networking and storage systems
- Graphics cards and battery power systems
- Portable electronics
- Point-of-Load modules

Environmental data

- Storage temperature range (Component): -40 °C to +125 °C
- Operating temperature range: -40 °C to +125 °C (ambient plus self-temperature rise)
- Solder reflow temperature: J-STD-020D compliant

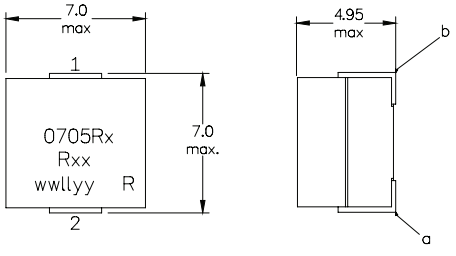
Powering Business Worldwide

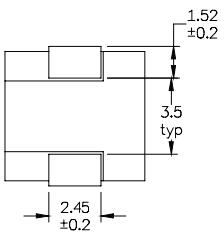
Product specifications

Part Number[7]	OCL[1] (nH) ±10%	FLL[2] (nH) minimum	I_{rms}[3] (A)	$I_{sat}1$[4] (A)	$I_{sat}2$[5] (A)	DCR (mΩ) @ 20°C	K-factor[7]
R1 version							
FP0705R1-R07-R	72	51	43	65	50	0.25 ± 10%	826
FP0705R1-R10-R	105	78	43	44	34	0.25 ± 10%	826
FP0705R1-R12-R	120	86	43	37	30	0.25 ± 10%	826
FP0705R1-R15-R	150	108	43	30	24	0.25 ± 10%	826
FP0705R1-R18-R	180	130	43	25	20	0.25 ± 10%	826
FP0705R1-R22-R	226	159	43	20	16	0.25 ± 10%	826
R2 version							
FP0705R2-R07-R	72	51	38	65	50	0.32 ± 9.4%	826
FP0705R2-R10-R	105	78	38	44	34	0.32 ± 9.4%	826
FP0705R2-R12-R	120	86	38	37	30	0.32 ± 9.4%	826
FP0705R2-R15-R	150	108	38	30	24	0.32 ± 9.4%	826
FP0705R2-R18-R	180	130	38	25	20	0.32 ± 9.4%	826
FP0705R2-R22-R	226	159	38	20	16	0.32 ± 9.4%	826
R2 version							
FP0705R3-R07-R	72	51	32	65	50	0.46 ± 6.5%	826
FP0705R3-R10-R	105	78	32	44	34	0.46 ± 6.5%	826
FP0705R3-R12-R	120	86	32	37	30	0.46 ± 6.5%	826
FP0705R3-R15-R	150	108	32	30	24	0.46 ± 6.5%	826
FP0705R3-R18-R	180	130	32	25	20	0.46 ± 6.5%	826
FP0705R3-R22-R	226	159	32	20	16	0.46 ± 6.5%	826

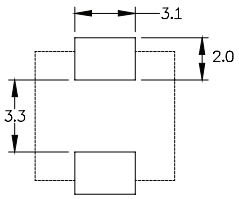
1. Open Circuit Inductance (OCL) Test Parameters: 100 kHz, 0.1 Vrms, 0.0 Adc, +25 °C
2. Full Load Inductance (FLL) Test Parameters: 100 kHz, 0.1 Vrms, $I_{sat}1$, +25 °C
3. I_{rms}: DC current for an approximate temperature rise of 40 °C without core loss. Derating is necessary for AC currents. PCB layout, trace thickness and width, air-flow, and proximity of other heat generating components will affect the temperature rise. It is recommended that the temperature of the part not exceed 125 °C under worst case operating conditions verified in the end application.
4. $I_{sat}1$: Peak current for approximately 20% rolloff @ +25 °C
5. $I_{sat}2$: Peak current for approximately 20% rolloff @ +125 °C
6. K-factor: Used to determine B_{p-p} for core loss (see graph).
   $B_{p-p} = K * L * \Delta I * 10^{-3}$. B_{p-p}:(Gauss), K: (K-factor from table),
   L: (Inductance in nH), ΔI (Peak to peak ripple current in Amps).
7. Part Number Definition: FP0705Rx-Rxx-R
   FP0705= Product code and size
   Rx= Version indicator
   -Rxx= Inductance value in µH, R= decimal point
   -R suffix = RoHS compliant

Dimensions (mm)

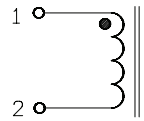




Recommended Pad Layout



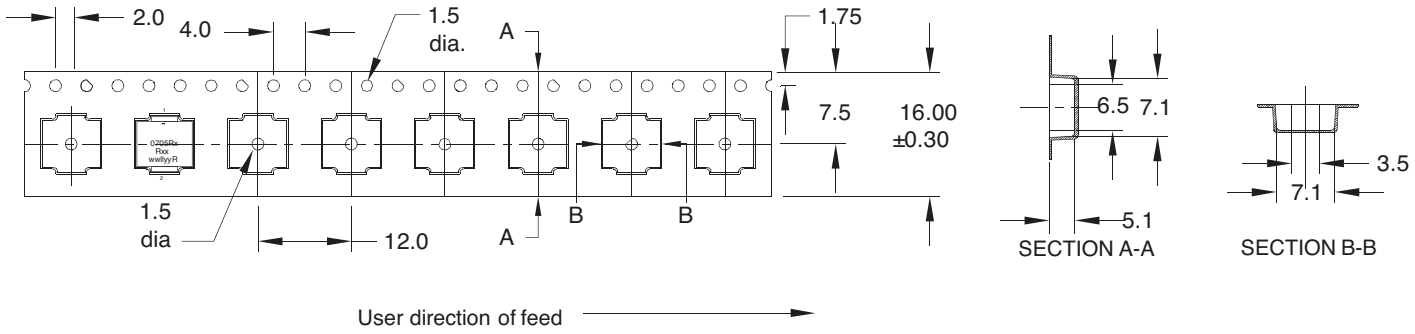
Schematic



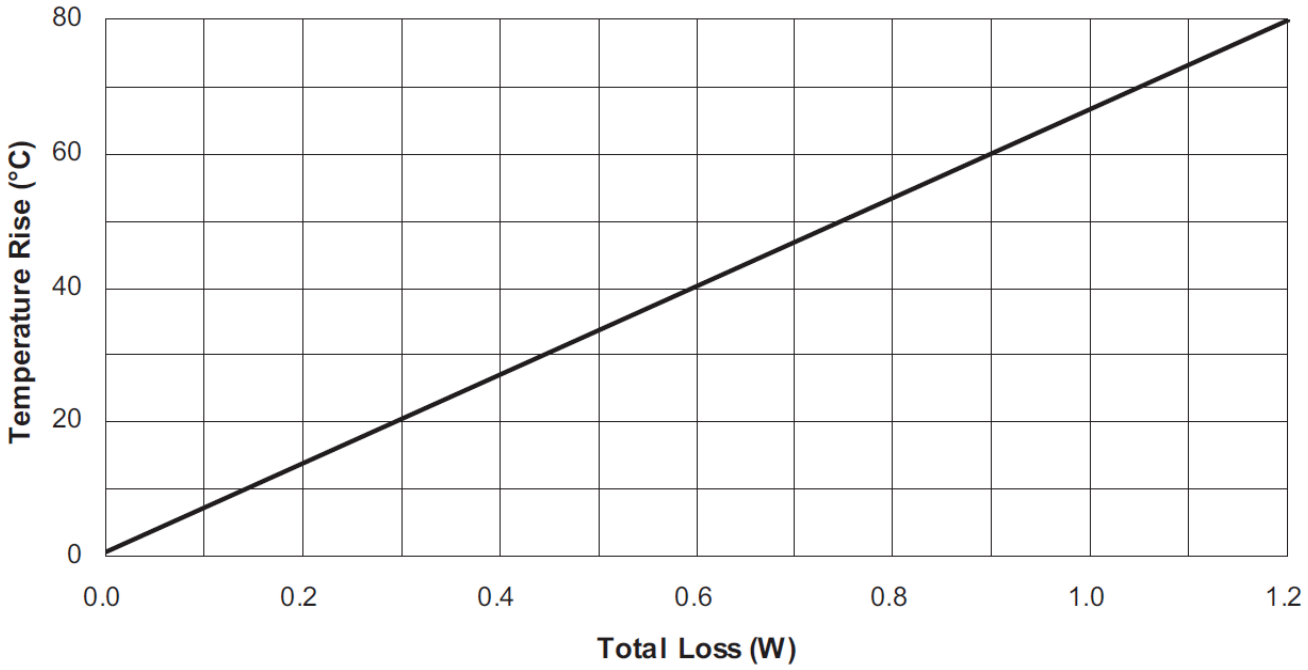
Part marking: 0705Rx (Rx = version indicator), Rxx = Inductance value in uH, R = decimal point,
wwllyy = date code, R = revision level
Tolerances are ±0.25 millimeters unless stated otherwise
PCB tolerances are ±0.1 millimeters unless stated otherwise
All soldering surface to be coplanar within 0.1016 millimeters
DCR measured between point "a" and point "b"
Do not route traces or vias underneath the inductor

Packaging information (mm)

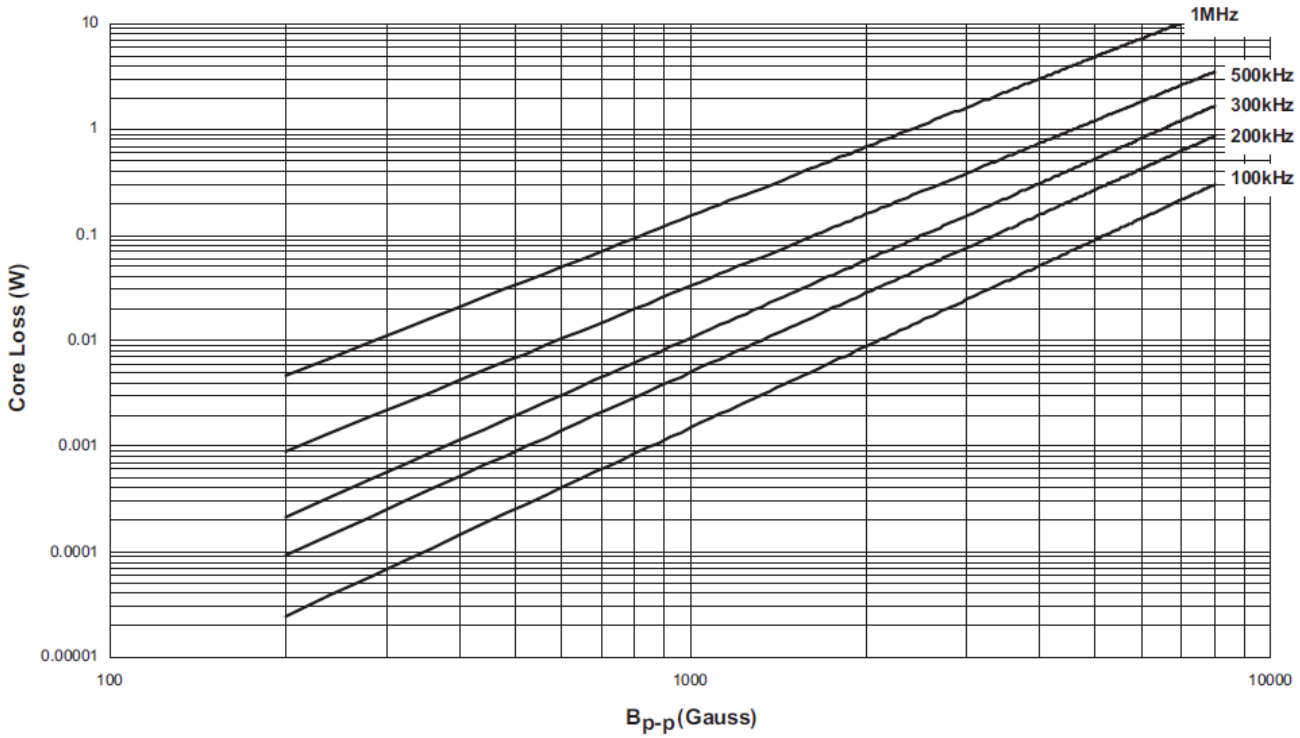
Supplied in tape and reel packaging , 950 parts per 13” diameter reel



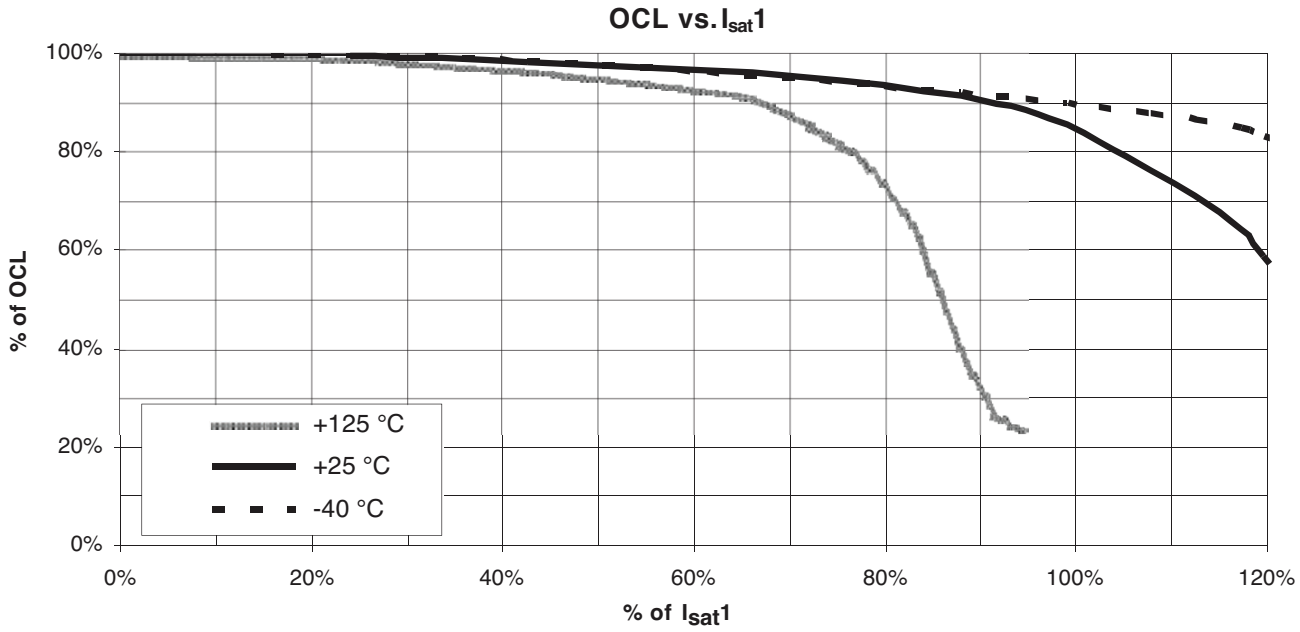
Temperature rise vs. total loss



Core loss vs. B_{p-p}



Inductance characteristics



Solder reflow profile

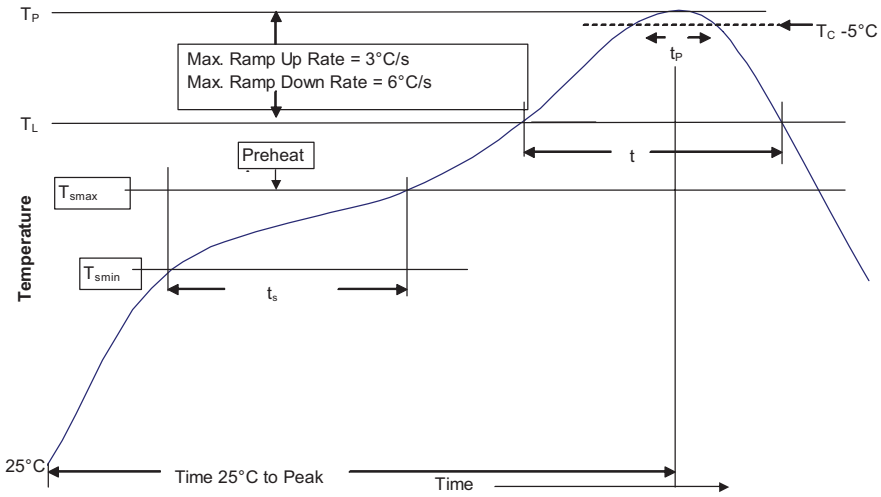


Table 1 - Standard SnPb Solder (T_C)

Package Thickness	Volume mm3 <350	Volume mm3 ≥350
<2.5mm)	235°C	220°C
≥2.5mm	220°C	220°C

Table 2 - Lead (Pb) Free Solder (T_C)

Package Thickness	Volume mm³ <350	Volume mm³ 350 - 2000	Volume mm³ >2000
<1.6mm	260°C	260°C	260°C
1.6 – 2.5mm	260°C	250°C	245°C
>2.5mm	250°C	245°C	245°C

Reference JDEC J-STD-020D

Profile Feature		Standard SnPb Solder	Lead (Pb) Free Solder
Preheat and Soak	• Temperature min. (T_{smin})	100°C	150°C
	• Temperature max. (T_{smax})	150°C	200°C
	• Time (T_{smin} to T_{smax}) (t_s)	60-120 Seconds	60-120 Seconds
Average ramp up rate T_{smax} to T_p		3°C/ Second Max.	3°C/ Second Max.
Liquidous temperature (T_L) Time at liquidous (t_L)		183°C 60-150 Seconds	217°C 60-150 Seconds
Peak package body temperature (T_P)*		Table 1	Table 2
Time (t_p)** within 5 °C of the specified classification temperature (T_C)		20 Seconds**	30 Seconds**
Average ramp-down rate (T_p to T_{smax})		6°C/ Second Max.	6°C/ Second Max.
Time 25°C to Peak Temperature		6 Minutes Max.	8 Minutes Max.

* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

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