CY7C1471BV25

72-Mbit (2 M × 36) Flow-Through SRAM with NoBL™ Architecture

Features

- No Bus Latency™ (NoBL™) architecture eliminates dead cycles between write and read cycles
- Supports up to 133 MHz bus operations with zero wait states
- Data transfers on every clock
- Pin compatible and functionally equivalent to ZBT™ devices
- Internally self timed output buffer control to eliminate the need to use $\overline{OE}$
- Registered inputs for flow through operation
- Byte Write capability
- 2.5-V I/O supply (V_{DDQ})
- Fast clock-to-output times
  - 6.5 ns (for 133-MHz device)
- Clock Enable ($\overline{CEN}$) pin to enable clock and suspend operation
- Synchronous self timed writes
- Asynchronous Output Enable ($\overline{OE}$)
- CY7C1471BV25 available in JEDEC-standard Pb-free 100-pin TQFP package.
- Three Chip Enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) for simple depth expansion.
- Automatic power down feature available using ZZ mode or CE deselect.
- Burst Capability – linear or interleaved burst order
- Low standby power

Functional Description

The CY7C1471BV25, is 2.5 V, 2 M × 36 synchronous flow through burst SRAMs designed specifically to support unlimited true back-to-back read or write operations without the insertion of wait states. The CY7C1471BV25, is equipped with the advanced No Bus Latency (NoBL) logic required to enable consecutive read or write operations with data transferred on every clock cycle. This feature dramatically improves the throughput of data through the SRAM, especially in systems that require frequent write-read transitions.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable ($\overline{CEN}$) signal, which when deasserted suspends operation and extends the previous clock cycle. Maximum access delay from the clock rise is 6.5 ns (133-MHz device).

Write operations are controlled by two or four Byte Write Select ($\overline{BW}_X$) and a Write Enable ($\overline{WE}$) input. All writes are conducted with on-chip synchronous self timed write circuitry.

Three synchronous Chip Enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) provide easy bank selection and output tristate control. To avoid bus contention, the output drivers are synchronously tristated during the data portion of a write sequence.

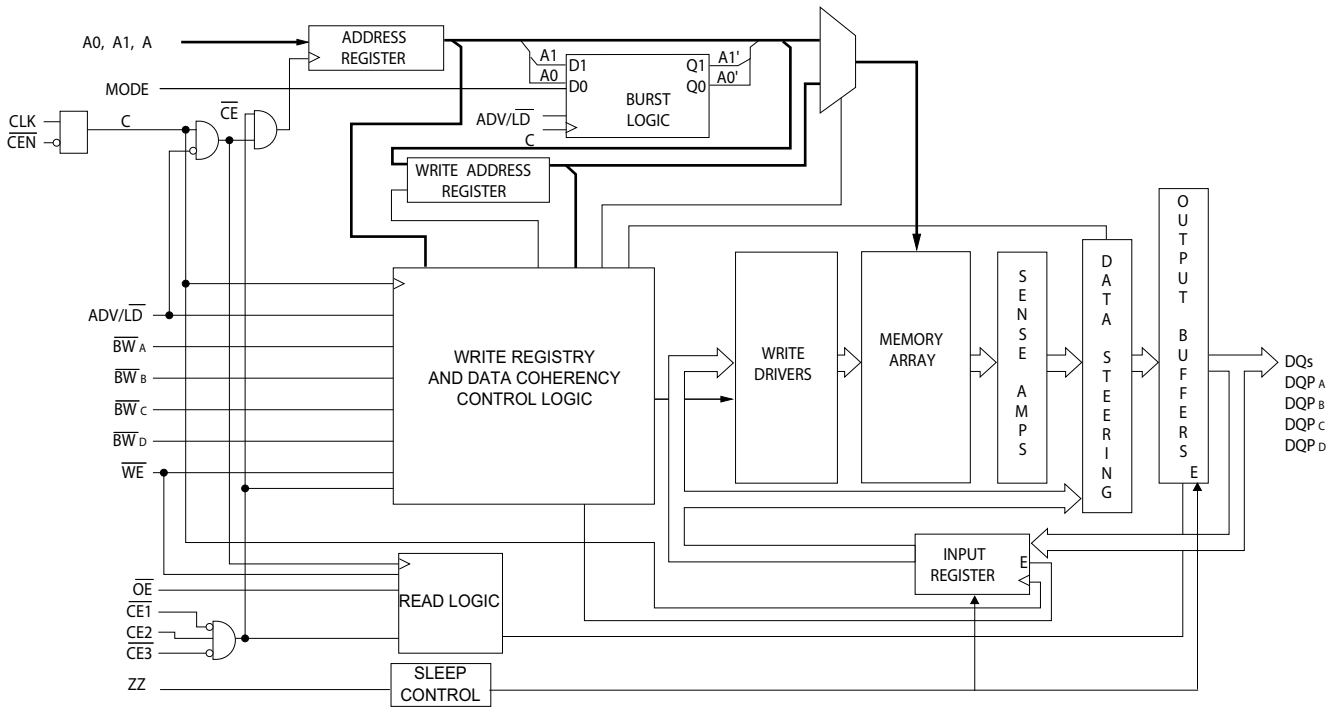
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Selection Guide

Description	133 MHz	Unit
Maximum Access Time	6.5	ns
Maximum Operating Current	305	mA
Maximum CMOS Standby Current	120	mA

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Logic Block Diagram – CY7C1471BV25



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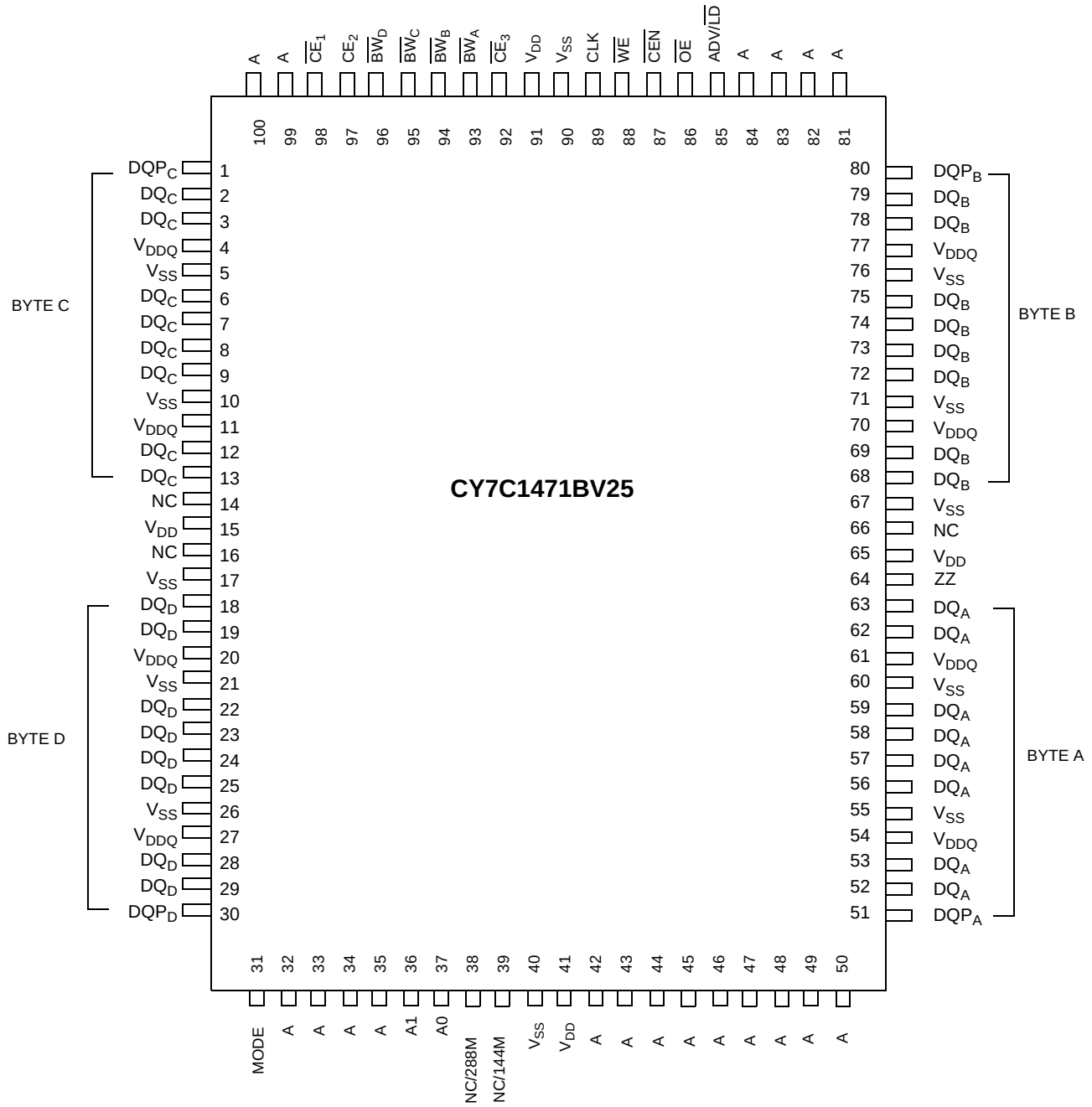
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Pin Configurations

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) Pinout



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Pin Definitions

Name	I/O	Description
A_0, A_1, A	Input-Synchronous	**Address Inputs Used to Select One of the Address Locations**. Sampled at the rising edge of the CLK. $A_{[1:0]}$ are fed to the two-bit burst counter.
$\overline{BW_A}$, $\overline{BW_B}$, $\overline{BW_C}$, $\overline{BW_D}$	Input-Synchronous	**Byte Write Inputs, Active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{WE}$	Input-Synchronous	**Write Enable Input, Active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/$\overline{LD}$	Input-Synchronous	**Advance/Load Input**. Used to advance the on-chip address counter or load a new address. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ must be driven LOW to load a new address.
CLK	Input-Clock	**Clock Input**. Captures all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE_1}$	Input-Synchronous	**Chip Enable 1 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE_3}$ to select or deselect the device.
CE_2	Input-Synchronous	**Chip Enable 2 Input, Active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and $\overline{CE_3}$ to select or deselect the device.
$\overline{CE_3}$	Input-Synchronous	**Chip Enable 3 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and CE_2 to select or deselect the device.
$\overline{OE}$	Input-Asynchronous	**Output Enable, Asynchronous Input, Active LOW**. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are enabled to behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state, when the device has been deselected.
$\overline{CEN}$	Input-Synchronous	**Clock Enable Input, Active LOW**. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Because deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required.
ZZ	Input-Asynchronous	**ZZ "Sleep" Input**. This active HIGH input places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin must be LOW or left floating. ZZ pin has an internal pull down.
DQ_s	I/O-Synchronous	**Bidirectional Data I/O Lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ_s and DQP_X are placed in a tristate condition.The outputs are automatically tristated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
DQP_X	I/O-Synchronous	**Bidirectional Data Parity I/O Lines.** Functionally, these signals are identical to DQ_s. During write sequences, DQP_X is controlled by BW_X correspondingly.
MODE	Input Strap Pin	**Mode Input. Selects the Burst Order of the Device.** When tied to Gnd selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence.
V_{DD}	Power Supply	**Power Supply Inputs to the Core of the Device**.
V_{DDQ}	I/O Power Supply	**Power Supply for the I/O Circuitry**.
V_{SS}	Ground	**Ground for the Device**.
NC	–	**No Connects**. Not internally connected to the die. 144M, 288M, 576M, and 1G are address expansion pins and are not internally connected to the die.

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Functional Overview

The CY7C1471BV25, is synchronous flow through burst SRAMs designed specifically to eliminate wait states during write read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the Clock Enable input signal (CEN). If CEN is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with CEN. Maximum access delay from the clock rise (t_{CDV}) is 6.5 ns (133-MHz device).

Accesses are initiated by asserting all three Chip Enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) active at the rising edge of the clock. If CEN is active LOW and ADV/LD is asserted LOW, the address presented to the device is latched. The access is either a read or write operation, depending on the status of the Write Enable ($\overline{WE}$). Use Byte Write Select ($\overline{BW}_X$) to conduct Byte Write operations.

Write operations are qualified by the $\overline{WE}$. All writes are simplified with on-chip synchronous self- timed write circuitry.

Three synchronous Chip Enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) simplify depth expansion. All operations (reads, writes, and deselects) are pipelined. ADV/LD must be driven LOW after the device is deselected to load a new address for the next operation.

Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise:

- $\overline{CEN}$ is asserted LOW
- $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are ALL asserted active
- $\overline{WE}$ is deasserted HIGH
- ADV/$\overline{LD}$ is asserted LOW.

The address presented to the address inputs is latched into the Address Register and presented to the memory array and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the output buffers. The data is available within 6.5 ns (133-MHz device) provided $\overline{OE}$ is active LOW. After the first clock of the read access, the output buffers are controlled by $\overline{OE}$ and the internal control logic. $\overline{OE}$ must be driven LOW to drive out the requested data. On the subsequent clock, another operation (read/write/deselect) can be initiated. When the SRAM is deselected at clock rise by one of the chip enable signals, the output is tristated immediately.

Burst Read Accesses

The CY7C1471BV25, has an on-chip burst counter that enables the user the ability to supply a single address and conduct up to four reads without reasserting the address inputs. ADV/LD must be driven LOW to load a new address into the SRAM, as described in the Single Read Accesses section. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A_0 and A_1 in the burst sequence, and wraps around when incremented sufficiently. A HIGH input on ADV/LD increments the internal burst counter regardless of the state of chip enable inputs or $\overline{WE}$. $\overline{WE}$ is latched at the beginning of a burst cycle. Therefore, the type of access (read or write) is maintained throughout the burst sequence.

Single Write Accesses

Write accesses are initiated when these conditions are satisfied at clock rise:

- $\overline{CEN}$ is asserted LOW
- $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are ALL asserted active
- $\overline{WE}$ is asserted LOW.

The address presented to the address bus is loaded into the Address Register. The write signals are latched into the Control Logic block. The data lines are automatically tristated regardless of the state of the $\overline{OE}$ input signal. This allows the external logic to present the data on DQs and DQP_X.

On the next clock rise the data presented to DQs and DQP_X (or a subset for Byte Write operations, see Truth Table for Read/Write on page 9 for details) inputs is latched into the device and the write is complete. Additional accesses (read/write/deselect) can be initiated on this cycle.

The data written during the write operation is controlled by $\overline{BW}_X$ signals. The CY7C1471BV25, provides Byte Write capability that is described in the Truth Table for Read/Write on page 9. The input $\overline{WE}$ with the selected $\overline{BW}_x$ input selectively writes to only the desired bytes. Bytes not selected during a Byte Write operation remain unaltered. A synchronous self timed write mechanism is provided to simplify the write operations. Byte Write capability is included to greatly simplify read/modify/write sequences, which can be reduced to simple byte write operations.

Because the CY7C1471BV25, is common I/O devices, data must not be driven into the device while the outputs are active. The $\overline{OE}$ can be deasserted HIGH before presenting data to the DQs and DQP_X inputs. This tristates the output drivers. As a safety precaution, DQs and DQP_X are automatically tristated during the data portion of a write cycle, regardless of the state of $\overline{OE}$.

Burst Write Accesses

The CY7C1471BV25, has an on-chip burst counter that makes it possible to supply a single address and conduct up to four Write operations without reasserting the address inputs. Drive ADV/LD LOW to load the initial address, as described in Single Write Accesses on page 6. When ADV/LD is driven HIGH on the subsequent clock rise, the Chip Enables ($\overline{CE}_1$, CE_2, and $\overline{CE}_3$) and $\overline{WE}$ inputs are ignored and the burst counter is incremented. You must drive the correct $\overline{BW}_X$ inputs in each cycle of the Burst Write to write the correct data bytes.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. You must select the device before entering the “sleep” mode. $\overline{CE}_1$, CE_2, and $\overline{CE}_3$, must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

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Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	ZZ ≥ V_{DD} – 0.2 V	–	120	mA
t_{ZZS}	Device operation to ZZ	ZZ ≥ V_{DD} – 0.2 V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ ≤ 0.2 V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0	–	ns

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Truth Table

The truth table for CY7C1471BV25 follows. [1, 2, 3, 4, 5, 6, 7]

Operation	Address Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	ADV/$\overline{LD}$	$\overline{WE}$	$\overline{BW_X}$	$\overline{OE}$	$\overline{CEN}$	CLK	DQ
Deselect Cycle	None	H	X	X	L	L	X	X	X	L	L->H	Tristate
Deselect Cycle	None	X	X	H	L	L	X	X	X	L	L->H	Tristate
Deselect Cycle	None	X	L	X	L	L	X	X	X	L	L->H	Tristate
Continue Deselect Cycle	None	X	X	X	L	H	X	X	X	L	L->H	Tristate
Read Cycle (Begin Burst)	External	L	H	L	L	L	H	X	L	L	L->H	Data Out (Q)
Read Cycle (Continue Burst)	Next	X	X	X	L	H	X	X	L	L	L->H	Data Out (Q)
NOP/Dummy Read (Begin Burst)	External	L	H	L	L	L	H	X	H	L	L->H	Tristate
Dummy Read (Continue Burst)	Next	X	X	X	L	H	X	X	H	L	L->H	Tristate
Write Cycle (Begin Burst)	External	L	H	L	L	L	L	L	X	L	L->H	Data In (D)
Write Cycle (Continue Burst)	Next	X	X	X	L	H	X	L	X	L	L->H	Data In (D)
NOP/Write Abort (Begin Burst)	None	L	H	L	L	L	L	H	X	L	L->H	Tristate
Write Abort (Continue Burst)	Next	X	X	X	L	H	X	H	X	L	L->H	Tristate
Ignore Clock Edge (Stall)	Current	X	X	X	L	X	X	X	X	H	L->H	–
Sleep Mode	None	X	X	X	H	X	X	X	X	X	X	Tristate

Notes

1. X = "Don't Care." H = Logic HIGH, L = Logic LOW. $\overline{BW_X}$ = L signifies at least one Byte Write Select is active, $\overline{BW_X}$ = Valid signifies that the desired Byte Write Selects are asserted, see Truth Table for Read/Write on page 9 for details.
2. Write is defined by $\overline{BW_X}$, and $\overline{WE}$. See Truth Table for Read/Write on page 9.
3. When a write cycle is detected, all IOs are tristated, even during byte writes.
4. The DQs and DQP_X pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
5. $\overline{CEN}$ = H, inserts wait states.
6. Device powers up deselected with the IOs in a tristate condition, regardless of $\overline{OE}$.
7. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQs and DQP_X = tristate when $\overline{OE}$ is inactive or when the device is deselected, and DQs and DQP_X = data when $\overline{OE}$ is active.

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Truth Table for Read/Write

The read-write truth table for CY7C1471BV25 follows. [8, 9, 10]

Function	$\overline{WE}$	$\overline{BW_A}$	$\overline{BW_B}$	$\overline{BW_C}$	$\overline{BW_D}$
Read	H	X	X	X	X
Write No bytes written	L	H	H	H	H
Write Byte A – (DQ_A and DQP_A)	L	L	H	H	H
Write Byte B – (DQ_B and DQP_B)	L	H	L	H	H
Write Byte C – (DQ_C and DQP_C)	L	H	H	L	H
Write Byte D – (DQ_D and DQP_D)	L	H	H	H	L
Write All Bytes	L	L	L	L	L

Notes
8. X = “Don't Care.” H = Logic HIGH, L = Logic LOW. $\overline{BW}_X$ = L signifies at least one Byte Write Select is active, $\overline{BW}_X$ = Valid signifies that the desired Byte Write Selects are asserted, see Truth Table for Read/Write on page 9 for details.
9. Write is defined by $\overline{BW}_X$, and $\overline{WE}$. See Truth Table for Read/Write on page 9.
10. This table is only a partial listing of the byte write combinations. Any combination of $\overline{BW}_X$ is valid. Appropriate write is based on which byte write is active.

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Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{DD} Relative to GND .....–0.5 V to +3.6 V

Supply Voltage on V_{DDQ} Relative to GND .... –0.5 V to +V_{DD}

DC Voltage Applied to Outputs in tristate .....–0.5 V to V_{DDQ} + 0.5 V

DC Input Voltage .....–0.5 V to V_{DD} + 0.5 V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Industrial	–40 °C to +85 °C	2.5 V – 5% / + 5%	2.5 V – 5% to V_{DD}

Electrical Characteristics

Over the Operating Range

Parameter [11, 12]	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power Supply Voltage			2.375	2.625	V
V_{DDQ}	I/O Supply Voltage	For 2.5 V I/O		2.375	V_{DD}	V
V_{OH}	Output HIGH Voltage	For 2.5 V I/O, I_{OH} = –1.0 mA		2.0	–	V
V_{OL}	Output LOW Voltage	For 2.5 V I/O, I_{OL}= 1.0 mA		–	0.4	V
V_{IH}	Input HIGH Voltage [11]	For 2.5 V I/O		1.7	V_{DD} + 0.3 V	V
V_{IL}	Input LOW Voltage [11]	For 2.5 V I/O		–0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30	–	µA
		Input = V_{DD}		–	5	µA
	Input Current of ZZ	Input = V_{SS}		–5	–	µA
		Input = V_{DD}		–	30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled		–5	5	µA
I_{DD} [13]	V_{DD} Operating Supply Current	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	6.5 ns cycle, 133 MHz	–	305	mA
I_{SB1}	Automatic CE Power Down Current – TTL Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}, inputs switching	6.5 ns cycle, 133 MHz	–	170	mA
I_{SB2}	Automatic CE Power Down Current – CMOS Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≤ 0.3 V or V_{IN} ≥ V_{DD} – 0.3 V, f = 0, inputs static	6.5 ns cycle, 133 MHz	–	120	mA
I_{SB3}	Automatic CE Power Down Current – CMOS Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≤ 0.3 V or V_{IN} ≥ V_{DDQ} – 0.3 V, f = f_{MAX}, inputs switching	6.5 ns cycle, 133 MHz	–	170	mA
I_{SB4}	Automatic CE Power Down Current – TTL Inputs	V_{DD} = Max, Device Deselected, V_{IN} ≥ V_{DD} – 0.3 V or V_{IN} ≤ 0.3 V, f = 0, inputs static	6.5 ns cycle, 133 MHz	–	135	mA

Notes

11. Overshoot: $V_{IH(AC)}$ < V_{DD} + 1.5 V (pulse width less than t_{CYC}/2). Undershoot: $V_{IL(AC)}$ > –2 V (pulse width less than t_{CYC}/2).
12. $T_{Power\text{-}up}$: assumes a linear ramp from 0 V to $V_{DD(min)}$ within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.
13. The operation current is calculated with 50% read cycle and 50% write cycle.

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Capacitance

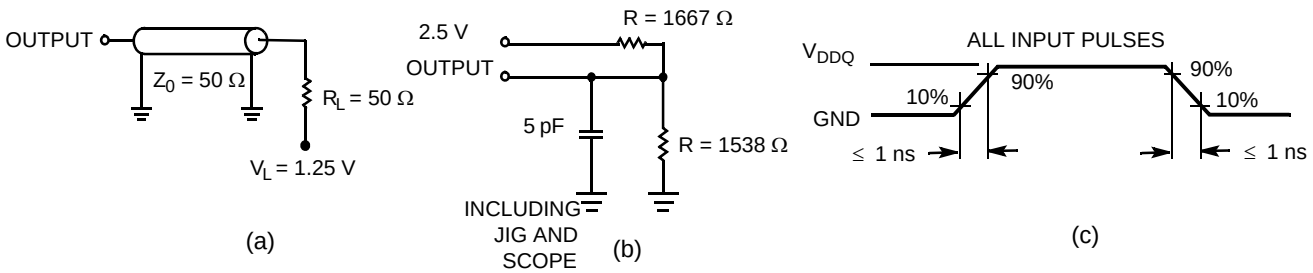
Parameter [14]	Description	Test Conditions	100-pin TQFP Max	Unit
$C_{ADDRESS}$	Address input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 2.5 V, V_{DDQ} = 2.5 V	6	pF
C_{DATA}	Data input capacitance		5	pF
C_{CTRL}	Control input capacitance		8	pF
C_{CLK}	Clock input capacitance		6	pF
C_{IO}	Input-Output capacitance		5	pF

Thermal Resistance

Parameter [14]	Description	Test Conditions	100-pin TQFP Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA/JESD51.	24.63	°C/W
Θ_{JC}	Thermal resistance (junction to case)		2.28	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Note
14. Tested initially and after any design or process change that may affect these parameters.

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Switching Characteristics

Over the Operating Range

Parameter [15, 16]	Description	133 MHz		Unit
		Min	Max	
t_{POWER} [17]		1	–	ms
Clock				
t_{CYC}	Clock Cycle Time	7.5	–	ns
t_{CH}	Clock HIGH	2.5	–	ns
$t_{C]L}$	Clock LOW	2.5	–	ns
Output Times				
t_{CDV}	Data Output Valid After CLK Rise	–	6.5	ns
t_{DOH}	Data Output Hold After CLK Rise	2.5	–	ns
t_{CLZ}	Clock to Low Z [18, 19, 20]	3.0	–	ns
t_{CHZ}	Clock to High Z [18, 19, 20]	–	3.8	ns
t_{OEV}	$\overline{OE}$ LOW to Output Valid	–	3.0	ns
t_{OELZ}	$\overline{OE}$ LOW to Output Low Z [18, 19, 20]	0	–	ns
t_{OEHZ}	$\overline{OE}$ HIGH to Output High Z [18, 19, 20]	–	3.0	ns
Setup Times				
t_{AS}	Address Setup Before CLK Rise	1.5	–	ns
t_{ALS}	ADV/$\overline{LD}$ Setup Before CLK Rise	1.5	–	ns
t_{WES}	$\overline{WE}$, $\overline{BW}_X$ Setup Before CLK Rise	1.5	–	ns
t_{CENS}	$\overline{CEN}$ Setup Before CLK Rise	1.5	–	ns
t_{DS}	Data Input Setup Before CLK Rise	1.5	–	ns
t_{CES}	Chip Enable Setup Before CLK Rise	1.5	–	ns
Hold Times				
t_{AH}	Address Hold After CLK Rise	0.5	–	ns
t_{ALH}	ADV/$\overline{LD}$ Hold After CLK Rise	0.5	–	ns
t_{WEH}	$\overline{WE}$, $\overline{BW}_X$ Hold After CLK Rise	0.5	–	ns
t_{CENH}	$\overline{CEN}$ Hold After CLK Rise	0.5	–	ns
t_{DH}	Data Input Hold After CLK Rise	0.5	–	ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.5	–	ns

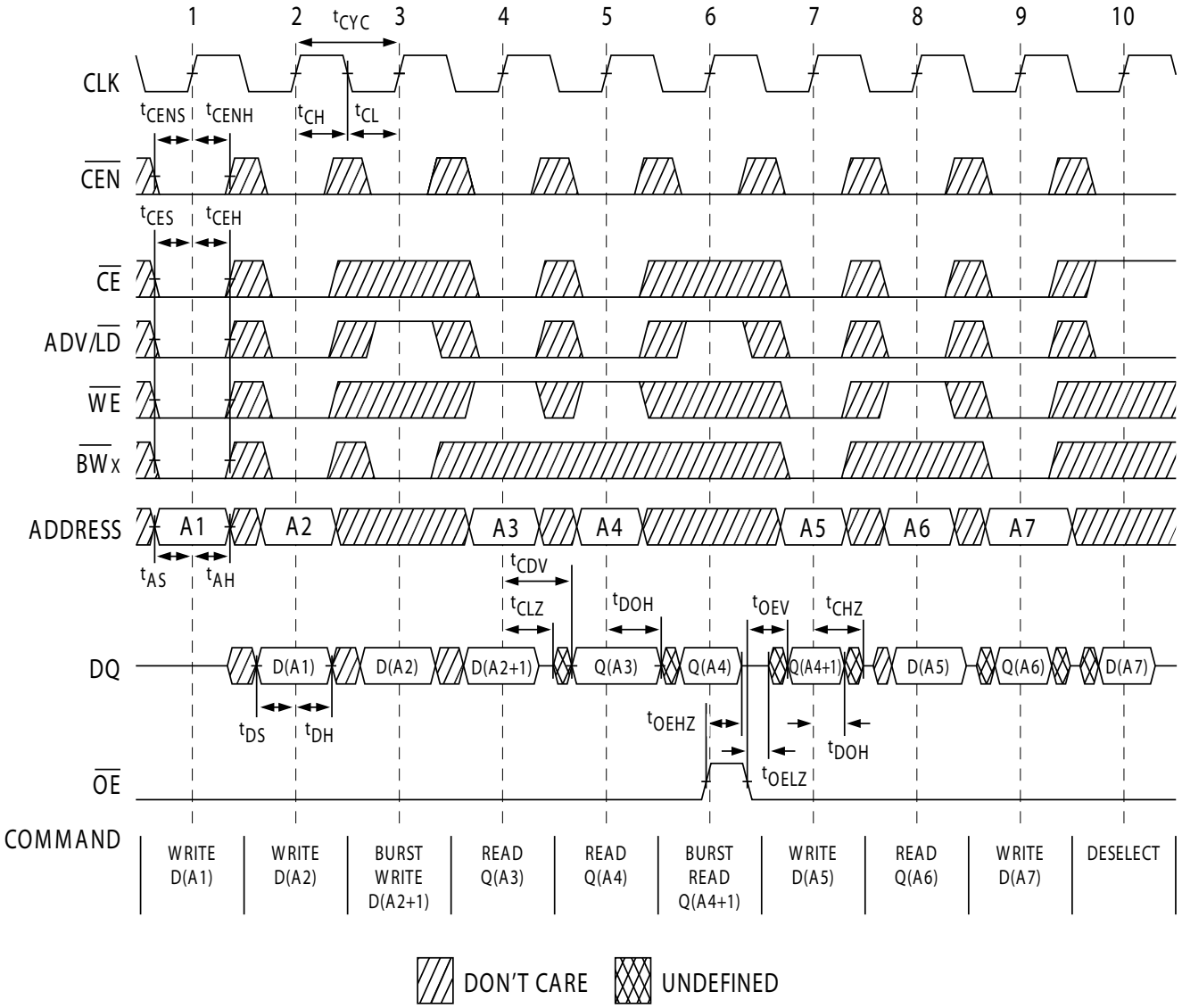
Notes

15. Timing reference level is 1.25 V when V_{DDQ} = 2.5 V.
16. Test conditions shown in (a) of Figure 2 on page 11 unless otherwise noted.
17. This part has a voltage regulator internally; t_{POWER} is the time that the power is supplied above $V_{DD(minimum)}$ initially, before a read or write operation can be initiated.
18. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of Figure 2 on page 11. Transition is measured ±200 mV from steady-state voltage.
19. At any supplied voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High Z before Low Z under the same system conditions.
20. This parameter is sampled and not 100% tested.

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Switching Waveforms

Figure 3. Read/Write Timing [21, 22, 23]

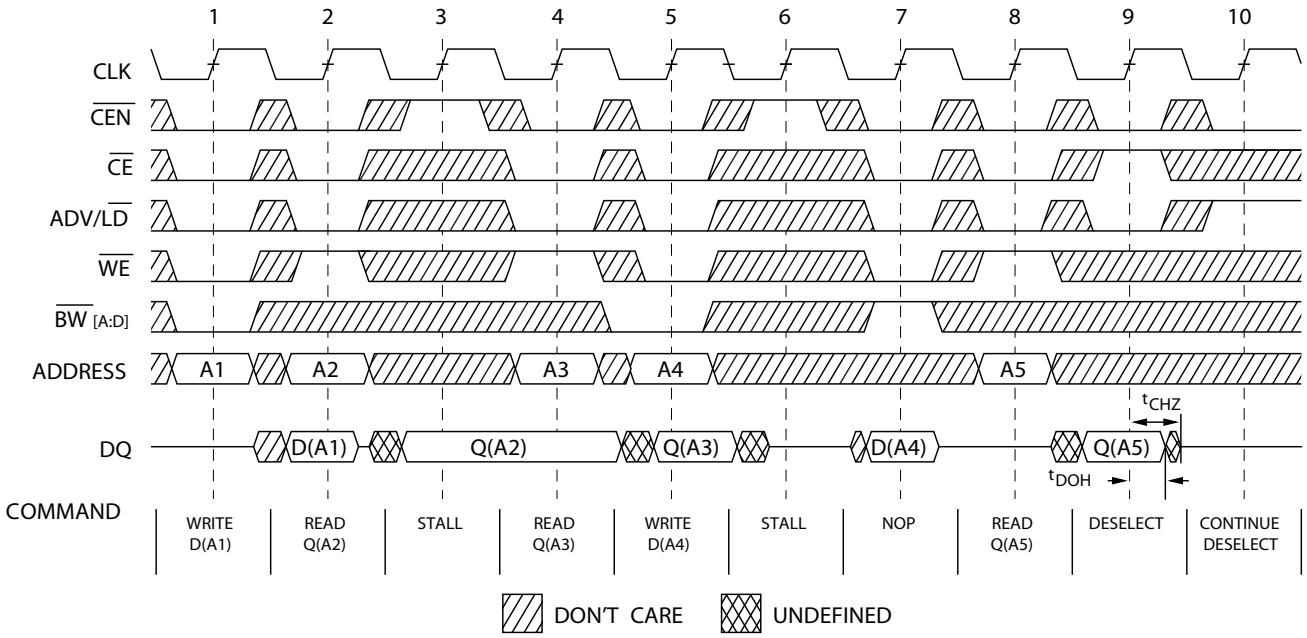


Notes
21. For this waveform ZZ is tied LOW.
22. When $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH, and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH, CE_2 is LOW or $\overline{CE}_3$ is HIGH.
23. Order of the Burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved). Burst operations are optional.

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Switching Waveforms (continued)

Figure 4. NOP, STALL and DESELECT Cycles [24, 25, 26]

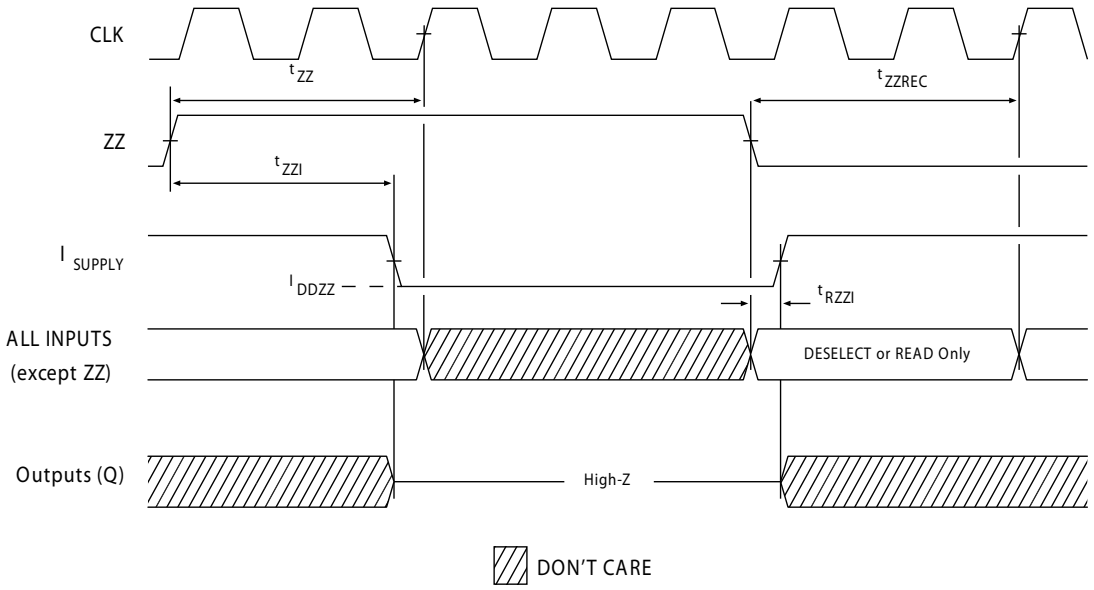


Notes
24. For this waveform ZZ is tied LOW.
25. When $\overline{CE}$ is LOW, $\overline{CE_1}$ is LOW, CE_2 is HIGH, and $\overline{CE_3}$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE_1}$ is HIGH, CE_2 is LOW or $\overline{CE_3}$ is HIGH.
26. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrates $\overline{CEN}$ being used to create a pause. A write is not performed during this cycle.

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Switching Waveforms (continued)

Figure 5. ZZ Mode Timing [27, 28]



Notes
27. Device must be deselected when entering ZZ mode. See Truth Table on page 8 for all possible signal conditions to deselect the device.
28. DQs are in high Z when exiting ZZ sleep mode.

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Ordering Information

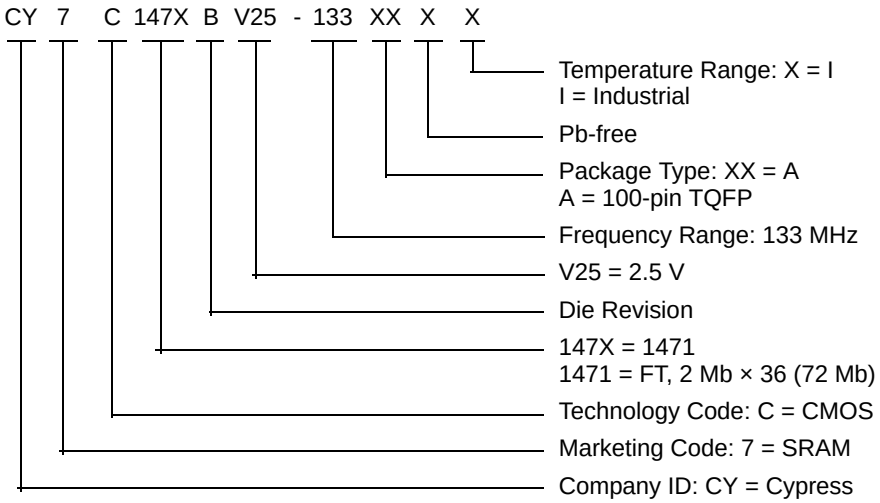
Cypress offers other versions of this type of product in different configurations and features. The following table contains only the list of parts that are currently available.

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Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
133	CY7C1471BV25-133AXI	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Industrial

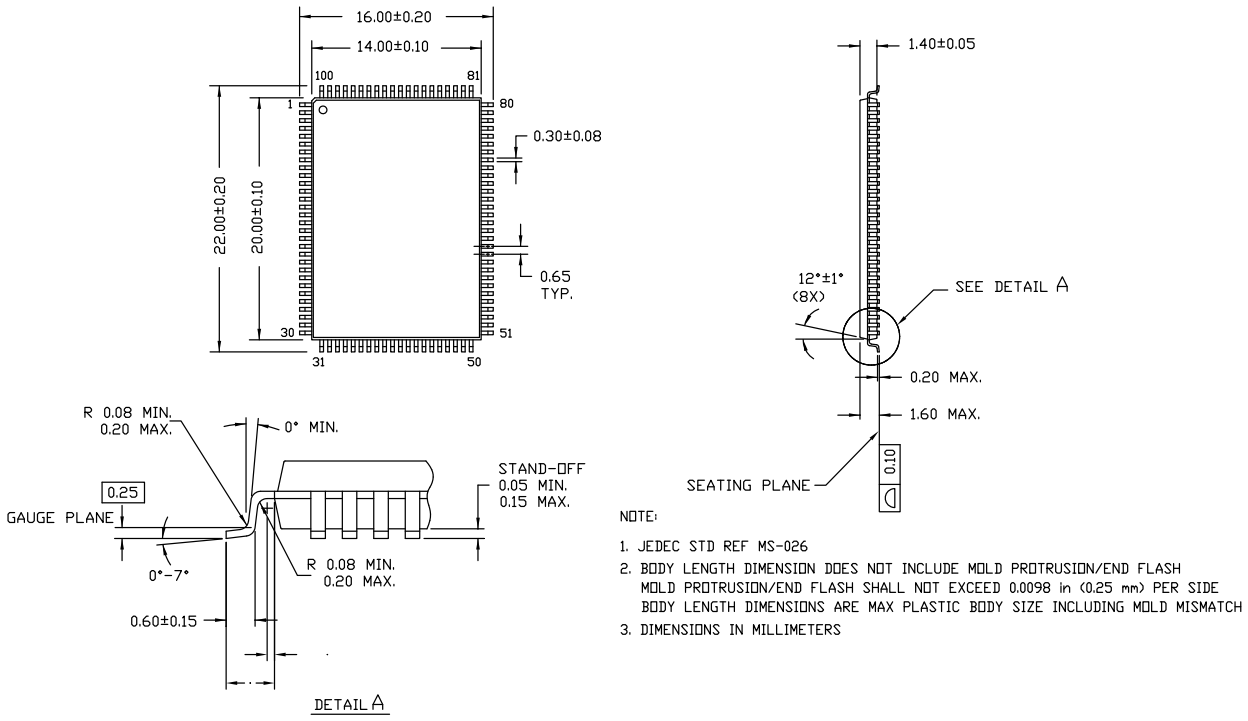
Ordering Code Definitions



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Package Diagrams

Figure 6. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050



51-85050 *E

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Acronyms

Acronym	Description
$\overline{BWS}$	Byte Write Select
CMOS	Complementary Metal Oxide Semiconductor
EIA	Electronic Industries Alliance
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
LSB	Least Significant Bit
MSB	Most Significant Bit
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
MHz	megahertz
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

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Document History Page

Document Title: CY7C1471BV25 72-Mbit (2 M × 36) Flow-Through SRAM with NoBL™ Architecture Document Number: 001-15013				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	1024500	See ECN	VKN / KKVTMP	New data sheet.
*A	1274731	See ECN	VKN / AESA	Updated Switching Waveforms (Corrected typo in the “NOP, STALL and DESELECT Cycles” waveform (Figure 4)).
*B	1562503	See ECN	VKN / AESA	Updated Features (Removed 1.8 V I/O supply information). Updated IEEE 1149.1 Serial Boundary Scan (JTAG) (Removed 1.8 V I/O supply information). Removed the section “1.8 V TAP AC Test Conditions”. Removed the section “1.8 V TAP AC Output Load Equivalent”. Updated TAP DC Electrical Characteristics and Operating Conditions (Removed 1.8 V I/O supply information). Updated Electrical Characteristics (Removed 1.8 V I/O supply information). Updated AC Test Loads and Waveforms (Removed 1.8 V I/O supply information). Updated Switching Characteristics (Removed 1.8 V I/O supply information).
*C	1897447	See ECN	VKN / AESA	Updated Electrical Characteristics (Added Note 13 and referred the same note in I_{DD} parameter).
*D	2082487	See ECN	VKN	Changed status from Preliminary to Final.
*E	2159486	See ECN	VKN / PYRS	Minor Change (Moved to the external web).
*F	2898501	03/24/2010	NJY	Updated Ordering Information (Removed inactive part numbers). Updated Package Diagrams.
*G	3207526	03/28/2011	NJY	Updated Ordering Information (Updated part numbers) and added Ordering Code Definitions. Updated Package Diagrams. Updated in new template.
*H	3256583	05/13/2011	NJY	Added Acronyms and Units of Measure.

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Document History Page (continued)

Document Title: CY7C1471BV25 72-Mbit (2 M × 36) Flow-Through SRAM with NoBL™ Architecture Document Number: 001-15013				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
*I	3544389	03/07/2012	PRIT / NJY	Updated Features (Removed CY7C1473BV25 related information). Updated Functional Description (Removed CY7C1473BV25 related information, removed “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.”). Updated Selection Guide (Removed 100 MHz related information). Removed Logic Block Diagram – CY7C1473BV25. Updated Pin Configurations (Removed CY7C1473BV25 related information). Updated Functional Overview (Removed CY7C1473BV25 related information). Updated Truth Table (Removed CY7C1473BV25 related information). Updated IEEE 1149.1 Serial Boundary Scan (JTAG) (Removed CY7C1471BV25 and CY7C1473BV25 related information). Updated Identification Register Definitions (Removed CY7C1473BV25 related information). Updated Scan Register Sizes (Removed Bit Size (× 36) and Bit Size (× 18) columns). Removed “Boundary Scan Exit Order (2 M × 36)” and “Boundary Scan Exit Order (4 M × 18)”. Updated Electrical Characteristics (Removed 100 MHz related information). Updated Capacitance (Removed 165-ball FBGA package related information). Updated Thermal Resistance (Removed 165-ball FBGA package related information). Updated Switching Characteristics (Removed 100 MHz related information). Updated Ordering Information (Updated part numbers). Updated Package Diagrams. Replaced IO with I/O in all instances across the document.
*J	3564344	03/28/2012	PRIT / NJY	Updated Features (Included 165-ball FBGA package related information). Updated Pin Configurations (Included 165-ball FBGA package related information). Updated IEEE 1149.1 Serial Boundary Scan (JTAG) (Included CY7C1471BV25 related information). Updated Identification Register Definitions (Included CY7C1471BV25 related information). Updated Scan Register Sizes (Included 165-ball FBGA package related information, included Bit Size (× 36) column). Included Boundary Scan Exit Order. Updated Operating Range (Included Commercial Temperature range). Updated Capacitance (Included 165-ball FBGA package related information). Updated Thermal Resistance (Included 165-ball FBGA package related information). Updated Ordering Information (Updated part numbers). Updated Package Diagrams.
*K	4396347	06/02/2014	PRIT	Updated Package Diagrams: spec 51-85050 – Changed revision from *D to *E. spec 51-85167 – Changed revision from *B to *C. Updated to new template. Completing Sunset Review.
*L	4575272	11/20/2014	PRIT	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*M	4785434	06/03/2015	PRIT	Updated Ordering Information (Updated part numbers). Updated Package Diagrams: Spec 51-85165 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.

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Document Title: CY7C1471BV25 72-Mbit (2 M × 36) Flow-Through SRAM with NoBL™ Architecture Document Number: 001-15013				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
*N	5267388	05/11/2016	PRIT	Removed references to obsolete devices. Updated the template.

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