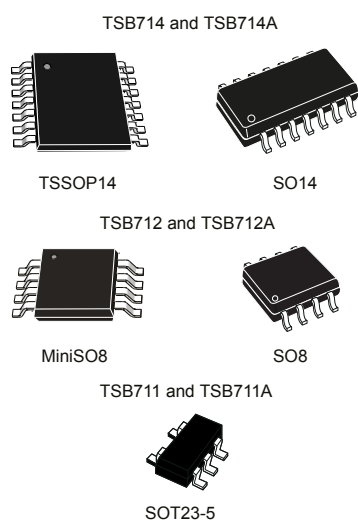


Precision rail-to-rail input / output 36 V, 6 MHz op-amps



Features

- Rail-to-rail input and output
- Low offset voltage: 300 μ V maximum
- Wide supply voltage range: 2.7 V to 36 V
- Gain bandwidth product: 6 MHz
- Slew rate : 3 V/ μ s
- Low noise : 12 nV/ $\sqrt{\text{Hz}}$
- Integrated EMI filter
- 2 kV HBM ESD tolerance
- Extended temperature range : -40 °C to +125 °C
- Automotive-grade available

Applications

- High-side and low-side current sensing
- Hall effect sensors
- Data acquisition and instrumentation
- Test and measurement equipments
- Motor control
- Industrial process control
- Strain gauge

Description

The TSB711, TSB711A, TSB712, TSB712A, TSB714 and TSB714A 6 MHz bandwidth amplifiers feature rail-to-rail input and output, which is guaranteed to operate from +2.7 V to +36 V single supply as well as from ± 1.35 V to ± 18 V dual supplies.

These amplifiers have the advantage of offering a large span of supply voltage and an excellent input offset voltage of 300 μ V maximum at 25 °C.

The combination of wide bandwidth, slew rate, low noise, rail-to-rail capability and precision makes the TSB711, TSB711A, TSB712, TSB712A, TSB714 and TSB714A useful in a wide variety of applications such as: filters, power supply and motor control, actuator driving, hall effect sensors and resistive transducers.

Maturity status link

TSB711, TSB711A, TSB712, TSB712A,
TSB714, TSB714A

Related products

TSB571,
TSB572

Single, Dual op-amps for
the low-power consumption
version (380 μ A with
2.5 MHz GBP)

1 Pin description

Figure 1. TSB711 pin connections (top view)

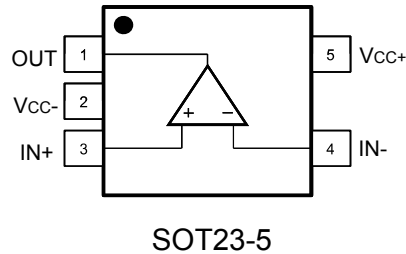


Table 1. TSB711 pin description (SOT23-5)

Pin n°	Pin name	Description
1	OUT	Output channel
2	V _{CC-}	Negative supply voltage
3	IN1+	Non-inverting input channel
4	IN-	Inverting input channel
5	V _{CC+}	Positive supply voltage

Figure 2. TSB712 pin connections (top view)

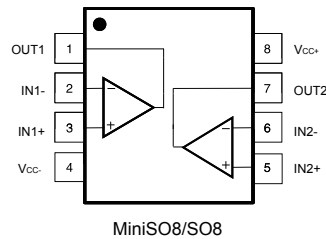
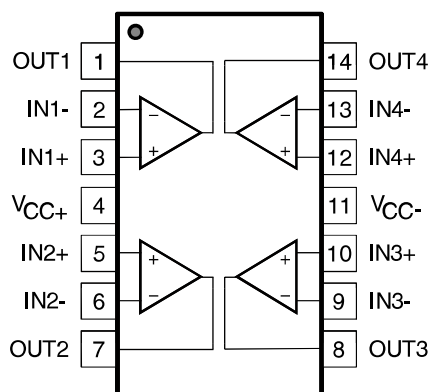


Table 2. TSB712 pin description (miniSO8/SO8)

Pin n°	Pin name	Description
1	OUT1	Output channel 1
2	IN1-	Inverting input channel 1
3	IN1+	Non-inverting input channel 1
4	V _{CC-}	Negative supply voltage
5	IN2+	Non-inverting input channel 2
6	IN2-	Inverting input channel 2
7	OUT2	Output channel 2
8	V _{CC+}	Positive supply voltage

Figure 3. TSB714 pin connections (top view)

Table 3. TSB714 pin description

Pin n°	Pin name	Description
1	OUT1	Output channel 1
2	IN1-	Inverting input channel 1
3	IN1+	Non-inverting input channel 1
4	V _{CC} +	Positive supply voltage
5	IN2+	Non-inverting input channel 2
6	IN2-	Inverting input channel 2
7	OUT2	Output channel 2
8	OUT3	Output channel 3
9	IN3-	Inverting input channel 3
10	IN3+	Non-inverting input channel 3
11	V _{CC} -	Negative supply voltage
12	IN4+	Non-inverting input channel 4
13	IN4-	Inverting input channel 4
14	OUT4	Output channel 4

2 Absolute maximum ratings and operating conditions

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage ⁽¹⁾	+40 or ± 20	V
V_{id}	Input voltage differential ⁽²⁾	± 2	V
V_{in}	Input voltage	$(V_{CC-}) - 0.2$ to $(V_{CC+}) + 0.2$	V
I_{in}	Input current ⁽³⁾	± 10	mA
	Storage temperature	-65 to +150	°C
R_{th-ja}	Thermal resistance junction-to-ambient ^{(4) (5)}		°C / W
	MiniSO-8	190	
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model ⁽⁶⁾	2	kV
	CDM: charged device model ⁽⁷⁾	1	kV
	Latch-up immunity	100	mA

1. All voltage values, except the differential voltage are with respect to the network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal. The maximum input voltage differential value may be extended to the condition that the input current is limited to ± 10 mA. See [Section 5.2 Input pin voltage range](#).
3. Input current must be limited by a resistor in series with the inputs when the input voltage is beyond the rails (see [Section 5.2 Input pin voltage range](#)).
4. Short-circuits can cause excessive heating and destructive dissipation.
5. R_{th} are typical values.
6. Human body according to JEDEC standard JESD22-A114F.
7. According to ANSI/ESD STM5.3.1.

Table 5. Operating conditions

Symbol	Parameter	Value
V_{CC}	Supply voltage	2.7 V to 36 V
V_{icm}	Common mode input voltage range	(V_{CC-}) to $(V_{CC+}) + 0.1$ V
T_{oper}	Operating free air temperature range	-40 °C to +125 °C

3 Electrical characteristics

Table 6. Electrical characteristics at $V_{CC} = 36\text{ V}$, $V_{ICM} = V_{OUT} = V_{CC} / 2$, $T_{amb} = 25\text{ °C}$ and R_L connected to $V_{CC} / 2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	TSB711A, TSB712A, $T = 25\text{ °C}$, $V_{CC-} \leq V_{ICM} \leq V_{CC+} - 1.5\text{ V}$			± 300	μV
		TSB711A, TSB712A, $T = 25\text{ °C}$, $V_{CC-} \leq V_{ICM} \leq V_{CC+}$			± 650	
		TSB711A, TSB712A, $-40\text{ °C} < T < 125\text{ °C}$, $V_{CC-} \leq V_{ICM} \leq V_{CC+} - 1.5\text{ V}$			± 580	
		TSB711A, TSB712A, $-40\text{ °C} < T < 125\text{ °C}$, $V_{CC-} \leq V_{ICM} \leq V_{CC+}$			± 930	
		TSB711, TSB712, $T = 25\text{ °C}$, $V_{CC-} \leq V_{ICM} \leq V_{CC+} - 1.5\text{ V}$			± 800	
		TSB711, TSB712, $T = 25\text{ °C}$, $V_{CC-} \leq V_{ICM} \leq V_{CC+}$			± 1200	
		TSB711, TSB712, $-40\text{ °C} < T < 125\text{ °C}$, $V_{CC-} \leq V_{ICM} \leq V_{CC+} - 1.5\text{ V}$			± 1100	
		TSB711, TSB712, $-40\text{ °C} < T < 125\text{ °C}$, $V_{CC-} \leq V_{ICM} \leq V_{CC+}$			± 1400	
$\Delta V_{io} / \Delta T$	Input offset voltage drift	$-40\text{ °C} < T < 125\text{ °C}$ ⁽¹⁾			2.8	$\mu\text{V} / \text{°C}$
ΔV_{io}	Long-term input offset voltage drift	$T = 25\text{ °C}$ ⁽²⁾		0.57		$\mu\text{V} / \sqrt{\text{mo}}$
I_{IB}	Input bias current ⁽³⁾	$V_{ICM} = V_{CC+}$, $T = 25\text{ °C}$	0		300	nA
		$V_{ICM} = V_{CC+}$, $-40\text{ °C} < T < 125\text{ °C}$	0		900	
		$V_{ICM} = V_{CC-}$, $T = 25\text{ °C}$	-100		0	
		$V_{ICM} = V_{CC-}$, $-40\text{ °C} < T < 125\text{ °C}$	-200		0	
I_{IO}	Input offset current ⁽⁴⁾	$V_{ICM} = V_{CC+}$		10		
		$V_{ICM} = V_{CC-}$		10		
A_{VD}	Open loop gain	$R_L \geq 10\text{ k}\Omega$, $(V_{CC-}) + 0.5\text{ V} \leq V_{OUT} \leq (V_{CC+}) - 0.5\text{ V}$, $T = 25\text{ °C}$	110	125		dB
		$R_L \geq 10\text{ k}\Omega$, $(V_{CC-}) + 0.5\text{ V} \leq V_{OUT} \leq (V_{CC+}) - 0.5\text{ V}$, $-40\text{ °C} < T < 125\text{ °C}$	105			
CMR	Common-mode rejection ratio $20 \log (\Delta V_{INCM} / \Delta V_{IO})$	$(V_{CC-}) \leq V_{ICM} \leq (V_{CC+}) - 1.5\text{ V}$, $T = 25\text{ °C}$	115	130		
		$(V_{CC-}) \leq V_{ICM} \leq (V_{CC+}) - 1.5\text{ V}$, $-40\text{ °C} < T < 125\text{ °C}$	110			
		TSB711A, TSB712A $(V_{CC-}) \leq V_{ICM} \leq (V_{CC+})$	100	120		

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
CMR	Common-mode rejection ratio 20 log (ΔV _{INCM} / ΔV _{IO})	T = 25 °C				dB
		TSB711A,TSB712A (V _{CC-}) ≤ V _{ICM} ≤ (V _{CC+}), -40 °C < T < 125 °C	95			
		TSB711, TSB712 (V _{CC-}) ≤ V _{ICM} ≤ (V _{CC+}), T = 25 °C	90	120		
		TSB711 , TSB712 (V _{CC-}) ≤ V _{ICM} ≤ (V _{CC+}), -40 °C < T < 125 °C	85			
SVR	Power supply rejection ratio 20 log (ΔV _{CC} / ΔV _{IO})	5 V < (V _{CC+}) - (V _{CC-}) < 36 V, V _{ICM} = V _{CC} / 2 -40 °C < T < 125 °C	100	125		
V _{OH}	High level output voltage (drop voltage from V _{CC+})	No load, -40 °C < T < 125 °C			120	mV
		I _{SOURCE} = 2 mA, -40 °C < T < 125 °C			200	
		I _{SOURCE} = 15 mA, -40 °C < T < 125 °C			1000	
V _{OL}	Low level output voltage	No load , -40 °C < T < 125 °C			120	mV
		I _{SINK} = 2 mA, -40 °C < T < 125 °C			200	
		I _{SINK} = 15 mA , -40 °C < T < 125 °C			1000	
I _{OUT}	I _{SINK}	V _{OUT} = V _{CC} , T = 25 °C	25	50		mA
		V _{OUT} = V _{CC} , -40 °C < T < 125 °C	20			
	I _{SOURCE}	V _{OUT} = 0 V, T = 25 °C	25	50		
		V _{OUT} = 0 V, -40 °C < T < 125 °C	20			
I _{CC}	Supply current by op-amp	No load, T = 25 °C		1.8		mA
		No load, -40 °C < T < 125 °C			3	
AC performance						
GBP	Gain bandwidth product	R _L = 10 kΩ, C _L = 100 pF	4.5	6		MHz
SR	Slew rate	9 V step, R _L = 10 kΩ, C _L = 100 pF, A _V = 1 V/V, 10% to 90%	2.2	3		V / μs
THD+N	Total harmonic distortson + noise	V _{IN} = 1 Vrms , R _L = 10 kΩ, A _V = +1, f = 1 kHz, BW = 22 kHz		0,0003		%
		V _{IN} = 1 Vrms , R _L = 1 kΩ, A _V = +1, f = 1 kHz, BW = 22 kHz		0,00034		
CR	Crosstalk	V _{OUT} = 5 Vpp, f = 1 kHz, A _V = +11, R _L = 10 kΩ		125		dB
		V _{OUT} = 5Vpp, f = 10 kHz, A _V = +11, R _L = 10 kΩ		100		
Φ _m	Phase margin	At unity gain, 25 °C, 10 kΩ, 100 pF		45		°
C _{LOAD}	Capacitive load drive		100 ⁽⁵⁾			pF
e _n	Input voltage noise density	f = 10 Hz		20		nV / √Hz
		f = 100 Hz		13		
		f = 10 kHz		12		
e _{n p-p}	Input noise voltage	0.1 Hz ≤ f ≤ 10 Hz		0.5		μV _{PP}

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
i_n	Input current noise density	$f = 1 \text{ kHz}$		0.15 ⁽⁶⁾		pA / $\sqrt{\text{Hz}}$

1. See [Section 5.4 Input offset voltage drift over the temperature](#) in application information.
2. Typical value is based on the V_{IO} drift observed after 1000 h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration. See [Section 5.5 Long term input offset voltage drift](#).
3. Current is positive when it is sunk into the op-amp.
4. I_{IO} is defined as $|I_{ibp} - I_{ibn}|$
5. For higher capacitive values see [Figure 26. Phase margin vs. output current at \$V_{CC} = 36 \text{ V}\$](#) , [Figure 27. Phase margin vs. capacitive load and Figure 28. Overshoot vs. capacitive load at \$V_{CC} = 36 \text{ V}\$](#)
6. Theoretical value of the input current noise density based on the measurement of the input transistor base current:

$$i_n = \sqrt{2 \cdot q \cdot I_b}$$

Table 7. Electrical characteristics at $V_{CC} = 5\text{ V}$, $V_{ICM} = V_{OUT} = V_{CC} / 2$, $T_{amb} = 25\text{ °C}$ and R_L connected to $V_{CC} / 2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{IO}	Input offset voltage	TSB711A, TSB712A, $T = 25\text{ °C}$, $V_{CC-} \leq V_{ICM} \leq V_{CC+} - 1.5\text{ V}$			± 350	μV
		TSB711A, TSB712A, $T = 25\text{ °C}$, $V_{CC-} \leq V_{ICM} \leq V_{CC+}$			± 650	
		TSB711A, TSB712A, $-40\text{ °C} < T < 125\text{ °C}$, $V_{CC-} \leq V_{ICM} \leq V_{CC+} - 1.5\text{ V}$			± 750	
		TSB711A, TSB712A, $-40\text{ °C} < T < 125\text{ °C}$, $V_{CC-} \leq V_{ICM} \leq V_{CC+}$			± 1050	
		TSB711, TSB712, $T = 25\text{ °C}$, $V_{CC-} \leq V_{ICM} \leq V_{CC+} - 1.5\text{ V}$			± 800	
		TSB711, TSB712, $T = 25\text{ °C}$, $V_{CC-} \leq V_{ICM} \leq V_{CC+}$			± 1200	
		TSB711, TSB712, $-40\text{ °C} < T < 125\text{ °C}$, $V_{CC-} \leq V_{ICM} \leq V_{CC+} - 1.5\text{ V}$			± 1100	
		TSB711, TSB712, $-40\text{ °C} < T < 125\text{ °C}$, $V_{CC-} \leq V_{ICM} \leq V_{CC+}$			± 1400	
$\Delta V_{IO} / \Delta T$	Input offset voltage drift	$-40\text{ °C} < T < 125\text{ °C}$ ⁽¹⁾			4	$\mu\text{V} / \text{°C}$
I_{IB}	Input bias current ⁽²⁾	$V_{ICM} = V_{CC+}$, $T = 25\text{ °C}$	0		300	nA
		$V_{ICM} = V_{CC+}$, $-40\text{ °C} < T < 125\text{ °C}$	0		900	
		$V_{ICM} = V_{CC-}$, $T = 25\text{ °C}$	-100		0	
		$V_{ICM} = V_{CC-}$, $-40\text{ °C} < T < 125\text{ °C}$	-200		0	
I_{IO}	Input offset current ⁽³⁾	$V_{ICM} = V_{CC+}$		10		
		$V_{ICM} = V_{CC-}$		10		
A_{VD}	Open loop gain	$R_L \geq 10\text{ k}\Omega$, $(V_{CC-}) + 0.5\text{ V} \leq V_{OUT} \leq (V_{CC+}) - 0.5\text{ V}$, $T = 25\text{ °C}$	105	120		dB
		$R_L \geq 10\text{ k}\Omega$, $(V_{CC-}) + 0.5\text{ V} \leq V_{OUT} \leq (V_{CC+}) - 0.5\text{ V}$, $-40\text{ °C} < T < 125\text{ °C}$	100			
CMR	Common-mode rejection ratio $20 \log (\Delta V_{INCM} / \Delta V_{IO})$	$(V_{CC-}) \leq V_{ICM} \leq (V_{CC+}) - 1.5\text{ V}$, $T = 25\text{ °C}$	95	125		dB
		$(V_{CC-}) \leq V_{ICM} \leq (V_{CC+}) - 1.5\text{ V}$, $-40\text{ °C} < T < 125\text{ °C}$	90			
		TSB711A, TSB712A $(V_{CC-}) \leq V_{ICM} \leq (V_{CC+})$, $T = 25\text{ °C}$	80	105		
		TSB711A, TSB712A $(V_{CC-}) \leq V_{ICM} \leq (V_{CC+})$, $-40\text{ °C} < T < 125\text{ °C}$	75			
		TSB711, TSB712 $(V_{CC-}) \leq V_{ICM} \leq (V_{CC+})$,	75	105		

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
CMR	Common-mode rejection ratio 20 log (ΔV _{INCM} / ΔV _{IO})	T = 25 °C				dB
		TSB711, TSB712 (V _{CC-}) ≤ V _{ICM} ≤ (V _{CC+}), -40 °C < T < 125 °C	70			
V _{OH}	High level output voltage (drop voltage from VCC+)	No load, -40 °C < T < 125 °C			90	mV
		I _{SOURCE} = 2 mA, -40 °C < T < 125 °C			200	
V _{OL}	Low level output voltage	No load, -40 °C < T < 125 °C			90	mV
		I _{SINK} = 2 mA, -40 °C < T < 125 °C			200	
I _{OUT}	I _{SINK}	V _{OUT} = V _{CC} , T = 25 °C	20	50		mA
		V _{OUT} = V _{CC} , -40 °C < T < 125 °C	15			
	I _{SOURCE}	V _{OUT} = 0 V, T = 25 °C	20	50		
		V _{OUT} = 0 V, -40 °C < T < 125 °C	15			
I _{CC}	Supply current by op-amp	No load, T = 25 °C		1.4		mA
		No load, -40 °C < T < 125 °C			2.3	
AC performance						
GBP	Gain bandwidth product	R _L = 10 kΩ, C _L = 100 pF	4.5	6		MHz
SR	Slew rate	3 V step, R _L = 10 kΩ, C _L = 100 pF, A _V = 1 V/V, 10% to 90%	2	2.7		V / μs
THD+N	Total harmonic distorsion + noise	V _{IN} = 1 Vrms , R _L = 10 kΩ, A _V = +1, f = 1 kHz, BW = 22 kHz		0,00032		%
		V _{IN} = 1 Vrms , R _L = 1 kΩ, A _V = +1, f = 1 kHz, BW = 22 kHz		0,0004		
Φ _m	Phase margin	At unity gain, 25 °C, 10 kΩ, 100 pF		34		°
C _{LOAD}	Capacitive load drive		100 ⁽⁴⁾			pF
e _n	Input voltage noise density	f = 10 Hz		20		nV / √Hz
		f = 100 Hz		13		
		f = 10 kHz		12		
e _{n p-p}	Input noise voltage	0.1 Hz ≤ f ≤ 10 Hz		0.8		μV _{PP}
i _n	Input current noise density	f = 1 kHz		0.15 ⁽⁵⁾		pA / √Hz

1. See Section 5.4 Input offset voltage drift over the temperature in application information.
2. Current is positive when it is sinked into the op-amp.
3. I_{IO} is defined as $|I_{\text{ibp}} - I_{\text{ibn}}|$.
4. For higher capacitive values see Figure 25. Phase margin vs. output current at $V_{\text{CC}} = 5 \text{ V}$, Figure 27. Phase margin vs. capacitive load
5. Theoretical value of the input current noise density based on the measurement of the input transistor base current:

$$i_{\text{n}} = \sqrt{2 \cdot q \cdot I_{\text{b}}}$$

4 Typical performance characteristics

R_L connected to $V_{CC} / 2$ (unless otherwise specified).

Figure 4. Supply current vs. supply voltage

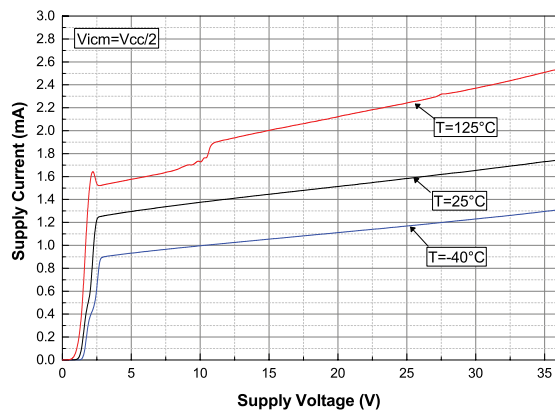


Figure 5. Input offset voltage distribution at $V_{CC} = 5\text{ V}$ TSB711A, TSB712A

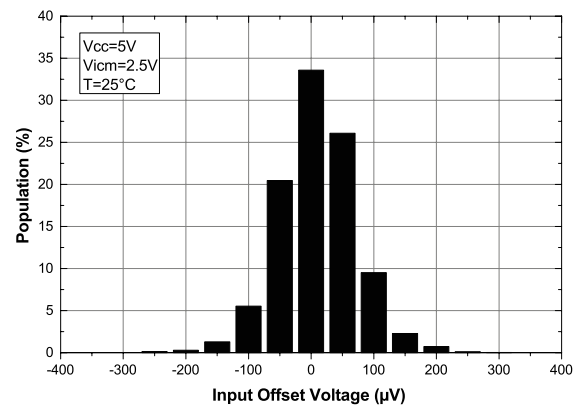


Figure 6. Input offset voltage distribution at $V_{CC} = 36\text{ V}$ TSB711A, TSB712A

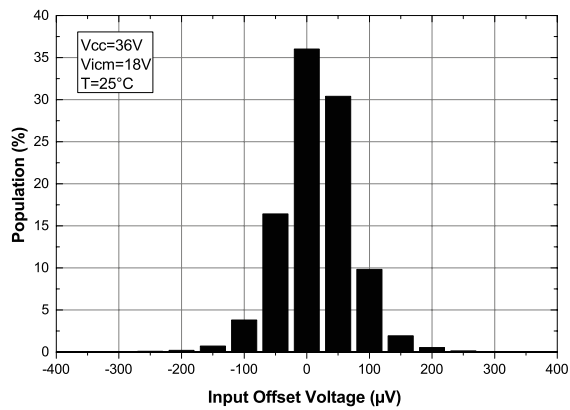


Figure 7. Input offset voltage vs. temperature at $V_{CC} = 5\text{ V}$

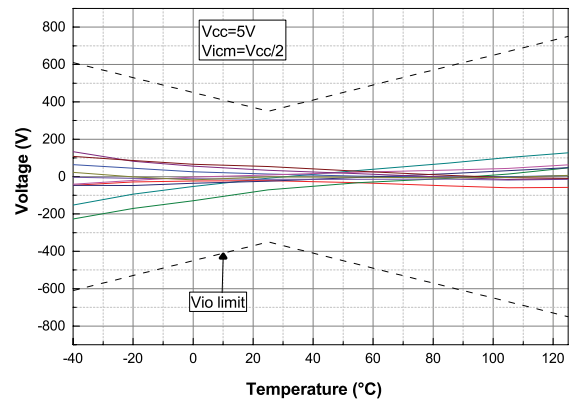


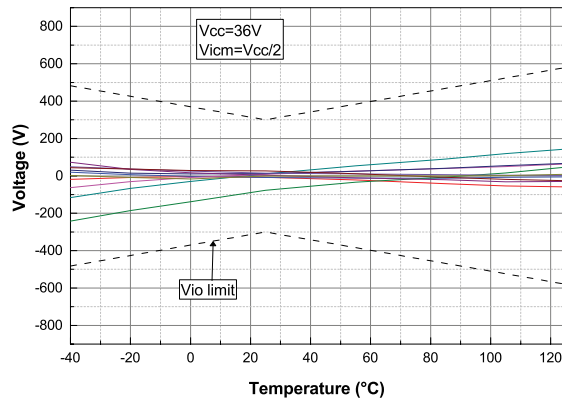
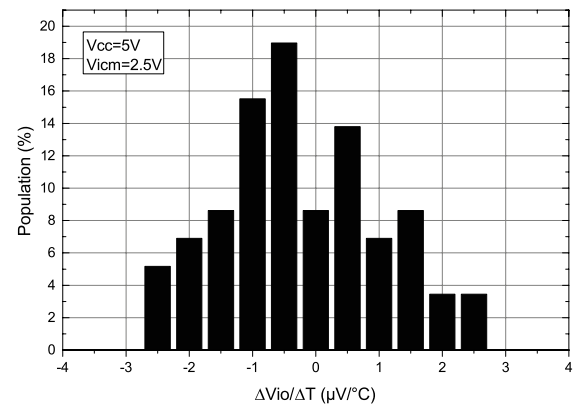
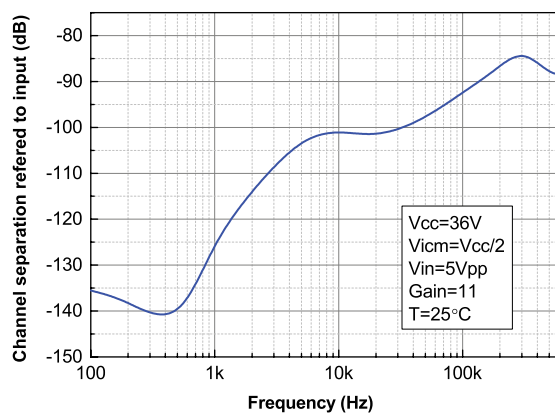
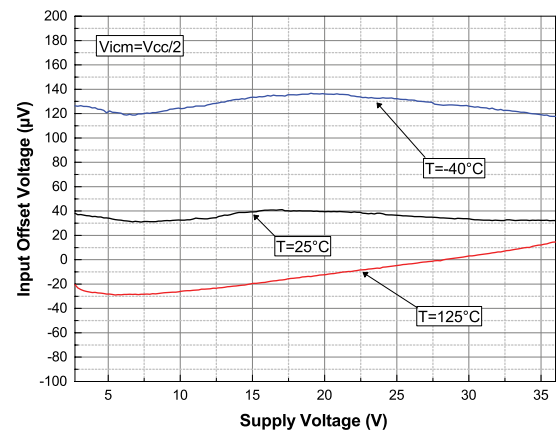
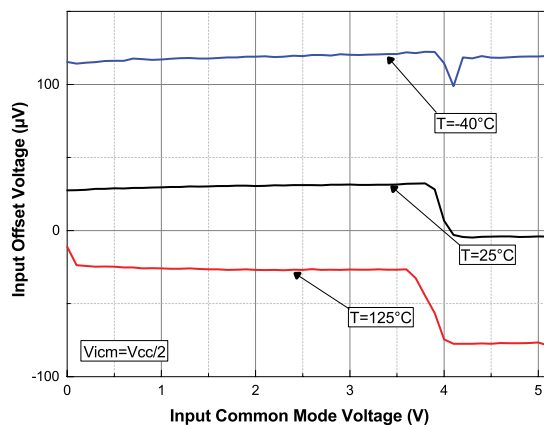
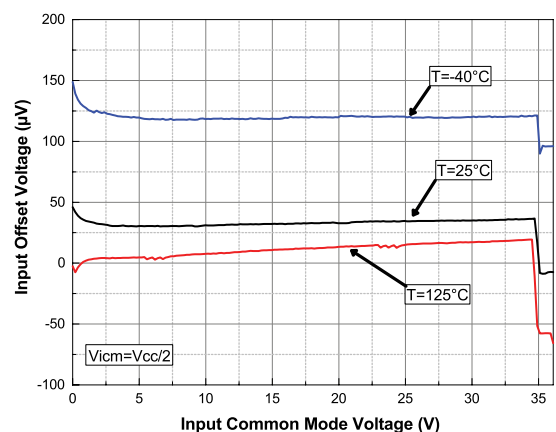
Figure 8. Input offset voltage vs. temperature at $V_{CC} = 36\text{ V}$

Figure 9. Input offset voltage thermal coefficient distribution at $V_{CC} = 5\text{ V}$

Figure 10. Channel separation vs. frequency at $V_{CC} = 36\text{ V}$

Figure 11. Input offset voltage vs. supply voltage

Figure 12. Input offset voltage vs. common mode voltage at $V_{CC} = 5\text{ V}$ TSB711A, TSB712A

Figure 13. Input offset voltage vs. common mode voltage at $V_{CC} = 36\text{ V}$ TSB711A, TSB712A


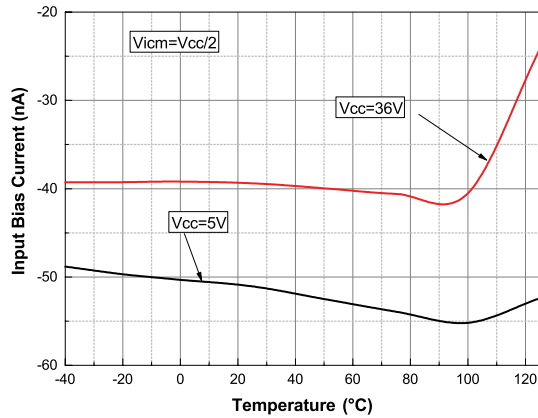
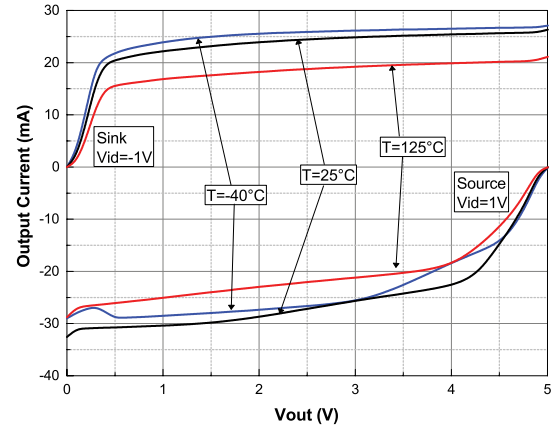
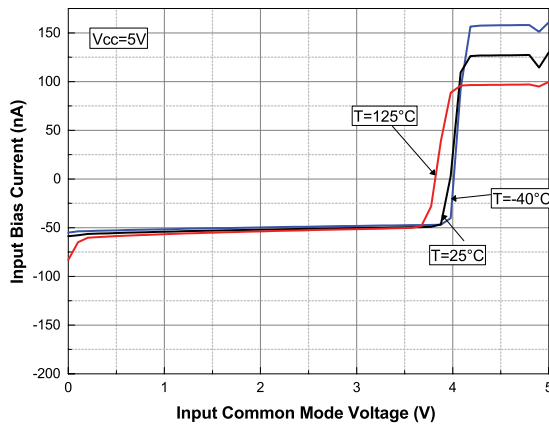
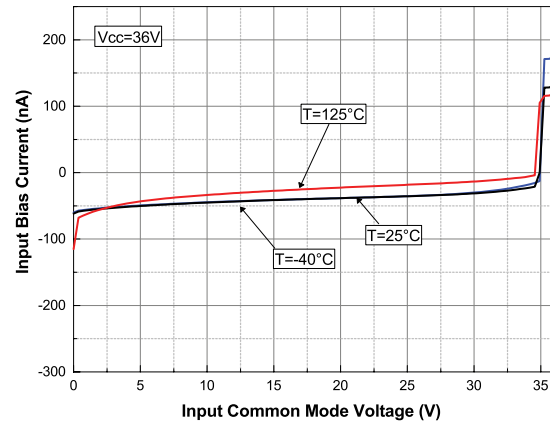
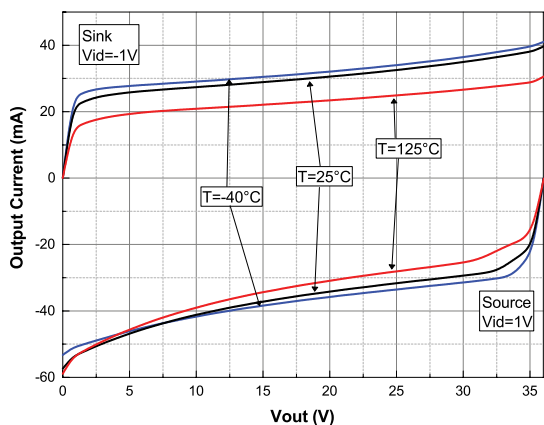
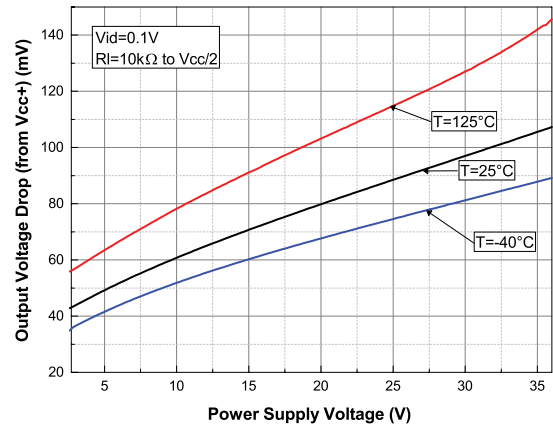
Figure 14. Input bias current vs. temperature at $V_{ICM} = V_{CC} / 2$

Figure 15. Output current vs. output voltage at $V_{CC} = 5\text{ V}$

Figure 16. Input bias current vs. common mode voltage at $V_{CC} = 5\text{ V}$

Figure 17. Input bias current vs. common mode voltage at $V_{CC} = 36\text{ V}$

Figure 18. Output current vs. output voltage at $V_{CC} = 36\text{ V}$

Figure 19. Output voltage (V_{OH}) vs. supply voltage


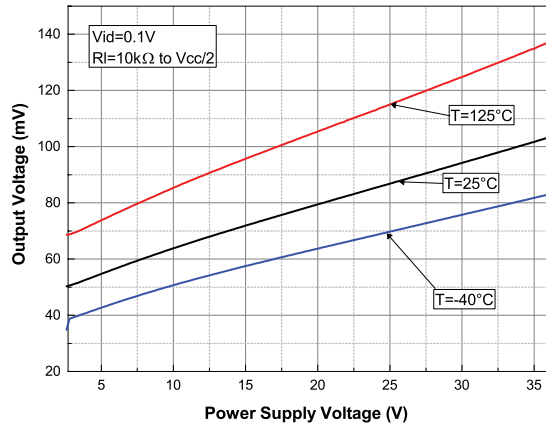
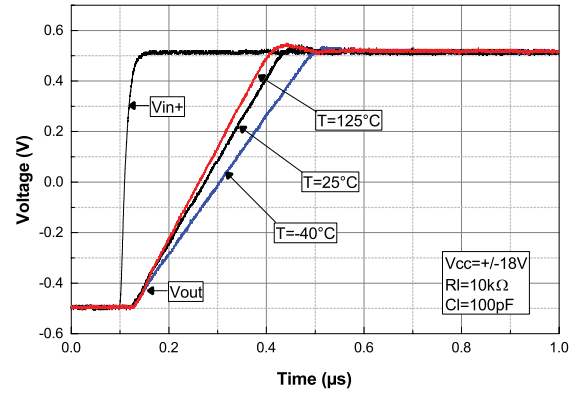
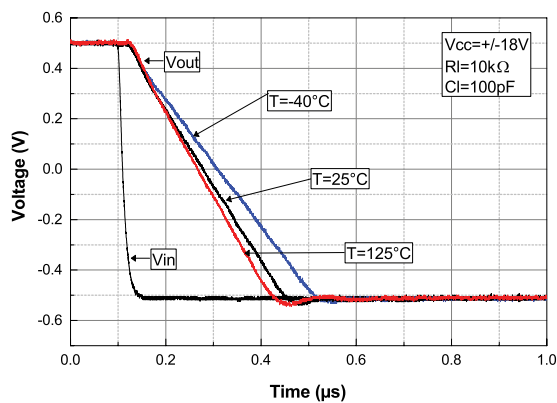
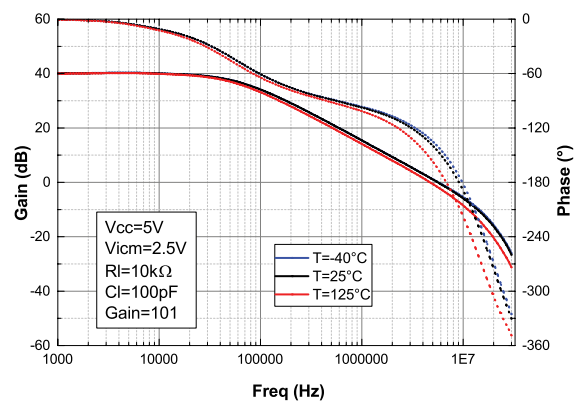
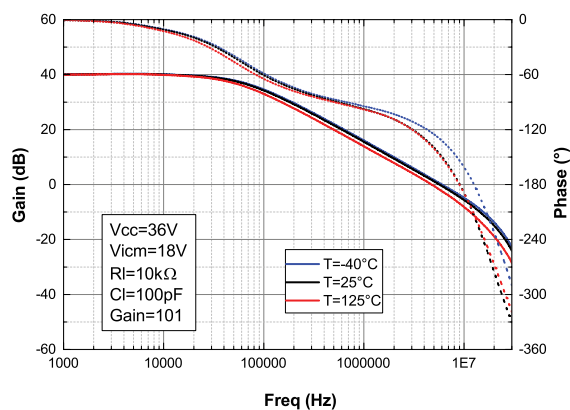
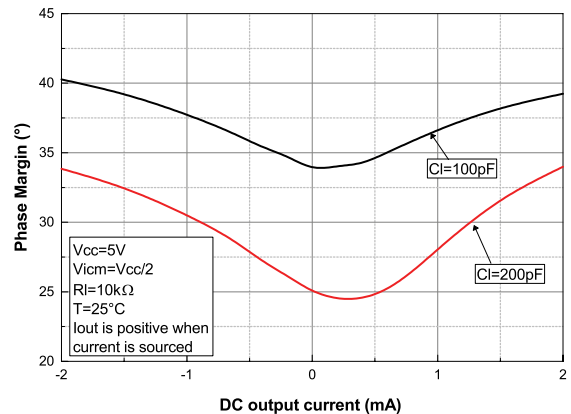
Figure 20. Output voltage (V_{OL}) vs. supply voltage

Figure 21. Positive slew rate at $V_{CC} = 36\text{ V}$

Figure 22. Negative slew rate at $V_{CC} = 36\text{ V}$

Figure 23. Bode diagram at $V_{CC} = 5\text{ V}$

Figure 24. Bode diagram at $V_{CC} = 36\text{ V}$

Figure 25. Phase margin vs. output current at $V_{CC} = 5\text{ V}$


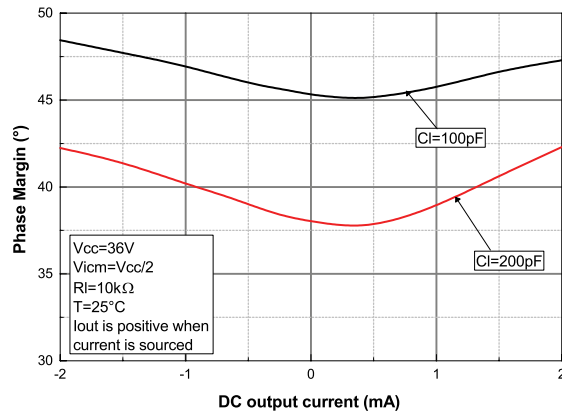
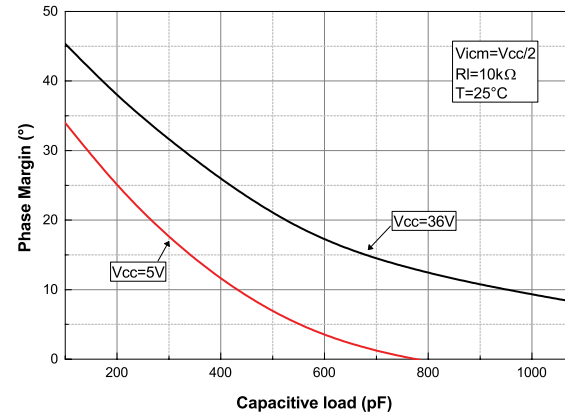
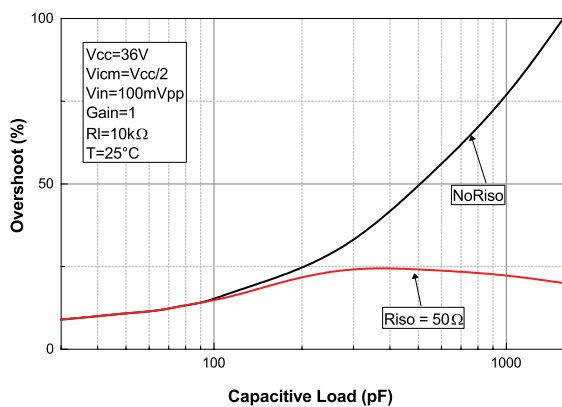
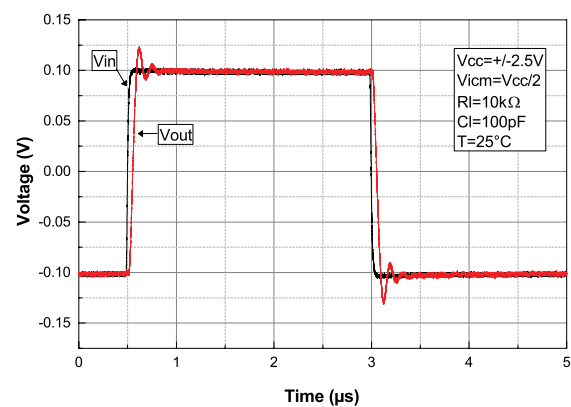
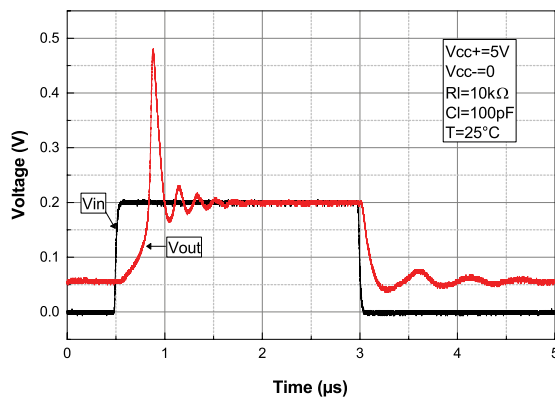
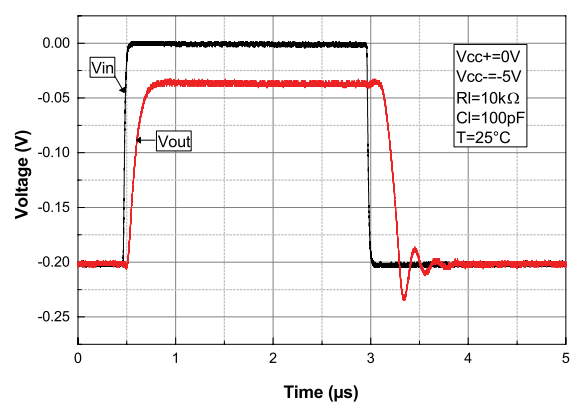
Figure 26. Phase margin vs. output current at $V_{CC} = 36\text{ V}$

Figure 27. Phase margin vs. capacitive load

Figure 28. Overshoot vs. capacitive load at $V_{CC} = 36\text{ V}$

Figure 29. Small step response vs. time at $V_{CC} = 5\text{ V}$

Figure 30. Desaturation time at low rail at $V_{CC} = 5\text{ V}$

Figure 31. Desaturation time at high rail at $V_{CC} = 5\text{ V}$


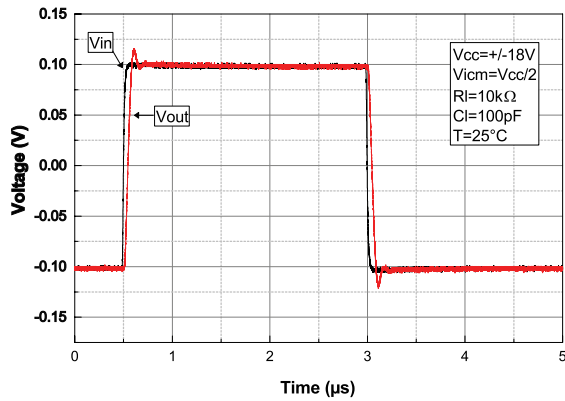
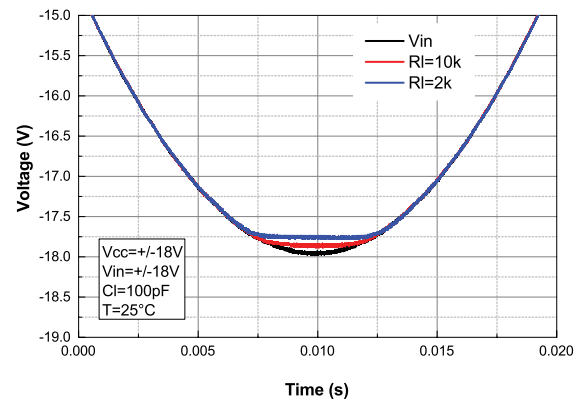
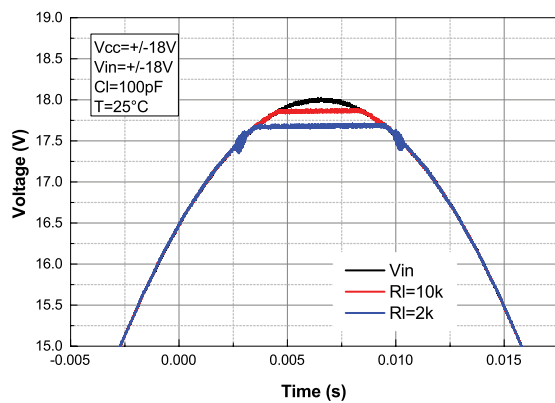
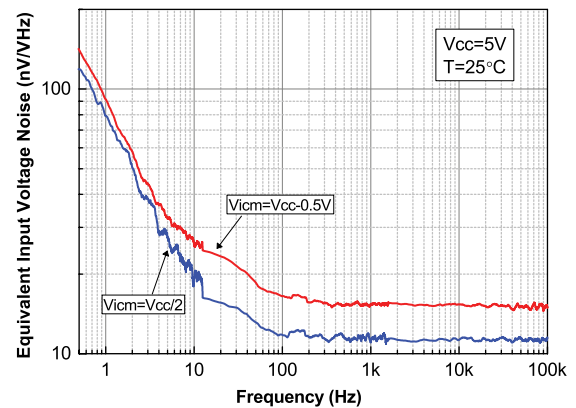
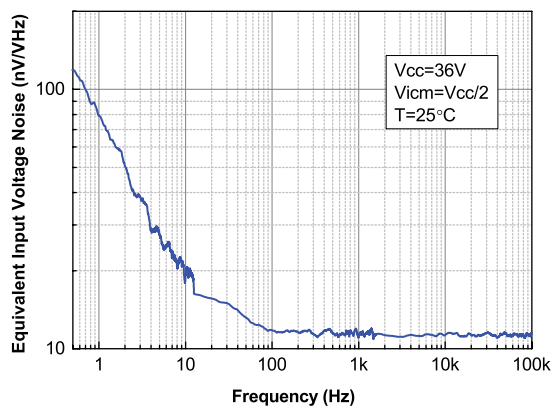
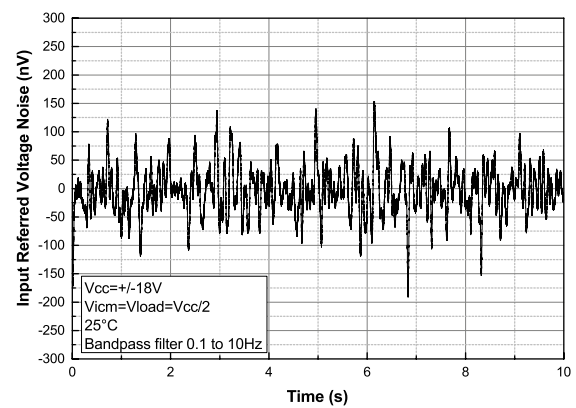
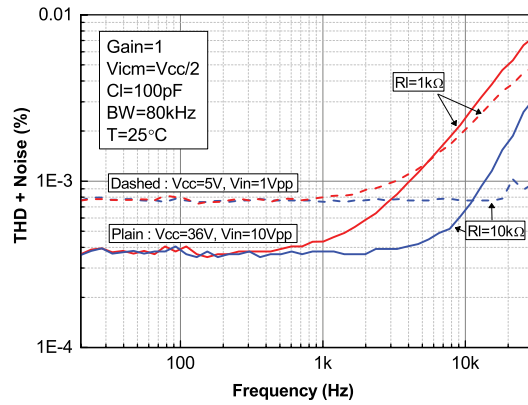
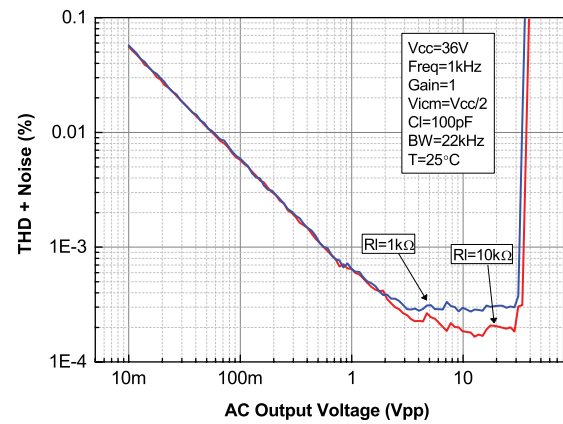
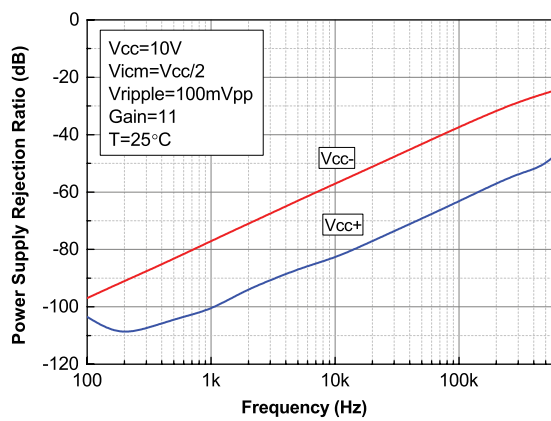
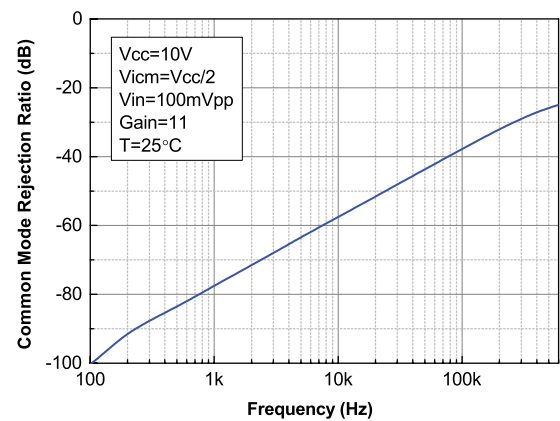
Figure 32. Small step response vs. time at $V_{CC} = 36\text{ V}$

Figure 33. Amplifier behavior close to the low rail at $V_{CC} = 36\text{ V}$

Figure 34. Amplifier behavior close to the high rail at $V_{CC} = 36\text{ V}$

Figure 35. Noise vs. frequency at $V_{CC} = 5\text{ V}$

Figure 36. Noise vs. frequency at $V_{CC} = 36\text{ V}$

Figure 37. Noise vs. time at $V_{CC} = 36\text{ V}$


Figure 38. THD+N vs. frequency

Figure 39. THD+N vs. output voltage

Figure 40. PSRR vs. frequency at $V_{CC} = 10\text{ V}$

Figure 41. CMRR vs. frequency at $V_{CC} = 10\text{ V}$


5 Application information

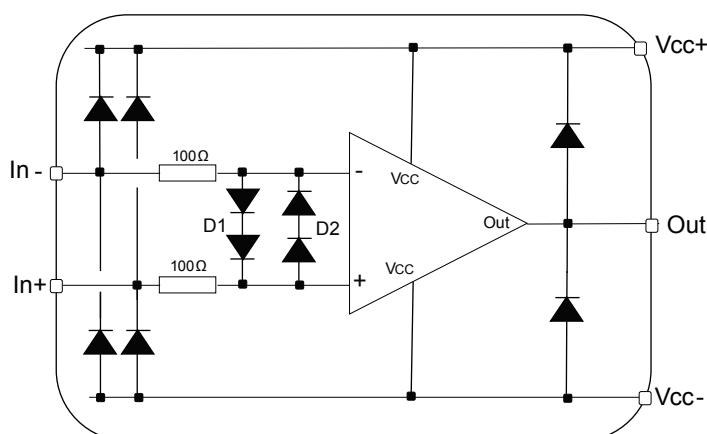
5.1 Operating voltages

The TSB711, TSB711A, TSB712, TSB712A devices can operate from 2.7 to 36 V. The parameters are fully specified at 5 V and 36 V power supplies. However, the parameters are very stable over the full V_{CC} range and several characterization curves show the TSB711, TSB711A, TSB712, TSB712A device characteristics over the full operating range. Additionally, the main specifications are guaranteed in extended temperature range from -40 to 125 °C.

5.2 Input pin voltage range

The TSB711, TSB711A, TSB712 and TSB712A devices have an internal ESD diode protection on the inputs. These diodes are connected between the inputs and each supply rail to protect the input stage from electrical discharge, as shown in the figure below.

Figure 42. Input current limitation



When the input pin voltage exceeds the power supply, the ESD diodes become conductive and, depending on this voltage, excessive current can flow through them. Without limitation this overcurrent can damage the device. In this case, the current has to be limited to 10 mA by adding a resistance in series with the input pin.

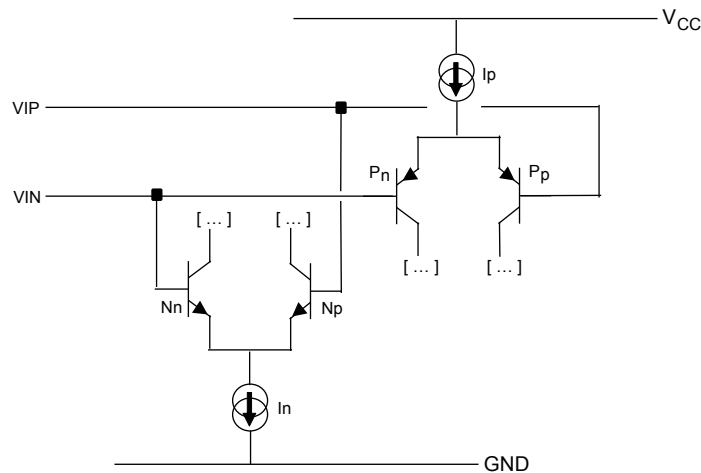
Similarly, in order to avoid excessive current in the protection diodes between the positive and negative inputs, the differential voltage should be limited to ± 2 V, or the current limited to 10 mA. Such a high differential voltage can be reached when the output is in saturation mode, or slew rate limited. In particular, it can happen when the device is used in comparator mode.

The TSB711, TSB711A, TSB712, TSB712A do not show any phase reversal for any input common mode voltage inside the absolute maximum ratings (AMR) voltage window, $(V_{CC-}) - 200 \text{ mV} < V_{ICM} < (V_{CC+}) + 200 \text{ mV}$.

5.3 Rail-to-rail input stage

The TSB711, TSB711A, TSB712, TSB712A devices are built with two complementary NPN and PNP input differential pairs, as shown in the figure below.

Figure 43. Rail-to-rail input stage



The devices have rail-to-rail inputs, and the input common mode range is extended from V_{CC-} to $(V_{CC+}) + 0.1$ V. However, the performance of these devices is optimized for the P-channel differential pair (which means from V_{CC-} to $(V_{CC+}) - 1.5$ V). Around $(V_{CC+}) - 1$ V, and with slight variations depending on the process, a transition occurs between the P-channel and the N-channel differential pair, impacting the input offset voltage (see Figure 12. Input offset voltage vs. common mode voltage at $V_{CC} = 5$ V TSB711A, TSB712A and Figure 13. Input offset voltage vs. common mode voltage at $V_{CC} = 36$ V TSB711A, TSB712A). As a consequence, CMRR can be degraded around this transition region. In order to achieve the best possible performance, this operating point should be avoided.

Please also notice that the input bias current polarity depends on the operation of NPN or PNP input stage. This transition is visible in figures Figure 16. Input bias current vs. common mode voltage at $V_{CC} = 5$ V and Figure 17. Input bias current vs. common mode voltage at $V_{CC} = 36$ V.

5.4 Input offset voltage drift over the temperature

The maximum input voltage drift variation over temperature is defined as the offset variation related to the offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during the production at application level. The maximum input voltage drift overtemperature enables the system designer to anticipate the effect of temperature variations. The maximum input voltage drift overtemperature is computed using the following formula:

$$\frac{\Delta V_{io}}{\Delta T} = \max \left| \frac{V_{io}(T) - V_{io}(25^{\circ}\text{C})}{T - 25^{\circ}\text{C}} \right|_{T = -40^{\circ}\text{C} \text{ and } T = 125^{\circ}\text{C}} \quad (1)$$

The datasheet maximum value is guaranteed by a measurement on a representative sample size ensuring a Cpk (process capability index) greater than 1.3.

5.5 Long term input offset voltage drift

To evaluate product reliability, two types of stress acceleration are used:

- Voltage acceleration, by changing the applied voltage.
- Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature.

The voltage acceleration has been defined based on JEDEC results, and is defined using:

$$A_{FV} = e^{\beta \cdot (V_S - V_U)} \quad (2)$$

Where:

A_{FV} is the voltage acceleration factor

β is the voltage acceleration coefficient in $1/V$, constant technology parameter ($\beta = 1$)

V_S is the stress voltage used for the accelerated test

V_U is the voltage used for the application

The temperature acceleration is driven by the Arrhenius model, and is defined as follows:

$$A_{FT} = e^{\frac{E_a}{k} \cdot \left(\frac{1}{T_U} - \frac{1}{T_S} \right)} \quad (3)$$

Where:

A_{FT} is the temperature acceleration factor

E_a is the activation energy of the technology based on the failure rate

k is the Boltzmann constant ($8.6173 \times 10^{-5} \text{ eV.K}^{-1}$)

T_U is the temperature of the die when V_U is used (K)

T_S is the temperature of the die under temperature stress (K)

The final acceleration factor, A_F , is the multiplication of the voltage acceleration factor and the temperature acceleration factor.

$$A_F = A_{FT} \cdot A_{FV} \quad (4)$$

A_F is calculated using the temperature and voltage defined in the mission profile of the product. The A_F value can then be used in Equation 5 to calculate the number of months of use equivalent to 1000 hours of reliable stress duration.

$$\text{Months} = A_F \times 1000 \text{ h} \times 12 \text{ months} / (24 \text{ h} \times 365.25 \text{ days}) \quad (5)$$

To evaluate the op-amp reliability, a follower stress condition is used where V_{CC} is defined as a function of the maximum operating voltage and the absolute maximum ratings (as recommended by JEDEC rules). V_{io} drift (in μV) of the product after 1000 h of stress is tracked with parameters at different measurement conditions.

$$V_{CC} = \max(V_{OP}) \text{ with } V_{icm} = V_{CC}/2 \quad (6)$$

The long term drift parameter ΔV_{io} (in $\mu V \cdot \text{month}^{-1/2}$), estimating the reliability performance of the product, is obtained using the ratio of the V_{io} (input offset voltage value) drift over the square root of the calculated number of months.

$$\Delta V_{io} = \frac{V_{io \text{ drift}}}{\sqrt{\text{months}}} \quad (7)$$

Where V_{io} drift is the measured drift value in the specified test conditions after 1000 h stress duration.

The V_{io} final drift, in μV , to be measured on the device in real operation conditions can be computed from:

$$V_{io \text{ final drift}}(t_{op}, T_{op}, V_{CC}) = \Delta V_{io, 25^\circ C} \cdot \sqrt{t_{op} \cdot e^{\beta \cdot (V_{CC} - V_{CC \text{ nom}})} \cdot e^{\frac{E_a}{k} \cdot \left(\frac{1}{297} - \frac{1}{T_{op}} \right)}} \quad (8)$$

Where:

ΔV_{io} is the long term drift parameter in $\mu V \cdot month^{-1/2}$

t_{op} is the operating time seen by the device, in months

T_{op} is the operating temperature

V_{CC} is the power supply during operating time

$V_{CC \text{ nom}}$ is the nominal V_{CC} at which the ΔV_{io} is computed (36 V for the TSB712A).

E_a is the activation energy of the technology (here 0.7 eV).

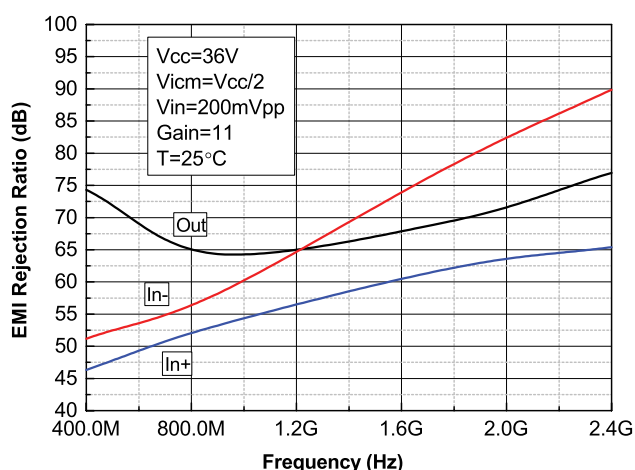
5.6 EMI rejection

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op-amps is a change in the offset voltage as a result of RF signal rectification. EMIRR is defined as follows:

$$EMIRR = 20 \cdot \log \left(\frac{V_{in \text{ pp}}}{\Delta V_{io}} \right) \quad (9)$$

The TSB711, TSB711A, TSB712, TSB712A have been specially designed to minimize susceptibility to EMIRR and shows a low sensitivity. As visible on figure below, EMI rejection ratio has been measured on both inputs and outputs, from 400 MHz to 2.4 GHz.

Figure 44. EMIRR on In+, In- and out pins



EMIRR performance might be improved by adding small capacitances (in the pF range) on the inputs, power supply and output pins. These capacitances help in minimizing the impedance of these nodes at high frequencies.

5.7 Maximum power dissipation

The usable output load current drive is limited by the maximum power dissipation allowed by the device package. The absolute maximum junction temperature for the TSB711, TSB711A, TSB712, TSB712A is 150 °C. The junction temperature can be estimated as follows:

$$T_J = P_D \times R_{th-jA} + T_A \quad (10)$$

T_J is the die junction temperature

P_D is the power dissipated in the package

R_{th-jA} is the junction to ambient thermal resistance of the package

T_A is the ambient temperature

The power dissipated in the package P_D is the sum of the quiescent power dissipated and the power dissipated by the output stage transistor. It is calculated as follows:

$$P_D = (V_{CC} \times I_{CC}) + (V_{CC+} - V_{OUT}) \times I_{Load} \quad (11)$$

when the op-amp sources the current

$$P_D = (V_{CC} \times I_{CC}) + (V_{OUT} - V_{CC-}) \times I_{Load} \quad (12)$$

when the op-amp sinks the current.

Do not exceed the 150 °C maximum junction temperature for the device. Exceeding the junction temperature limit can cause degradation in the parametric performance or even destroy the device.

5.8 Capacitive load and stability

Stability analysis must be performed for large capacitive loads over 100 pF. Increasing the load capacitance to high values produces gain peaking in the frequency response, with overshoot and ringing in the step response.

Generally, unity gain configuration is the worst situation for stability and the ability to drive large capacitive loads. For additional capacitive load drive capability in unity-gain configuration, stability can be improved by inserting a small resistor R_{ISO} (10 Ω to 30 Ω) in series with the output. This resistor significantly reduces ringing while maintaining DC performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created introducing a gain error on the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L . R_{ISO} modifies the maximum capacitive load acceptable from a stability point-of-view as described in the following figure:

Figure 45. Stability criteria with a serial resistor at different capacitive loads

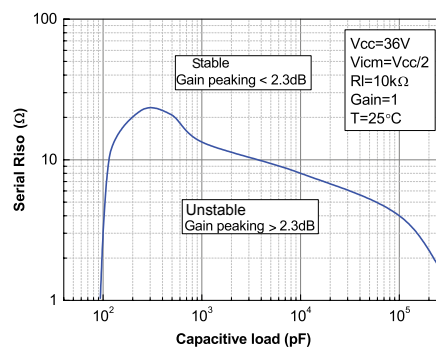
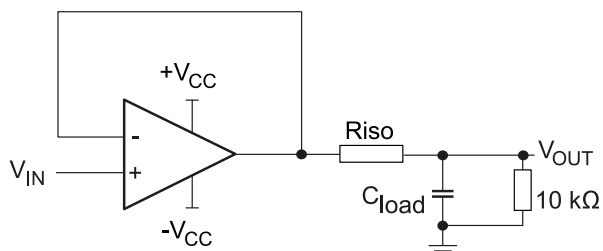


Figure 46. Test configuration for R_{ISO}



Please note that $R_{ISO} = 30 \Omega$ is sufficient to make the TSB711, TSB711A, TSB712, TSB712A stable whatever the capacitive load.

5.9 PCB layout recommendations

Particular attention must be paid to the layout of the PCB tracks connected to the amplifier, load, and power supply. The power and ground traces are critical as they must provide adequate energy and grounding for all circuits. The best practice is to use short and wide PCB traces to minimize voltage drops and parasitic inductance. In addition, to minimize parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used. The copper traces connecting the output pins to the load and supply pins should be as wide as possible to minimize trace resistance.

5.10 Decoupling capacitor

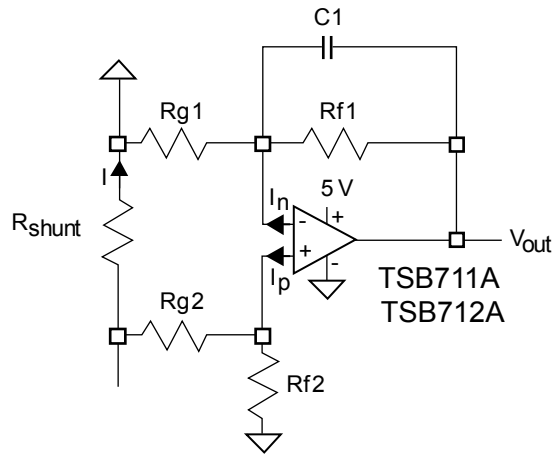
In order to ensure op-amp full functionality, it is mandatory to place a decoupling capacitor of at least 22 nF as close as possible to the op-amp supply pin. A good decoupling helps to reduce electromagnetic interference impact.

6 Typical applications

6.1 Low-side current sensing

Power management mechanisms are found in most electronic systems. Current sensing is useful to protect applications. The low-side current sensing method consists of placing a sense resistor between the load and the circuit ground. The resulting voltage drop is amplified using the TSB711A and the TSB712A (see the following figure).

Figure 47. Low-side current sensing schematic



V_{out} can be expressed as follows:

$$V_{OUT} = R_{shunt} \cdot I \left(1 - \frac{R_{g2}}{R_{g2} + R_{f2}} \right) \cdot \left(1 - \frac{R_{f1}}{R_{g1}} \right) + I_p \cdot \frac{R_{g2} \cdot R_{f2}}{R_{g2} + R_{f2}} \cdot \left(1 + \frac{R_{f1}}{R_{g1}} \right) - I_n \cdot R_{f1} - V_{io} \cdot \left(1 - \frac{R_{f1}}{R_{g1}} \right) \quad (13)$$

Assuming that $R_{f2} = R_{f1} = R_f$ and $R_{g2} = R_{g1} = R_g$, can be simplified in the following manner:

$$V_{OUT} = R_{shunt} \cdot I \cdot \frac{R_f}{R_g} - V_{io} \cdot \left(1 + \frac{R_f}{R_g} \right) + R_f \cdot I_{io} \quad (14)$$

The main advantage of using the TSB711A and the TSB712A for a low-side current sensing relies on its low V_{io} , compared to general purpose operational amplifiers. For the same current and targeted accuracy, the shunt resistor can be chosen with a lower value, resulting in lower power dissipation, lower drop in the ground path, and lower cost. Particular attention must be paid to the matching and precision of R_{g1} , R_{g2} , R_{f1} , and R_{f2} , to maximize the accuracy of the measurement.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 SOT23-5 package information

Figure 48. SOT23-5 package outline

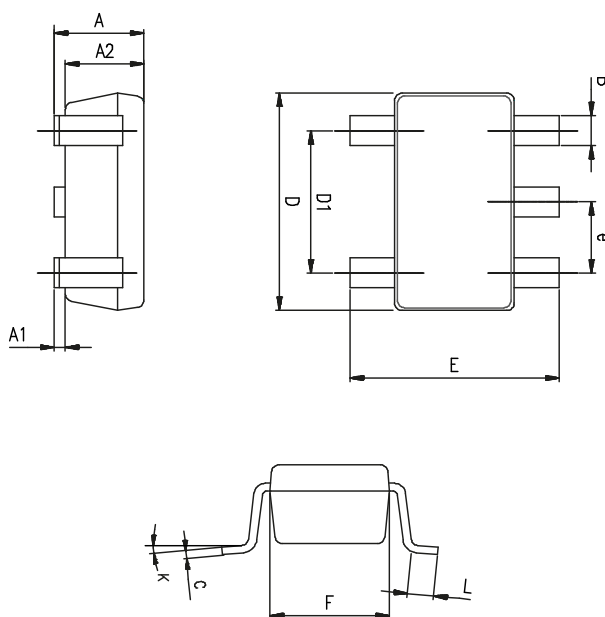


Table 8. SOT23-5 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.014	0.016	0.020
C	0.09	0.15	0.20	0.004	0.006	0.020
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.014	0.024
K	0°		10°	0°		10°

7.2 MiniSO8 package information

Figure 49. MiniSO8 package outline

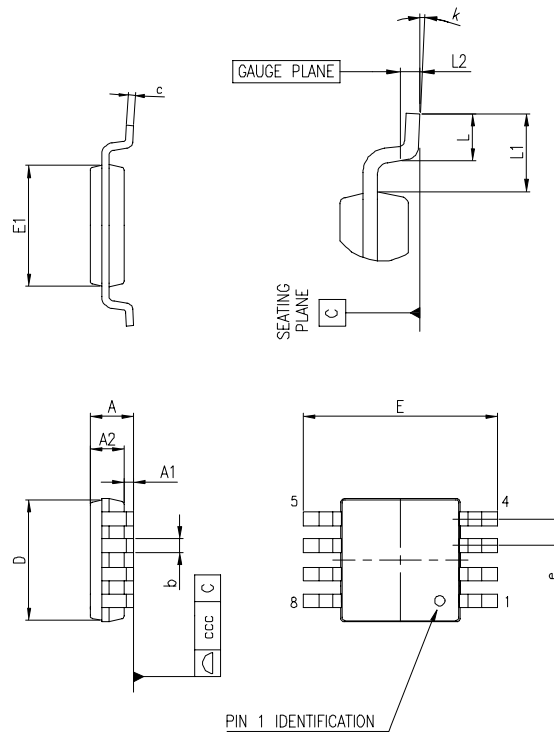
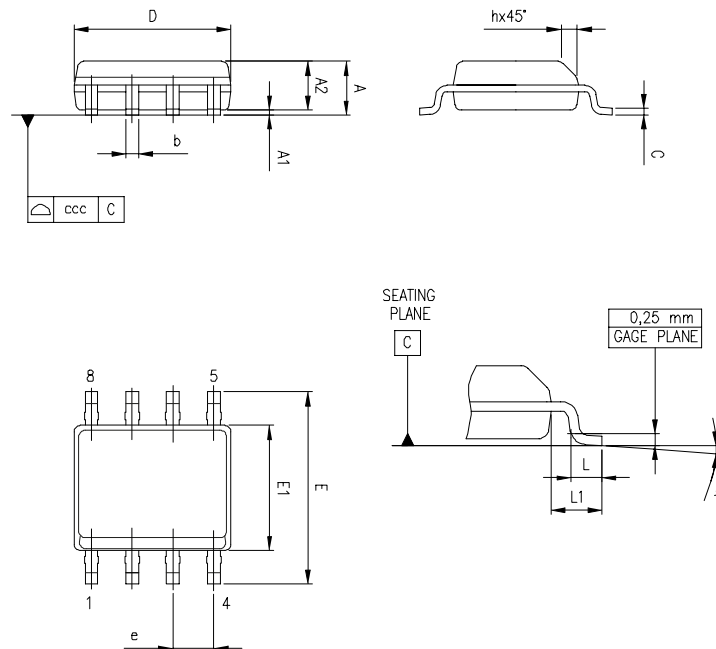


Table 9. MiniSO8 mechanical data

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.03	0.033	0.037
b	0.22		0.4	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.8	3	3.2	0.11	0.118	0.126
E	4.65	4.9	5.15	0.183	0.193	0.203
E1	2.8	3	3.1	0.11	0.118	0.122
e		0.65			0.026	
L	0.4	0.6	0.8	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.01	
k	0°		8°	0°		8°
ccc			0.1			0.004

7.3 SO8 package information

Figure 50. SO8 package outline

Table 10. SO-8 mechanical data

Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.1		0.25	0.004		0.01
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.01
D	4.8	4.9	5	0.189	0.193	0.197
E	5.8	6	6.2	0.228	0.236	0.244
E1	3.8	3.9	4	0.15	0.154	0.157
e		1.27			0.05	
h	0.25		0.5	0.01		0.02
L	0.4		1.27	0.016		0.05
L1		1.04			0.04	
k	0		8 °	1 °		8 °
ccc			0.1			0.004

7.4 SO14 package information

Figure 51. SO14 package outline

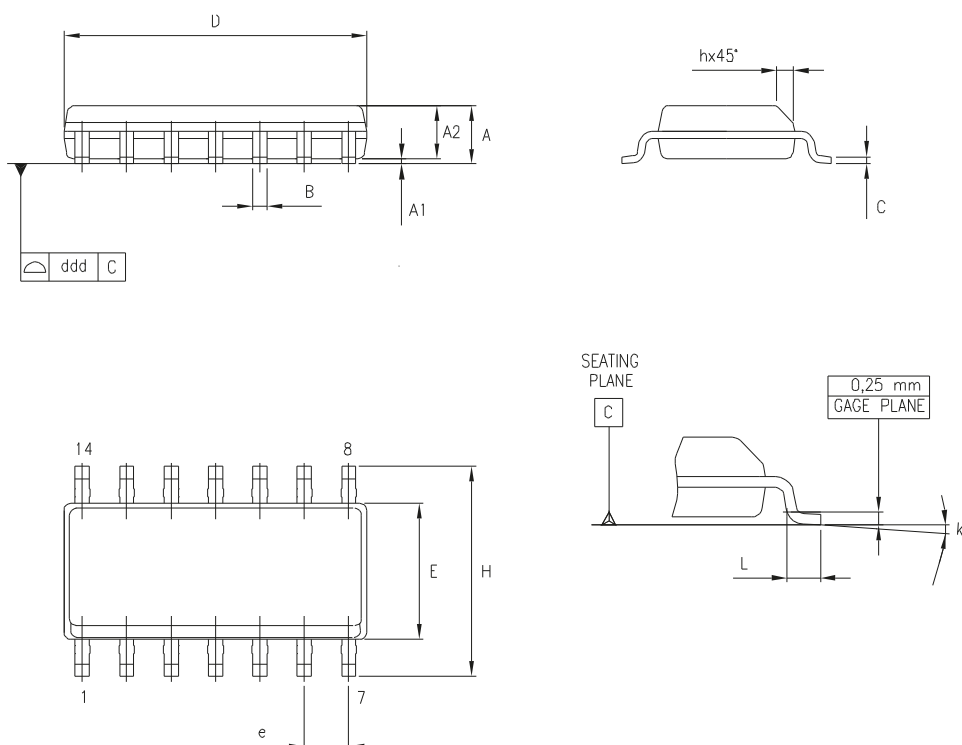


Table 11. SO14 mechanical data

Dimensions ⁽¹⁾						
Symbol	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.05		0.068
A1	0.10		0.25	0.004		0.009
A2	1.10		1.65	0.04		0.06
B	0.33		0.51	0.01		0.02
C	0.19		0.25	0.007		0.009
D ⁽²⁾	8.55		8.75	0.33		0.34
E	3.80		4.0	0.15		0.15
e		1.27			0.05	
H	5.80		6.20	0.22		0.24
L	0.40		1.27	0.015		0.05
k	0°		8°	0°		8°
ddd			0.10			0.004

1. Drawing dimensions include "Single" and "Matrix" versions.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.

7.5 TSSOP14 package information

Figure 52. TSSOP14 package outline

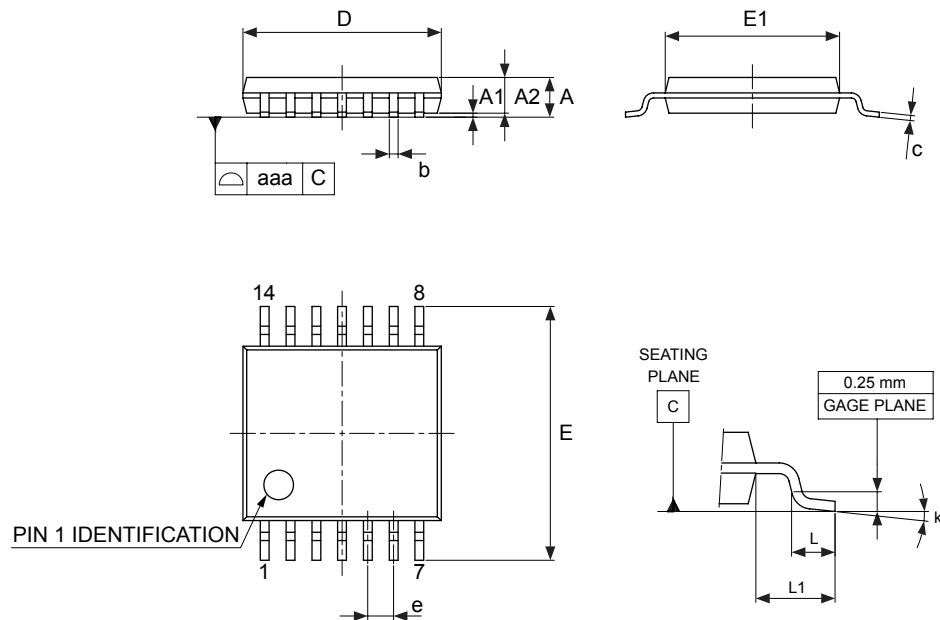


Table 12. TSSOP14 mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.90	5.00	5.10	0.193	0.197	0.201
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.176
e		0.65			0.0256	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°		8°	0°		8°
aaa			0.10			0.004

8 Ordering information

Table 13. Order code

Order code	Temperature range	Package	Packing	Marking
TSB711AILT	-40° to +125 °C	SOT23-5	Tape and reel	K223
TSB711ILT		SOT23-5		K219
TSB711AIYLT	-40 °C to +125 °C automotive grade	SOT23-5		K225
TSB711IYLT		SOT23-5		K221
TSB712AIST	-40° to +125 °C	MiniSO8		K214
TSB712AIDT		SO8		TSB712AI
TSB712IDT		SO8		TSB712I
TSB712IST		MiniSO8		712S
TSB712AIYDT	-40 to 125 °C automotive grade ⁽¹⁾	SO8		712AIY
TSB712AIYST		MiniSO8		712Y
TSB712IYDT		SO8		712IY
TSB712IYST		MiniSO8		K215
TSB714AIDT	-40° to +125 °C	SO14		B714AI
TSB714IDT				B714I
TSB714AIYDT	-40 to 125 °C automotive grade ⁽¹⁾			B714AY
TSB714IYDT				B714Y
TSB714AIPT	-40° to +125 °C	TSSOP14		B714AI
TSB714IPT				B714I
TSB714AIYPT	-40 to 125 °C automotive grade ⁽¹⁾			B714AY
TSB714IYPT				B714IY

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.

SO8 package for single op-amp may be available for qualification under customer request. Please contact sales office for such request.

DFN8 package for dual op-amp may be available for qualification under customer request. Please contact sales office for such request.

Revision history

Table 14. Document revision history

Date	Revision	Changes
23-Apr-2018	1	Initial release.
17-Sep-2018	2	Added the TSB712 as root part number; cover page has been updated accordingly. Updated Section 3 Electrical characteristics, Section 4 Typical performance characteristics, Section 5 Application information and Table 7. Order code. Added Section 7.2 SO8 package information.
29-Nov-2018	3	Updated Table 3. Electrical characteristics at $V_{CC} = 36\text{ V}$, $V_{ICM} = V_{OUT} = V_{CC} / 2$, $T_{amb} = 25\text{ }^{\circ}\text{C}$ and R_L connected to $V_{CC} / 2$ (unless otherwise specified) and Table 4. Electrical characteristics at $V_{CC} = 5\text{ V}$, $V_{ICM} = V_{OUT} = V_{CC} / 2$, $T_{amb} = 25\text{ }^{\circ}\text{C}$ and R_L connected to $V_{CC} / 2$ (unless otherwise specified).
18-Feb-2019	4	Updated Figure 44. Stability criteria with a serial resistor at different capacitive loads.
11-Jun-2019	5	Added the root part numbers TSB711 and TSB711A, therefore the whole document has been updated accordingly.
28-Oct-2020	6	Added new part numbers in Table 13. Order code , new Section 7.4 SO14 package information and Section 7.5 TSSOP14 package information .

Contents

1	Pin description	2
2	Absolute maximum ratings and operating conditions	4
3	Electrical characteristics	5
4	Typical performance characteristics	10
5	Application information	17
5.1	Operating voltages	17
5.2	Input pin voltage range	17
5.3	Rail-to-rail input stage	18
5.4	Input offset voltage drift over the temperature	18
5.5	Long term input offset voltage drift	19
5.6	EMI rejection	20
5.7	Maximum power dissipation	21
5.8	Capacitive load and stability	21
5.9	PCB layout recommendations	23
5.10	Decoupling capacitor	23
6	Typical applications	24
6.1	Low-side current sensing	24
7	Package information	25
7.1	SOT23-5 package information	25
7.2	MiniSO8 package information	26
7.3	SO8 package information	27
7.4	SO14 package information	28
7.5	TSSOP14 package information	29
8	Ordering information	30
	Revision history	31



List of tables

Table 1.	TSB711 pin description (SOT23-5)	2
Table 2.	TSB712 pin description (miniSO8/SO8)	2
Table 3.	TSB714 pin description	3
Table 4.	Absolute maximum ratings	4
Table 5.	Operating conditions	4
Table 6.	Electrical characteristics at $V_{CC} = 36\text{ V}$, $V_{ICM} = V_{OUT} = V_{CC} / 2$, $T_{amb} = 25\text{ °C}$ and R_L connected to $V_{CC} / 2$ (unless otherwise specified)	5
Table 7.	Electrical characteristics at $V_{CC} = 5\text{ V}$, $V_{ICM} = V_{OUT} = V_{CC} / 2$, $T_{amb} = 25\text{ °C}$ and R_L connected to $V_{CC} / 2$ (unless otherwise specified)	8
Table 8.	SOT23-5 package mechanical data	25
Table 9.	MiniSO8 mechanical data	26
Table 10.	SO-8 mechanical data	27
Table 11.	SO14 mechanical data	28
Table 12.	TSSOP14 mechanical data	29
Table 13.	Order code	30
Table 14.	Document revision history	31

List of figures

Figure 1.	TSB711 pin connections (top view)	2
Figure 2.	TSB712 pin connections (top view)	2
Figure 3.	TSB714 pin connections (top view)	3
Figure 4.	Supply current vs. supply voltage	10
Figure 5.	Input offset voltage distribution at $V_{CC} = 5\text{ V}$ TSB711A, TSB712A	10
Figure 6.	Input offset voltage distribution at $V_{CC} = 36\text{ V}$ TSB711A, TSB712A	10
Figure 7.	Input offset voltage vs. temperature at $V_{CC} = 5\text{ V}$	10
Figure 8.	Input offset voltage vs. temperature at $V_{CC} = 36\text{ V}$	11
Figure 9.	Input offset voltage thermal coefficient distribution at $V_{CC} = 5\text{ V}$	11
Figure 10.	Channel separation vs. frequency at $V_{CC} = 36\text{ V}$	11
Figure 11.	Input offset voltage vs. supply voltage	11
Figure 12.	Input offset voltage vs. common mode voltage at $V_{CC} = 5\text{ V}$ TSB711A, TSB712A	11
Figure 13.	Input offset voltage vs. common mode voltage at $V_{CC} = 36\text{ V}$ TSB711A, TSB712A	11
Figure 14.	Input bias current vs. temperature at $V_{ICM} = V_{CC} / 2$	12
Figure 15.	Output current vs. output voltage at $V_{CC} = 5\text{ V}$	12
Figure 16.	Input bias current vs. common mode voltage at $V_{CC} = 5\text{ V}$	12
Figure 17.	Input bias current vs. common mode voltage at $V_{CC} = 36\text{ V}$	12
Figure 18.	Output current vs. output voltage at $V_{CC} = 36\text{ V}$	12
Figure 19.	Output voltage (V_{OH}) vs. supply voltage	12
Figure 20.	Output voltage (V_{OL}) vs. supply voltage	13
Figure 21.	Positive slew rate at $V_{CC} = 36\text{ V}$	13
Figure 22.	Negative slew rate at $V_{CC} = 36\text{ V}$	13
Figure 23.	Bode diagram at $V_{CC} = 5\text{ V}$	13
Figure 24.	Bode diagram at $V_{CC} = 36\text{ V}$	13
Figure 25.	Phase margin vs. output current at $V_{CC} = 5\text{ V}$	13
Figure 26.	Phase margin vs. output current at $V_{CC} = 36\text{ V}$	14
Figure 27.	Phase margin vs. capacitive load	14
Figure 28.	Overshoot vs. capacitive load at $V_{CC} = 36\text{ V}$	14
Figure 29.	Small step response vs. time at $V_{CC} = 5\text{ V}$	14
Figure 30.	Desaturation time at low rail at $V_{CC} = 5\text{ V}$	14
Figure 31.	Desaturation time at high rail at $V_{CC} = 5\text{ V}$	14
Figure 32.	Small step response vs. time at $V_{CC} = 36\text{ V}$	15
Figure 33.	Amplifier behavior close to the low rail at $V_{CC} = 36\text{ V}$	15
Figure 34.	Amplifier behavior close to the high rail at $V_{CC} = 36\text{ V}$	15
Figure 35.	Noise vs. frequency at $V_{CC} = 5\text{ V}$	15
Figure 36.	Noise vs. frequency at $V_{CC} = 36\text{ V}$	15
Figure 37.	Noise vs. time at $V_{CC} = 36\text{ V}$	15
Figure 38.	THD+N vs. frequency	16
Figure 39.	THD+N vs. output voltage	16
Figure 40.	PSRR vs. frequency at $V_{CC} = 10\text{ V}$	16
Figure 41.	CMRR vs. frequency at $V_{CC} = 10\text{ V}$	16
Figure 42.	Input current limitation	17
Figure 43.	Rail-to-rail input stage	18
Figure 44.	EMIRR on In+, In- and out pins	20
Figure 45.	Stability criteria with a serial resistor at different capacitive loads	21
Figure 46.	Test configuration for R_{ISO}	22
Figure 47.	Low-side current sensing schematic	24
Figure 48.	SOT23-5 package outline	25



Figure 49.	MiniSO8 package outline	26
Figure 50.	SO8 package outline	27
Figure 51.	SO14 package outline	28
Figure 52.	TSSOP14 package outline	29



IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2020 STMicroelectronics – All rights reserved