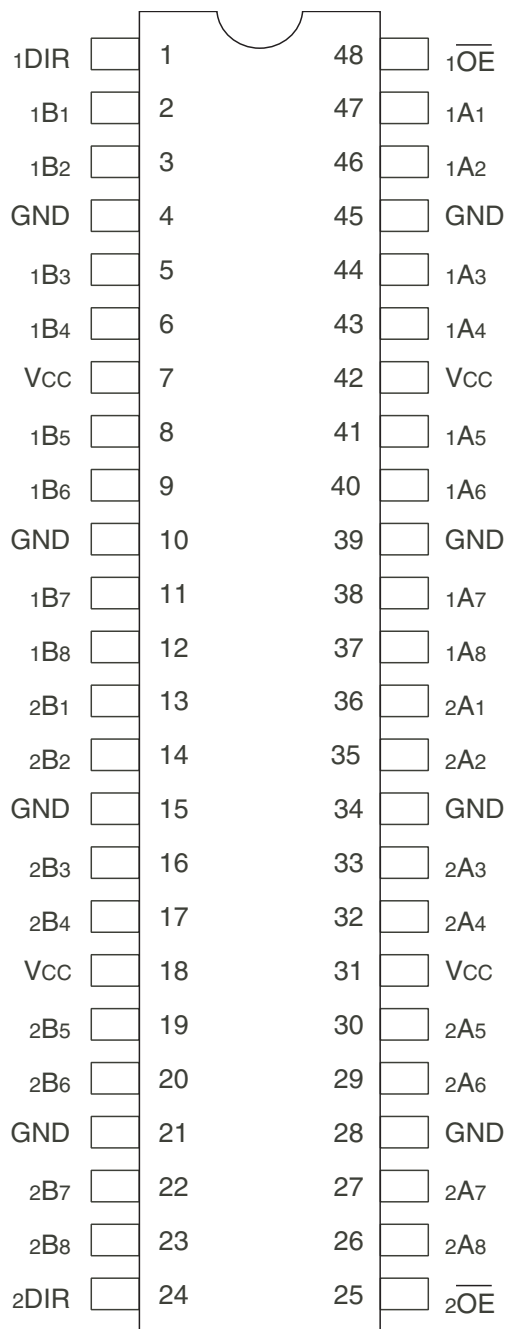


The FCT162245T has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times—reducing the need for external series terminating resistors. The FCT162245T is a plug-in replacement for the FCT16245T and ABT16245 for on-board interface applications.

The logic diagram shows a 2-to-8 decoder implemented with NAND and NOT gates. The inputs are labeled 2 DIR and 2A1 through 2A8. The outputs are labeled 2OE, 2B1 through 2B8. The circuit uses two NAND gates at the top to generate the active-low output 2OE from the 2 DIR input. The 2A1 through 2A8 inputs are each connected to a NOT gate, which produces the active-low outputs 2B1 through 2B8. The 2A1 input is also connected to a NAND gate that produces 2B1, and the 2A2 input is connected to a NAND gate that produces 2B2. The 2A3 input is connected to a NAND gate that produces 2B3, and the 2A4 input is connected to a NAND gate that produces 2B4. The 2A5 input is connected to a NAND gate that produces 2B5, and the 2A6 input is connected to a NAND gate that produces 2B6. The 2A7 input is connected to a NAND gate that produces 2B7, and the 2A8 input is connected to a NAND gate that produces 2B8.

Downloaded from [Arrow.com](https://arrow.com).

PIN CONFIGURATION



SSOP/ TSSOP/ CERPACK
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	−0.5 to +7	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	−0.5 to V _{CC} +0.5	V
T _{STG}	Storage Temperature	−65 to +150	°C
I _{OUT}	DC Output Current	−60 to +120	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXXT AND FCT166XXXT (A-Port) Output and I/O terminals.
- Output and I/O terminals terminals for FCT162XXXT AND FCT166XXXT (A-Port).

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	3.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	3.5	8	pF

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
x $\overline{OE}$	Output Enable Inputs (Active LOW)
xDIR	Direction Control Input
xAx	Side A Inputs or 3-State Outputs
xBx	Side B Inputs or 3-State Outputs

FUNCTION TABLE⁽¹⁾

Inputs		Outputs
x $\overline{OE}$	xDIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	± 1	μA
	Input HIGH Current (I/O pins) ⁽⁵⁾			—	—	± 1	
I_{IL}	Input LOW Current (Input pins) ⁽⁵⁾		$V_I = \text{GND}$	—	—	± 1	
	Input LOW Current (I/O pins) ⁽⁵⁾			—	—	± 1	
I_{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}			$V_O = 0.5\text{V}$	—	—	± 1	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}$, $V_O = \text{GND}^{(3)}$		-80	-140	-250	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND}$ or V_{CC}		—	5	500	μA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I_{ODL}	Output LOW Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_O = 1.5\text{V}^{(3)}$		60	115	200	mA
I_{ODH}	Output HIGH Current	$V_{CC} = 5\text{V}$, $V_{IN} = V_{IH}$ or V_{IL} , $V_O = 1.5\text{V}^{(3)}$		-60	-115	-200	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -16\text{mA MIL}$ $I_{OH} = -24\text{mA IND}$	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = 16\text{mA MIL}$ $I_{OH} = 24\text{mA IND}$	—	0.3	0.55	V

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. This test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{xOE} = xDIR = GND$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	60	100	$\mu A /$ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE} = xDIR = GND$ One Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	0.6	1.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = GND$	—	0.9	2.3	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{xOE} = xDIR = GND$ Sixteen Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	2.4	4.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = GND$	—	6.4	16.5 ⁽⁵⁾	

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at $V_{CC} = 5.0V$, +25°C ambient.

3. Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND.

4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$

$I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$

$\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V \text{)}$

$D_H = \text{Duty Cycle for TTL Inputs High}$

$N_T = \text{Number of TTL Inputs at } D_H$

$I_{CCD} = \text{Dynamic Current caused by an Input Transition Pair (HLH or LHL)}$

$f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$

$N_{CP} = \text{Number of Clock Inputs at } f_{CP}$

$f_i = \text{Input Frequency}$

$N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	54FCT162445T		54/74FCT162245AT				54/74FCT162245CT				Unit
			Mil.		Ind.		Mil.		Ind.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH	Propagation Delay	CL = 50pF RL = 500Ω	1.5	7.5	1.5	4.6	1.5	4.9	1.5	3.5	1.5	4.5	ns
tPHL	A to B, B to A												
tPZH	Output Enable Time		1.5	10	1.5	6.2	1.5	6.5	1.5	4.4	1.5	6.2	ns
tPZL	xOE to A or B												
tPHZ	Output Disable Time		1.5	10	1.5	5	1.5	6	1.5	4	1.5	5.2	ns
tPLZ	xOE to A or B												
tPZH	Output Enable Time		1.5	10	1.5	6.2	1.5	6.5	1.5	4.8	1.5	6.2	ns
tPZL	xDIR to A or B ⁽⁴⁾												
tPHZ	Output Disable Time	1.5	10	1.5	5	1.5	6	1.5	4	1.5	5.2	ns	
tPLZ	xDIR to A or B ⁽⁴⁾												
tSK(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

NOTES:

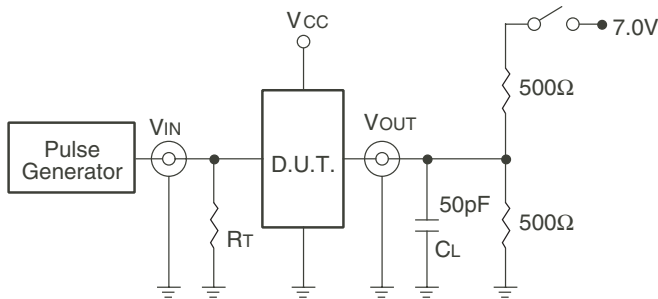
1. See test circuit and waveforms.

2. Minimum limits are guaranteed but not tested on Propagation Delays.

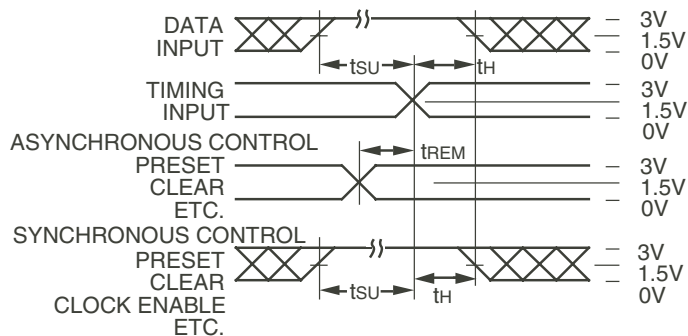
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

4. This parameter is guaranteed but not tested.

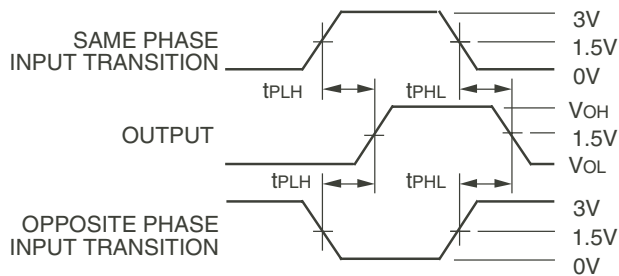
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Waveforms



Set-up, Hold, and Release Times



Propagation Delay

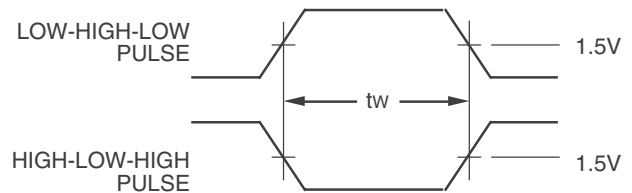
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

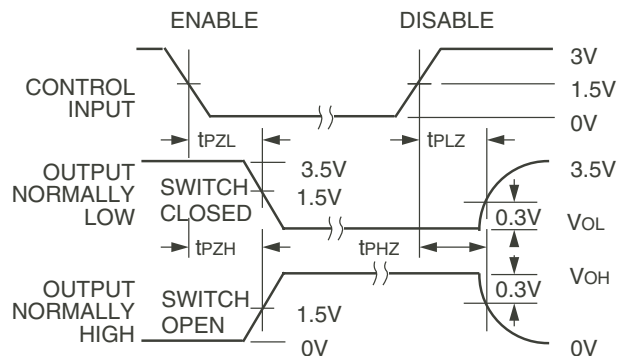
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to Zout of the Pulse Generator.



Pulse Width



Enable and Disable Times

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.

ORDERING INFORMATION

XX	FCT	XXX	XXXX	XX	X		
Temp. Range		Family	Device Type	Package	Process		
					Blank B	Industrial MIL-STD-883, Class B	
					PVG PAG	<u>Industrial Options</u> Shrink Small Outline Package - Green Thin Shrink Small Outline Package - Green	
						E	<u>Military Options</u> CERPACK
				245T 245AT 245CT	16-Bit Buffer/Line Driver		
				162	Double-Density, 5 Volt, Balanced Drive		
				54 74	55 C to +125 C 40 C to +85 C		

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.