

# MOSFET – Dual, N-Channel, POWERTRENCH®

**Q1: 40 V, 156 A, 1.5 mΩ**

**Q2: 40 V, 156 A, 1.5 mΩ**



**ON Semiconductor®**

[www.onsemi.com](http://www.onsemi.com)

## FDMD8540L

### General Description

This device includes two 40 V N-Channel MOSFETs in a dual Power (5 mm x 6 mm) package. HS source and LS drain internally connected for half/full bridge, low source inductance package, low  $r_{DS(on)}$ /Qg FOM silicon.

### Features

Q1: N-Channel

- Max  $r_{DS(on)}$  = 1.5 mΩ at  $V_{GS}$  = 10 V,  $I_D$  = 33 A
- Max  $r_{DS(on)}$  = 2.2 mΩ at  $V_{GS}$  = 4.5 V,  $I_D$  = 26 A

Q2: N-Channel

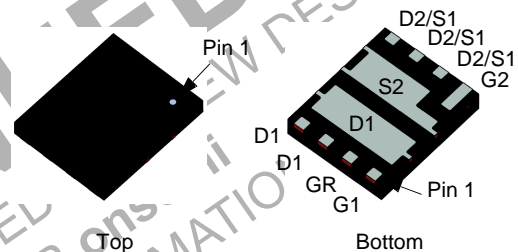
- Max  $r_{DS(on)}$  = 1.5 mΩ at  $V_{GS}$  = 10 V,  $I_D$  = 33 A
- Max  $r_{DS(on)}$  = 2.2 mΩ at  $V_{GS}$  = 4.5 V,  $I_D$  = 26 A

- Ideal for Flexible Layout in Primary Side of Bridge Topology
- 100% UIL Tested
- Kelvin High Side MOSFET Drive Pin-out Capability
- This Device is Pb-Free and are RoHS Compliant

### Applications

- POL Synchronous Dual
- One Phase Motor Half Bridge
- Half/Full Bridge Secondary Synchronous Rectification

$V_{DS}$	$r_{DS(on)}$ MAX	$I_D$ MAX
40 V	1.5 mΩ @ 10 V	156 A
	2.2 mΩ @ 4.5 V	

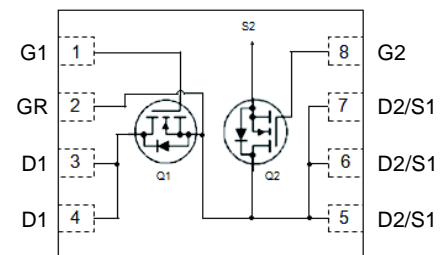


**PQFN8 5X6, 1.27P**  
**Power 5 x 6**  
**CASE 483AT**

### MARKING DIAGRAM

\$Y&Z&3&K  
FDMD  
8540L

FDMD8540L = Specific Device Code  
\$Y = ON Semiconductor Logo  
&Z = Assembly Plant Code  
&3 = 3-Digit Date Code Format  
&K = 2-Digits Lot Run Traceability Data



### ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

# FDMD8540L

## MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		Q1	Q2	Unit
$V_{DS}$	Drain to Source Voltage		40	40	V
$V_{GS}$	Gate to Source Voltage		$\pm 20$	$\pm 20$	V
$I_D$	Drain Current	– Continuous	$T_C = 25^\circ\text{C}$ (Note 3)	156	A
		– Continuous	$T_C = 100^\circ\text{C}$ (Note 3)	99	
		– Continuous	$T_A = 25^\circ\text{C}$	33 (Note 4a)	
		– Pulsed	(Note 2)	886	
$E_{AS}$	Single Pulse Avalanche Energy (Note 1)		541	541	mJ
$P_D$	Power Dissipation	$T_C = 25^\circ\text{C}$	62	62	W
	Power Dissipation	$T_A = 25^\circ\text{C}$	2.3 (Note 4a)	2.3 (Note 4b)	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range		–55 to +150		$^\circ\text{C}$

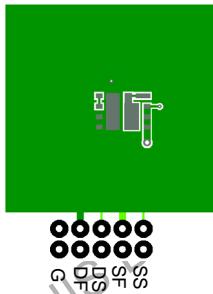
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Q1:  $E_{AS}$  of 541 mJ is based on starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 19\text{ A}$ ,  $V_{DD} = 40\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% tested at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 59\text{ A}$ .  
Q2:  $E_{AS}$  of 541 mJ is based on starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 19\text{ A}$ ,  $V_{DD} = 40\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% tested at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 59\text{ A}$ .
2. Pulsed  $I_D$  please refer to Figure 11 and Figure 24 SOA graph for more details.
3. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

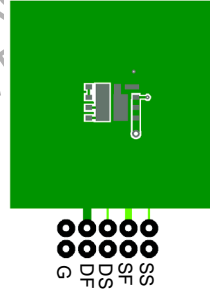
## THERMAL CHARACTERISTICS

Symbol	Parameter	Q1	Q2	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.0	2.0	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	55 (Note 4a)	55 (Note 4b)	

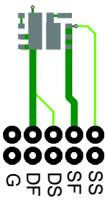
4.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



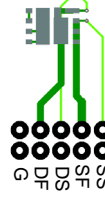
a.  $55^\circ\text{C/W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b.  $55^\circ\text{C/W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



c.  $155^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper



d.  $155^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper

# FDMD8540L

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit
--------	-----------	----------------	------	-----	-----	-----	------

### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 $\mu$ A, V <sub>GS</sub> = 0 V	Q1 Q2	40 40	– –	– –	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 mA, referenced to 25°C	Q1 Q2	– –	20 20	– –	mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 32 V, V <sub>GS</sub> = 0 V	Q1 Q2	– –	– –	1 1	$\mu$ A
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = $\pm$ 20 V, V <sub>DS</sub> = 0 V	Q1 Q2	– –	– –	$\pm$ 100 $\pm$ 100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 mA	Q1 Q2	1.0 1.0	1.8 1.8	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 $\mu$ A, referenced to 25°C	Q1 Q2	– –	–6 –6	– –	mV/°C
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 33 A	Q1	–	1.25	1.5	m $\Omega$
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 26 A			1.65	2.2	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 33 A, T <sub>J</sub> = 125°C		–	1.7	2.1	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 33 A	Q2	–	1.25	1.5	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 26 A			1.65	2.2	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 33 A, T <sub>J</sub> = 125°C		–	1.7	2.1	
g <sub>FS</sub>	Forward Transconductance	V <sub>DD</sub> = 5 V, I <sub>D</sub> = 33 A	Q1 Q2	– –	178 178	– –	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V f = 1 MHz	Q1 Q2	– –	5670 5670	7940 7940	pF
C <sub>oss</sub>	Output Capacitance		Q1 Q2	– –	1668 1668	2335 2335	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		Q1 Q2	– –	75 75	135 135	pF
R <sub>g</sub>	Gate Resistance		Q1 Q2	0.1 0.1	1.6 1.6	3.2 3.2	$\Omega$

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 20 V, I <sub>D</sub> = 33 A V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 $\Omega$		Q1 Q2	– –	15 15	28 28	ns
t <sub>r</sub>	Rise Time			Q1 Q2	– –	13 13	24 24	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			Q1 Q2	– –	51 51	81 81	ns
t <sub>f</sub>	Fall Time			Q1 Q2	– –	14 14	25 25	ns
Q <sub>g(TOT)</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V	V <sub>DD</sub> = 20 V, I <sub>D</sub> = 33 A	Q1 Q2	– –	81 81	113 113	nC
Q <sub>g(TOT)</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 4.5 V	V <sub>DD</sub> = 20 V, I <sub>D</sub> = 33 A	Q1 Q2	– –	38 38	54 54	nC
Q <sub>gs</sub>	Gate to Source Charge	V <sub>DD</sub> = 20 V, I <sub>D</sub> = 33 A		Q1 Q2	– –	15 15	– –	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge	V <sub>DD</sub> = 20 V, I <sub>D</sub> = 33 A		Q1 Q2	– –	11 11	– –	nC

**ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>							
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 33\text{ A}$ (Note 5)	Q1 Q2	— —	0.8 0.8	1.3 1.3	V
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 2\text{ A}$ (Note 5)	Q1 Q2	— —	0.7 0.7	1.2 1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 33\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	Q1 Q2	— —	54 54	86 86	ns
$Q_{rr}$	Reverse Recovery Charge		Q1 Q2	— —	38 38	60 60	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0 %.

**TYPICAL CHARACTERISTICS (Q1 N-CHANNEL)**

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

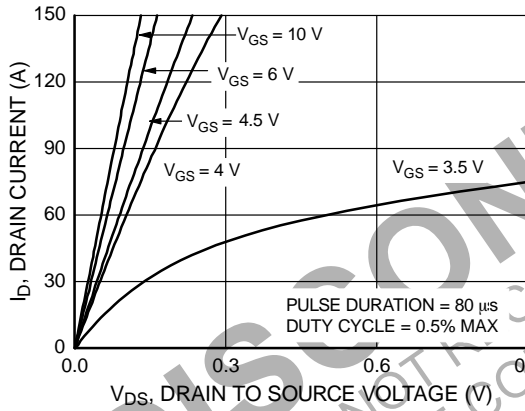


Figure 1. On Region Characteristics

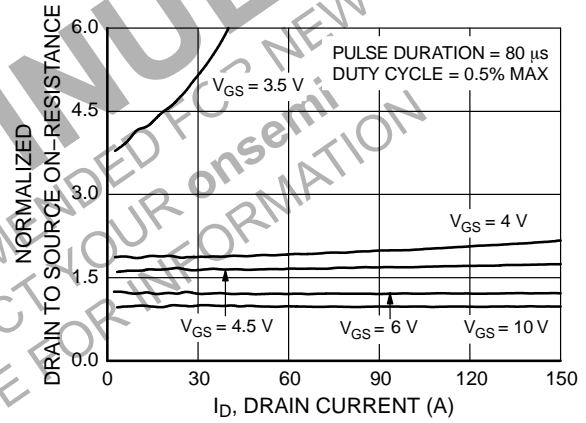


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

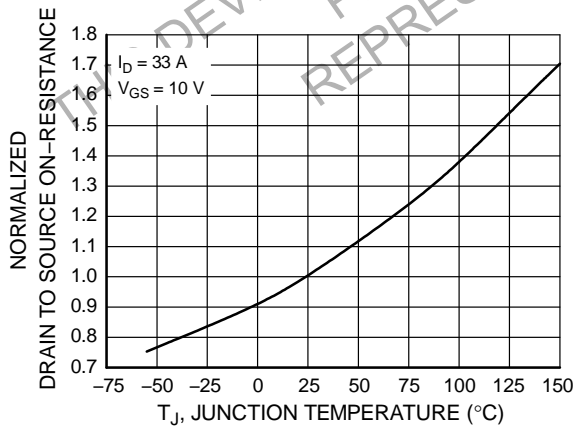


Figure 3. Normalized On Resistance vs. Junction Temperature

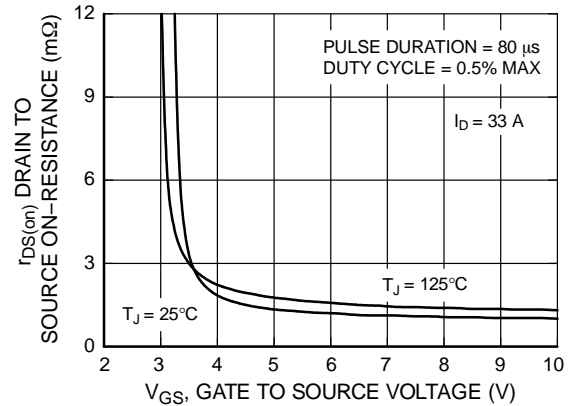
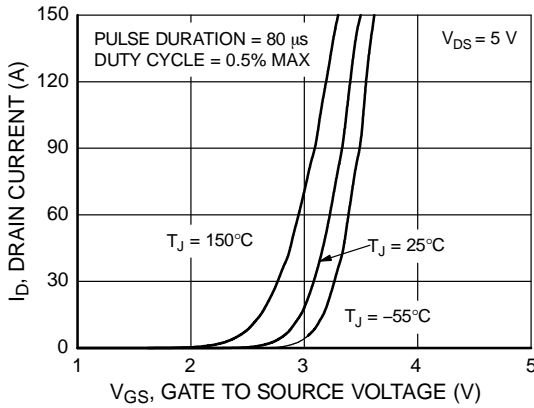


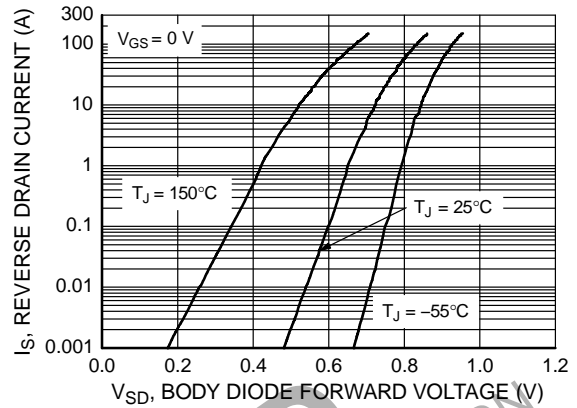
Figure 4. On-Resistance vs. Gate to Source Voltage

**TYPICAL CHARACTERISTICS (Q1 N-CHANNEL)**

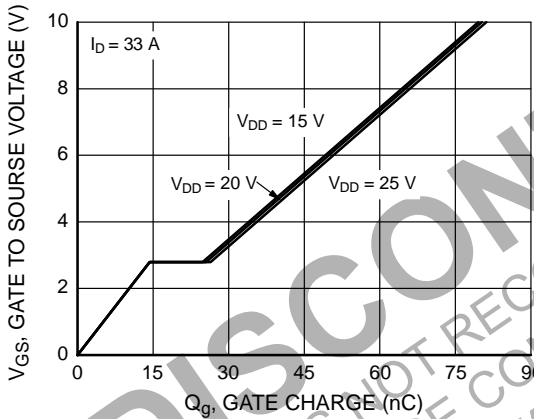
( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)



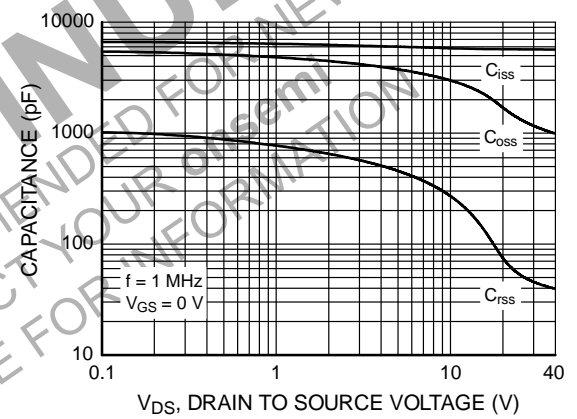
**Figure 5. Transfer Characteristics**



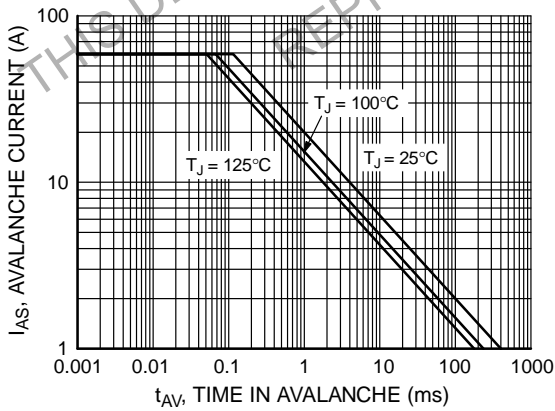
**Figure 6. Source to Gate Diode Forward Voltage vs. Source Current**



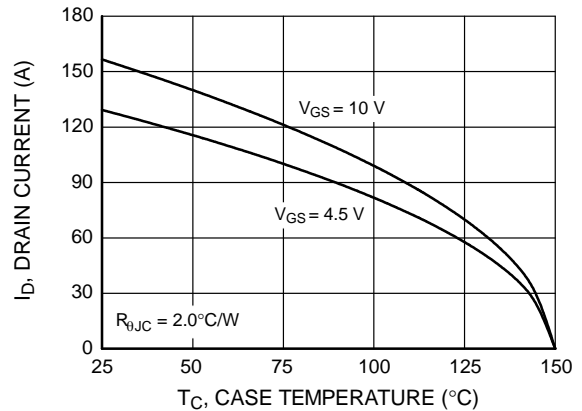
**Figure 7. Gate Charge Characteristics**



**Figure 8. Capacitance vs. Drain to Source Voltage**



**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL)

( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

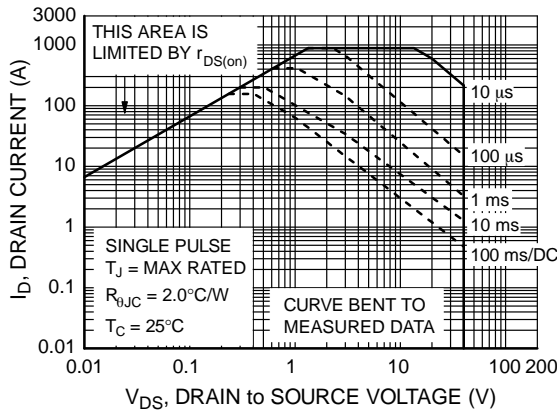


Figure 11. Forward Bias Safe Operating Area

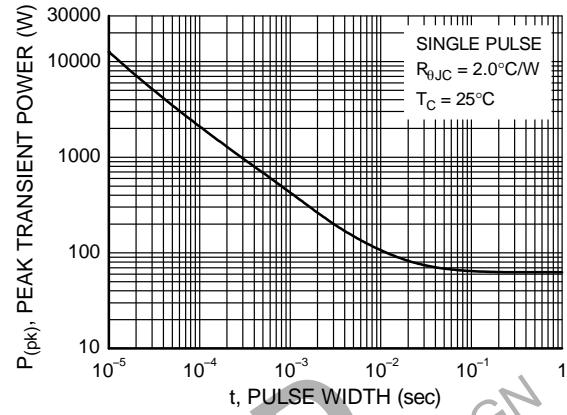


Figure 12. Single Pulse Maximum Power Dissipation

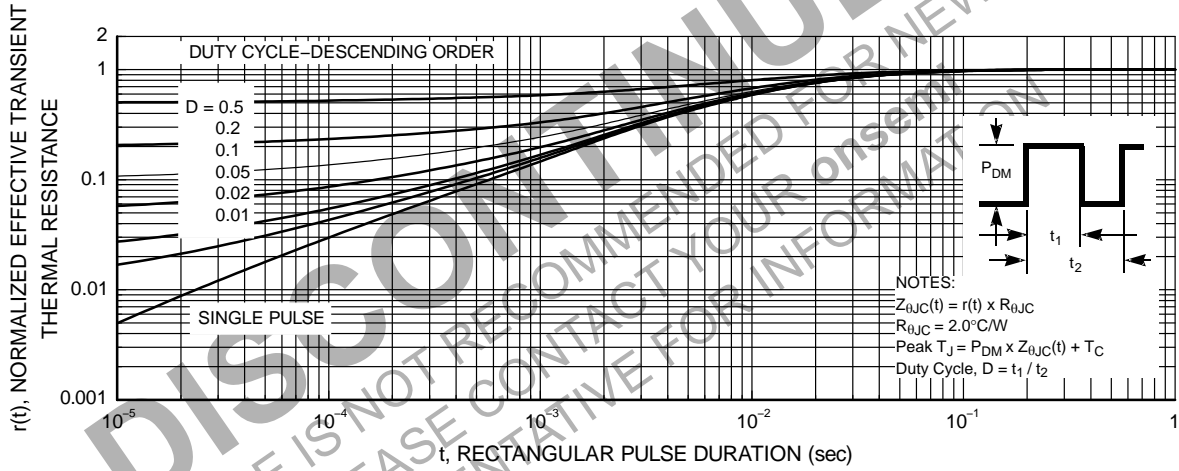


Figure 13. Junction-to-Case Transient Thermal Response Curve

## TYPICAL CHARACTERISTICS (Q2 N-CHANNEL)

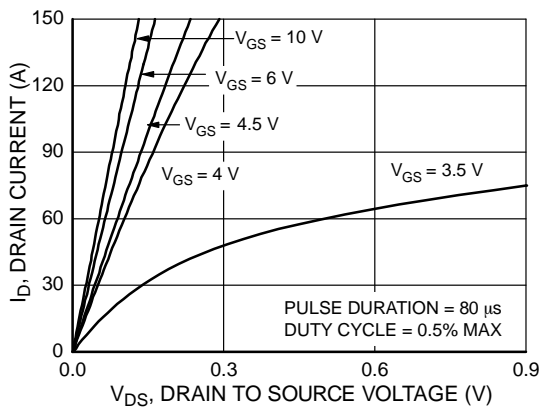
(T<sub>J</sub> = 25°C unless otherwise noted)

Figure 14. On-Region Characteristics

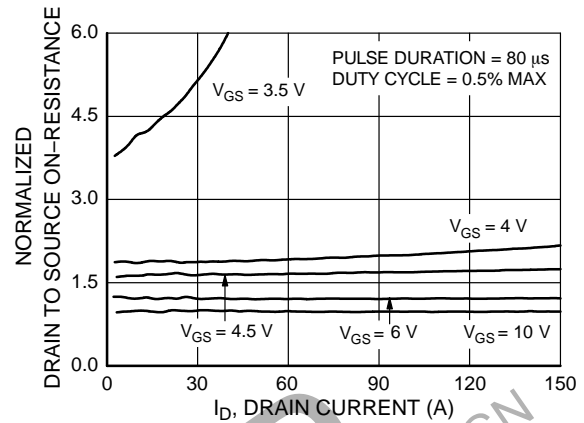


Figure 15. Normalized On-Resistance vs. Drain Current and Gate Voltage

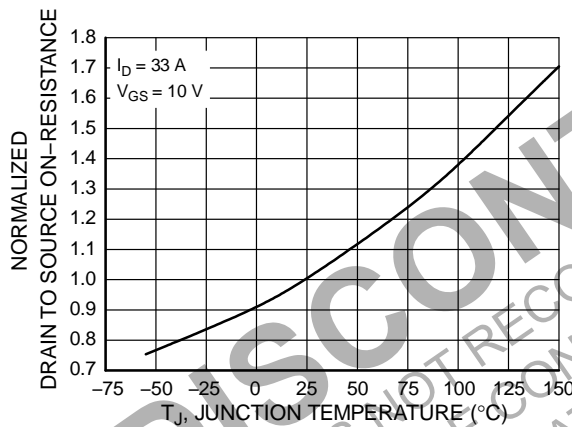


Figure 16. Normalized On Resistance vs. Junction Temperature

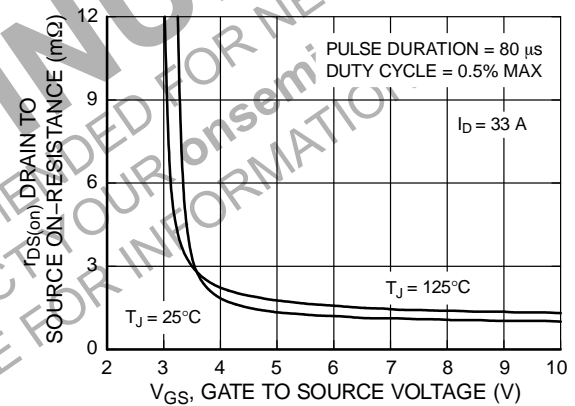


Figure 17. On-Resistance vs. Gate to Source Voltage

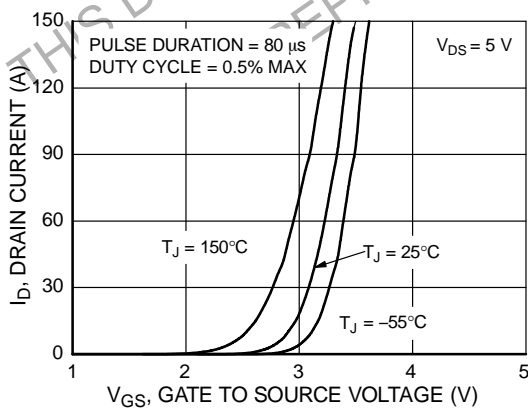


Figure 18. Transfer Characteristics

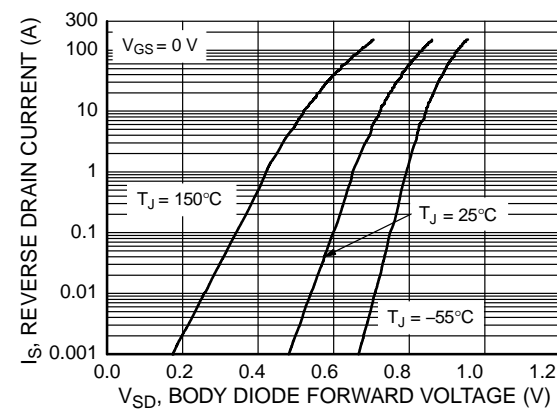


Figure 19. Source to Gate Diode Forward Voltage vs. Source Current



TYPICAL CHARACTERISTICS (Q2 N-CHANNEL)

( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

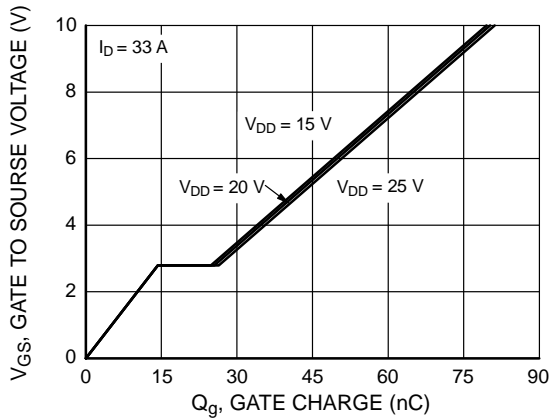


Figure 20. Gate Charge Characteristics

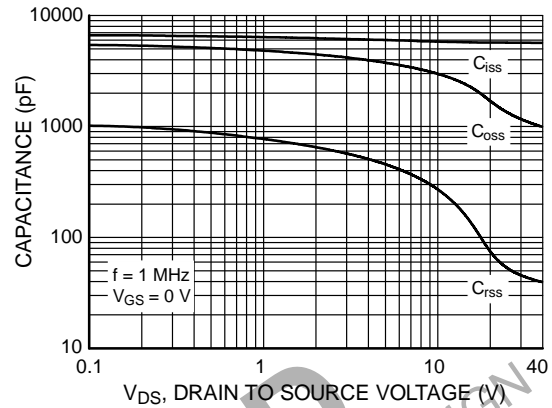


Figure 21. Capacitance vs. Drain to Source Voltage

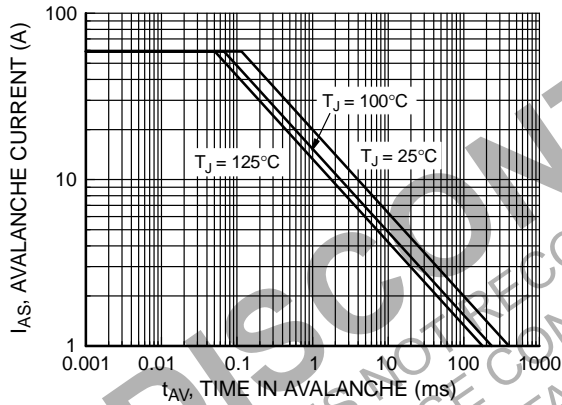


Figure 22. Unclamped Inductive Switching Capability

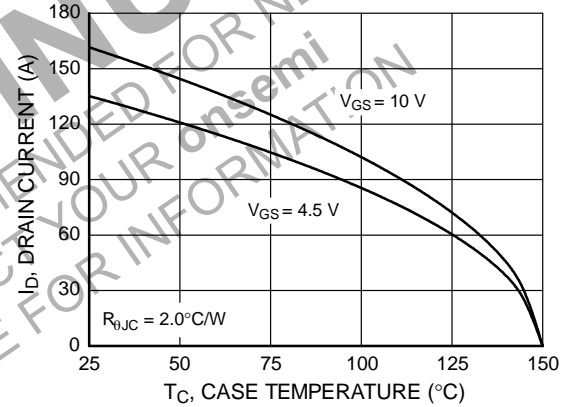


Figure 23. Maximum Continuous Drain Current vs. Case Temperature

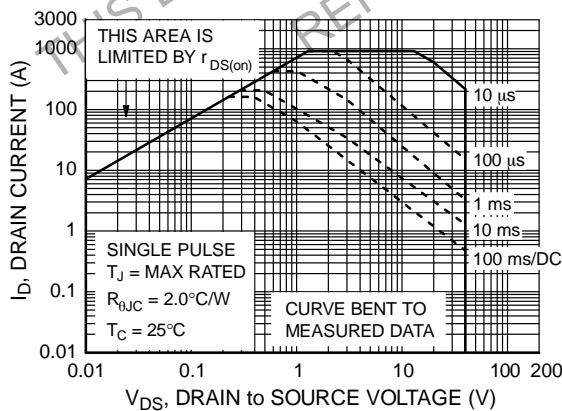


Figure 24. Forward Bias Safe Operating Area

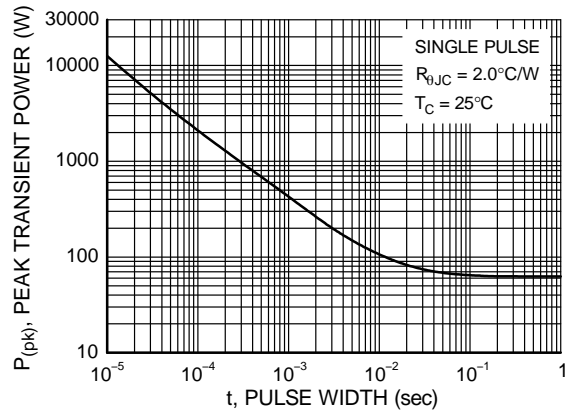


Figure 25. Single Pulse Maximum Power Dissipation



# FDMD8540L

## TYPICAL CHARACTERISTICS (Q2 N-CHANNEL)

( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

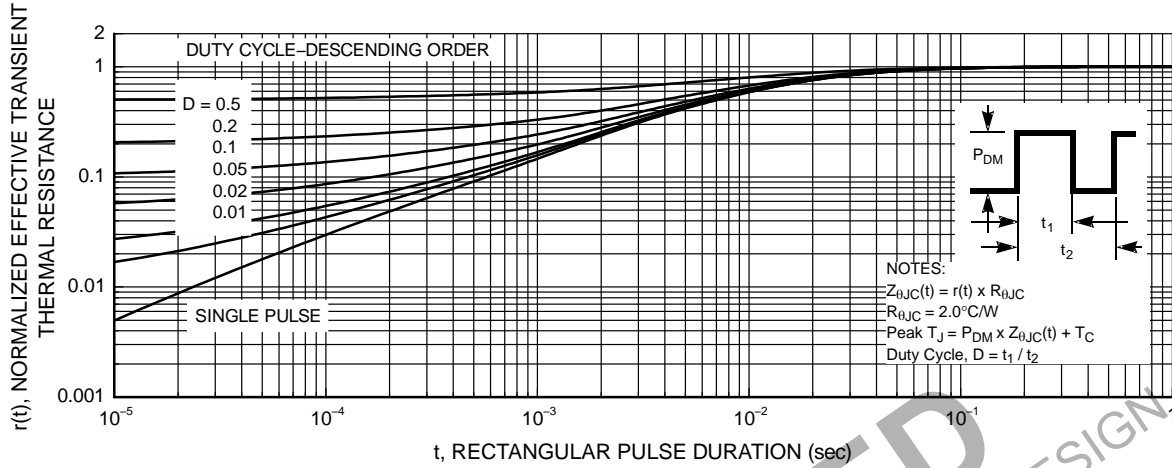


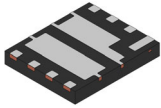
Figure 26. Junction-to-Case Transient Thermal Response Curve

### PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package Type	Reel Size	Tape Width	Shipping <sup>†</sup>
FDMD8540L	FDMD8540L	PQFN8 5X6, 1.27P Power 5 x 6 (Pb-Free)	13"	12 mm	3000 / Tape & Reel

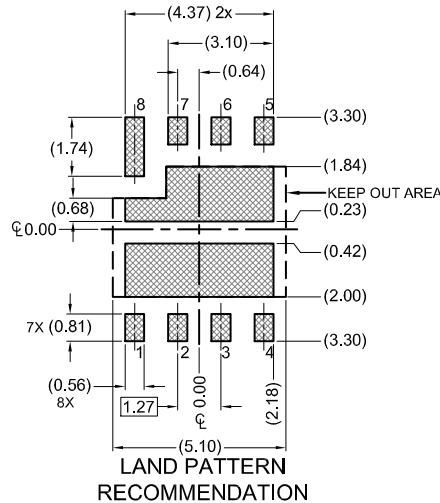
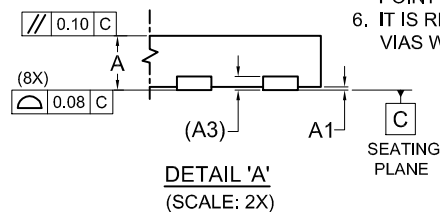
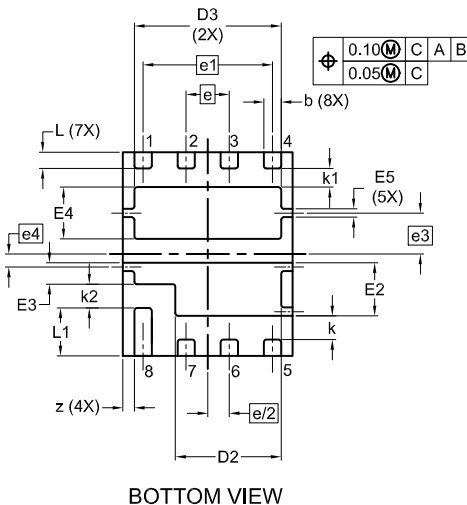
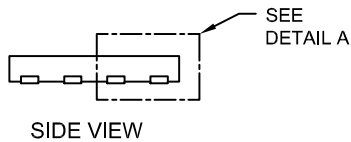
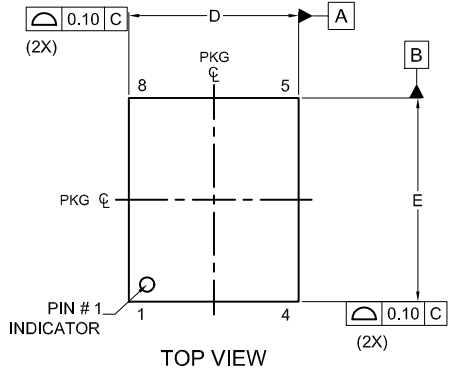
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

POWERTRENCH is registered trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.



**PQFN8 5X6, 1.27P**  
**CASE 483AT**  
**ISSUE B**

DATE 28 APR 2021



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.20 REF		
b	0.41	0.51	0.61
D	4.90	5.00	5.10
D2	3.01	3.11	3.21
D3	4.22	4.32	4.42
E	5.90	6.00	6.10
E2	1.47	1.57	1.67
E3	0.53	0.63	0.73
E4	1.42	1.52	1.62
E5	0.20	0.25	0.30
e	1.27 BSC		
e1	3.81 BSC		
e/2	0.64 BSC		
e3	1.08 BSC		
e4	0.25 BSC		
k	0.60	0.70	0.80
k1	0.45	0.55	0.65
k2	0.60	0.70	0.80
L	0.38	0.48	0.58
L1	1.31	1.41	1.51
z	0.34 REF		

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

<b>DOCUMENT NUMBER:</b>	<b>98AON13668G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>PQFN8 5X6, 1.27P</b>	<b>PAGE 1 OF 1</b>

onsemi and Onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at  
[www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)

