Automotive Grade Non-Synchronous Boost Controller

NCV8871



SOIC−8
D SUFFIX
CASE 751

The NCV8871 is an adjustable output non−synchronous boost controller which drives an external N−channel MOSFET. The device uses peak current mode control with internal slope compensation. The IC incorporates an internal regulator that supplies charge to the gate driver.

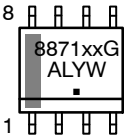
Protection features include internally−set soft−start, undervoltage lockout, cycle−by−cycle current limiting, hiccup−mode short−circuit protection and thermal shutdown.

Additional features include low quiescent current sleep mode and externally−synchronizable switching frequency.

Features

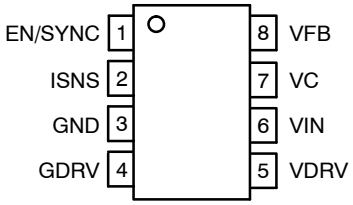
- Peak Current Mode Control with Internal Slope Compensation
- 1.2 V ±2% Reference voltage
- Fixed Frequency Operation
- Wide Input Voltage Range of 3.2 V to 40 Vdc, 45 V Load Dump
- Input Undervoltage Lockout (UVLO)
- Internal Soft−Start
- Low Quiescent Current in Sleep Mode
- Cycle−by−Cycle Current Limit Protection
- Hiccup−Mode Overcurrent Protection (OCP)
- Hiccup−Mode Short−Circuit Protection (SCP)
- Thermal Shutdown (TSD)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This is a Pb−Free Device

MARKING DIAGRAM



8871xxG = Specific Device Code
xx = 00, 03, 04, 05
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCV887100D1R2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV887103D1R2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV887104D1R2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV887105D1R2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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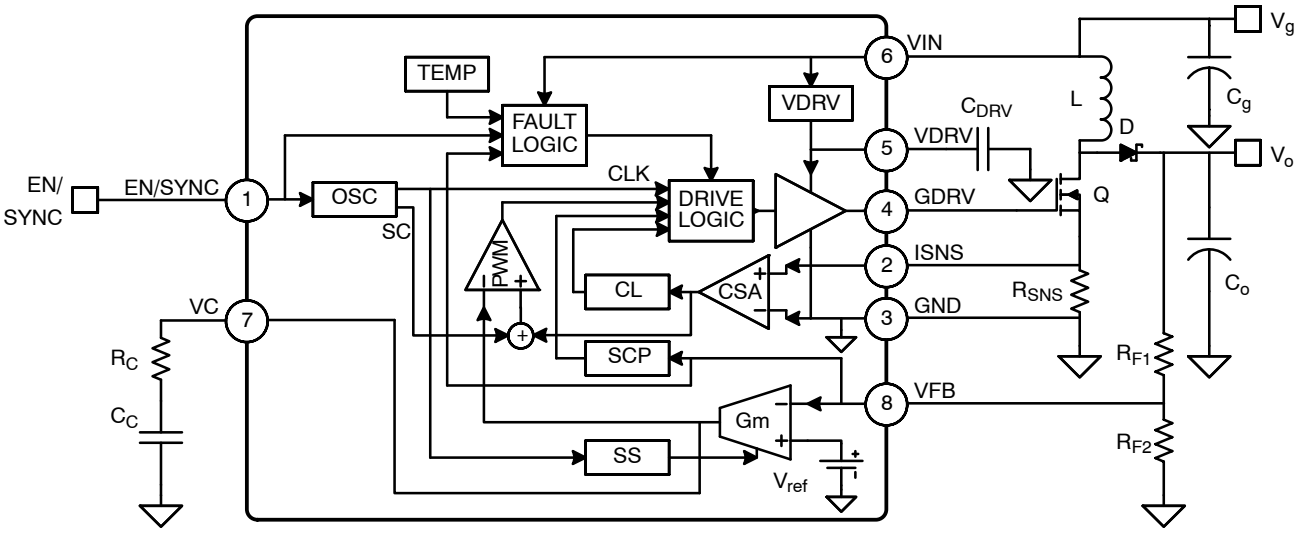


Figure 1. Simplified Block Diagram and Application Schematic

PACKAGE PIN DESCRIPTIONS

Pin No.	Pin Symbol	Function
1	EN/SYNC	Enable and synchronization input. The falling edge synchronizes the internal oscillator. The part is disabled into sleep mode when this pin is brought low for longer than the enable time−out period.
2	ISNS	Current sense input. Connect this pin to the source of the external N−MOSFET, through a current−sense resistor to ground to sense the switching current for regulation and current limiting.
3	GND	Ground reference.
4	GDRV	Gate driver output. Connect to gate of the external N−MOSFET. A series resistance can be added from GDRV to the gate to tailor EMC performance.
5	VDRV	Driving voltage. Internally−regulated supply for driving the external N−MOSFET, sourced from VIN. Bypass with a 1.0 μF ceramic capacitor to ground.
6	VIN	Input voltage. If bootstrapping operation is desired, connect a diode from the input supply to VIN, in addition to a diode from the output voltage to VDRV and/or VIN.
7	VC	Output of the voltage error amplifier. An external compensator network from VC to GND is used to stabilize the converter.
8	VFB	Output voltage feedback. A resistor from the output voltage to VFB with another resistor from VFB to GND creates a voltage divider for regulation and programming of the output voltage.

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ABSOLUTE MAXIMUM RATINGS (Voltages are with respect to GND, unless otherwise indicated)

Rating	Value	Unit
Dc Supply Voltage (VIN)	−0.3 to 40	V
Peak Transient Voltage (Load Dump on VIN)	45	V
Dc Supply Voltage (VDRV, GDRV)	12	V
Peak Transient Voltage (VFB)	−0.3 to 6	V
Dc Voltage (VC, VFB, ISNS)	−0.3 to 3.6	V
Dc Voltage (EN/SYNC)	−0.3 to 6	V
Dc Voltage Stress (VIN − VDRV)*	−0.7 to 45	V
Operating Junction Temperature	−40 to 150	°C
Storage Temperature Range	−65 to 150	°C
Peak Reflow Soldering Temperature: Pb−Free, 60 to 150 seconds at 217°C	265 peak	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*An external diode from the input to the VIN pin is required if bootstrapping VDRV and VIN off of the output voltage.

PACKAGE CAPABILITIES

Characteristic		Value	Unit
ESD Capability (All Pins)	Human Body Model Machine Model	≥ 2.0 ≥ 200	kV V
Moisture Sensitivity Level		1	−
Package Thermal Resistance	Junction−to−Ambient, $R_{\theta JA}$ (Note 1)	100	°C/W

1. 1 in^2, 1 oz copper area used for heatsinking.

Device Variations

The NCV8871 features several variants to better fit a multitude of applications. The table below shows the typical values of parameters for the parts that are currently available.

TYPICAL VALUES

Part No.	D_{max}	f_s	t_{ss}	S_a	V_{cl}	I_{src}	I_{sink}	V_{DRV}	SCE
NCV887100	88%	170 kHz	7.4 ms	53 mV/μs	400 mV	800 mA	600 mA	10.5 V	Y
NCV887103	93%	340 kHz	3.7 ms	53 mV/μs	200 mV	575 mA	350 mA	8.4 V	Y
NCV887104	93%	340 kHz	3.7 ms	53 mV/μs	200 mV	800 mA	600 mA	8.4 V	N
NCV887105	88%	170 kHz	7.4 ms	53 mV/μs	400 mV	800 mA	600 mA	10.5 V	N

DEFINITIONS

Symbol	Characteristic	Symbol	Characteristic	Symbol	Characteristic
D_{max}	Maximum Duty Cycle	f_s	Switching Frequency	t_{ss}	Soft−Start Time
S_a	Slope Compensating Ramp	V_{cl}	Current Limit Trip Voltage	I_{src}	Gate Drive Sourcing Current
I_{sink}	Gate Drive Sinking Current	V_{DRV}	Drive Voltage	SCE	Short Circuit Enable

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ELECTRICAL CHARACTERISTICS ($-40°C < T_J < 150°C$, $3.2\ V < V_{IN} < 40\ V$, unless otherwise specified) Min/Max values are guaranteed by test, design or statistical correlation.

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
GENERAL						
Quiescent Current, Sleep Mode	$I_{q,sleep}$	V_{IN} = 13.2 V, EN = 0, T_J = 25°C	–	2.0	–	μA
Quiescent Current, Sleep Mode	$I_{q,sleep}$	V_{IN} = 13.2 V, EN = 0, $-40°C < T_J < 125°C$	–	2.0	6.0	μA
Quiescent Current, No switching	$I_{q,off}$	Into VIN pin, EN = 1, No switching	–	1.5	2.5	mA
Quiescent Current, Switching, normal operation	$I_{q,on}$	Into VIN pin, EN = 1, Switching	–	3.0	6.0	mA
OSCILLATOR						
Minimum pulse width	$t_{on,min}$		90	115	140	ns
Maximum duty cycle	D_{max}	NCV887100 NCV887103 NCV887104 NCV887105	86 91 91 86	88 93 93 88	90 95 95 90	%
Switching frequency	f_s	NCV887100 NCV887103 NCV887104 NCV887105	153 306 306 153	170 340 340 170	187 374 374 187	kHz
Soft−start time	t_{ss}	From start of switching with V_{FB} = 0 until reference voltage = V_{REF} NCV887100 NCV887103 NCV887104 NCV887105	 6.0 3.0 3.0 6.0	 7.4 3.7 3.7 7.4	 8.8 4.4 4.4 8.8	ms
Soft−start delay	$t_{ss,dly}$	From EN → 1 until start of switching with V_{FB} = 0	–	240	280	μs
Slope compensating ramp	S_a	NCV887100 NCV887103 NCV887104 NCV887105	46 46 46 46	53 53 53 53	60 60 60 60	mV/μs
ENABLE/SYNCHRONIZATION						
EN/SYNC pull−down current	$I_{EN/SYNC}$	$V_{EN/SYNC}$ = 5 V	–	5.0	10	μA
EN/SYNC input high voltage	$V_{s,ih}$	$V_{IN} > V_{UVLO}$	2.0	–	5.0	V
EN/SYNC input low voltage	$V_{s,il}$		0	–	800	mV
EN/SYNC time−out ratio	$\%t_{en}$	From SYNC falling edge, to oscillator control (EN high) or shutdown (EN low), Percent of typical switching period	–	–	350	%
SYNC minimum frequency ratio	$\%f_{sync,min}$	Percent of f_s	–	–	80	%
SYNC maximum frequency	$f_{sync,max}$		1.1	–	–	MHz
Synchronization delay	$t_{s,dly}$	From SYNC falling edge to GDRV falling edge under open loop conditions	–	50	100	ns
Synchronization duty cycle	D_{sync}		25	–	75	%
CURRENT SENSE AMPLIFIER						
Low−frequency gain	A_{csa}	Input−to−output gain at dc, ISNS ≤ 1 V	0.9	1.0	1.1	V/V
Bandwidth	BW_{csa}	Gain of A_{csa} − 3 dB	2.5	–	–	MHz
ISNS input bias current	$I_{sns,bias}$	Out of ISNS pin	–	30	50	μA
Current limit threshold voltage	V_{cl}	Voltage on ISNS pin NCV887100 NCV887103 NCV887104 NCV887105	 360 180 180 360	 400 200 200 400	 440 220 220 440	mV
Current limit, Response time	t_{cl}	CL tripped until GDRV falling edge, $V_{ISNS} = V_{cl}(typ) + 60\ mV$	–	80	125	ns

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ELECTRICAL CHARACTERISTICS (−40°C < T_J < 150°C, 3.2 V < V_{IN} < 40 V, unless otherwise specified) Min/Max values are guaranteed by test, design or statistical correlation.

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
CURRENT SENSE AMPLIFIER						
Overcurrent protection, Threshold voltage	%V_{ocp}	Percent of V_{cl}	125	150	175	%
Overcurrent protection, Response Time	t_{ocp}	From overcurrent event, Until switching stops, V_{ISNS} = V_{OCP} + 40 mV	–	–	125	ns
VOLTAGE ERROR OPERATIONAL TRANSCONDUCTANCE AMPLIFIER						
Transconductance	$g_{m,vea}$	V_{FB} − V_{ref} = ± 20 mV	0.8	1.2	1.63	mS
VEA output resistance	$R_{o,vea}$		2.0	–	–	MΩ
VFB input bias current	$I_{vfb,bias}$	Current out of VFB pin	–	0.5	2.0	μA
Reference voltage	V_{ref}		1.176	1.200	1.224	V
VEA maximum output voltage	$V_{c,max}$		2.5	–	–	V
VEA minimum output voltage	$V_{c,min}$		–	–	0.3	V
VEA sourcing current	$I_{src,vea}$	VEA output current, Vc = 2.0 V	80	100	–	μA
VEA sinking current	$I_{snk,vea}$	VEA output current, Vc = 0.7 V	80	100	–	μA
GATE DRIVER						
Sourcing current	I_{src}	V_{DRV} ≥ 6 V, V_{DRV} − V_{GDRV} = 2 V NCV887100 NCV887103 NCV887104 NCV887105	 600 400 600 600	 800 575 800 800	 – – – –	mA
Sinking current	I_{sink}	V_{GDRV} ≥ 2 V NCV887100 NCV887103 NCV887104 NCV887105	 500 250 500 500	 600 350 600 600	 – – – –	mA
Driving voltage dropout	$V_{drv,do}$	V_{IN} − V_{DRV}, Iv_{DRV} = 25 mA	–	0.3	0.6	V
Driving voltage source current	I_{drv}	V_{IN} − V_{DRV} = 1 V	35	45	–	mA
Backdrive diode voltage drop	$V_{d,bd}$	V_{DRV} − V_{IN}, $I_{d,bd}$ = 5 mA	–	–	0.7	V
Driving voltage	V_{DRV}	I_{VDRV} = 0.1 − 25 mA NCV887100 NCV887103 NCV887104 NCV887105	 10 8.0 8.0 10	 10.5 8.4 8.4 10.5	 11 8.8 8.8 11	V
Pull−down resistance	R_{pd}		–	15	–	kΩ
UVLO						
Undervoltage lock−out, Threshold voltage	V_{uvlo}	V_{IN} falling	3.0	3.1	3.2	V
Undervoltage lock−out, Hysteresis	$V_{uvlo,hys}$	V_{IN} rising	50	125	200	mV

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ELECTRICAL CHARACTERISTICS ($-40°C < T_J < 150°C$, $3.2\ V < V_{IN} < 40\ V$, unless otherwise specified) Min/Max values are guaranteed by test, design or statistical correlation.

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
SHORT CIRCUIT PROTECTION						
Startup blanking period	$\%t_{scp,dly}$	From start of soft−start, Percent of t_{ss}	100	120	150	%
Hiccup−mode period	$\%t_{hcp,dly}$	From shutdown to start of soft−start, Percent of t_{ss}	70	85	100	%
Short circuit threshold voltage	$\%V_{scp}$	V_{FB} as percent of V_{ref}	60	67	75	%
Short circuit delay	t_{scp}	From $V_{FB} < V_{scp}$ to stop switching	–	35	100	ns
THERMAL SHUTDOWN						
Thermal shutdown threshold	T_{sd}	T_J rising	160	170	180	°C
Thermal shutdown hysteresis	$T_{sd,hys}$	T_J falling	10	15	20	°C
Thermal shutdown delay	$t_{sd,dly}$	From $T_J > T_{sd}$ to stop switching	–	–	100	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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TYPICAL PERFORMANCE CHARACTERISTICS

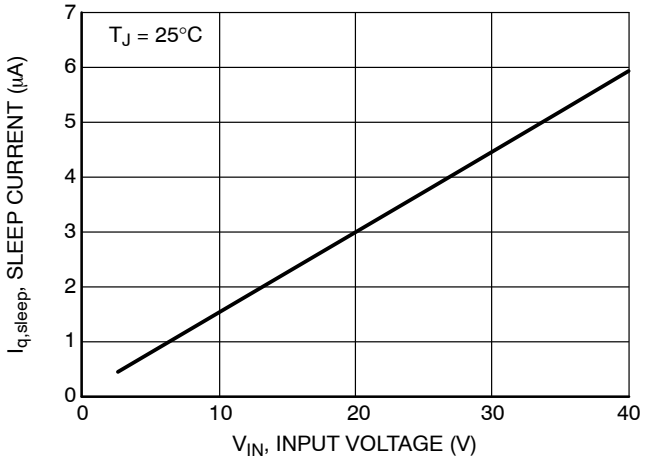


Figure 2. Sleep Current vs. Input Voltage

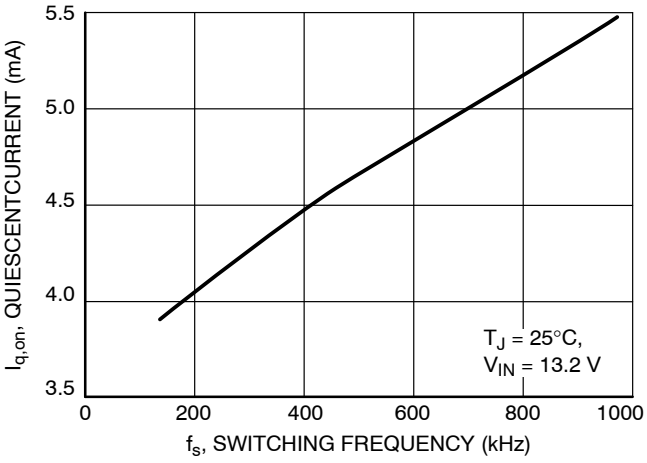


Figure 3. Quiescent Current vs. Switching Frequency

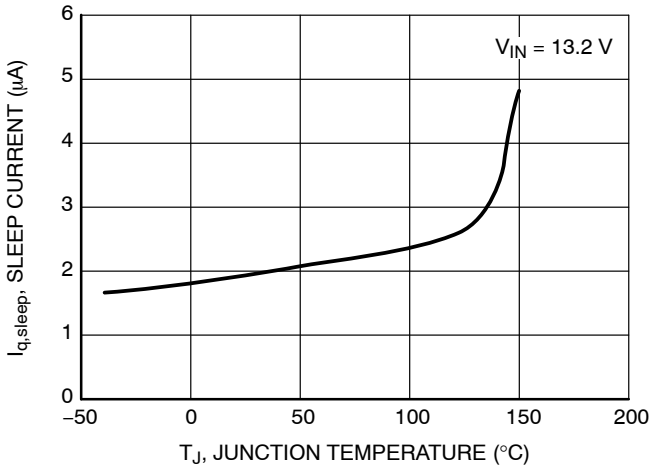


Figure 4. Sleep Current vs. Temperature

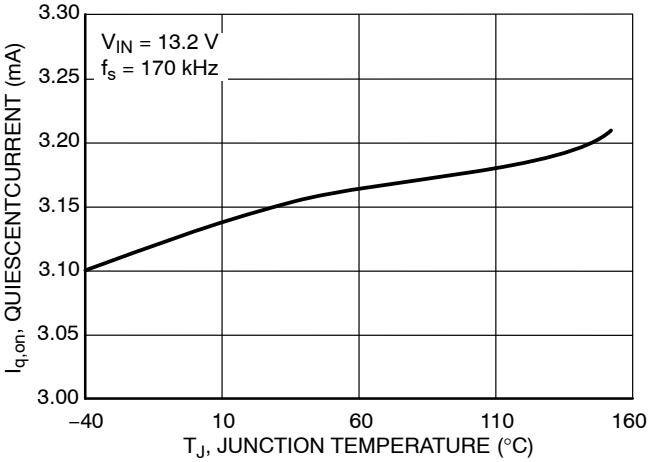


Figure 5. Quiescent Current vs. Temperature

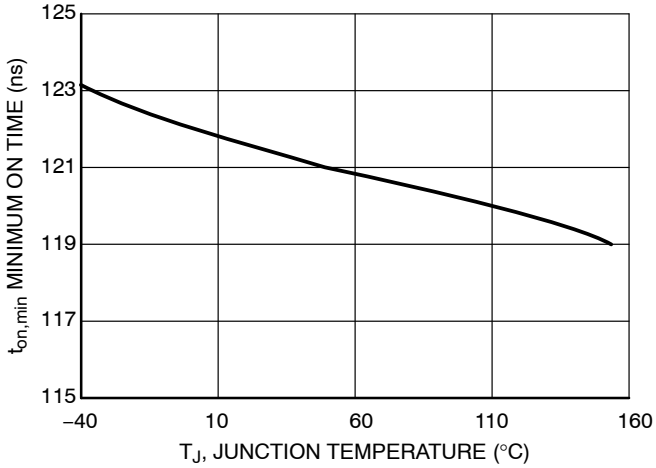


Figure 6. Minimum On Time vs. Temperature

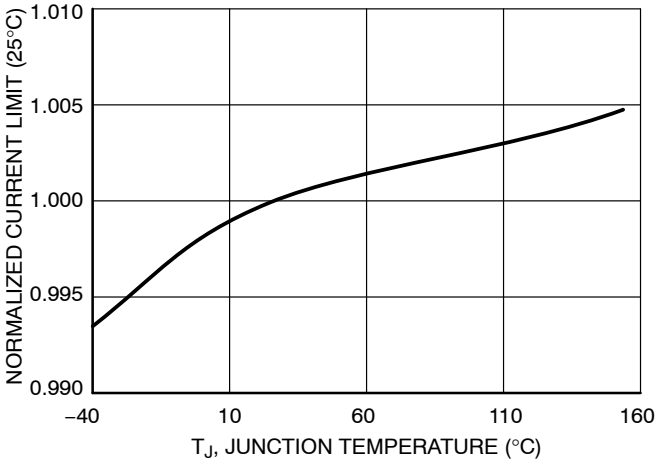


Figure 7. Normalized Current Limit vs. Temperature

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TYPICAL PERFORMANCE CHARACTERISTICS

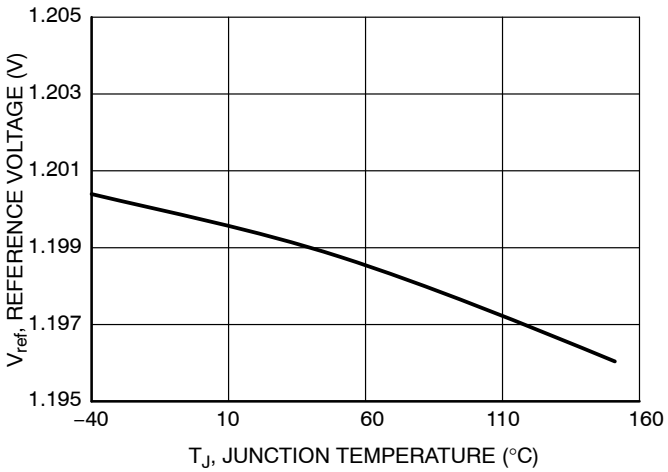


Figure 8. Reference Voltage vs. Temperature

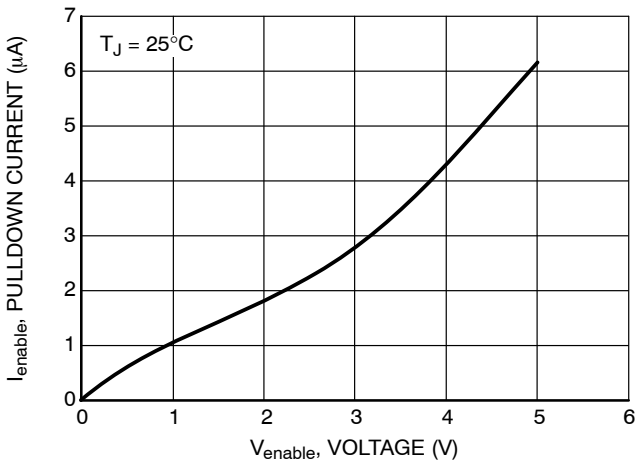


Figure 9. Enable Pulldown Current vs. Voltage

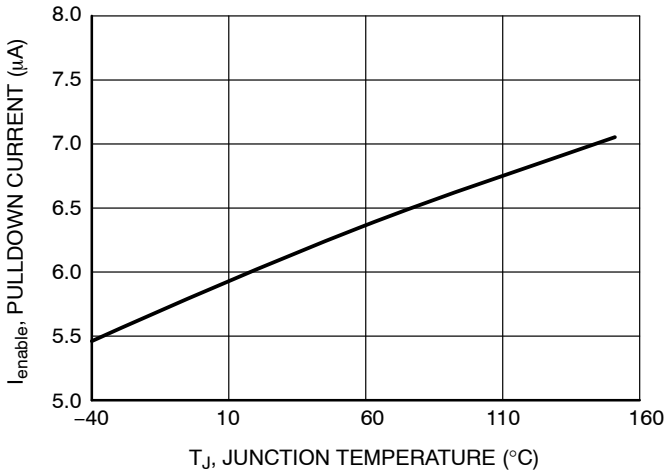


Figure 10. Enable Pulldown Current vs. Temperature

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THEORY OF OPERATION

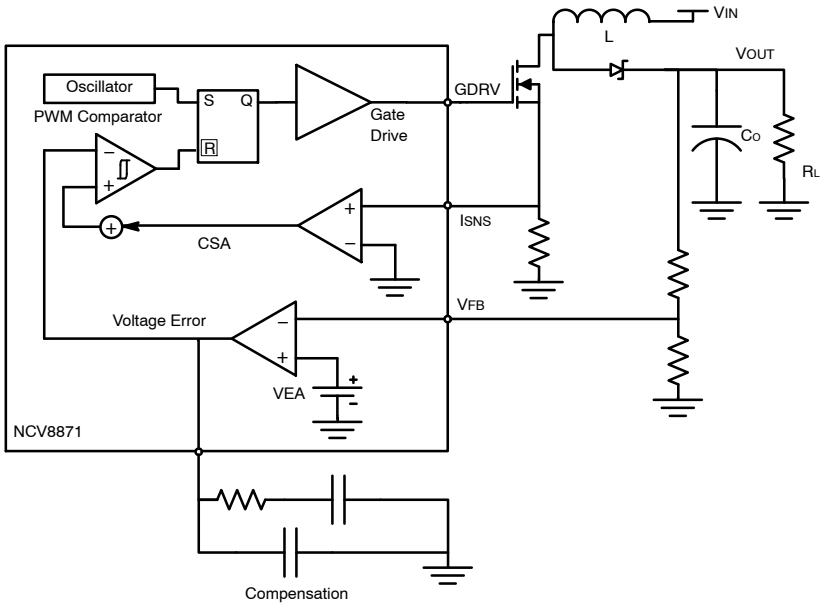


Figure 11. Current Mode Control Schematic

Current Mode Control

The NCV8871 incorporates a current mode control scheme, in which the PWM ramp signal is derived from the power switch current. This ramp signal is compared to the output of the error amplifier to control the on−time of the power switch. The oscillator is used as a fixed−frequency clock to ensure a constant operational frequency. The resulting control scheme features several advantages over conventional voltage mode control. First, derived directly from the inductor, the ramp signal responds immediately to line voltage changes. This eliminates the delay caused by the output filter and the error amplifier, which is commonly found in voltage mode controllers. The second benefit comes from inherent pulse−by−pulse current limiting by merely clamping the peak switching current. Finally, since current mode commands an output current rather than voltage, the filter offers only a single pole to the feedback loop. This allows for a simpler compensation.

The NCV8871 also includes a slope compensation scheme in which a fixed ramp generated by the oscillator is added to the current ramp. A proper slope rate is provided to improve circuit stability without sacrificing the advantages of current mode control.

Current Limit

The NCV8871 features two current limit protections, peak current mode and over current latch off. When the current sense amplifier detects a voltage above the peak current limit between ISNS and GND after the current limit leading edge blanking time, the peak current limit causes the power switch to turn off for the remainder of the cycle. Set the current limit with a resistor from ISNS to GND, with $R = V_{CL} / I_{limit}$.

If the voltage across the current sense resistor exceeds the over current threshold voltage the device enters over current hiccup mode. The device will remain off for the hiccup time and then go through the soft−start procedure.

Short Circuit Protection

If the short circuit enable bit is set (SCE = Y) the device will attempt to protect the power MOSFET from damage. When the output voltage falls below the short circuit trip voltage, after the initial short circuit blanking time, the device enters short circuit latch off. The device will remain off for the hiccup time and then go through the soft−start.

EN/SYNC

The Enable/Synchronization pin has three modes. When a dc logic high (CMOS/TTL compatible) voltage is applied to this pin the NCV8871 operates at the programmed frequency. When a dc logic low voltage is applied to this pin the NCV8871 enters a low quiescent current sleep mode. When a square wave of at least $\%f_{sync,min}$ of the free running switching frequency is applied to this pin, the switcher operates at the same frequency as the square wave. If the signal is slower than this, it will be interpreted as enabling and disabling the part. The falling edge of the square wave corresponds to the start of the switching cycle. If device is disabled, it must be disabled for 42 μs before being re−enabled.

As VIN ramps up from 0 V, and EN/SYNC is low (0 V), all die internal voltage rails are normally 0 V. If VIN of sufficient amplitude and a high slew rate is applied, these internal voltage rails may elevate momentarily due to die parasitic coupling. Elevation of the rails can inadvertently cause an internal power−on reset (POR) circuit and some internal logic to momentarily activate. With EN/SYNC is

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held low during VIN ramp, the internal voltage rails and the POR circuit will decay down to 0 V. If EN/SYNC asserts high before decay of the POR circuit, the logic could become stuck in an invalid state (no switching). To avoid the possibility for such a power up issue, the EN/SYNC signal should be applied a minimum of 500 μs after application of voltage on VIN.

If the VIN pin voltage falls below V_{UVLO} when EN/SYNC pin is at logic−high, the IC may not power up when VIN returns back above the UVLO. To resume a normal operating state, the EN/SYNC pin must be cycled with a single logic−low to logic−high transition.

UVLO

Input Undervoltage Lockout (UVLO) is provided to ensure that unexpected behavior does not occur when VIN is too low to support the internal rails and power the controller. The IC will start up when enabled and VIN surpasses the UVLO threshold plus the UVLO hysteresis and will shut down when VIN drops below the UVLO threshold or the part is disabled.

To avoid any lock state under UVLO conditions, the EN/SYNC pin should be in logic−low state. For further details, please refer to EN/SYNC paragraph.

Internal Soft−Start

To insure moderate inrush current and reduce output overshoot, the NCV8871 features a soft start which charges a capacitor with a fixed current to ramp up the reference voltage. This fixed current is based on the switching frequency, so that if the NCV8871 is synchronized to twice the default switching frequency the soft start will last half as long.

VDRV

An internal regulator provides the drive voltage for the gate driver. Bypass with a ceramic capacitor to ground to ensure fast turn on times. The capacitor should be between 0.1 μF and 1 μF, depending on switching speed and charge requirements of the external MOSFET.

APPLICATION INFORMATION

Design Methodology

This section details an overview of the component selection process for the NCV8871 in continuous conduction mode boost. It is intended to assist with the design process but does not remove all engineering design work. Many of the equations make heavy use of the small ripple approximation. This process entails the following steps:

1. Define Operational Parameters
2. Select Current Sense Resistor
3. Select Output Inductor
4. Select Output Capacitors
5. Select Input Capacitors
6. Select Feedback Resistors
7. Select Compensator Components
8. Select MOSFET(s)
9. Select Diode
10. Determine Feedback Loop Compensation Network

1. Define Operational Parameters

Before beginning the design, define the operating parameters of the application. These include:

$V_{IN(min)}$: minimum input voltage [V]
$V_{IN(max)}$: maximum input voltage [V]
V_{OUT}: output voltage [V]
$I_{OUT(max)}$: maximum output current [A]
I_{CL}: desired typical cycle-by-cycle current limit [A]

From this the ideal minimum and maximum duty cycles can be calculated as follows:

$$D_{min} = 1 - \frac{V_{IN(max)}}{V_{OUT}}$$

$$D_{max} = 1 - \frac{V_{IN(min)}}{V_{OUT}}$$

Both duty cycles will actually be higher due to power loss in the conversion. The exact duty cycles will depend on conduction and switching losses. If the maximum input voltage is higher than the output voltage, the minimum duty cycle will be negative. This is because a boost converter cannot have an output lower than the input. In situations where the input is higher than the output, the output will follow the input, minus the diode drop of the output diode and the converter will not attempt to switch.

If the calculated D_{max} is higher the D_{max} of the NCV8871, the conversion will not be possible. It is important for a boost converter to have a restricted D_{max}, because while the ideal conversion ration of a boost converter goes up to infinity as D approaches 1, a real converter's conversion ratio starts to decrease as losses overtake the increased power transfer. If the converter is in this range it will not be able to regulate properly.

If the following equation is not satisfied, the device will skip pulses at high V_{IN}:

$$\frac{D_{min}}{f_s} \geq t_{on(min)}$$

Where: f_s: switching frequency [Hz]
$t_{on(min)}$: minimum on time [s]

2. Select Current Sense Resistor

Current sensing for peak current mode control and current limit relies on the MOSFET current signal, which is measured with a ground referenced amplifier. The easiest method of generating this signal is to use a current sense resistor from the source of the MOSFET to device ground. The sense resistor should be selected as follows:

$$R_S = \frac{V_{CL}}{I_{CL}}$$

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Where: R_S: sense resistor [Ω]
V_{CL}: current limit threshold voltage [V]
I_{CL}: desire current limit [A]

3. Select Output Inductor

The output inductor controls the current ripple that occurs over a switching period. A high current ripple will result in excessive power loss and ripple current requirements. A low current ripple will result in a poor control signal and a slow current slew rate in case of load steps. A good starting point for peak to peak ripple is around 20−40% of the inductor current at the maximum load at the worst case V_{IN}, but operation should be verified empirically. The worst case V_{IN} is half of V_{OUT}, or whatever V_{IN} is closest to half of V_{OUT}. After choosing a peak current ripple value, calculate the inductor value as follows:

$$L = \frac{V_{IN(WC)}\, D_{WC}}{\Delta I_{L,max}\, f_s}$$

Where: $V_{IN(WC)}$: V_{IN} value as close as possible to half of V_{OUT} [V]
D_{WC}: duty cycle at $V_{IN(WC)}$
$\Delta I_{L,max}$: maximum peak to peak ripple [A]

The maximum average inductor current can be calculated as follows:

$$I_{L,AVG} = \frac{V_{OUT} I_{OUT(max)}}{V_{IN(min)} \eta}$$

The Peak Inductor current can be calculated as follows:

$$I_{L,peak} = I_{L,avg} + \frac{\Delta I_{L,max}}{2}$$

Where: $I_{L,peak}$: Peak inductor current value [A]

4. Select Output Capacitors

The output capacitors smooth the output voltage and reduce the overshoot and undershoot associated with line transients. The steady state output ripple associated with the output capacitors can be calculated as follows:

$$V_{OUT(ripple)} = \frac{D I_{OUT(max)}}{f C_{OUT}} + \left(\frac{I_{OUT(max)}}{1 - D} + \frac{V_{IN(min)} D}{2 f L} \right) R_{ESR}$$

The capacitors need to survive an RMS ripple current as follows:

$$I_{Cout(RMS)} = I_{OUT} \sqrt{\frac{D_{WC}}{D'_{WC}} + \frac{D_{WC}}{12} \left(\frac{D'_{WC}}{\frac{L}{R_{OUT} \times T_{SW}}} \right)^2}$$

The use of parallel ceramic bypass capacitors is strongly encouraged to help with the transient response.

5. Select Input Capacitors

The input capacitor reduces voltage ripple on the input to the module associated with the ac component of the input current.

$$I_{Cin(RMS)} = \frac{V_{IN(min)}^{\,2}\, D_{WC}}{L f_s V_{OUT} 2\sqrt{3}}$$

6. Select Feedback Resistors

The feedback resistors form a resistor divider from the output of the converter to ground, with a tap to the feedback pin. During regulation, the divided voltage will equal V_{ref}. The lower feedback resistor can be chosen, and the upper feedback resistor value is calculated as follows:

$$R_{upper} = R_{lower} \frac{(V_{out} - V_{ref})}{V_{ref}}$$

The total feedback resistance (R_{upper} + R_{lower}) should be in the range of 1 kΩ – 100 kΩ.

7. Select Compensator Components

Current Mode control method employed by the NCV8871 allows the use of a simple, Type II compensation to optimize the dynamic response according to system requirements.

8. Select MOSFET(s)

In order to ensure the gate drive voltage does not drop out the MOSFET(s) chosen must not violate the following inequality:

$$Q_{g(total)} \le \frac{I_{drv}}{f_s}$$

Where: $Q_{g(total)}$: Total Gate Charge of MOSFET(s) [C]
I_{drv}: Drive voltage current [A]
f_s: Switching Frequency [Hz]

The maximum RMS Current can be calculated as follows:

$$I_{Q(max)} = I_{out} \frac{\sqrt{D}}{D'}$$

The maximum voltage across the MOSFET will be the maximum output voltage, which is the higher of the maximum input voltage and the regulated output voltaged:

$$V_{Q(max)} = V_{OUT(max)}$$

9. Select Diode

The output diode rectifies the output current. The average current through diode will be equal to the output current:

$$I_{D(avg)} = I_{OUT(max)}$$

Additionally, the diode must block voltage equal to the higher of the output voltage and the maximum input voltage:

$$V_{D(max)} = V_{OUT(max)}$$

The maximum power dissipation in the diode can be calculated as follows:

$$P_D = V_{f(max)}\, I_{OUT(max)}$$

Where: P_d: Power dissipation in the diode [W]
$V_{f(max)}$: Maximum forward voltage of the diode [V]

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10. Determine Feedback Loop Compensation Network

The purpose of a compensation network is to stabilize the dynamic response of the converter. By optimizing the compensation network, stable regulation response is achieved for input line and load transients.

Compensator design involves the placement of poles and zeros in the closed loop transfer function. Losses from the boost inductor, MOSFET, current sensing and boost diode losses also influence the gain and compensation expressions. The OTA has an ESD protection structure ($R_{ESD} \approx 502\ \Omega$, data not provided in the datasheet) located on the die between the OTA output and the IC package compensation pin (VC). The information from the OTA PWM feedback control signal (V_{CTRL}) may differ from the IC-VC signal if R_2 is of similar order of magnitude as R_{ESD}. The compensation and gain expressions which follow take influence from the OTA output impedance elements into account.

Type-I compensation is not possible due to the presence of R_{ESD}. The Figures 12 and 13 compensation networks correspond to a Type-II network in series with R_{ESD}. The resulting control-output transfer function is an accurate mathematical model of the IC in a boost converter topology. The model does have limitations and a more accurate SPICE model should be considered for a more detailed analysis:

- The attenuating effect of large value ceramic capacitors in parallel with output electrolytic capacitor ESR is not considered in the equations.
- The CCM Boost control-output transfer function includes operating efficiency as a correction factor to improve modeling accuracy under low input voltage and high output current operating conditions where operating losses becomes significant.

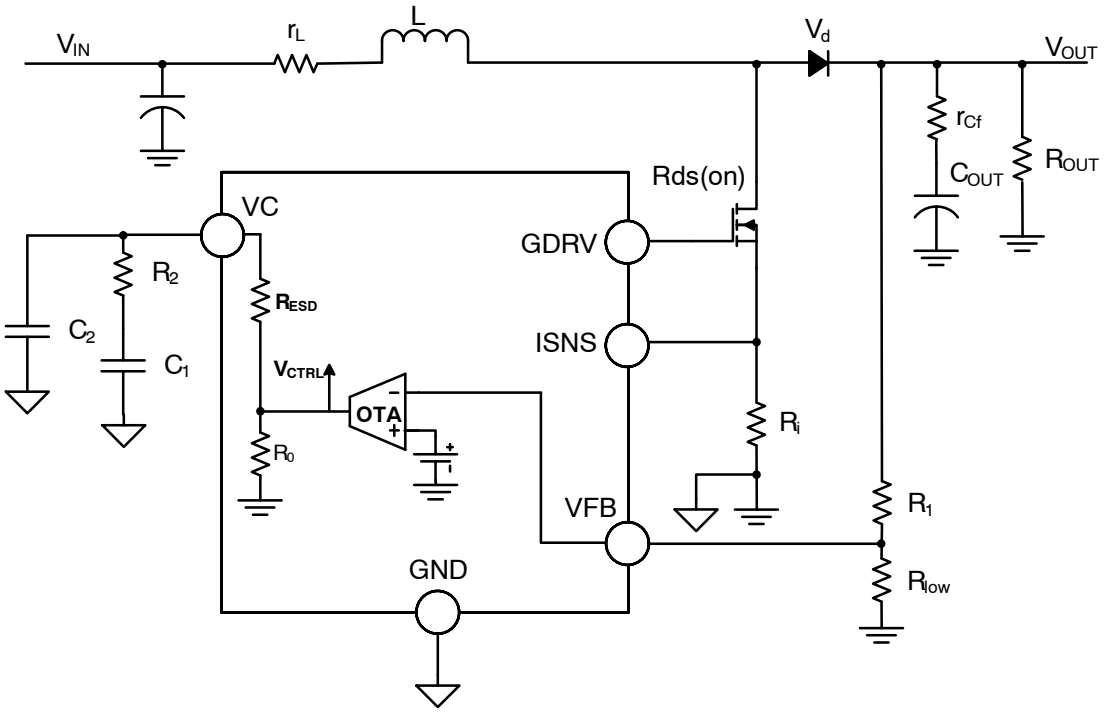


Figure 12. NCV8871 Boost Converter OTA and Compensation

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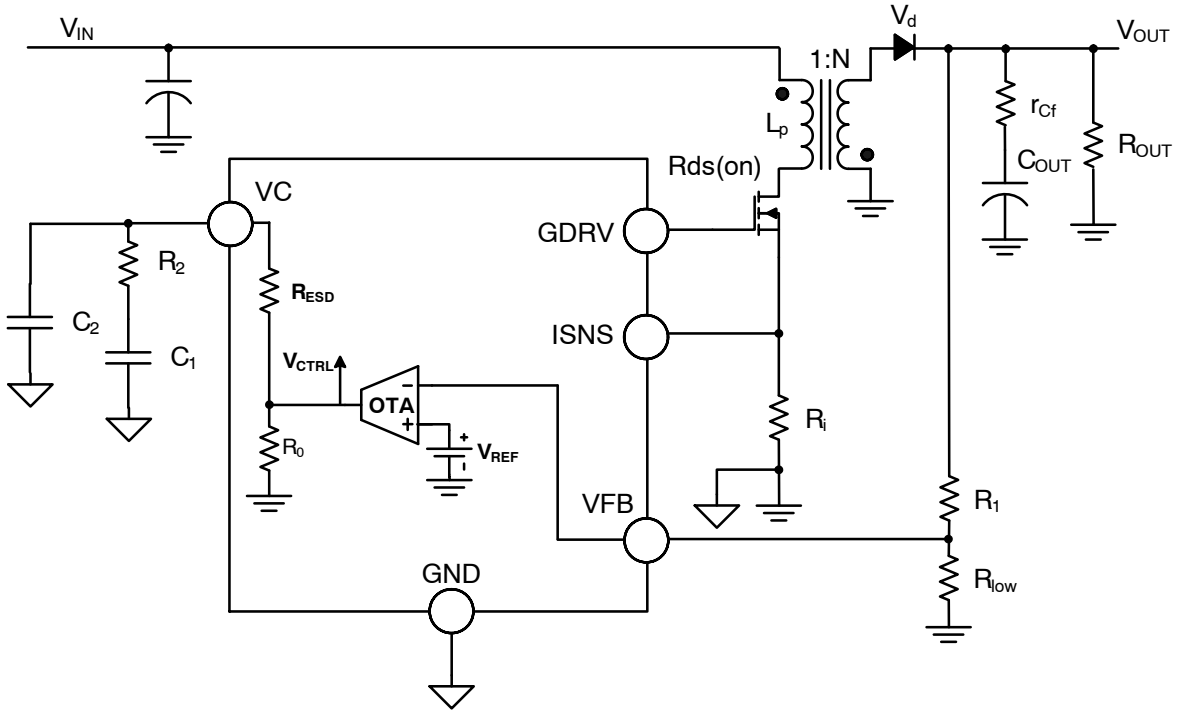


Figure 13. NCV8871 Flyback Converter OTA and Compensation

The following equations may be used to select compensation components R_2, C_1, C_2 for Figures 12 & 13 power supply. Required input design parameters for analysis are:

V_d = Output diode V_f (V)

V_{IN} = Power supply input voltage (V)

$N = N_s/N_p$ (Flyback transformer turns ratio)

R_i = Current sense resistor (Ω)

$R_{DS(on)}$ = MOSFET $R_{DS(on)}$ (Ω)
($R_{sw_eq} = R_{DS(on)} + R_i$ for the boost continuous conduction mode (CCM) expressions)

C_{OUT} = Bulk output capacitor value (F)

r_{CF} = Bulk output capacitor ESR (Ω)

R_{OUT} = Equivalent resistance of output load (Ω)

P_{out} = Output Power (W)

L = Boost inductor value or flyback transformer primary side inductance (H)

r_L = Boost inductor ESR (Ω)

$T_s = 1/f_s$, where f_s = clock frequency (Hz)

R_1 and R_{low} = Feedback resistor divider values used to set the output voltage (Ω)

V_{OUT} = Device specific output voltage (defined by R_1 and R_{low} values) (V)

R_0 = OTA output resistance = 3 MΩ

S_a = IC slope compensation (e.g. 53 mV/μs for NCV887100)

g_m = OTA transconductance = 1.2 mS

D = Controller duty ratio

D' = 1 − D

Necessary equations for describing the modulator gain (V_{ctrl}-to-V_{out} gain) $H_{ctrl_output}(f)$ are described next. Boost continuous conduction mode (CCM) and discontinuous conduction mode (DCM) transfer function expressions are summarized in Table 1. Flyback CCM and DCM transfer function expressions are summarized in Table 2.

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Table 1. BOOST CCM AND DCM TRANSFER FUNCTION EXPRESSIONS

	CCM	DCM
Duty Ratio (**D**)	$\frac{\left[2R_{OUT}V_dV_{IN}-\left[R_{sw_eq}+R_{OUT}\left(\frac{V_{IN}}{V_{OUT}}-2\right)\right]V_{OUT}^{\ 2} -V_{OUT}\sqrt{R_{OUT}\left(\begin{array}{c}R_{OUT}V_{IN}^{\ 2}+2R_{sw_eq}V_{IN}V_{OUT}-4V_dR_{sw_eq}V_{IN}\\ -4R_{sw_eq}V_{OUT}^{\ 2}-4r_LV_dV_{IN}-4r_LV_{OUT}^{\ 2}\end{array}\right)+R_{sw_eq}^{\ 2}V_{OUT}^{\ 2}}\right]}{2R_{OUT}\left(V_{OUT}^{\ 2}+V_dV_{IN}\right)}$	$\sqrt{2\tau_L M(M-1)}$ Where: $\tau_L=\frac{L}{R_{OUT}T_s}$
V_{OUT}/V_{IN} DC Voltage Gain (**M**)	$\frac{1}{1-D}\left[1-\frac{(1-D)V_d}{V_{out}}\right]\left[\frac{1}{1+\frac{1}{(1-D)^2\left(\frac{r_L+DR_{sw_eq}}{R_{OUT}}\right)}}\right]$	$\frac{1}{2}\left(1+\sqrt{1+\frac{2D^2}{\tau_L}}\right)$
Inductor On-slope (S_n), V/s	$\frac{V_{IN}-I_{Lave}\left(r_L+R_{sw_eq}\right)}{L}R_i$ Where average inductor current: $I_{Lave}=\frac{P_{out}}{V_{IN}\eta}$	$\frac{V_{IN}}{L}R_i$
Compensation Ramp (m_c)	$1+\frac{S_a}{S_n}$	$1+\frac{S_a}{S_n}$
C_{out} ESR Zero (ω_{z1})	$\frac{1}{r_{CF}C_{OUT}}$	$\frac{1}{r_{CF}C_{OUT}}$
Right-Half-Plane Zero (ω_{z2})	$\frac{(1-D)^2}{L}\left(R_{OUT}-\frac{r_{CF}R_{OUT}}{r_{CF}+R_{OUT}}\right)-\frac{r_L}{L}$	$\frac{R_{OUT}}{M^2L}$
Low Frequency Modulator Pole (ω_{p1})	$\frac{\frac{2}{R_{OUT}}+\frac{T_s}{LM^3}m_c}{C_{OUT}}$	$\frac{1}{R_{CF}C_{OUT}}\cdot\frac{2M-1}{M-1}$
High Frequency Modulator Pole (ω_{p2})	–	$2F_{SW}\left(\frac{1-\frac{1}{M}}{D}\right)^2$
Sampling Double Pole (ω_n)	$\frac{\pi}{T_s}$	–
Sampling Quality Coefficient (Q_p)	$\frac{1}{\pi\left(m_c(1-D)-0.5\right)}$	–
F_m	$\frac{1}{2M+\frac{R_{OUT}T_s}{LM^2}\left(\frac{1}{2}+\frac{S_a}{S_n}\right)}$	$\frac{1}{S_n m_c T_s}$
H_d	$\frac{\eta R_{OUT}}{R_i}$	$\frac{2V_{OUT}}{D}\cdot\frac{M-1}{2M-1}$
Control-Output Transfer Function ($H_{ctrl_output}(f)$)	$F_m H_d\frac{\left(1+j\frac{2\pi f}{\omega_{z1}}\right)\left(1-j\frac{2\pi f}{\omega_{z2}}\right)}{\left(1+j\frac{2\pi f}{\omega_{p1}}\right)\left(1+j\frac{2\pi f}{\omega_n Q_p}+\left(j\frac{2\pi f}{\omega_n}\right)^2\right)}$	$F_m H_d\frac{\left(1+j\frac{2\pi f}{\omega_{z1}}\right)\left(1-j\frac{2\pi f}{\omega_{z2}}\right)}{\left(1+j\frac{2\pi f}{\omega_{p1}}\right)\left(1+j\frac{2\pi f}{\omega_{p2}}\right)}$

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Table 2. FLYBACK CCM AND DCM TRANSFER FUNCTION EXPRESSIONS

	CCM	DCM
Duty ratio (**D**)	$\frac{V_{OUT}}{V_{OUT} + NV_{IN}}$	$\frac{V_{OUT}}{NV_{IN}}\sqrt{2\tau_L}$ Where: $\tau_L = \frac{N^2 L_p}{T_s R_{OUT}}$
V_{OUT}/V_{IN} DC Conversion Ratio (**M**)	$\frac{N \cdot D}{1 - D}$	$\frac{N \cdot D}{\sqrt{2 \cdot \tau_L}}$
Inductor On-slope (S_n), V/s	$\frac{V_{IN}}{L_p} R_i$	$\frac{V_{IN}}{L_p} R_i$
Compensation Ramp (m_c)	$1 + \frac{S_a}{S_n}$	$1 + \frac{S_a}{S_n}$
C_{out} ESR Zero (ω_{z1})	$\frac{1}{r_{CF} C_{OUT}}$	$\frac{1}{r_{CF} C_{OUT}}$
Right-Half-Plane Zero (ω_{z2})	$\frac{(1 - D)^2 R_{OUT}}{D L_p N^2}$	$\frac{R_{OUT}}{N^2 L_p} \cdot \frac{1}{M (M + 1)}$
Modulator Pole (ω_{p1})	$\frac{\frac{D'^3}{\tau_L}\left(1 + 2\frac{S_a}{S_n}\right) + 1 + D}{R_{OUT} C_{OUT}}$	$\frac{2}{R_{OUT} C_{OUT}}$
ω_{p2}	–	$2F_{SW}\left(\frac{\frac{1}{D}}{1 + \frac{1}{M}}\right)^2$
F_m	$\frac{1}{\frac{D'^2}{\tau_L}\left(1 + 2\frac{S_a}{S_n}\right) + 2M + 1}$	$\frac{1}{S_n m_c T_s}$
H_d	$\frac{R_{OUT}}{R_i N}$	$V_{IN}\sqrt{\frac{1}{2\tau_L}}$
Control-output Transfer Function ($H_{ctrl_output}(f)$)	$F_m H_d \frac{\left(1 + j\frac{2\pi f}{\omega_{z1}}\right)\left(1 - j\frac{2\pi f}{\omega_{z2}}\right)}{\left(1 + j\frac{2\pi f}{\omega_{p1}}\right)}$	$F_m H_d \frac{\left(1 + j\frac{2\pi f}{\omega_{z1}}\right)\left(1 - j\frac{2\pi f}{\omega_{z2}}\right)}{\left(1 + j\frac{2\pi f}{\omega_{p1}}\right)\left(1 + j\frac{2\pi f}{\omega_{p2}}\right)}$

Once the desired cross-over frequency (f_c) gain adjustment and necessary phase boost are determined from the $H_{ctrl_output}(f)$ gain and phase plots, the Table 3 equations may be used. It should be noted that minor compensation component value adjustments may become necessary when $R_2 \leq \sim 10 \cdot R_{esd}$ as a result of approximations for determining components R_2, C_1, C_2.

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Table 3. OTA COMPENSATION TRANSFER FUNCTION AND COMPENSATION VALUES

Desired OTA Gain at Cross-over Frequency f_c (***G***)	$10^{\frac{\text{desired_G}_{\text{fc_gain_db}}}{20}}$
Desired Phase Boost at Cross-over Frequency f_c (***boost***)	$\left(\theta_{\text{margin}} - \arg\left(H_{\text{ctrl_output}}(\text{fc})\right)\frac{180^\circ}{\pi} - 90^\circ\right)\frac{\pi}{180^\circ}$
Select OTA Compensation Zero to Coincide with Modulator Pole at f_{p1} (f_z)	$\frac{\omega_{\text{p1e}}}{2\pi}$
Resulting OTA High Frequency Pole Placement (f_p)	$\frac{f_z f_c + f_c^{\,2}\tan(\text{boost})}{f_c - f_z\tan(\text{boost})}$
Compensation Resistor R_2	$\frac{f_p G}{f_p - f_z}\,\frac{V_{OUT}}{1.2\,g_m}\,\frac{\sqrt{1+\left(\frac{f_c}{f_p}\right)^2}}{\sqrt{1+\left(\frac{f_z}{f_p}\right)}}$
Compensation Capacitor C_1	$\frac{1}{2\pi f_z R_2}$
Compensation Capacitor C_2	$\frac{1}{2\pi f_p G}\cdot\frac{R_{low}\,g_m}{R_{low}+R_1}$
OTA DC Gain (G_{0_OTA})	$\frac{R_{low}}{R_{low}+R_1}\cdot g_m\cdot R_0$
Low Frequency Zero (ω_{z1e})	$\frac{1}{2}\frac{(R_2+R_{esd})}{R_2R_{esd}C_2}\left[1-\sqrt{1-4\frac{R_2R_{esd}C_2}{(R_2+R_{esd})^2C_1}}\right]$
High Frequency Zero (ω_{z2e})	$\frac{1}{2}\frac{(R_2+R_{esd})}{R_2R_{esd}C_2}\left[1+\sqrt{1-4\frac{R_2R_{esd}C_2}{(R_2+R_{esd})^2C_1}}\right]$
Low Frequency Pole (ω_{p1e})	$\frac{1}{2}\frac{(R_0+R_2+R_{esd})}{R_2(R_0+R_{esd})C_2}\left[1-\sqrt{1-4\frac{R_2(R_0+R_{esd})C_2}{(R_0+R_2+R_{esd})^2C_1}}\right]$
High Frequency Pole (ω_{p2e})	$\frac{1}{2}\frac{(R_0+R_2+R_{esd})}{R_2(R_0+R_{esd})C_2}\left[1+\sqrt{1-4\frac{R_2(R_0+R_{esd})C_2}{(R_0+R_2+R_{esd})^2C_1}}\right]$
OTA Transfer Function ($G_{OTA}(f)$)	$-G_{0_OTA}\frac{\left(1+j\frac{2\pi f}{\omega_{z1e}}\right)}{\left(1+j\frac{2\pi f}{\omega_{p1e}}\right)}\frac{\left(1+j\frac{2\pi f}{\omega_{z2e}}\right)}{\left(1+j\frac{2\pi f}{\omega_{p2e}}\right)}$

The open-loop-response in closed-loop form to verify the gain/phase margins may be obtained from the following expression.

$$T(f) = G_{OTA}(f)\,H_{ctrl_output}(f)$$

Low Voltage Operation

If the input voltage drops below the UVLO or MOSFET threshold voltage, another voltage may be used to power the device. Simply connect the voltage you would like to boost to the inductor and connect the stable voltage to the VIN pin of the device. In boost configuration, the output of the converter can be used to power the device. In some cases it may be desirable to connect 2 sources to VIN pin, which can be accomplished simply by connecting each of the sources through a diode to the VIN pin.

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SEPIC TOPOLOGY APPLICATION INFORMATION

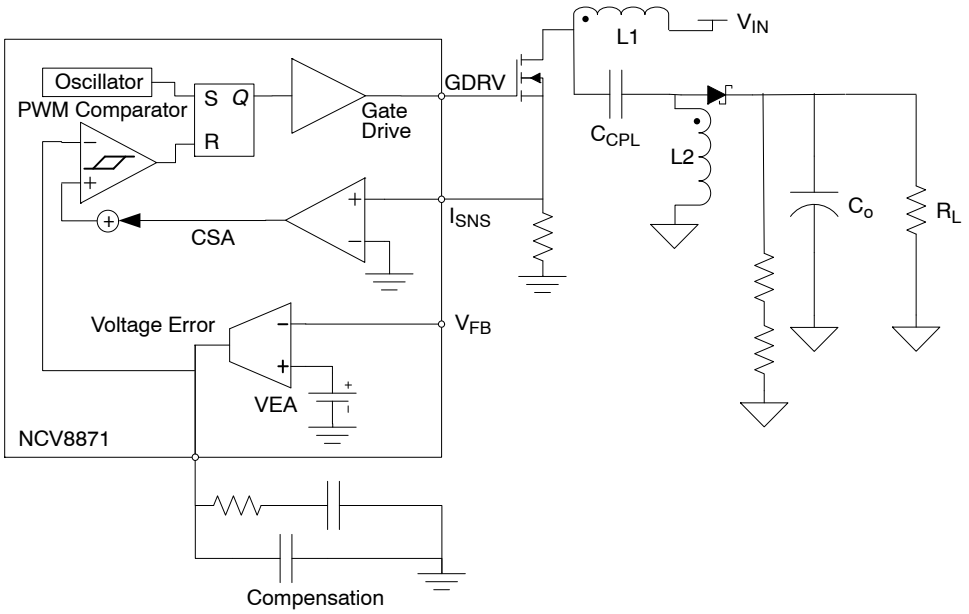


Figure 14. SEPIC Current Mode Schematic

SEPIC Design Methodology

This section details an overview of the component selection process for the NCV8871 in continuous conduction mode SEPIC. It is intended to assist with the design process but does not remove all engineering design work. Many of the equations make heavy use of the small ripple approximation. This process entails the following steps:

1. Define Operational Parameters
2. Select Current Sense Resistor
3. Select SEPIC Inductors
4. Select Coupling Capacitor
5. Select Output Capacitors
6. Select Input Capacitors
7. Select Feedback Resistors
8. Select Compensator Components
9. Select MOSFET(s)
10. Select Diode

1. Define Operational Parameters

Before beginning the design, define the operating parameters of the application. These include:

$V_{IN(min)}$: minimum input voltage [V]
$V_{IN(max)}$: maximum input voltage [V]
V_{OUT}: output voltage [V]
$I_{OUT(max)}$: maximum output current [A]
I_{CL}: desired typical cycle−by−cycle current limit [A]

From this the ideal minimum and maximum duty cycles can be calculated as follows:

$$D_{min} = \frac{V_{OUT}}{V_{IN(max)} + V_{OUT}}$$

$$D_{max} = \frac{V_{OUT}}{V_{IN(min)} + V_{OUT}}$$

Both duty cycles will actually be higher due to power loss in the conversion. The exact duty cycles will depend on conduction and switching losses.

If the calculated D_{WC} (worst case) is higher than the D_{max} limit of the NCV8871, the conversion will not be possible. It is important for a SEPIC converter to have a restricted D_{max}, because while the ideal conversion ratio of a SEPIC converter goes up to infinity as D approaches 1, a real converter's conversion ratio starts to decrease as losses overtake the increased power transfer. If the converter is in this range it will not be able to regulate properly.

If the following equation is not satisfied, the device will skip pulses at high V_{IN}:

$$\frac{D_{min}}{f_s} \geq t_{on(min)}$$

Where: f_s: switching frequency [Hz]
$t_{on(min)}$: minimum on time [s]

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2. Select Current Sense Resistor

Current sensing for peak current mode control and current limit relies on the MOSFET current signal, which is measured with a ground referenced amplifier. Note that the I_{CL} equals the sum of the currents from both inductors. The easiest method of generating this signal is to use a current sense resistor from the source of the MOSFET to device ground. The sense resistor should be selected as follows:

$$R_S = \frac{V_{CL}}{I_{CL}}$$

Where: R_S: sense resistor [Ω]
V_{CL}: current limit threshold voltage [V]
I_{CL}: desire current limit [A]

3. Select SEPIC Inductors

The output inductor controls the current ripple that occurs over a switching period. A high current ripple will result in excessive power loss and ripple current requirements. A low current ripple will result in a poor control signal and a slow current slew rate in case of load steps. A good starting point for peak to peak ripple is around 20−40% of the inductor current at the maximum load at the worst case V_{IN}, but operation should be verified empirically. The worst case V_{IN} is the minimum input voltage. After choosing a peak current ripple value, calculate the inductor value as follows:

$$L = \frac{V_{IN(WC)}\, D_{WC}}{\Delta I_{L,max}\, f_s}$$

Where: $V_{IN(WC)}$: V_{IN} value as close as possible to half of V_{OUT} [V]
D_{WC}: duty cycle at $V_{IN(WC)}$
$\Delta I_{L,max}$: maximum peak to peak ripple [A]

The maximum average inductor current can be calculated as follows:

$$I_{L,AVG} = \frac{V_{OUT}\, I_{OUT(max)}}{V_{IN(min)}\eta}$$

The Peak Inductor current can be calculated as follows:

$$I_{L1,peak} = I_{L1,avg} + \frac{\Delta I_{L1}}{2}$$

$$I_{L2,peak} = I_{OUT(max)} + \frac{\Delta I_{L2}}{2}$$

Where (if L1 = L2): $\Delta I_{L1} = \Delta I_{L2}$

4. Select Coupling Capacitor

Coupling capacitor RMS current is significant. A low ESR ceramic capacitor is required as a coupling capacitor. Selecting a capacitor value too low will result in high capacitor ripple voltage which will distort ripple current and diminish input line regulation capability. Budgeting 2−5% coupling capacitor ripple voltage is a reasonable guideline.

$$\Delta V_{coupling} = \frac{I_{out}\, D_{WC}}{C_{coupling}\, f_s}$$

Current mode control helps resolve some of the resonant frequencies that create issues in voltage mode SEPIC converter designs, but some resonance issues may occur. A resonant frequency exists at

$$f_{resonance} = \frac{1}{2\pi\sqrt{(L1 + L2)C_{coupling}}}$$

It may become necessary to place an RC damping network in parallel with the coupling capacitor if the resonance is within ~1 decade of the closed−loop crossover frequency. The capacitance of the damping capacitor should be ~5 times that of the coupling capacitor. The optimal damping resistance (including the ESR of the damping capacitor) is calculated as

$$R_{damping} = \sqrt{\frac{L1 + L2}{C_{coupling}}}$$

5. Select Output Capacitors

The output capacitors smooth the output voltage and reduce the overshoot and undershoot associated with line transients. The steady state output ripple associated with the output capacitors can be calculated as follows:

$$V_{OUT(ripple)} = \frac{I_{OUT(max)} D_{WC}}{C_{OUT}\, f_s} + \left(\frac{I_{OUT(max)}}{1 - D_{WC}} + \frac{D_{WC} V_{IN(min)}}{2\, f_s L_2}\right) R_{esr}$$

The capacitors need to survive an RMS ripple current as follows:

$$I_{Cout(RMS)} = \sqrt{I_{OUT(max)}{}^2\, D_{WC} + \left(I_a^2 + \frac{I_r^2}{3} - I_a I_r\right) D'_{WC}}$$

where

$$I_a = I_{L1_peak} + I_{L2_peak} - I_{out}$$

$$I_r = \Delta I_{L1} + \Delta I_{L2}$$

The use of parallel ceramic bypass capacitors is strongly encouraged to help with the transient response.

6. Select Input Capacitors

The input capacitor reduces voltage ripple on the input to the module associated with the ac component of the input current.

$$I_{Cin(RMS)} = \frac{\Delta I_{L1}}{\sqrt{12}}$$

7. Select Feedback Resistors

The feedback resistors form a resistor divider from the output of the converter to ground, with a tap to the feedback pin. During regulation, the divided voltage will equal V_{ref}. The lower feedback resistor can be chosen, and the upper feedback resistor value is calculated as follows:

$$R_{upper} = R_{lower}\frac{(V_{out} - V_{ref})}{V_{ref}}$$

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The total feedback resistance (R_{upper} + R_{lower}) should be in the range of 1 kΩ – 100 kΩ.

8. Select Compensator Components

Current Mode control method employed by the NCV8871 allows the use of a simple, Type II compensation to optimize the dynamic response according to system requirements.

The maximum RMS Current can be calculated as follows:

$$I_{D(max)} = \sqrt{D_{WC}\left(I_{Q(peak)}{}^2 + \frac{\left(\Delta I_{L1} + \Delta I_{L2}\right)^2}{3} - I_{Q(peak)}\left(\Delta I_{L1} + \Delta I_{L2}\right)\right)}$$

where

$$I_{Q(peak)} = I_{L1_peak} + I_{L2_peak}$$

The maximum voltage across the MOSFET will be the maximum output voltage, which is the higher of the maximum input voltage and the regulated output voltaged:

$$V_{Q(max)} = V_{OUT(max)} + V_{IN(max)}$$

9. Select MOSFET(s)

In order to ensure the gate drive voltage does not drop out the MOSFET(s) chosen must not violate the following inequality:

$$Q_{g(total)} \leq \frac{I_{drv}}{f_s}$$

Where: $Q_{g(total)}$: Total Gate Charge of MOSFET(s) [C]
I_{drv}: Drive voltage current [A]
f_s: Switching Frequency [Hz]

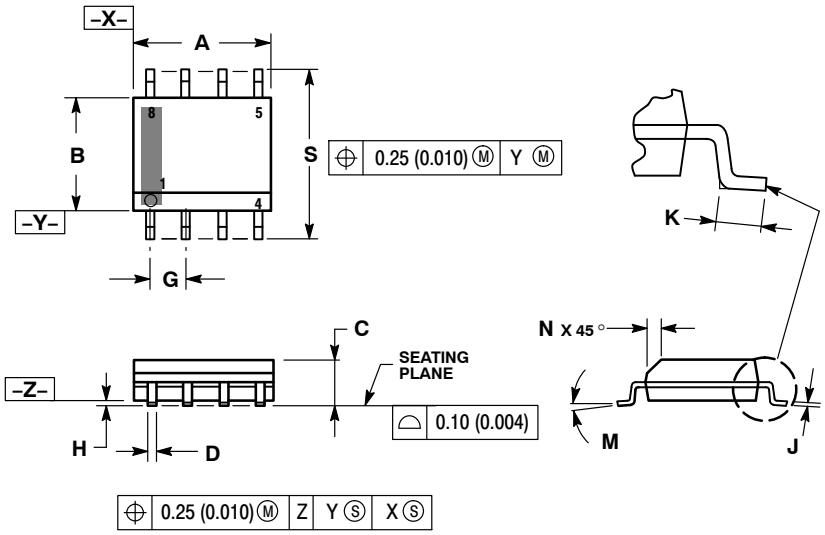
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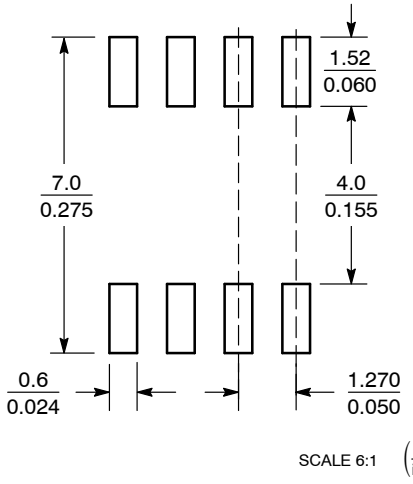
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NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

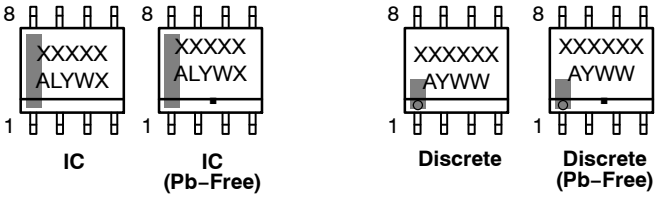
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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