



# PI7VD9008ABH

## Adaptive EQ 8-channel 960H Video Decoder

### General Features

- Real time AEQ 8-channel Video/Audio decoder for WD1(960H) and D1 cameras
- Built-in Adaptive Equalizer(AEQ) for the best picture image in the several hundred meter coax cable condition
- Proprietary Pericom AEQ technology recover weak, noisy, or unstable analog input signals
- Resilient SYNC TIP detection to lock video signal in a noisy environment
- Programmable sharpness, CTI, hue, saturation, contrast and brightness
- Support time multiplexed format of ITU-R BT.656 output with 54/108MHz or 72/144MHz
- Provides a programmable mapping from four or eight (non-real-time) analog video inputs to four BT.656 digital outputs
- NTSC(M), NTSC 4.43, PAL (B, D, G, H, I, M, Nc, 60) standard support
- High performance 5H comb filter for all NTSC/PAL standards
- Built-in 10-bit audio Codec to allow 10 analog audio inputs and 1 audio output
- Mixed audio analog output for multiple audio channels with multiple audio sample rates for 8, 16, 32, 44.1, 48KHz audio frequency
- Two serial audio formats (I2S and DSP) are supported for recording/mixing output and playback input
- Selectable Master and Slave serial audio interface
- Integrated video PLL for 108MHz, 144MHz clock output
- Two-wire serial interface(I2C) for register access
- Industrial grade temperature support (-40°C ~ 85°C)
- Packages: 128-pin LQFP

### Description

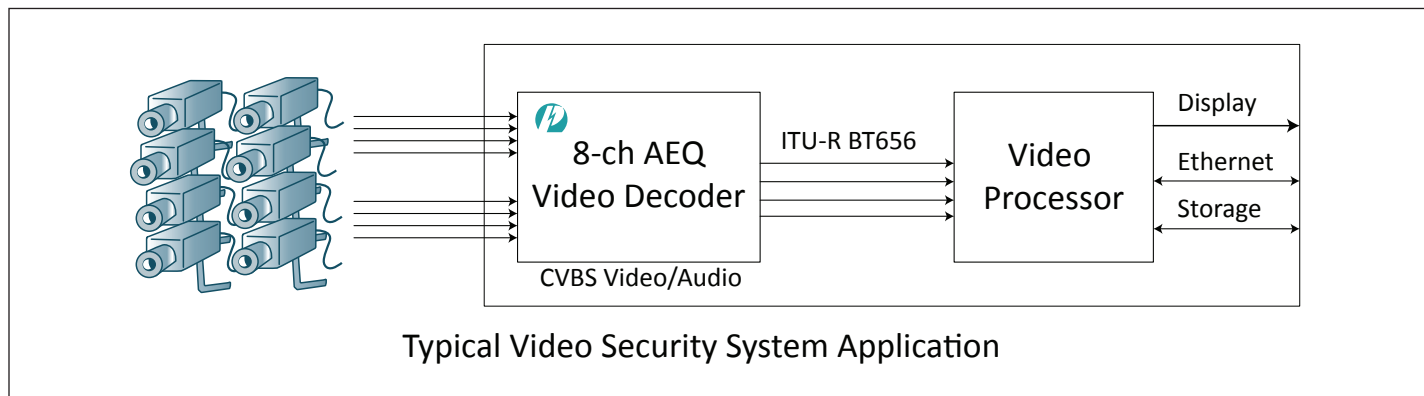
PI7VD9008ABH is AEQ 8-Channel Video Decoders and Audio Codec. Built-in Adaptive equalizer (AEQ) recover the noisy signals caused by long or small wire gauge Coax cables and display the best picture image view quality. The video decoder converts NTSC, PAL analog composite video broadcasting signal (CVBS) into digital components YCbCr for video controller or processor to perform pre-view, compression and storage etc. The converted digital video streams complying with ITU-R BT.656 are transported in time multiplexed format, which contains one, two or four video channels.

Single 27MHz reference crystal clock support NTSC, PAL and 960H standard resolution. Each video channel contains 10-bit ADC, proprietary clamp, automatic gain controller and 5H comb filter for separating luminance & chrominance to reduce artificial noise.

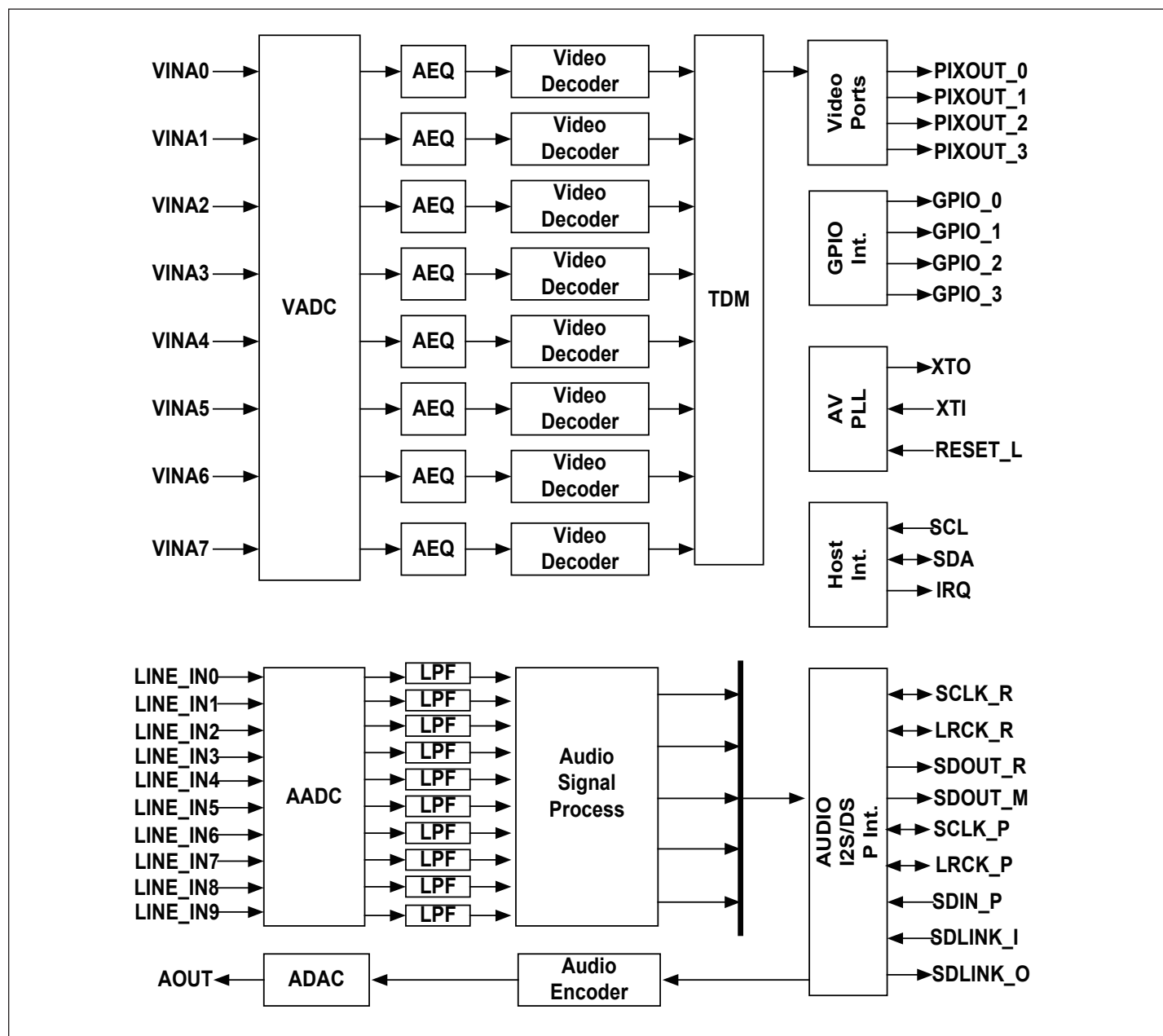
### Application

- Video Security DVRs
- Automotive Camera Driver Assistant Systems
- Video Capture Cards

### PI7VD9008ABH System Application Diagram

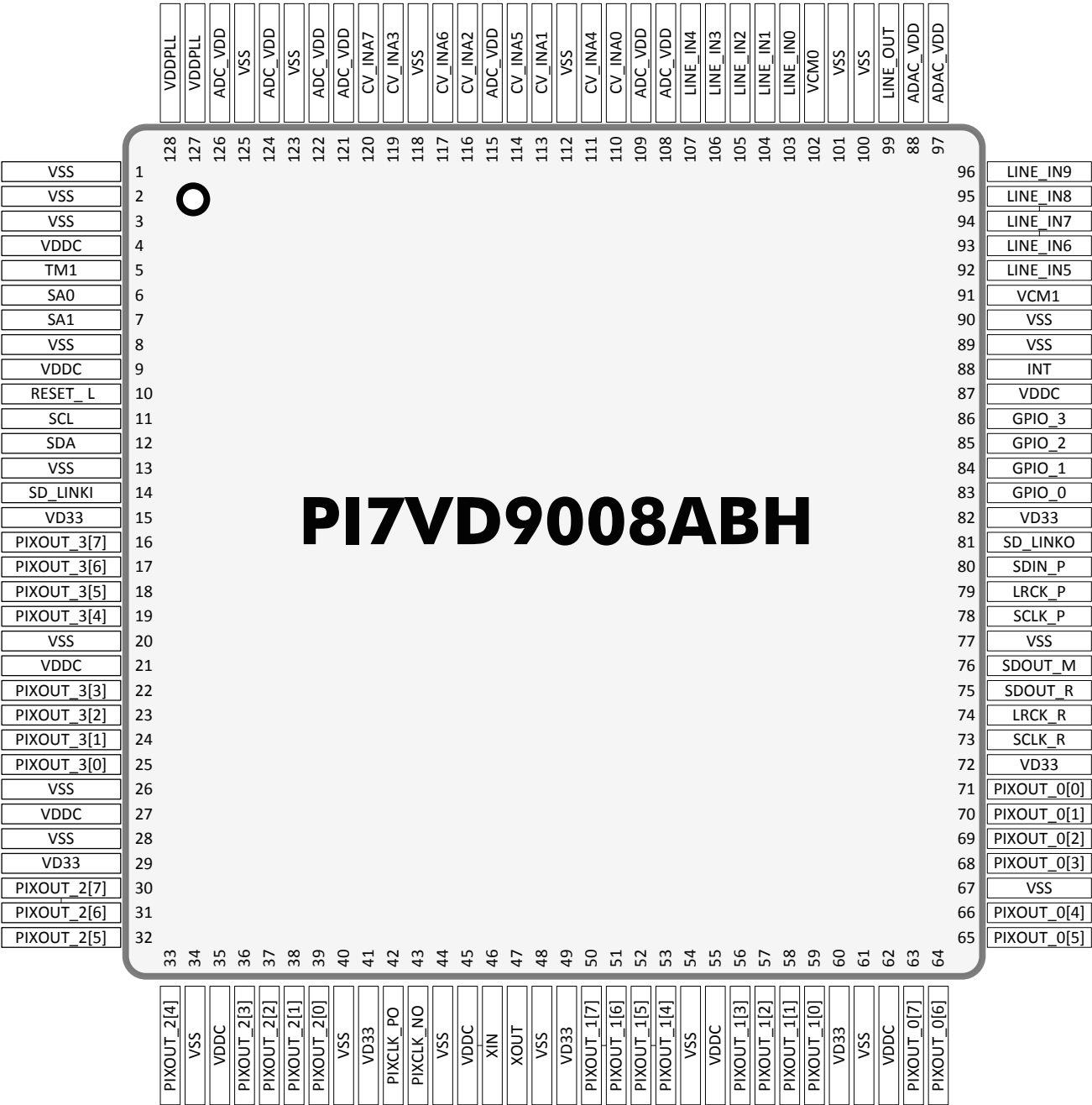


## PI7VD9008ABH Block Diagram



|                         |                                                                                                    |
|-------------------------|----------------------------------------------------------------------------------------------------|
| Video input sources:    | CV_INA0, CV_INA1, CV_INA2, CV_INA3, CV_INA4, CV_INA5, CV_INA6, CV_INA7                             |
| BT.656 TDM ports:       | PIXOUT_0, PIXOUT_1, PIXOUT_2 and PIXOUT_3                                                          |
| Audio input sources:    | LINE_IN0, LINE_IN1, LINE_IN2, LINE_IN3, LINE_IN4, LINE_IN5, LINE_IN6, LINE_IN7, LINE_IN8, LINE_IN9 |
| I2S/DSP Audio Interface | (SCLK_R, LRCK_R, SDOUT_R and SDOUT_M), (SCLK_P, LRCK_P and SDIN_P), (SD_LINKI, SD_LINKO)           |

Pin Configuration(128-LQFP)



## Pin Configuration (128-LQFP)

| Pin | Name        | Pin | Name        | Pin | Name        | Pin | Name     |
|-----|-------------|-----|-------------|-----|-------------|-----|----------|
| 1   | VSS         | 33  | PIXOUT_2[4] | 65  | PIXOUT_0[5] | 97  | ADAC_VDD |
| 2   | VSS         | 34  | VSS         | 66  | PIXOUT_0[4] | 98  | ADAC_VDD |
| 3   | VSS         | 35  | VDDC        | 67  | VSS         | 99  | LINE_OUT |
| 4   | VDDC        | 36  | PIXOUT_2[3] | 68  | PIXOUT_0[3] | 100 | VSS      |
| 5   | TM1         | 37  | PIXOUT_2[2] | 69  | PIXOUT_0[2] | 101 | VSS      |
| 6   | SA0         | 38  | PIXOUT_2[1] | 70  | PIXOUT_0[1] | 102 | VCM0     |
| 7   | SA1         | 39  | PIXOUT_2[0] | 71  | PIXOUT_0[0] | 103 | LINE_IN0 |
| 8   | VSS         | 40  | VSS         | 72  | VD33        | 104 | LINE_IN1 |
| 9   | VDDC        | 41  | VD33        | 73  | SCLK_R      | 105 | LINE_IN2 |
| 10  | RESET_L     | 42  | PIXCLK_PO   | 74  | LRCK_R      | 106 | LINE_IN3 |
| 11  | SCL         | 43  | PIXCLK_NO   | 75  | SDOUT_R     | 107 | LINE_IN4 |
| 12  | SDA         | 44  | VSS         | 76  | SDOUT_M     | 108 | ADC_VDD  |
| 13  | VSS         | 45  | VDDC        | 77  | VSS         | 109 | ADC_VDD  |
| 14  | SD_LINKI    | 46  | XIN         | 78  | SCLK_P      | 110 | CV_INA0  |
| 15  | VD33        | 47  | XOUT        | 79  | LRCK_P      | 111 | CV_INA4  |
| 16  | PIXOUT_3[7] | 48  | VSS         | 80  | SDIN_P      | 112 | VSS      |
| 17  | PIXOUT_3[6] | 49  | VD33        | 81  | SD_LINKO    | 113 | CV_INA1  |
| 18  | PIXOUT_3[5] | 50  | PIXOUT_1[7] | 82  | VD33        | 114 | CV_INA5  |
| 19  | PIXOUT_3[4] | 51  | PIXOUT_1[6] | 83  | GPIO_0      | 115 | ADC_VDD  |
| 20  | VSS         | 52  | PIXOUT_1[5] | 84  | GPIO_1      | 116 | CV_INA2  |
| 21  | VDDC        | 53  | PIXOUT_1[4] | 85  | GPIO_2      | 117 | CV_INA6  |
| 22  | PIXOUT_3[3] | 54  | VSS         | 86  | GPIO_3      | 118 | VSS      |
| 23  | PIXOUT_3[2] | 55  | VDDC        | 87  | VDDC        | 119 | CV_INA3  |
| 24  | PIXOUT_3[1] | 56  | PIXOUT_1[3] | 88  | INT         | 120 | CV_INA7  |
| 25  | PIXOUT_3[0] | 57  | PIXOUT_1[2] | 89  | VSS         | 121 | ADC_VDD  |
| 26  | VSS         | 58  | PIXOUT_1[1] | 90  | VSS         | 122 | ADC_VDD  |
| 27  | VDDC        | 59  | PIXOUT_1[0] | 91  | VCM1        | 123 | VSS      |
| 28  | VSS         | 60  | VD33        | 92  | LINE_IN5    | 124 | ADC_VDD  |
| 29  | VD33        | 61  | VSS         | 93  | LINE_IN6    | 125 | VSS      |
| 30  | PIXOUT_2[7] | 62  | VDDC        | 94  | LINE_IN7    | 126 | ADC_VDD  |
| 31  | PIXOUT_2[6] | 63  | PIXOUT_0[7] | 95  | LINE_IN8    | 127 | VDDPLL   |
| 32  | PIXOUT_2[5] | 64  | PIXOUT_0[6] | 96  | LINE_IN9    | 128 | VDDPLL   |

**Pin-out Information****Analog Video/Audio Interface**

| Pin Name                                                                                                                     | Pin Number                                                        | Type   | Description                                                                                                                                                                                                                                                                                                                            |
|------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CV_INA0,<br>CV_INA4,<br>CV_INA1,<br>CV_INA5,<br>CV_INA2,<br>CV_INA6,<br>CV_INA3,<br>CV_INA7                                  | 110,<br>111,<br>113,<br>114,<br>116,<br>117,<br>119,<br>120       | Analog | CVBS input of Video channel 0<br>CVBS input of Video channel 4<br>CVBS input of Video channel 1<br>CVBS input of Video channel 5<br>CVBS input of Video channel 2<br>CVBS input of Video channel 6<br>CVBS input of Video channel 3<br>CVBS input of Video channel 7                                                                   |
| VCM0,<br>VCM1                                                                                                                | 102,<br>91                                                        | Analog | Connect to an external capacitor                                                                                                                                                                                                                                                                                                       |
| LINE_IN0,<br>LINE_IN1,<br>LINE_IN2,<br>LINE_IN3,<br>LINE_IN4<br>LINE_IN5,<br>LINE_IN6,<br>LINE_IN7,<br>LINE_IN8,<br>LINE_IN9 | 103,<br>104,<br>105,<br>106,<br>107<br>92<br>93<br>94<br>95<br>96 | Analog | Line input of Audio channel 0<br>Line input of Audio channel 1<br>Line input of Audio channel 2<br>Line input of Audio channel 3<br>Line input of Audio channel 4<br>Line input of Audio channel 5<br>Line input of Audio channel 6<br>Line input of Audio channel 7<br>Line input of Audio channel 8<br>Line input of Audio channel 9 |
| LINE_OUT                                                                                                                     | 99                                                                | Analog | Mixed Analog Audio Output                                                                                                                                                                                                                                                                                                              |

**Digital Video/Audio Interface**

| Pin Name      | Pin Number                     | Type   | Description                                                                                           |
|---------------|--------------------------------|--------|-------------------------------------------------------------------------------------------------------|
| PIXOUT_0[7:0] | 63, 64, 65, 66,68,69, 70,71    | Output | Bt.656 Time Multiplex Division output of port 0                                                       |
| PIXOUT_1[7:0] | 50, 51, 52, 53, 56,57,58,59    | Output | Bt.656 Time Multiplex Division output of port 1                                                       |
| PIXOUT_2[7:0] | 30, 31, 32, 33, 36, 37, 38, 39 | Output | Bt.656 Time Multiplex Division output of port 2                                                       |
| PIXOUT_3[7:0] | 16, 17, 18, 19, 22, 23, 24, 25 | Output | Bt.656 Time Multiplex Division output of port 3                                                       |
| GPIO_0        | 83                             | Output | According to register setting, it outputs GPO, HSYC, VSYNC, FDFLAG, ACTIVE and VDLOSS of channel 0, 4 |
| GPIO_1        | 84                             | Output | According to register setting, it outputs GPO, HSYC, VSYNC, FDFLAG, ACTIVE and VDLOSS of channel 1, 5 |
| GPIO_2        | 85                             | Output | According to register setting, it outputs GPO, HSYC, VSYNC, FDFLAG, ACTIVE and VDLOSS of channel 2, 6 |
| GPIO_3        | 86                             | Output | According to register setting, it outputs GPO, HSYC, VSYNC, FDFLAG, ACTIVE and VDLOSS of channel 3, 7 |

|          |    |                  |                                                                                                            |
|----------|----|------------------|------------------------------------------------------------------------------------------------------------|
| SCLK_R   | 73 | Input/<br>Output | Record audio serial clock. It is an input pin under slave mode, while output pin under master mode.        |
| LRCK_R   | 74 | Input/<br>Output | Record audio serial sync pulse. It is an input pin under slave mode, while output pin under master mode.   |
| SDOUT_R  | 75 | Output           | Record audio serial data output.                                                                           |
| SDOUT_M  | 76 | Output           | Mixing audio serial data output.                                                                           |
| SCLK_P   | 78 | Input/<br>Output | Playback audio serial clock. It is an input pin under slave mode, while output pin under master mode       |
| LRCK_P   | 79 | Input/<br>Output | Playback audio serial sync pulse. It is an input pin under slave mode, while output pin under master mode. |
| SDIN_P   | 80 | Input            | Playback audio serial data input.                                                                          |
| SD_LINKI | 14 | Input            | Chip-to-Chip audio serial data input.                                                                      |
| SD_LINKO | 81 | Output           | Chip-to-Chip audio serial data output.                                                                     |

## System Control Interface

| Pin Name  | Pin Number | Type          | Description                                                                                                    |
|-----------|------------|---------------|----------------------------------------------------------------------------------------------------------------|
| RESET_L   | 10         | Input         | Chip Reset. Active Low.                                                                                        |
| XIN       | 46         | Input         | 27MHz or 54MHz crystal input or 27MHz/54MHz/108MHz oscillator input                                            |
| XOUT      | 47         | Output        | 27MHz or 54MHz crystal output                                                                                  |
| PIXCLK_P0 | 42         | Output        | Positive Output clock signal running at 27/54/108MHz (720H mode) or 36/72/144MHz (960H mode) for bus PIXOUT_0. |
| PIXCLK_N0 | 43         | Output        | Negative Output clock signal running at 27/54/108MHz (720H mode) or 36/72/144MHz (960H mode) for bus PIXOUT_0  |
| TM1       | 5          | Input         | Test pin. Tied to VSS.                                                                                         |
| SA1       | 7          | Input         | Device Address 1 of I2C slave interface                                                                        |
| SA0       | 6          | Input         | Device Address 0 of I2C slave interface                                                                        |
| SCL       | 11         | Input         | Input clock signal of I2C slave interface                                                                      |
| SDA       | 12         | Input/ Output | Data signal of I2C slave interface                                                                             |
| INT       | 88         | Output        | Interrupt signal to system. Active High.                                                                       |

# PI7VD9008ABH

Adaptive EQ 8-channel 960H Video Decoder



## Power and Ground

| Pin Name | Pin Number                                                                                       | Type   | Description                                                             |
|----------|--------------------------------------------------------------------------------------------------|--------|-------------------------------------------------------------------------|
| VDDC     | 4, 9, 21, 27, 35, 45, 55, 62, 87                                                                 | Power  | 1.0V Power for core logic                                               |
| VD33     | 15, 29, 41, 49, 60, 72, 82                                                                       | Power  | 3.3V Power for IO pads                                                  |
| VSS      | 1, 2, 3, 8, 13, 20, 26, 28, 34, 40, 44, 48, 54, 61, 67, 77, 89, 90, 100, 101, 112, 118, 123, 125 | Ground | Ground for video ADC, audio ADC, audio DAC, PLL, core logic and IO pads |
| ADC_VDD  | 108, 109, 115, 121, 122, 124, 126                                                                | Power  | 3.3V Power for video ADC and audio ADC.                                 |
| ADAC_VDD | 97, 98                                                                                           | Power  | 3.3V Power for audio DAC                                                |
| VDDPLL   | 127, 128                                                                                         | Power  | 3.3V Power for AV PLL                                                   |

## Functional Description

### Video/Audio Analog Input

PI7VD9004ABH offers 4 channels NTSC, PAL (720H or 960H) format composite (CVBS) inputs (CV\_INA<sub>x</sub> x= 0,1,2,3,4,5,6,7). When the input signal is weak and the color burst is not able to be recognized, the video is automatically switched to Black and White mode to enhance the picture image quality.

| Format        | Lines | Field | Fsc          | Country                              |
|---------------|-------|-------|--------------|--------------------------------------|
| NTSC-M        | 525   | 60    | 3.579545 MHz | U.S., many others                    |
| NTSC-Japan    | 525   | 60    | 3.579545 MHz | Japan *                              |
| NTSC (4.43)   | 525   | 60    | 4.433619 MHz | Transcoding                          |
| PAL-B, G, N   | 625   | 50    | 4.433619 MHz | Many                                 |
| PAL-I / H / D | 625   | 50    | 4.433619 MHz | Belgium ,China Great Britain, others |
| PAL-M         | 525   | 60    | 3.575612 MHz | Brazil                               |
| PAL-CN        | 625   | 50    | 3.582056 MHz | Argentina                            |
| PAL-60        | 525   | 60    | 4.433619 MHz | China                                |

\* PNTSC-Japan has 0 IRE setup

### Clamping and Automatic Gain Control

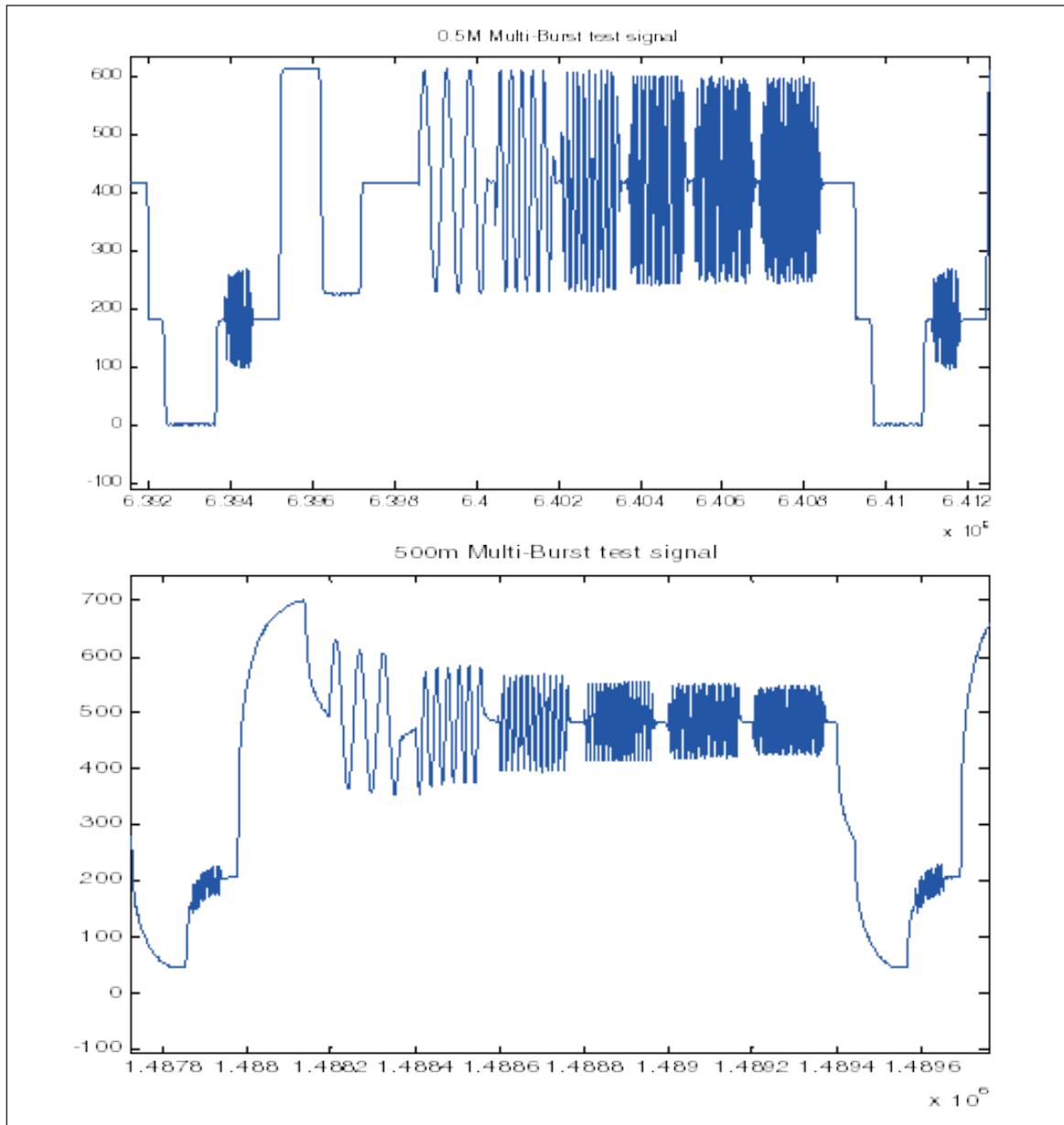
Each analog input channel has built-in clamping circuits to restore signal DC level. Automatic Gain Control (AGC) circuits in the internal video processor can compensate average input video signal level for each analog input channel. The AGC and clamping circuits prevent signal level saturation and allow the video decoder to deliver the best signal-to-noise performance. On the other hand, the AGC cooperates with the digital multiplier of video decoder to boost the weak signals. The circuits perform Automatic Gain Control through internal feedback loop. Manual gain control is also available through configuring the Video Decoder Control and Status Registers.

### Video Decoder

The video decoder in the chip converts NTSC and PAL video signals to 8-bit ITU-R BT.656 format. The chip includes four high speed and low power 10-bit analog-to-digital converters (ADC) with 2x sampling rate to support 4-channel video decoding. When the incoming video is in the 720H format, the sampling rate is 27MHz or 54MHz by 2x factor. For 960H format, the sampling rate is 36MHz or 72MHz by 2x factor. The chip implements proprietary circuit design that is optimized for locking in weak, noisy, or unstable signals. The minimal signal voltage that can be locked in is at 160/80 mV.

### Adaptive Equalization

The CVBS is suffered from channel loss by an extended transmission distance (greater than 500m) and a small diameter (less than 0.5mm) of CCTV cable. The distortion on CVBS after the energy reduction effect of cable length is illustrated as below. For example, a Multi-Burst test signal is respectively measured at 0.5m and 500m of cable. It appears that color burst and sync tip have severe degradation after 500m transmission distance. Adaptive equalization on the distorted CVBS recovers the signal back to close to the original level. Since the different cable conditions present various effects on CVBS picture image, the adaptive equalization provides to compensate the signal loss on some frequency components pertinent to the Coax cable.



## Comb filter and Y/C Separation

The video decoder is capable of separating luma (Y) and chroma (C) of NTSC or PAL video signals using 5-line adaptive comb filter or notch/band-pass filter. The comb filter searches for correlation between 5 lines of input video stored in the internal buffer. The lines are averaged based on the degree of correlation to produce the output video line. If no correlation is found between the 5 lines of video, notch/band-pass filter is used. This process is very effective at reducing cross-luma and cross-chroma noise. The noise appears as artifacts that degrade the image quality. Reduction of the noise improves the image quality significantly.

## Video Signal Processing

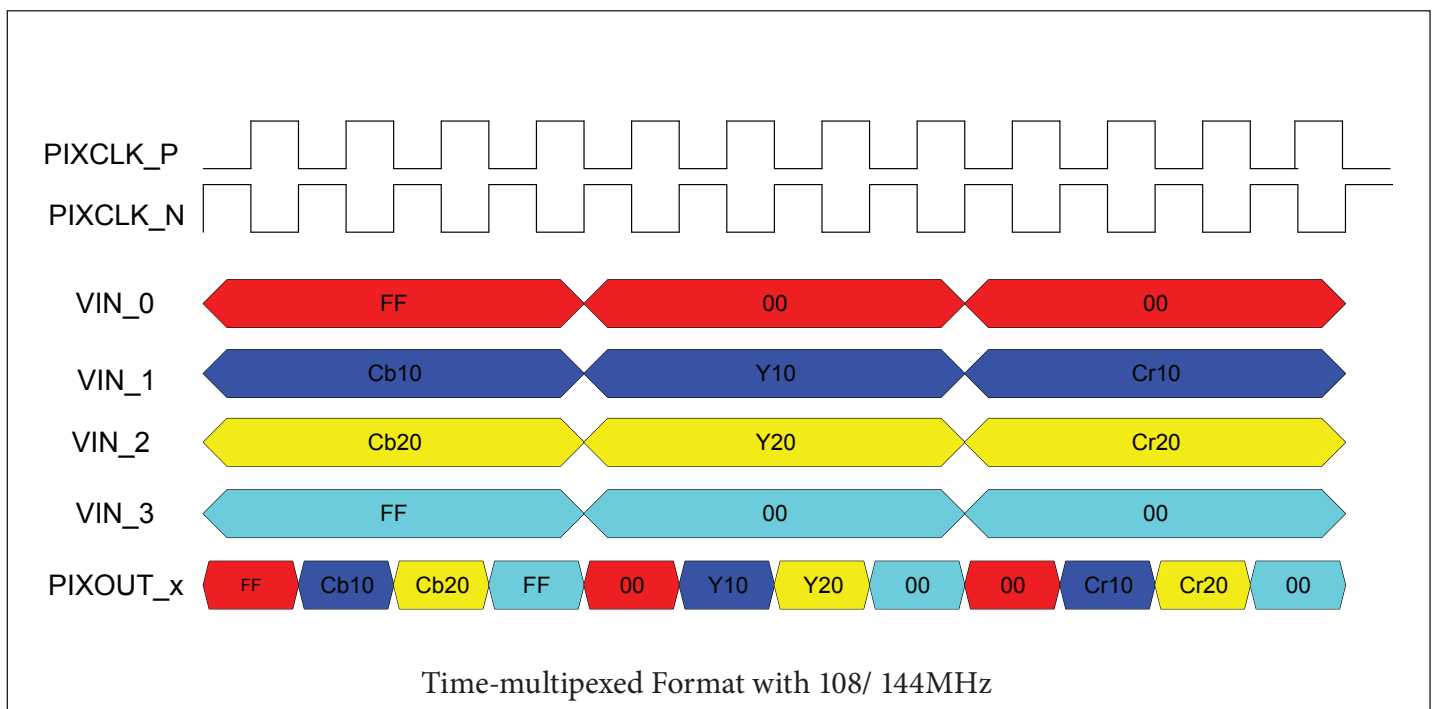
The chip is capable of processing digital video signal to fulfill better detection in a noisy environment and achieve good image quality for viewing as well. For video signal detection, a resilient SYNC TIP detection mechanism is implemented to locate VSYNC and HSYNC correctly in order to lock the video frame or video line.

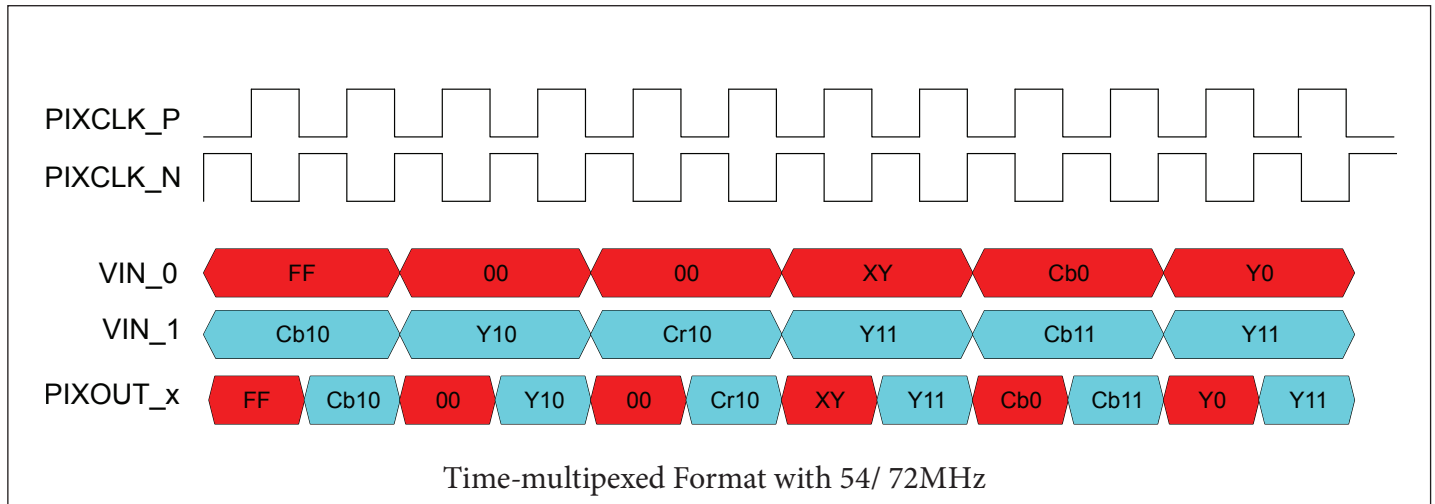
In general, the poor power adaptor or camera would introduce high frequency ripples coupling with sync tip to cause the misjudgment on the beginning of a video frame or line. The built-in video processing circuit is able to decouple the noise from sync tip to prevent from video loss.

A sharpness filter is implemented to offer programmable 16 level gains to increase the high frequency and edge information of luma for better viewing on the contour of each object. Through the I2C serial interface, hue, contrast, brightness and saturation can be programmed in the configuration registers. Hue can be controlled in 256 steps from -180 degrees to +180 degrees. Saturation can be programmed in 256 grades. Brightness can be adjusted in 256 levels.

## Video Output Port

The four CVBS analog video channels are converted into four individual digital video data streams. There are four video output ports (PIXOUT\_0, PIXOUT\_1, PIXOUT\_2 and PIXOUT\_3) in the chip and each video output port can carry several converted digital video data stream following ITU-R BT.656 compatible data format. The video data of each port is synchronous with the corresponding clock signals of PIXCLK\_PO or PIXCLK\_NO. The frequency of PIXCLK\_\*O can be operated at 1x, 2x or 4x of 27MHz (720H mode) or 36MHz (960H mode). When the clock frequency is 2x or 4x rate, the video port outputs 2-channel or 4-channel video data stream in time-multiplexed format. The clock phase of PIXCLK\_PO or PIXCLK\_NO can be programmed by delay cells through writing delay value into the registers of PIXCLK\_P\_DEL or PIXCLK\_N\_DEL. Also, the clock polarity can be controlled through inverter by setting or resetting the register of PIXCLK\_P\_POL or PIXCLK\_N\_POL. The flexibility on changing clock phase or polarity facilitates the timing design for video data stream on PCB.





## ANALOG AUDIO INPUT

The audioADC offers 5 channels of analog inputs (LINE\_INx, x= 0, 1, 2, 3, 4, 5, 6, 7, 8, 9) with a peak-to-peak voltage range from 0.5V to 2V. Each input channel contains 4-bit programmable gain amplifier and an ADC with maximum over-sampling speed of 3.6M Sample/s. A pseudo differential input is used to minimize board level noise problems. The converted audio data stream is fed into a low pass filter to decimate audio sample at an appropriate audio sampling rate such as 8 KHz, 16 KHz, 32 KHz, 44.1 KHz and 48 KHz etc.

## AUDIO PROCESSING

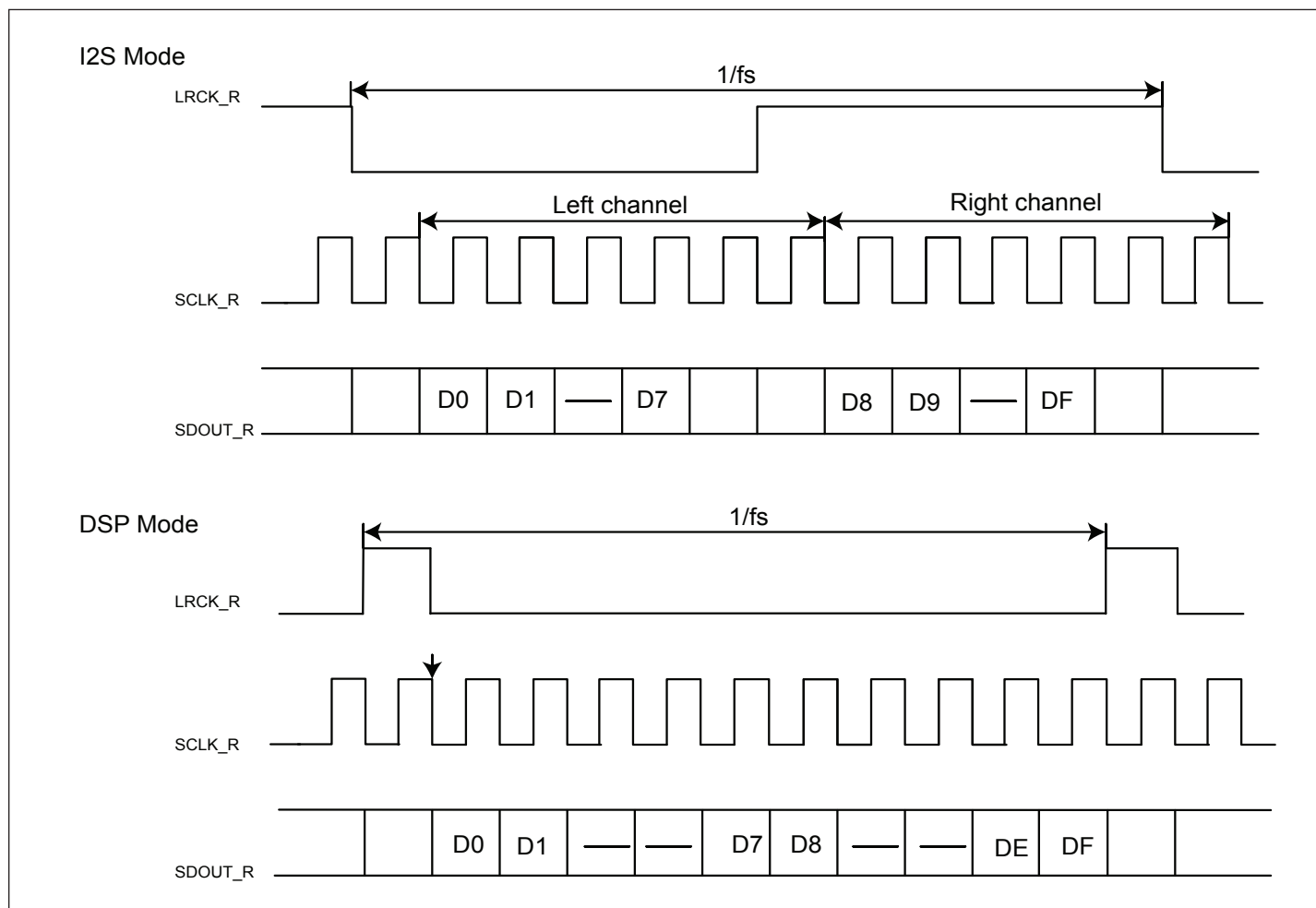
The audio processor accepts 5 digital audio streams from audio ADC. It also receives 2 additional digital serial audio data from pins. One digital serial audio data is SDIN\_P coming from AV compression processor, while the other one is SD\_LINKI coming from companion device.

SDIN\_P represents the decompressed audio data for playback purpose. SD\_LINKI is used to cascade with digital audio outputs from one other PI7VD9008ABH chips for forming one timing multiplexed I2S digital serial audio data containing 8 or 10 digital audio channels. This device processes these 10 digital audio streams and 2 digital serial audio data, then generates one mixing analog audio signal and three digital serial audio data to fulfill the functions of mixing, recording and cascading etc.

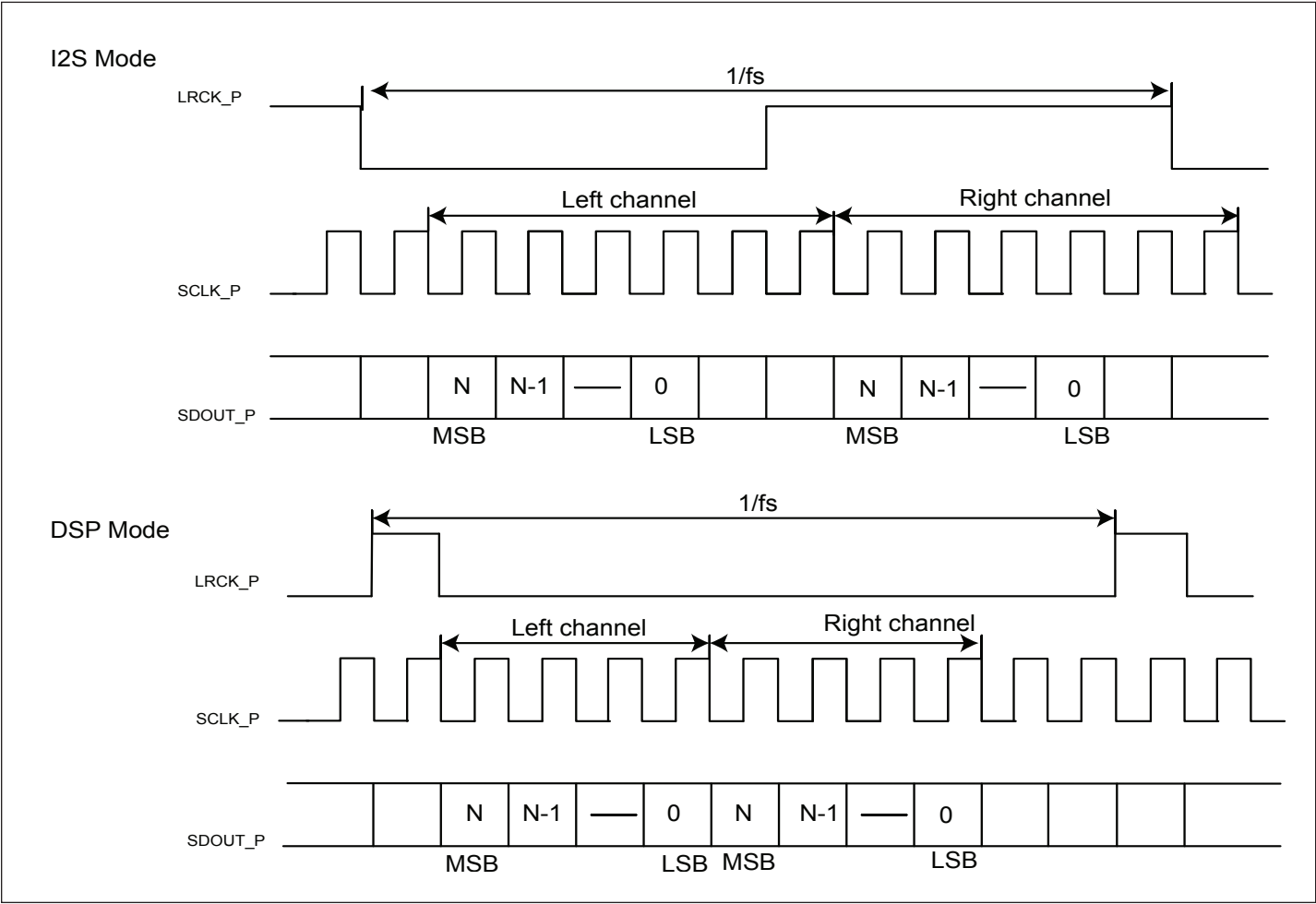
For audio mixing, this device has both analog and digital format. The built-in mixer selects among all audio input data to generate the mixing digital audio data (SDOUT\_M), which connects to audio DAC for converting to mixing analog audio signal output (LINE\_OUT).

For audio recording, the audio processor performs multiplexing over 16 digital audio streams in timing division way to generate record digital audio output data (SDOUT\_R). For the digital serial audio data SDOUT\_R and SDOUT\_M, they are both synchronized with SCLK\_R and LRCK\_R. As to SDIN\_P, it is synchronized with SCLK\_P and LRCK\_P. These digital serial audio data support two formats of I2S and DSP that can be selected by control bits RM\_SYNC in the register at offset 0xD2 and PB\_SYNC in the register at offset 0xDB. Meanwhile, the record and playback digital serial audio interfaces of PI7VD9008ABH can be acted as Master or Slave mode based upon the setting of ACLKRMASER and PB\_MASTER bits in the register at offset 0xDB

This device supports audio system clock with 256fs or 320fs mode, which is controlled by AIN5MD register. The record output pin contains several channel inputs that can be defined by the registers at offset of 0xD2~ 0xDA describing the number and sequence of recorded audio streams. It supports 8bit and 16bit record data width for trading off between higher audio qualities and saving disk storage space. By controlling bit2 of register at offset 0xDB, the chip allows to select the output record data width to be either 8-bit or 16-bit mode.



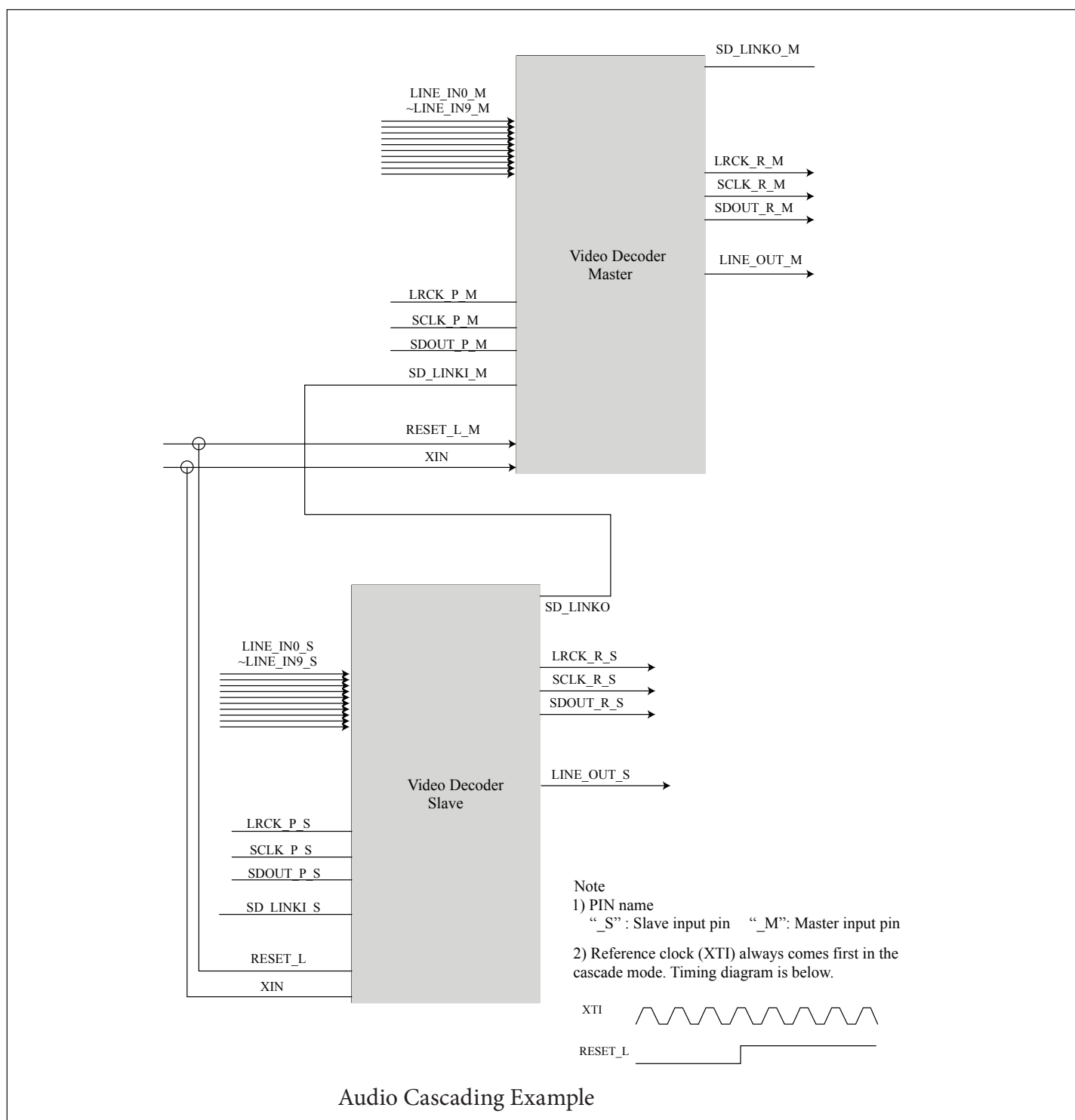
Audio Record Signal Output Format



Playback Input Format

## PI7VD9008ABH Cascade Mode

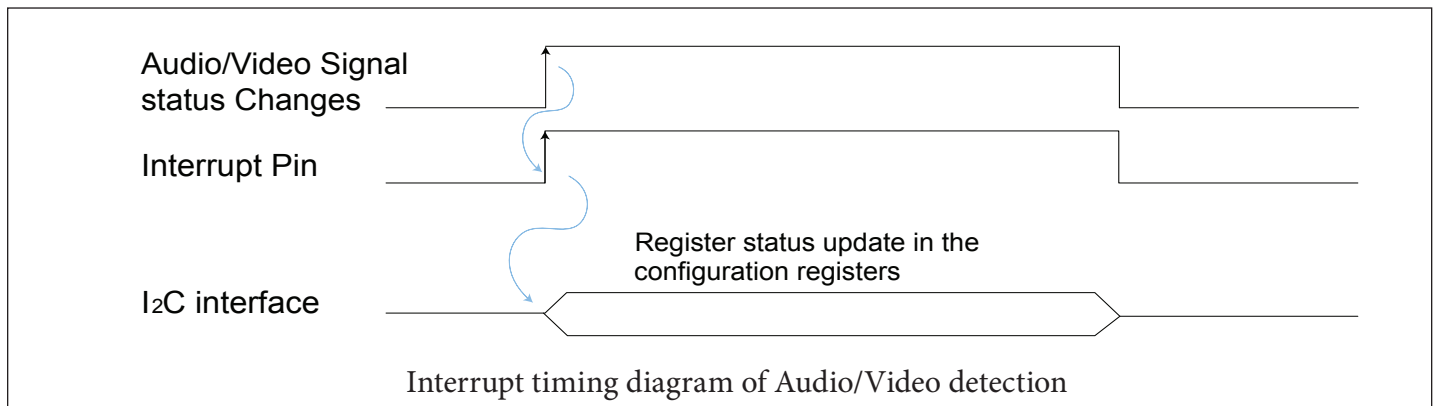
For audio cascading, the chip redirects SDOUT\_R as SD\_LINKO to connect with SD\_LINKI of another PI7VD9008AB product, which cascades its original SDOUT\_R and SD\_LINKI to create a new SDOUT\_R. PI7VD9008AB can support 16 channel data output on first level chip recordoutput pin for saving pin layout on PCB board. The cascade chips have to use same crystal clock source and same reset signal.



## I2C Host Interface

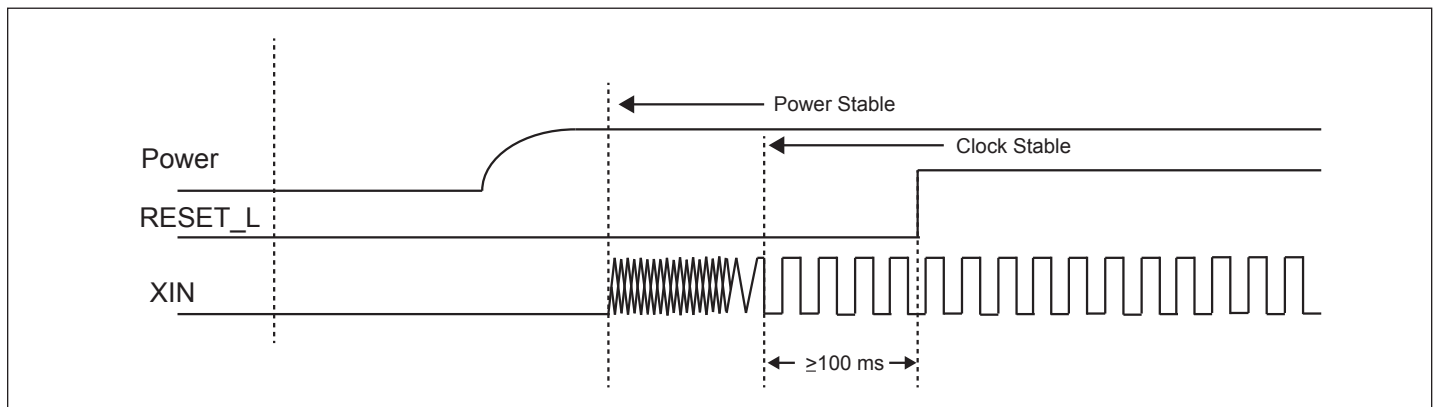
The processor can access the internal register by executing read or write command to the indexed locations to implement the function of detecting audio and video signal and reveals the detection status through the configuration registers. If any audio or video channel is present or absent, interrupt pin (INT) can notify the status to the processor to manage CPU resource effectively by polling the status. The chip supports flexibilities to select various detection modes and enable individual audio/video channel for generating interrupt.

These control bits to interrupt pin are defined in the registers of AVDET\_MODE, AVDET1\_ENA, AVDET2\_ENA, A51DET\_ENA and A52DET\_ENA.



## Power Sequence

The power supply should be turned on first. After the power is turned on, the clock signal should be supplied. Finally, after both power and clock signals are turned on, the RESET\_L signal is turned to HIGH to complete the power sequence.



## CONFIGURATION, CONTROL AND STATUS REGISTER MAP

### PAGE\_0 REGISTER MAP ( address 40h =00h)

| Address               | Function                           |
|-----------------------|------------------------------------|
| 00h/10h/20h/30h (00h) | Video Status                       |
| 01h/11h/21h/31h (00h) | Brightness Control                 |
| 02h/12h/22h/32h (64h) | Contrast Control                   |
| 03h/13h/23h/33h (00h) | Sharpness Control                  |
| 04h/14h/24h/34h (80h) | Chroma (U) Gain                    |
| 05h/15h/25h/35h (80h) | Chroma (V) Gain                    |
| 06h/16h/26h/36h (00h) | Hue Control                        |
| 07h/17h/27h/37h       | Reserved                           |
| 08h/18h/28h/38h       | Reserved                           |
| 09h/19h/29h/39h       | Reserved                           |
| 0Ah/1Ah/2Ah/3Ah       | Hdelay                             |
| 0Bh/1Bh/2Bh/3Bh       | Reserved                           |
| 0Ch/1Ch/2Ch/3Ch       | Reserved                           |
| 0Dh/1Dh/2Dh/3Dh       | Reserved                           |
| 0Eh/1Eh/2Eh/3Eh (77h) | Standard Selection                 |
| 0Fh/1Fh/2Fh/3Fh       | Reserved                           |
| 40h-50h               | Reserved                           |
| 51h (00h)             | F-Bit of SAV/EAV Inverted          |
| 52h-55h               | Reserved                           |
| 56h                   | Blanking Length of Horizontal Line |
| 57h/58h/59h/5Ah (90h) | Blanking Length of Horizontal Line |
| 5Bh-5Ch               | Reserved                           |
| 5Dh(C0h)              | Vin2 Color Kill Enable             |
| 5Eh(C0h)              | Vin3 Color Kill Enable             |
| 5Fh(C0h)              | Vin4 Color Kill Enable             |
| 60h                   | Reserved                           |
| 61h (03h)             | Crystal Clock Select               |
| 62h (00h)             | GPIO Output Enable                 |
| 63h (10h)             | ID for Video Channel 0&1           |
| 64h (32h)             | ID for Video Channel 2&3           |
| 65h (54h)             | ID for Video Channel 4&5           |
| 66h (76h)             | ID for Video Channel 6&7           |
| 67h(80h)              | HZOOM Enable                       |
| 68h(00h)              | HI-Bits of 1234 HZOOM              |
| 69h(00h)              | LOW-Bits of 1 HZOOM                |
| 6Ah(00h)              | LOW-Bits of 2 HZOOM                |
| 6Bh(00h)              | LOW-Bits of 3 HZOOM                |
| 6Ch(00h)              | LOW-Bits of 4 HZOOM                |
| 6Dh-6Dh               | Reserved                           |
| 6Fh(00h)              | Video Output Enable                |
| 70h (08h)             | Audio Clock Control                |
| 71h (00h)             | I2S Audio Input Control            |
| 72h                   | Reserved                           |
| 73h(00h)              | LINE_IN4 Control                   |
| 74h(00h)              | LINE_IN4 Detect Enable             |
| 75h-7Ah               | Reserved                           |
| 7Bh (00h)             | SDOUT_M Select (R)                 |
| 7Ch (00h)             | SDOUT_M Select (L)                 |
| 7Dh (E4h)             | Extended Line Select               |
| 7Eh                   | SDOUT_M I2S                        |
| 7Fh (00h)             | Mix Ratio LINE_IN4                 |

# PI7VD9008ABH

Adaptive EQ 8-channel 960H Video Decoder



| Address   | Function                        |
|-----------|---------------------------------|
| 80h (00h) | Software Reset                  |
| 81h-88h   | Reserved                        |
| 89h (00h) | Audio FS Mode                   |
| 8Ah-95h   | Reserved                        |
| 96h(C0h)  | Vin1 Color Kill Enable          |
| 97h-9Eh   | Reserved                        |
| 9Fh (00h) | PIXCLK 0Delay                   |
| A0h-B1h   | Reserved                        |
| B2h (00h) | Vin1~Vin8 Video Loss Status     |
| B3h-C7h   | Reserved                        |
| C8h (00h) | GPIO_0_1 Mode                   |
| C9h (00h) | GPIO_2_3 Mode                   |
| CAh (55h) | Reserved                        |
| CBh (00h) | GPIO Polarity                   |
| CCh (00h) | Reserved                        |
| CDh (00h) | WD1 ,D1 Select                  |
| CEh       | Reserved                        |
| CFh (00h) | Serial Mode Control             |
| D0h-D1h   | Reserved                        |
| D2h (03h) | SDOUT_RM Output                 |
| D3h (10h) | SDOUT_R_SEQ_1_0                 |
| D4h(32h)  | SDOUT_R_SEQ_3_2                 |
| D5h (54h) | SDOUT_R_SEQ_5_4                 |
| D6h (76h) | SDOUT_R_SEQ_7_6                 |
| D7h (98h) | SDOUT_R_SEQ_9_8                 |
| D8h (BAh) | SDOUT_R_SEQ_B_A                 |
| D9h (DCh) | SDOUT_R_SEQ_D_C                 |
| DAh (FEh) | SDOUT_R_SEQ_F_E                 |
| DBh (C2h) | I2S Master Control              |
| DCh(10h)  | MIX MUTE Control                |
| DDh (00h) | Mix Ratio 0 & 1                 |
| DEh (00h) | Mix Ratio 2 & 3                 |
| DFh (08h) | PB Ratio                        |
| E0h (14h) | Mixing Output Control           |
| E1h (00h) | Audio Detect Threshold 0123 MSB |
| E2h (aah) | Audio Detect Threshold 01 LSB   |
| E3h (aah) | Audio Detect Threshold 23 LSB   |
| E4h-E6h   | Reserved                        |
| E7h(55h)  | VD0~VD4 Output Mode             |
| E8h (10h) | PIXOUT_0 Output CH12 Select     |
| E9h (32h) | PIXOUT_0 Output CH34 Select     |
| EAh (32h) | PIXOUT_1 Output CH12 Select     |
| EBh (54h) | PIXOUT_1 Output CH34 Select     |
| ECh (54h) | PIXOUT_2 Output CH12 Select     |
| EDh (76h) | PIXOUT_2 Output CH34 Select     |
| EEh (76h) | PIXOUT_3 Output CH12 Select     |
| EFh (10h) | PIXOUT_3 Output CH34 Select     |
| F0h-F8_h  | Reserved                        |
| F9h (00h) | PIXCLK Output Mode              |
| FAh (00h) | CCIR656 Control                 |
| FBh (0Fh) | Clock Polarity                  |
| FCh (FFh) | AV Detection Enable             |
| FDh (00h) | AV Detection Status             |
| FEh (00h) | Device ID_H                     |
| FFh (F0h) | Device ID_L                     |

## PAGE\_0 REGISTER MAP ( address 40h =01h)

| Address               | Function                           |
|-----------------------|------------------------------------|
| 00h/10h/20h/30h (00h) | Video Status                       |
| 01h/11h/21h/31h (00h) | Brightness Control                 |
| 02h/12h/22h/32h (64h) | Contrast Control                   |
| 03h/13h/23h/33h (00h) | Sharpness Control                  |
| 04h/14h/24h/34h (80h) | Chroma (U) Gain                    |
| 05h/15h/25h/35h (80h) | Chroma (V) Gain                    |
| 06h/16h/26h/36h (00h) | Hue Control                        |
| 0Ah/1Ah/2Ah/3Ah       | Hdelay                             |
| 0Eh/1Eh/2Eh/3Eh (77h) | Standard Selection                 |
| 56h                   | Blanking Length of Horizontal Line |
| 57h/58h/59h/5Ah (90h) | Blanking Length of Horizontal Line |
| 5Dh(C0h)              | Vin6 Color Kill Enable             |
| 5Eh(C0h)              | Vin7 Color Kill Enable             |
| 5Fh(C0h)              | Vin8 Color Kill Enable             |
| 68h(00h)              | HI-Bits of 5 6 7 8HZOOM            |
| 69h(00h)              | LOW-Bits of 5 HZOOM                |
| 6Ah(00h)              | LOW-Bits of 6 HZOOM                |
| 6Bh(00h)              | LOW-Bits of 7 HZOOM                |
| 6Ch(00h)              | LOW-Bits of 8 HZOOM                |
| 73h(00h)              | LINE_IN9 Control                   |
| 74h(00h)              | LINE_IN9 Detect Enable             |
| 7Eh                   | LINE_IN9 Detect Threshold          |
| 7Fh (00h)             | Mix Ratio LINE_IN9                 |
| 96h(C0h)              | Vin5 Color Kill Enable             |
| C8h (00h)             | GPIO_4_5 Mode                      |
| C9h (00h)             | GPIO_6_7 Mode                      |
| DDh (00h)             | Mix Ratio 4 & 5                    |
| DEh (00h)             | Mix Ratio 6 & 7                    |
| E1h (00h)             | Audio Detect Threshold 5678 MSB    |
| E2h (aah)             | Audio Detect Threshold 56 LSB      |
| E3h (aah)             | Audio Detect Threshold 78 LSB      |
| FCh (FFh)             | AV Detection Enable                |
| FDh (00h)             | AV Detection Status                |

**Control Register****PAGE 0 REGISTERS**

| Register Type | Descriptions |
|---------------|--------------|
| R             | Read Only    |
| RW            | Read/Write   |

**VIDEO STATUS REGISTER – OFFSET 00H/10H/20H/30H (Default: 00H)**

| BIT | FUNCTION | TYPE | DESCRIPTION                                                                      |
|-----|----------|------|----------------------------------------------------------------------------------|
| 0   | DET50    | R    | 0: 60Hz source detected<br>1: 50Hz source detected                               |
| 1   | MONO     | R    | 0: Color burst signal detected<br>1: No color burst signal detected              |
| 2   | Reserved | R    | Reset to 0b                                                                      |
| 3   | VLOCK    | R    | 0: Vertical logic is not locked<br>1: Vertical logic is locked to incoming video |
| 4   | Reserved | R    | Reset to 0b                                                                      |
| 5   | SLOCK    | R    | 0: Sub-carrier sync is not detected<br>1: Sub-carrier sync is detected           |
| 6   | HLOCK    | R    | 0: Horizontal sync is not detected<br>1: Horizontal sync is detected             |
| 7   | VDLOSS   | R    | 0: Video is detected<br>1: Video not present                                     |

**BRIGHTNESS CONTROL REGISTER – OFFSET 01H/11H/21H/31H(Default=00H)**

| BIT   | FUNCTION   | TYPE | DESCRIPTION                                                                                                                    |
|-------|------------|------|--------------------------------------------------------------------------------------------------------------------------------|
| [7:0] | Brightness | RW   | These Signed bits control the brightness. Value range from -128 to 127<br>8'h7F: brightest; 8'h80: darkest ; 8'h00 : no effect |

**CONTRASTCONTROL REGISTER – OFFSET 02H/12H/22H/32H(Default=64H)**

| BIT   | FUNCTION | TYPE | DESCRIPTION                                                                                           |
|-------|----------|------|-------------------------------------------------------------------------------------------------------|
| [7:0] | Contrast | RW   | These unsigned bits control the luminance gain.<br>8'h7F: maximum contrast<br>8'h00: minimum contrast |

## SHARPNESSCONTROL REGISTER – OFFSET 03H/13H/23H/33H(Default=00H)

| BITS  | FUNCTION  | TYPE | DESCRIPTION                                                                                                                                                                                               |
|-------|-----------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | Sharpness | RW   | These bits control the amount of sharpness enhancement on the luminance signals<br>"0" has no effect on the output image<br>"1" through "15" provides sharpness enhancement with "15" being the strongest |
| [7:4] | Reserved  | R    | Reset to 0h                                                                                                                                                                                               |

## CHROMA(U) GAIN REGISTER – OFFSET 04H/14H/24H/34H(Default=80H)

| BITS  | FUNCTION        | TYPE | DESCRIPTION                                           |
|-------|-----------------|------|-------------------------------------------------------|
| [7:0] | Chroma (U) Gain | RW   | Chroma gain value of controlling the color saturation |

## CHROMA(V) GAIN REGISTER – OFFSET 05H/15H/25H/35H(Default=80H)

| BITS  | FUNCTION        | TYPE | DESCRIPTION                                           |
|-------|-----------------|------|-------------------------------------------------------|
| [7:0] | Chroma (V) Gain | RW   | Chroma gain value of controlling the color saturation |

## HUECONTROL REGISTER – OFFSET 06H/16H/26H/36H(Default=00H)

| BITS  | FUNCTION | TYPE | DESCRIPTION                                                    |
|-------|----------|------|----------------------------------------------------------------|
| [7:0] | Hue      | RW   | These signed bits control color hue.<br>+90C(7Fh) to -90C(80h) |

## RESERVED REGISTER– OFFSET07H/17H/27H/37H

## RESERVED REGISTER – OFFSET 08H/18H/28H/38H

## RESERVED REGISTER – OFFSET09H/19H/29H/39H

## H-Delay REGISTER – OFFSET 0AH/1AH/2AH/3AH(Default=00H)

| BITS  | FUNCTION                         | TYPE | DESCRIPTION                                  |
|-------|----------------------------------|------|----------------------------------------------|
| [7:5] | Reserved                         | R    | Reset to 0b                                  |
| [4:0] | HorizontalShift Pixels<br>Poinis | R/W  | Left shift the start points of video outputs |

## RESERVED REGISTER – OFFSET 0BH/1BH/2BH/3BH

## RESERVED REGISTER – OFFSET 0CH/1CH/2CH/3CH

**RESERVED REGISTER – OFFSET 0DH/1DH/2DH/3DH****STANDARD SELECTION REGISTER – OFFSET 0EH/1EH/2EH/3EH(Default=77H)**

| BITS  | FUNCTION                  | TYPE | DESCRIPTION                                                                                                               |
|-------|---------------------------|------|---------------------------------------------------------------------------------------------------------------------------|
| [2:0] | Standard Selection        | RW   | 0: NTSC(M)<br>1: PAL(B,D,G,H,I)<br>2:Not valid<br>3: NTSC4.43<br>4: PAL(M)<br>5: PAL(CN)<br>6: PAL60<br>7: Auto detection |
| [3]   | Reserved                  | R    | Reset to 0b                                                                                                               |
| [6:4] | Current Standard Detected | R    | 0: NTSC(M)<br>1: PAL(B,D,G,H,I)<br>2:Not valid<br>3: NTSC4.43<br>4: PAL(M)<br>5: PAL(CN)<br>6: PAL60<br>7:Not valid       |
| [7]   | Reserved                  | R    | Reset to 0b                                                                                                               |

**RESERVED REGISTER – OFFSET 0FH/1FH/2FH/3FH****RESERVED REGISTER – OFFSET 40H-50H****FBITINV REGISTER – OFFSET 51H(Default=00H)**

| BITS  | FUNCTION | TYPE | DESCRIPTION                                                                                                                   |
|-------|----------|------|-------------------------------------------------------------------------------------------------------------------------------|
| [0]   | FBITINV0 | R/W  | 0: F-bit in the 4th byte of 656 EAV/SAV for channel 1 is not inverted.<br>1: F-bit in the 4th byte for channel 0 is inverted. |
| [1]   | FBITINV1 | R/W  | 0: F-bit in the 4th byte of 656 EAV/SAV for channel 2 is not inverted.<br>1: F-bit in the 4th byte for channel 1 is inverted. |
| [2]   | FBITINV2 | R/W  | 0: F-bit in the 4th byte of 656 EAV/SAV for channel 3 is not inverted.<br>1: F-bit in the 4th byte for channel 2 is inverted. |
| [3]   | FBITINV3 | R/W  | 0: F-bit in the 4th byte of 656 EAV/SAV for channel 4 is not inverted.<br>1: F-bit in the 4th byte for channel 3 is inverted. |
| [7:4] | Reserved | R    | Reset to 0b                                                                                                                   |

**RESERVED REGISTER – OFFSET 52H-56H**

## High HBLN REGISTER – OFFSET 56H (Default=00H)

| BITS  | FUNCTION | TYPE | DESCRIPTION                                                |
|-------|----------|------|------------------------------------------------------------|
| [0]   | HBLN1[8] | R    | Display the blanking length starting from EAV to SAV code. |
| [1]   | HBLN2[8] | R    | Display the blanking length starting from EAV to SAV code. |
| [2]   | HBLN3[8] | R    | Display the blanking length starting from EAV to SAV code. |
| [3]   | HBLN4[8] | R    | Display the blanking length starting from EAV to SAV code. |
| [7:4] | Reserved | R    | Reset to 0b                                                |

## LOW HBLN REGISTER – OFFSET 57H/58H/59H/5AH(Default=90H)

| BITS  | FUNCTION                | TYPE | DESCRIPTION                                                                                                                                                                 |
|-------|-------------------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:0] | HBLNn[7:0]<br>n=1,2,3,4 | R    | Display the blanking length starting from EAV to SAV code.<br>(1) In 27MHz D1 Mode: 90H for PAL while 8AH for NTSC<br>(2) In 36MHz WD1 Mode: C0H for PAL while B8H for NTSC |

## RESERVED REGISTER – OFFSET 5BH-5CH

## VIN2 COLOR KILL ENABLE-REGISTER – OFFSET 5DH(Default=C0H)

| BITS  | FUNCTION      | TYPE | DESCRIPTION                                                           |
|-------|---------------|------|-----------------------------------------------------------------------|
| [5:0] | Reserved      | RW   | Reset to 0h                                                           |
| [6]   | PAL CKILL EN  | RW   | 1:enable color kill mode in PAL<br>0:disable color kill mode in PAL   |
| [7]   | NTSC CKILL EN | RW   | 1:enable color kill mode in NTSC<br>0:disable color kill mode in NTSC |

## VIN3 COLOR KILL ENABLE-REGISTER – OFFSET 5EH(Default=C0H)

| BITS  | FUNCTION      | TYPE | DESCRIPTION                                                           |
|-------|---------------|------|-----------------------------------------------------------------------|
| [5:0] | Reserved      | RW   | Reset to 0h                                                           |
| [6]   | PAL CKILL EN  | RW   | 1:enable color kill mode in PAL<br>0:disable color kill mode in PAL   |
| [7]   | NTSC CKILL EN | RW   | 1:enable color kill mode in NTSC<br>0:disable color kill mode in NTSC |

## VIN4 COLOR KILL ENABLE-REGISTER – OFFSET 5FH(Default=C0H)

| BITS  | FUNCTION     | TYPE | DESCRIPTION                                                         |
|-------|--------------|------|---------------------------------------------------------------------|
| [5:0] | Reserved     | RW   | Reset to 0h                                                         |
| [6]   | PAL CKILL EN | RW   | 1:enable color kill mode in PAL<br>0:disable color kill mode in PAL |

|     |               |    |                                                                       |
|-----|---------------|----|-----------------------------------------------------------------------|
| [7] | NTSC CKILL EN | RW | 1:enable color kill mode in NTSC<br>0:disable color kill mode in NTSC |
|-----|---------------|----|-----------------------------------------------------------------------|

**RESERVED REGISTER – OFFSET 60H****CRYSTAL CLOCK SELECT REGISTER – OFFSET 61H(Default=03H)**

| BITS  | FUNCTION | TYPE | DESCRIPTION                                                      |
|-------|----------|------|------------------------------------------------------------------|
| [1:0] | XINMD    | RW   | XIN input frequency<br>0:27Mhz<br>1:54Mhz<br>2:108Mhz<br>3:27Mhz |
| [7:2] | Reserved | RW   | Reset to 00h                                                     |

**GPIO\_OE REGISTER – OFFSET 62H(Default=00H)**

| BITS  | FUNCTION | TYPE | DESCRIPTION                                         |
|-------|----------|------|-----------------------------------------------------|
| [0]   | GPIO_0OE | RW   | 0: GPIO_0 pin is input.<br>1: GPIO_0 pin is output. |
| [1]   | GPIO_1OE | RW   | 0: GPIO_1 pin is input.<br>1: GPIO_1 pin is output. |
| [2]   | GPIO_2OE | RW   | 0: GPIO_2 pin is input.<br>1: GPIO_2 pin is output. |
| [3]   | GPIO_3OE | RW   | 0: GPIO_3 pin is input.<br>1: GPIO_3 pin is output. |
| [7:4] | Reserved | RW   | Reset to 00h                                        |

**CHANNEL ID01 REGISTER – OFFSET 63H(Default=10H)**

| BITS  | FUNCTION | TYPE | DESCRIPTION                                           |
|-------|----------|------|-------------------------------------------------------|
| [3:0] | CH0NUM   | RW   | Assign channel ID number in CV_IN0A video data output |
| [7:4] | CH1NUM   | RW   | Assign channel ID number in CV_IN1A video data output |

**CHANNEL ID23 REGISTER – OFFSET 64H(Default=32H)**

| BITS  | FUNCTION | TYPE | DESCRIPTION                                           |
|-------|----------|------|-------------------------------------------------------|
| [3:0] | CH2NUM   | RW   | Assign channel ID number in CV_IN2A video data output |
| [7:4] | CH3NUM   | RW   | Assign channel ID number in CV_IN3A video data output |

## CHANNEL ID45 REGISTER – OFFSET 65H(Default=54H)

| BIT   | FUNCTION | TYPE | DESCRIPTION                                           |
|-------|----------|------|-------------------------------------------------------|
| [3:0] | CH4NUM   | RW   | Assign channel ID number in CV_IN4A video data output |
| [7:4] | CH5NUM   | RW   | Assign channel ID number in CV_IN5A video data output |

## CHANNEL ID67 REGISTER – OFFSET 66H(Default=76H)

| BIT   | FUNCTION | TYPE | DESCRIPTION                                           |
|-------|----------|------|-------------------------------------------------------|
| [3:0] | CH6NUM   | RW   | Assign channel ID number in CV_IN6A video data output |
| [7:4] | CH7NUM   | RW   | Assign channel ID number in CV_IN7A video data output |

## HZOOM ENABLE REGISTER – OFFSET 67H(Default=80H)

| BIT   | FUNCTION     | TYPE | DESCRIPTION                                           |
|-------|--------------|------|-------------------------------------------------------|
| [6:0] | Reserved     | R    | Reset to 00h                                          |
| [7]   | HZOOM ENABLE | RW   | 1: Enable HZOOM function<br>0: Disable HZOOM function |

## HI –Bits HZOOM REGISTER – OFFSET 68H(Default=00H)

| BIT   | FUNCTION    | TYPE | DESCRIPTION  |
|-------|-------------|------|--------------|
| [1:0] | HZOOM1[9:8] | RW   | MSB of reg69 |
| [3:2] | HZOOM2[9:8] | RW   | MSB of reg6A |
| [5:4] | HZOOM3[9:8] | RW   | MSB of reg6B |
| [7:6] | HZOOM4[9:8] | RW   | MSB of reg6C |

## LOW–Bits HZOOM VIN1 REGISTER – OFFSET 69H(Default=00H)

| BIT   | FUNCTION    | TYPE | DESCRIPTION                                                                             |
|-------|-------------|------|-----------------------------------------------------------------------------------------|
| [7:0] | HZOOM1[7:0] | R/W  | HZOOM UP register the number is from<br>3DE to 3FF if HZOOM1[9:0]=00h No HZOOM Function |

## LOW–Bits HZOOM VIN2 REGISTER – OFFSET 6AH(Default=00H)

| BIT   | FUNCTION    | TYPE | DESCRIPTION                                                                             |
|-------|-------------|------|-----------------------------------------------------------------------------------------|
| [7:0] | HZOOM2[7:0] | R/W  | HZOOM UP register the number is from<br>3DE to 3FF if HZOOM2[9:0]=00h No HZOOM Function |

## LOW–Bits HZOOM VIN3 REGISTER – OFFSET 6BH(Default=00H)

| BIT   | FUNCTION    | TYPE | DESCRIPTION                                                                             |
|-------|-------------|------|-----------------------------------------------------------------------------------------|
| [7:0] | HZOOM3[7:0] | R/W  | HZOOM UP register the number is from<br>3DE to 3FF if HZOOM3[9:0]=00h No HZOOM Function |

**LOW-Bits HZOOM VIN4 REGISTER – OFFSET 6CH(Default=00H)**

| BITS  | FUNCTION    | TYPE | DESCRIPTION                                                                          |
|-------|-------------|------|--------------------------------------------------------------------------------------|
| [7:0] | HZOOM4[7:0] | R/W  | HZOOM UP register the number is from 3DE to 3FF if HZOOM4[9:0]=00h No HZOOM Function |

**RESERVED REGISTER – OFFSET 6DH-6EH****PIXOUT OUTPUT ENABLE REGISTER – OFFSET 6FH(Default=00H)**

| BITS  | FUNCTION    | TYPE | DESCRIPTION                           |
|-------|-------------|------|---------------------------------------|
| [0]   | PIXOUT0_OEB | R    | 0: enable output<br>1: disable output |
| [1]   | PIXOUT1_OEB | R    | 0: enable output<br>1: disable output |
| [2]   | PIXOUT2_OEB | R    | 0: enable output<br>1: disable output |
| [3]   | PIXOUT3_OEB | R    | 0: enable output<br>1: disable output |
| [7:4] | Reserved    | R    | Reset to 0b                           |

**AUDIO CLOCK CONTROL REGISTER – OFFSET 70H(Default=08H)**

| BITS  | FUNCTION | TYPE | DESCRIPTION                                                                                          |
|-------|----------|------|------------------------------------------------------------------------------------------------------|
| [2:0] | AFMD     | RW   | 0: 8KHz<br>1: 16KHz<br>2: 32KHz<br>3: 44.1KHz<br>4: 48KHz                                            |
| [3]   | Reserved | R    | Reset to 1b                                                                                          |
| [5:4] | Reserved | R    | Reset to 0b                                                                                          |
| [6]   | S2I_8BIT | RW   | 0:SCLK_P/LRCK_P/SDOUT_P pin input 16-bit control<br>1: SCLK_P/LRCK_P/SDOUT_P pin input 8-bit control |
| [7]   | Reserved | R    | Reset to 0b                                                                                          |

**I2S AUDIO INPUT CONTROL REGISTER – OFFSET 71H(Default=00H)**

| BITS  | FUNCTION | TYPE | DESCRIPTION                                                                                                                                                                  |
|-------|----------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [1:0] | Reserved | R    | Reset to 00b                                                                                                                                                                 |
| [2]   | SDINPDLY | RW   | SDIN_P input data delay by one SCLK_P clock<br>0:No delay; 1T delay for I2S interface<br>1:Add 1 SCLK_P clock delay in SDIN_P input.; 0T delay for left-justified interface. |
| [7:3] | Reserved | R    | Reset to 00h                                                                                                                                                                 |

## RESERVED REGISTER – OFFSET72H

### LINE\_IN4 CONTROL REGISTER – OFFSET 73H(Default=00H)

| BITS  | FUNCTION                              | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|---------------------------------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [0]   | LINE_IN4 DET_EN                       | RW   | 0 : Disable LINE_IN4 status register update and interrupt<br>1: Enable LINE_IN4 status register update and interrupt                                                                                                                                                                                                                                                                         |
| [1]   | Reserved                              | R    | Reset to 00b                                                                                                                                                                                                                                                                                                                                                                                 |
| [2]   | LINE_IN4 Location<br>In data sequence | RW   | LINE_IN4OUTOFF is set to 0<br>0 :<br>I2S Mode :<br>L: d0 d1 d2 d3 d4 d5 d6 d7 d51 d52<br>R :d8 d9 dA dB dC dD dE dF d53 d54<br>DSP mode<br>d0 d1 d2 d3 d4 d5 d6 d7 d8 d9 dA dB dC dD dE dF<br>d51 d52 d53 d54<br>1:<br>I2S Mode :<br>L: d0 d1 d2 d3 d51 d4 d5 d6 d7 d52<br>R :d8 d9 dA dB d53 dC dD dE dF d54<br>DSP mode<br>d0 d1 d2 d3 d51 d4 d5 d6 d7 d52 d8 d9 dA dB d53 dC dD dE dF d54 |
| [7:3] | Reserved                              | R    | Reset to 00h                                                                                                                                                                                                                                                                                                                                                                                 |

### LINE\_IN4 DETECT ENABLE REGISTER – OFFSET 74H(Default=00H)

| BITS  | FUNCTION              | TYPE | DESCRIPTION                                    |
|-------|-----------------------|------|------------------------------------------------|
| [0]   | LINE_IN4 DETECT_STATE | RW   | Audio LINE_IN4 detect<br>0:Disable<br>1:Enable |
| [7:1] | Reserved              | R    | Reset to 00h                                   |

## RESERVED REGISTER – OFFSET75H-7AH

**SDOUT\_M SELECT (R) REGISTER – OFFSET 7BH(Default=00H)**

| BIT   | FUNCTION  | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|-----------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [4:0] | I2SO_RSEL | RW   | Select R channel output on SDOUT_M pin when SDOUTM_I2SOEN=1<br>0:Select record audio channel LINE_IN0<br>1:Select record audio channel LINE_IN1<br>2:Select record audio channel LINE_IN2<br>3:Select record audio channel LINE_IN3<br>4:Select record audio channel LINE_IN5<br>5:Select record audio channel LINE_IN6<br>6:Select record audio channel LINE_IN7<br>7:Select record audio channel LINE_IN8<br>8:Select record audio channel LINE_IN10<br>9:Select record audio channel LINE_IN11<br>A:Select record audio channel LINE_IN12<br>B:Select record audio channel LINE_IN13<br>C:Select record audio channel LINE_IN15<br>D:Select record audio channel LINE_IN16<br>E:Select record audio channel LINE_IN17<br>F:Select record audio channel LINE_IN18<br>10h:Select playback audio of the master chip<br>11h:Reserved<br>12h:Select playback audio of the slave chip<br>13h:Reserved<br>14h:Playback data output and playback data can adjust volume by DF[3:0]<br>15h:Select record audio of channel LINE_IN4<br>16h:Select record audio of channel LINE_IN9<br>17h:Select record audio of channel LINE_IN14<br>18h:Select record audio of channel LINE_IN19<br>Others:No audio output |
| [7:5] | Reserved  | R    | Reset to 0h                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

### SDOUT\_M SELECT (L) REGISTER – OFFSET 7CH(Default=00H)

| BITS  | FUNCTION  | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|-----------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [4:0] | I2SO_RSEL | RW   | Select L channel output on SDOUT_M pin when SDOUTM_I2SOEN=1:<br>0:Select record audio channel LINE_IN0<br>1:Select record audio channel LINE_IN1<br>2:Select record audio channel LINE_IN2<br>3:Select record audio channel LINE_IN3<br>4:Select record audio channel LINE_IN5<br>5:Select record audio channel LINE_IN6<br>6:Select record audio channel LINE_IN7<br>7:Select record audio channel LINE_IN8<br>8:Select record audio channel LINE_IN10<br>9:Select record audio channel LINE_IN11<br>A:Select record audio channel LINE_IN12<br>B:Select record audio channel LINE_IN13<br>C:Select record audio channel LINE_IN15<br>D:Select record audio channel LINE_IN16<br>E:Select record audio channel LINE_IN17<br>F:Select record audio channel LINE_IN18<br>10h:Select playback audio of the master chip<br>11h:Reserved<br>12h:Select playback audio of the slave chip<br>13h:Reserved<br>14h:Playback data output and playback data can adjust volume by DF[3:0]<br>15h:Select record audio of channel LINE_IN4<br>16h:Select record audio of channel LINE_IN9<br>17h:Select record audio of channel LINE_IN14<br>18h:Select record audio of channel LINE_IN19<br>Others:No audio output Others:No audio output |
| [7:5] | Reserved  | R    | Reset to 000b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

### EXTENDED LINE SELECT REGISTER – OFFSET 7DH(Default=E4H)

| BITS  | FUNCTION                              | TYPE | DESCRIPTION                                                |
|-------|---------------------------------------|------|------------------------------------------------------------|
| [1:0] | Select Output Data In Data51 Position | RW   | 0: LINE_IN4<br>1: LINE_IN9<br>2: LINE_IN14<br>3: LINE_IN19 |

|       |                                       |    |                                                            |
|-------|---------------------------------------|----|------------------------------------------------------------|
| [3:2] | Select Output Data In Data52 Position | RW | 0: LINE_IN4<br>1: LINE_IN9<br>2: LINE_IN14<br>3: LINE_IN19 |
| [5:4] | Select Output Data In Data53 Position | RW | 0: LINE_IN4<br>1: LINE_IN9<br>2: LINE_IN14<br>3: LINE_IN19 |
| [7:6] | Select Output Data In Data54 Position | RW | 0: LINE_IN4<br>1: LINE_IN9<br>2: LINE_IN14<br>3: LINE_IN19 |

**SDOUT\_M REGISTER– OFFSET 7EH(Default=00H)**

| BITS  | FUNCTION        | TYPE | DESCRIPTION                                                                                                                                                                                     |
|-------|-----------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [5:0] | Reserved        | R    | Reset to 00b                                                                                                                                                                                    |
| [6]   | SDOUT_M I2S OEN | R/W  | Define SDOUT_M pin output 2 word data to make standard I2S output<br>0: Mixing Data or Playback input data are only output on SDOUT_M<br>1:L/R data on SDOUT_M pin is selected by 0x7B and 0x7C |
| [7]   | A5OUTOFF        | R/W  | 0:LINE_IN4/LINE_IN9/LINE_IN14 /LINE_IN19 output on SDOUT_R<br>1:LINE_IN4/LINE_IN9/LINE_IN14 /LINE_IN19 not output on SDOUT_R                                                                    |

**MIX RATIO VALUE FOR LINE\_IN4 REGISTER – OFFSET 7FH(Default=00H)**

| BITS  | FUNCTION   | TYPE | DESCRIPTION                                                                                                                                                            |
|-------|------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | Mix_Ratio4 | RW   | LINE_IN4 ratio value for audio mixing function<br>0 : 1/2^8<br>1 : 1/2^7<br>2 : 1/2^6<br>3 : 1/2^5<br>4 : 1/2^4<br>5 : 1/2^3<br>6 : 1/2^2<br>7 : 1/2^1<br>other : 100% |
| [7:4] | Reserved   | R    | Reset to 00b                                                                                                                                                           |

## SOFTWARE RESET REGISTER– OFFSET 80H(Default=00H)

| BITS  | FUNCTION | TYPE | DESCRIPTION                                                                                                                      |
|-------|----------|------|----------------------------------------------------------------------------------------------------------------------------------|
| [0]   | VDEC0RST | W    | Writing one reset the video decoder 0 to its default state but all register content remain unchanged. This bit is self-resetting |
| [1]   | VDEC1RST | W    | Writing one reset the video decoder 1 to its default state but all register content remain unchanged. This bit is self-resetting |
| [2]   | VDEC2RST | W    | Writing one reset the video decoder 2 to its default state but all register content remain unchanged. This bit is self-resetting |
| [3]   | VDEC3RST | W    | Writing one reset the video decoder 3 to its default state but all register content remain unchanged. This bit is self-resetting |
| [4]   | Reserved | R    | Reset to 00b                                                                                                                     |
| [5]   | AUDIORST | W    | Writing one reset the audio portion to its default state but all register content remain unchanged. This bit is self-resetting   |
| [7:6] | Reserved | R    | Reset to 00b                                                                                                                     |

## RESERVED REGISTER – OFFSET 81H-88H

## AUDIO FS MODE REGISTER– OFFSET 89H(Default=00H)

| BITS  | FUNCTION             | TYPE | DESCRIPTION          |
|-------|----------------------|------|----------------------|
| [1:0] | Reserved             | R    | Reset to 00b         |
| [2]   | Audio FS Mode Select | RW   | 0: 256fs<br>1: 320fs |
| [7:3] | Reserved             | R    | Reset to 00h         |

## RESERVED REGISTER – OFFSET 8AH-95H

## VIN1 COLOR KILL ENABLE-REGISTER – OFFSET 96H(Default=C0H)

| BITS  | FUNCTION      | TYPE | DESCRIPTION                                                           |
|-------|---------------|------|-----------------------------------------------------------------------|
| [5:0] | Reserved      | RW   | Reset to 0h                                                           |
| [6]   | PAL CKILL EN  | RW   | 1:enable color kill mode in PAL<br>0:disable color kill mode in PAL   |
| [7]   | NTSC CKILL EN | RW   | 1:enable color kill mode in NTSC<br>0:disable color kill mode in NTSC |

## RESERVED REGISTER – OFFSET 97H-9EH

**PIXCLK 0 DELAY REGISTER– OFFSET 9FH(Default=00H)**

| BIT   | FUNCTION                                | TYPE | DESCRIPTION                                                                                                          |
|-------|-----------------------------------------|------|----------------------------------------------------------------------------------------------------------------------|
| [3:0] | Control Clock Delay Of<br>PIXCLK_P0 Pin | RW   | 0h: No clock delay<br>1h: About 1ns more delay,<br>2h : About 2ns more delay,<br>.<br>.<br>Fh: About 15ns more delay |
| [7:4] | Control Clock Delay Of<br>PIXCLK_N0 Pin | RW   | 0h: No clock delay<br>1h: About 1ns more delay,<br>2h : About 2ns more delay,<br>.<br>.<br>Fh: About 15ns more delay |

**RESERVED REGISTER – OFFSET A0H-B1H****VIDEO LOSS STATUS REGISTER – OFFSET B2H(Default=00H)**

| BIT | FUNCTION  | TYPE | DESCRIPTION                                         |
|-----|-----------|------|-----------------------------------------------------|
| [0] | VDLOSS1EN | R/W  | 0: disable<br>1: MPP1 output VIN1 video loss status |
| [1] | VDLOSS2EN | R/W  | 0: disable<br>1: MPP2 output VIN2 video loss status |
| [2] | VDLOSS3EN | R/W  | 0: disable<br>1: MPP3 output VIN3 video loss status |
| [3] | VDLOSS4EN | R/W  | 0: disable<br>1: MPP4 output VIN4 video loss status |
| [4] | VDLOSS5EN | R/W  | 0: disable<br>1: MPP5 output VIN5 video loss status |
| [5] | VDLOSS6EN | R/W  | 0: disable<br>1: MPP6 output VIN6 video loss status |
| [6] | VDLOSS7EN | R/W  | 0: disable<br>1: MPP7 output VIN7 video loss status |
| [7] | VDLOSS8EN | R/W  | 0: disable<br>1: MPP8 output VIN8 video loss status |

**RESERVED REGISTER – OFFSET B3H-C7H**

## GPIO\_0\_1 MODE REGISTER- OFFSET C8H(Default=00H)

| BITS  | FUNCTION                            | TYPE | DESCRIPTION                                                                                                                                                        |
|-------|-------------------------------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [2:0] | Output Mode For GPIO_0 Pin          | RW   | Select output mode for GPIO_0 pin<br>0: Output HSYNC<br>1: Output VSYNC<br>2:Field<br>3:H-active<br>4:VH-active<br>5:27MHz clock output<br>6:VH-sync<br>7:GPP_VA1  |
| [3]   | General Purpose Value In GPIO_0 Pin | RW   | Set general purpose value in GPIO_0 pin                                                                                                                            |
| [6:4] | Output Mode For GPIO_1 Pin          | RW   | Select output mode for GPIO_1 pin<br>0: Output HSYNC<br>1: Output VSYNC<br>2:Field<br>3:H-active<br>4:VH-active<br>5:27MHz clock output<br>6: VH-sync<br>7:GPP_VA2 |
| [7]   | General Purpose Value In GPIO_1 Pin | RW   | Set general purpose value in GPIO_1 pin                                                                                                                            |

## GPIO\_2\_3 MODE REGISTER- OFFSET C9H(Default=00H)

| BITS  | FUNCTION                            | TYPE | DESCRIPTION                                                                                                                                                       |
|-------|-------------------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [2:0] | Output Mode For GPIO_2 Pin          | RW   | Select output mode for GPIO_2 pin<br>0: Output HSYNC<br>1: Output VSYNC<br>2:Field<br>3:H-active<br>4:VH-active<br>5:27MHz clock output<br>6:VH-sync<br>7:GPP_VA1 |
| [3]   | General Purpose Value In GPIO_2 Pin | RW   | Set general purpose value in GPIO_2 pin                                                                                                                           |

|       |                                     |    |                                                                                                                                                                         |
|-------|-------------------------------------|----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [6:4] | Output Mode For GPIO_3 Pin          | RW | Select output mode for GPIO_3 pin<br>0: Output HSYNC<br>1: Output VSYNC<br>2: Field<br>3: H-active<br>4: VH-active<br>5: 27MHz clock output<br>6: VH-sync<br>7: GPP_VA2 |
| [7]   | General Purpose Value In GPIO_3 Pin | RW | Set general purpose value in GPIO_3 pin                                                                                                                                 |

**RESERVED REGISTER – OFFSET CAH****GPIO POLARITY REGISTER – OFFSET CBH (Default=00H)**

| BIT | FUNCTION                           | TYPE | DESCRIPTION                      |
|-----|------------------------------------|------|----------------------------------|
| [0] | Select GPIO_0 Pin Output Polarity. | RW   | 0: Normal<br>1: Inverse polarity |
| [1] | Select GPIO_1 Pin Output Polarity. | RW   | 0: Normal<br>1: Inverse polarity |
| [2] | Select GPIO_2 Pin Output Polarity. | RW   | 0: Normal<br>1: Inverse polarity |
| [3] | Select GPIO_3 Pin Output Polarity. | RW   | 0: Normal<br>1: Inverse polarity |
| [4] | Select GPIO_4 Pin Output Polarity. | RW   | 0: Normal<br>1: Inverse polarity |
| [5] | Select GPIO_5 Pin Output Polarity. | RW   | 0: Normal<br>1: Inverse polarity |
| [6] | Select GPIO_6 Pin Output Polarity. | RW   | 0: Normal<br>1: Inverse polarity |
| [7] | Select GPIO_7 Pin Output Polarity. | RW   | 0: Normal<br>1: Inverse polarity |

**RESERVED REGISTER – OFFSET CCH****WD1 D1 SELECT REGISTER – OFFSET CDH (Default=00H)**

| BIT | FUNCTION | TYPE | DESCRIPTION                                                                        |
|-----|----------|------|------------------------------------------------------------------------------------|
| [0] | O36M1    | RW   | 0: Channel 1 generates 27MHz video data<br>1: Channel 1 generates 36MHz video data |
| [1] | O36M2    | RW   | 0: Channel 2 generates 27MHz video data<br>1: Channel 2 generates 36MHz video data |

|     |       |    |                                                                                    |
|-----|-------|----|------------------------------------------------------------------------------------|
| [2] | O36M3 | RW | 0: Channel 3 generates 27MHz video data<br>1: Channel 3 generates 36MHz video data |
| [3] | O36M4 | RW | 0: Channel 4 generates 27MHz video data<br>1: Channel 4 generates 36MHz video data |
| [4] | O36M5 | RW | 0: Channel 5 generates 27MHz video data<br>1: Channel 5 generates 36MHz video data |
| [5] | O36M6 | RW | 0: Channel 6 generates 27MHz video data<br>1: Channel 6 generates 36MHz video data |
| [6] | O36M7 | RW | 0: Channel 7 generates 27MHz video data<br>1: Channel 7 generates 36MHz video data |
| [7] | O36M8 | RW | 0: Channel 8 generates 27MHz video data<br>1: Channel 8 generates 36MHz video data |

## RESERVED REGISTER- OFFSET CEH

## SERIAL MODE CONTROL REGISTER- OFFSET CFH(Default=00H)

| BITS  | FUNCTION | TYPE | DESCRIPTION                                                                       |
|-------|----------|------|-----------------------------------------------------------------------------------|
| [6:0] | Reserved | R    | Reset to 00h                                                                      |
| [7]   | SMD      | RW   | Cascade Audio Serial mode.<br>0: SD_LINKO is tri stated<br>1: SD_LINKO is enabled |

## RESERVED REGISTER- OFFSET D0H-D1H

## SDOUT\_RM OUTPUT REGISTER- OFFSET D2H(Default=03H)

| BITS  | FUNCTION                              | TYPE | DESCRIPTION                                                                                                                                                    |
|-------|---------------------------------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [1:0] | 16 Audios Recorded On The SDOUT_R Pin | R    | Reset to 11b                                                                                                                                                   |
| [3:2] | R_SDOUTM                              | RW   | Select the output mode for SDOUT_M pin<br>0:The output is controlled by SDOUTM_I2SOE<br>1: Record audio in SDOUT_R format<br>2: Record audio in SDOUT_M format |
| [5:4] | Reserved                              | R    | Reset to 00b                                                                                                                                                   |
| [6]   | RM_SYNC                               | RW   | Record and mixing audio data format<br>0: I2S mode<br>1: DSP mode                                                                                              |

|     |               |    |                                                                                                                                                                                                                                                                                         |
|-----|---------------|----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7] | Data Position | RW | <p>I2S MODE</p> <p>0: Mix data on position 0, Playback data on position 8</p> <p>1: Mix data on position 8, Playback data on position 0</p> <p>DSP MODE</p> <p>0: Mix data on position 0, Playback data on position 1</p> <p>1: Mix data on position 1, Playback data on position 0</p> |
|-----|---------------|----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

**SDOUT\_R\_SEQ\_1\_0 REGISTER– OFFSET D3H(Default=10H)**

| BIT   | FUNCTION | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                |
|-------|----------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | R_SEQ0   | RW   | <p>The sequence on the SDOUT_R</p> <p>0: LINE_IN0</p> <p>1: LINE_IN1</p> <p>2: LINE_IN2</p> <p>3: LINE_IN3</p> <p>4: LINE_IN5</p> <p>5: LINE_IN6</p> <p>6: LINE_IN7</p> <p>7: LINE_IN8</p> <p>8: LINE_IN10</p> <p>9: LINE_IN11</p> <p>A: LINE_IN12</p> <p>B: LINE_IN13</p> <p>C: LINE_IN15</p> <p>D: LINE_IN16</p> <p>E: LINE_IN17</p> <p>F: LINE_IN18</p> |

|       |        |    |                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:4] | R_SEQ1 | RW | <p>The sequence on the SDOUT_R</p> <p>0: LINE_IN0</p> <p>1: LINE_IN1</p> <p>2: LINE_IN2</p> <p>3: LINE_IN3</p> <p>4: LINE_IN5</p> <p>5: LINE_IN6</p> <p>6: LINE_IN7</p> <p>7: LINE_IN8</p> <p>8: LINE_IN10</p> <p>9: LINE_IN11</p> <p>A: LINE_IN12</p> <p>B: LINE_IN13</p> <p>C: LINE_IN15</p> <p>D: LINE_IN16</p> <p>E: LINE_IN17</p> <p>F: LINE_IN18</p> |
|-------|--------|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## SDOUT\_R\_SEQ\_3\_2 REGISTER- OFFSET D4H(Default=32H)

| BITS  | FUNCTION | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                |
|-------|----------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | R_SEQ2   | RW   | <p>The sequence on the SDOUT_R</p> <p>0: LINE_IN0</p> <p>1: LINE_IN1</p> <p>2: LINE_IN2</p> <p>3: LINE_IN3</p> <p>4: LINE_IN5</p> <p>5: LINE_IN6</p> <p>6: LINE_IN7</p> <p>7: LINE_IN8</p> <p>8: LINE_IN10</p> <p>9: LINE_IN11</p> <p>A: LINE_IN12</p> <p>B: LINE_IN13</p> <p>C: LINE_IN15</p> <p>D: LINE_IN16</p> <p>E: LINE_IN17</p> <p>F: LINE_IN18</p> |

|       |        |    |                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:4] | R_SEQ3 | RW | <p>The sequence on the SDOUT_R</p> <p>0: LINE_IN0</p> <p>1: LINE_IN1</p> <p>2: LINE_IN2</p> <p>3: LINE_IN3</p> <p>4: LINE_IN5</p> <p>5: LINE_IN6</p> <p>6: LINE_IN7</p> <p>7: LINE_IN8</p> <p>8: LINE_IN10</p> <p>9: LINE_IN11</p> <p>A: LINE_IN12</p> <p>B: LINE_IN13</p> <p>C: LINE_IN15</p> <p>D: LINE_IN16</p> <p>E: LINE_IN17</p> <p>F: LINE_IN18</p> |
|-------|--------|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## SDOUT\_R\_SEQ\_5\_4 REGISTER- OFFSET D5H(Default=54H)

| BITS  | FUNCTION | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                |
|-------|----------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | R_SEQ4   | RW   | <p>The sequence on the SDOUT_R</p> <p>0: LINE_IN0</p> <p>1: LINE_IN1</p> <p>2: LINE_IN2</p> <p>3: LINE_IN3</p> <p>4: LINE_IN5</p> <p>5: LINE_IN6</p> <p>6: LINE_IN7</p> <p>7: LINE_IN8</p> <p>8: LINE_IN10</p> <p>9: LINE_IN11</p> <p>A: LINE_IN12</p> <p>B: LINE_IN13</p> <p>C: LINE_IN15</p> <p>D: LINE_IN16</p> <p>E: LINE_IN17</p> <p>F: LINE_IN18</p> |

|       |        |    |                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:4] | R_SEQ5 | RW | <p>The sequence on the SDOUT_R</p> <p>0: LINE_IN0</p> <p>1: LINE_IN1</p> <p>2: LINE_IN2</p> <p>3: LINE_IN3</p> <p>4: LINE_IN5</p> <p>5: LINE_IN6</p> <p>6: LINE_IN7</p> <p>7: LINE_IN8</p> <p>8: LINE_IN10</p> <p>9: LINE_IN11</p> <p>A: LINE_IN12</p> <p>B: LINE_IN13</p> <p>C: LINE_IN15</p> <p>D: LINE_IN16</p> <p>E: LINE_IN17</p> <p>F: LINE_IN18</p> |
|-------|--------|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## SDOUT\_R\_SEQ\_7\_6REGISTER- OFFSET D6H(Default=76H)

| BITS  | FUNCTION | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                |
|-------|----------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | R_SEQ6   | RW   | <p>The sequence on the SDOUT_R</p> <p>0: LINE_IN0</p> <p>1: LINE_IN1</p> <p>2: LINE_IN2</p> <p>3: LINE_IN3</p> <p>4: LINE_IN5</p> <p>5: LINE_IN6</p> <p>6: LINE_IN7</p> <p>7: LINE_IN8</p> <p>8: LINE_IN10</p> <p>9: LINE_IN11</p> <p>A: LINE_IN12</p> <p>B: LINE_IN13</p> <p>C: LINE_IN15</p> <p>D: LINE_IN16</p> <p>E: LINE_IN17</p> <p>F: LINE_IN18</p> |

|       |        |    |                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:4] | R_SEQ7 | RW | <p>The sequence on the SDOUT_R</p> <p>0: LINE_IN0</p> <p>1: LINE_IN1</p> <p>2: LINE_IN2</p> <p>3: LINE_IN3</p> <p>4: LINE_IN5</p> <p>5: LINE_IN6</p> <p>6: LINE_IN7</p> <p>7: LINE_IN8</p> <p>8: LINE_IN10</p> <p>9: LINE_IN11</p> <p>A: LINE_IN12</p> <p>B: LINE_IN13</p> <p>C: LINE_IN15</p> <p>D: LINE_IN16</p> <p>E: LINE_IN17</p> <p>F: LINE_IN18</p> |
|-------|--------|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## SDOUT\_R\_SEQ\_9\_8 REGISTER- OFFSET D7H(Default=98H)

| BITS  | FUNCTION | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                |
|-------|----------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | R_SEQ8   | RW   | <p>The sequence on the SDOUT_R</p> <p>0: LINE_IN0</p> <p>1: LINE_IN1</p> <p>2: LINE_IN2</p> <p>3: LINE_IN3</p> <p>4: LINE_IN5</p> <p>5: LINE_IN6</p> <p>6: LINE_IN7</p> <p>7: LINE_IN8</p> <p>8: LINE_IN10</p> <p>9: LINE_IN11</p> <p>A: LINE_IN12</p> <p>B: LINE_IN13</p> <p>C: LINE_IN15</p> <p>D: LINE_IN16</p> <p>E: LINE_IN17</p> <p>F: LINE_IN18</p> |

|       |        |    |                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:4] | R_SEQ9 | RW | <p>The sequence on the SDOUT_R</p> <p>0: LINE_IN0</p> <p>1: LINE_IN1</p> <p>2: LINE_IN2</p> <p>3: LINE_IN3</p> <p>4: LINE_IN5</p> <p>5: LINE_IN6</p> <p>6: LINE_IN7</p> <p>7: LINE_IN8</p> <p>8: LINE_IN10</p> <p>9: LINE_IN11</p> <p>A: LINE_IN12</p> <p>B: LINE_IN13</p> <p>C: LINE_IN15</p> <p>D: LINE_IN16</p> <p>E: LINE_IN17</p> <p>F: LINE_IN18</p> |
|-------|--------|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## SDOUT\_R\_SEQ\_B\_A REGISTER- OFFSET D8H(Default= BAH)

| BITS  | FUNCTION | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                |
|-------|----------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | R_SEQA   | RW   | <p>The sequence on the SDOUT_R</p> <p>0: LINE_IN0</p> <p>1: LINE_IN1</p> <p>2: LINE_IN2</p> <p>3: LINE_IN3</p> <p>4: LINE_IN5</p> <p>5: LINE_IN6</p> <p>6: LINE_IN7</p> <p>7: LINE_IN8</p> <p>8: LINE_IN10</p> <p>9: LINE_IN11</p> <p>A: LINE_IN12</p> <p>B: LINE_IN13</p> <p>C: LINE_IN15</p> <p>D: LINE_IN16</p> <p>E: LINE_IN17</p> <p>F: LINE_IN18</p> |

|       |        |    |                                                                                                                                                                                                                                                                                     |
|-------|--------|----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:4] | R_SEQB | RW | The sequence on the SDOUT_R<br>0: LINE_IN0<br>1: LINE_IN1<br>2: LINE_IN2<br>3: LINE_IN3<br>4: LINE_IN5<br>5: LINE_IN6<br>6: LINE_IN7<br>7: LINE_IN8<br>8: LINE_IN10<br>9: LINE_IN11<br>A: LINE_IN12<br>B: LINE_IN13<br>C: LINE_IN15<br>D: LINE_IN16<br>E: LINE_IN17<br>F: LINE_IN18 |
|-------|--------|----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

**SDOUT\_R\_SEQ\_D\_C REGISTER- OFFSET D9H(Default= DCH)**

| BITS  | FUNCTION | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                         |
|-------|----------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | R_SEQC   | RW   | The sequence on the SDOUT_R<br>0: LINE_IN0<br>1: LINE_IN1<br>2: LINE_IN2<br>3: LINE_IN3<br>4: LINE_IN5<br>5: LINE_IN6<br>6: LINE_IN7<br>7: LINE_IN8<br>8: LINE_IN10<br>9: LINE_IN11<br>A: LINE_IN12<br>B: LINE_IN13<br>C: LINE_IN15<br>D: LINE_IN16<br>E: LINE_IN17<br>F: LINE_IN18 |

|       |        |    |                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:4] | R_SEQD | RW | <p>The sequence on the SDOUT_R</p> <p>0: LINE_IN0</p> <p>1: LINE_IN1</p> <p>2: LINE_IN2</p> <p>3: LINE_IN3</p> <p>4: LINE_IN5</p> <p>5: LINE_IN6</p> <p>6: LINE_IN7</p> <p>7: LINE_IN8</p> <p>8: LINE_IN10</p> <p>9: LINE_IN11</p> <p>A: LINE_IN12</p> <p>B: LINE_IN13</p> <p>C: LINE_IN15</p> <p>D: LINE_IN16</p> <p>E: LINE_IN17</p> <p>F: LINE_IN18</p> |
|-------|--------|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## SDOUT\_R\_SEQ\_F\_E REGISTER- OFFSET DAH(Default= FEH)

| BITS  | FUNCTION | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                |
|-------|----------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | R_SEQE   | RW   | <p>The sequence on the SDOUT_R</p> <p>0: LINE_IN0</p> <p>1: LINE_IN1</p> <p>2: LINE_IN2</p> <p>3: LINE_IN3</p> <p>4: LINE_IN5</p> <p>5: LINE_IN6</p> <p>6: LINE_IN7</p> <p>7: LINE_IN8</p> <p>8: LINE_IN10</p> <p>9: LINE_IN11</p> <p>A: LINE_IN12</p> <p>B: LINE_IN13</p> <p>C: LINE_IN15</p> <p>D: LINE_IN16</p> <p>E: LINE_IN17</p> <p>F: LINE_IN18</p> |

|       |        |    |                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:4] | R_SEQF | RW | <p>The sequence on the SDOUT_R</p> <p>0: LINE_IN0</p> <p>1: LINE_IN1</p> <p>2: LINE_IN2</p> <p>3: LINE_IN3</p> <p>4: LINE_IN5</p> <p>5: LINE_IN6</p> <p>6: LINE_IN7</p> <p>7: LINE_IN8</p> <p>8: LINE_IN10</p> <p>9: LINE_IN11</p> <p>A: LINE_IN12</p> <p>B: LINE_IN13</p> <p>C: LINE_IN15</p> <p>D: LINE_IN16</p> <p>E: LINE_IN17</p> <p>F: LINE_IN18</p> |
|-------|--------|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## I2S MASTER CONTROL REGISTER- OFFSET DBH(Default= C2H)

| BIT | FUNCTION               | TYPE | DESCRIPTION                                                                                                                                                                                                                              |
|-----|------------------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [0] | ACLKRMMASTER           | RW   | <p>0: SCLK_R pin is slave mode</p> <p>1: SCLK_R pin is master mode</p>                                                                                                                                                                   |
| [1] | Reserved               | R    | Reset to 1b                                                                                                                                                                                                                              |
| [2] | SDOUT_RPin Data Format | RW   | <p>Per word unit on SDOUT_R Pin</p> <p>0: 16bit</p> <p>1: 8bit</p>                                                                                                                                                                       |
| [3] | PB_SYNC                | RW   | <p>The audio data format for audio playback mode</p> <p>0: I2S mode for playback</p> <p>1: DSP mode for playback</p>                                                                                                                     |
| [4] | PB_LRSEL               | RW   | <p>Select the audio data position in playback input</p> <p>I2S mode:</p> <p>0: 1st Left channel audio data</p> <p>1: 1st Right channel audio data</p> <p>DSP mode:</p> <p>0: 1st channel audio data</p> <p>1: 2nd channel audio data</p> |
| [5] | PB_MASTER              | RW   | <p>The operation mode for playback mode.</p> <p>0: SCLK_P pin is slave mode</p> <p>1: SCLK_P pin is master mode</p>                                                                                                                      |

|       |          |   |              |
|-------|----------|---|--------------|
| [7:6] | Reserved | R | Reset to 11b |
|-------|----------|---|--------------|

## MIX\_MUTE REGISTER- OFFSET DCH(Default=00H)

| BITS  | FUNCTION | TYPE | DESCRIPTION                                                                                                                                                   |
|-------|----------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [4:0] | MIX_MUTE | R    | Mute function Enable<br>0 : disable 1: mute<br>Bit[0] : LINE_0;<br>Bit[1] : LINE_1;<br>Bit[2] : LINE_2;<br>Bit[3] : LINE_3;<br>Bit[4] : Playback audio input; |
| [7:5] | Reserved | R    | Reset to 00b                                                                                                                                                  |

## MIX RATIO VALUE FOR LINE\_IN0 & LINE\_IN1 REGISTER - OFFSET DDH (Default=00H)

| BITS  | FUNCTION   | TYPE | DESCRIPTION                                                                                                                                                            |
|-------|------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | Mix_Ratio0 | RW   | LINE_IN0 ratio value for audio mixing function<br>0 : 1/2^8<br>1 : 1/2^7<br>2 : 1/2^6<br>3 : 1/2^5<br>4 : 1/2^4<br>5 : 1/2^3<br>6 : 1/2^2<br>7 : 1/2^1<br>other : 100% |
| [7:4] | Mix_Ratio1 | R/W  | LINE_IN1 ratio value for audio mixing function<br>0 : 1/2^8<br>1 : 1/2^7<br>2 : 1/2^6<br>3 : 1/2^5<br>4 : 1/2^4<br>5 : 1/2^3<br>6 : 1/2^2<br>7 : 1/2^1<br>other : 100% |

**MIX RATIO VALUE FOR LINE\_IN2 & LINE\_IN3 REGISTER – OFFSET DEH (Default=00H)**

| BIT   | FUNCTION   | TYPE | DESCRIPTION                                                                                                                                                                                                                                                    |
|-------|------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | Mix_Ratio2 | RW   | LINE_IN2 ratio value for audio mixing function<br>0 : 1/2 <sup>8</sup><br>1 : 1/2 <sup>7</sup><br>2 : 1/2 <sup>6</sup><br>3 : 1/2 <sup>5</sup><br>4 : 1/2 <sup>4</sup><br>5 : 1/2 <sup>3</sup><br>6 : 1/2 <sup>2</sup><br>7 : 1/2 <sup>1</sup><br>other : 100% |
| [7:4] | Mix_Ratio3 | R/W  | LINE_IN3 ratio value for audio mixing function<br>0 : 1/2 <sup>8</sup><br>1 : 1/2 <sup>7</sup><br>2 : 1/2 <sup>6</sup><br>3 : 1/2 <sup>5</sup><br>4 : 1/2 <sup>4</sup><br>5 : 1/2 <sup>3</sup><br>6 : 1/2 <sup>2</sup><br>7 : 1/2 <sup>1</sup><br>other : 100% |

**PB RATIO REGISTER – OFFSET DFH (Default=00H)**

| BIT   | FUNCTION                     | TYPE | DESCRIPTION                                                                                                                                                                                                                                                          |
|-------|------------------------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | Ratio Value For Audio Mixing | RW   | Playback input ratio value for audio mixing function<br>0 : 1/2 <sup>8</sup><br>1 : 1/2 <sup>7</sup><br>2 : 1/2 <sup>6</sup><br>3 : 1/2 <sup>5</sup><br>4 : 1/2 <sup>4</sup><br>5 : 1/2 <sup>3</sup><br>6 : 1/2 <sup>2</sup><br>7 : 1/2 <sup>1</sup><br>other : 100% |
| [7:4] | Reserved                     | R    | Reset to 0h                                                                                                                                                                                                                                                          |

## MIXING OUTPUT CONTROL REGISTER– OFFSET E0H(Default=14H)

| BITS  | FUNCTION   | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [4:0] | MIX_OUTSEL | RW   | <p>Define the final audio output for analog and digital mixing out:</p> <p>0:Select record audio channel LINE_IN0</p> <p>1:Select record audio channel LINE_IN1</p> <p>2:Select record audio channel LINE_IN2</p> <p>3:Select record audio channel LINE_IN3</p> <p>4:Select record audio channel LINE_IN5</p> <p>5:Select record audio channel LINE_IN6</p> <p>6:Select record audio channel LINE_IN7</p> <p>7:Select record audio channel LINE_IN8</p> <p>8:Select record audio channel LINE_IN10</p> <p>9:Select record audio channel LINE_IN11</p> <p>A:Select record audio channel LINE_IN12</p> <p>B:Select record audio channel LINE_IN13</p> <p>C:Select record audio channel LINE_IN15</p> <p>D:Select record audio channel LINE_IN16</p> <p>E:Select record audio channel LINE_IN17</p> <p>F:Select record audio channel LINE_IN18</p> <p>10h:Select playback audio of the master chip</p> <p>11h:Reserved</p> <p>12h:Select playback audio of the slave chip</p> <p>13h:Reserved</p> <p>14h:Playback data output and playback data can adjust volume by DF[3:0]</p> <p>15h:Select record audio of channel LINE_IN4</p> <p>16h:Select record audio of channel LINE_IN9</p> <p>17h:Select record audio of channel LINE_IN14</p> <p>18h:Select record audio of channel LINE_IN19</p> <p>Others :no audio input</p> |
| [7:5] | Reserved   | R    | Reset to 000b                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

## AUDIO DETECT TH 0123 MSB REGISTER– OFFSET E1H (Default=00H)

| BITS  | FUNCTION    | TYPE | DESCRIPTION                                          |
|-------|-------------|------|------------------------------------------------------|
| [0]   | ADET_TH0[4] | RW   | Bit4 of audio detection threshold value for LINE_IN0 |
| [1]   | ADET_TH1[4] | RW   | Bit4 of audio detection threshold value for LINE_IN1 |
| [2]   | ADET_TH2[3] | RW   | Bit4 of audio detection threshold value for LINE_IN2 |
| [3]   | ADET_TH3[4] | RW   | Bit4 of audio detection threshold value for LINE_IN3 |
| [7:4] | Reserved    | R    | Reset to 0h                                          |

**AUDIO DETECT TH 01 LSB REGISTER- OFFSET E2H (Default=AAH)**

| BITS  | FUNCTION      | TYPE | DESCRIPTION                                              |
|-------|---------------|------|----------------------------------------------------------|
| [3:0] | ADET_TH0[3:0] | RW   | Bit3 ~ 0 of audio detection threshold value for LINE_IN0 |
| [7:4] | ADET_TH1[3:0] | RW   | Bit3 ~ 0 of audio detection threshold value for LINE_IN1 |

**AUDIO DETECT TH 23 LSB REGISTER- OFFSET E3H (Default=AAH)**

| BITS  | FUNCTION      | TYPE | DESCRIPTION                                              |
|-------|---------------|------|----------------------------------------------------------|
| [3:0] | ADET_TH2[3:0] | RW   | Bit3 ~ 0 of audio detection threshold value for LINE_IN2 |
| [7:4] | ADET_TH3[3:0] | RW   | Bit3 ~ 0 of audio detection threshold value for LINE_IN3 |

**RESERVED REGISTER- OFFSET E4H-E6H****VD OUTPUT MODE REGISTER- OFFSET E7H (Default=55H)**

| BITS  | FUNCTION                      | TYPE | DESCRIPTION                                                                                                                   |
|-------|-------------------------------|------|-------------------------------------------------------------------------------------------------------------------------------|
| [1:0] | PIXOUT_0[7:0] Pin Output Mode | RW   | 0: Single output (Test Purpose Only)<br>1: 2xD1 dual channel video output<br>2: 4xD1 quad channel video output<br>3: Reserved |
| [3:2] | PIXOUT_1[7:0] Pin Output Mode | RW   | 0: Single output (Test Purpose Only)<br>1: 2xD1 dual channel video output<br>2: 4xD1 quad channel video output<br>3: Reserved |
| [5:4] | PIXOUT_2 Pin Output Mode      | RW   | 0: Single output with<br>1: 2xD1 dual channel video output<br>2: 4xD1 quad channel video output<br>3: Reserved                |
| [7:6] | PIXOUT_3 Pin Output Mode      | RW   | 0: Single output (Test Purpose Only)<br>1: 2xD1 dual channel video output<br>2: 4xD1 quad channel video output<br>3: Reserved |

## PIXOUT0 OUTPUT CH12 SELECT REGISTER– OFFSET E8H(Default=10H)

| BITS  | FUNCTION                          | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                         |
|-------|-----------------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | CH1 Data Selection In<br>PIXOUT_0 | RW   | 0: CV_INA0 Video Decoder data<br>1: CV_INA1 Video Decoder data<br>2: CV_INA2 Video Decoder data<br>3: CV_INA3 Video Decoder data<br>4: CV_INA4 Video Decoder data<br>5: CV_INA5 Video Decoder data<br>6: CV_INA6 Video Decoder data<br>7: CV_INA7 Video Decoder data<br>Reset to 0h |
| [7:4] | CH2 Data Selection In<br>PIXOUT_0 | RW   | 0: CV_INA0 Video Decoder data<br>1: CV_INA1 Video Decoder data<br>2: CV_INA2 Video Decoder data<br>3: CV_INA3 Video Decoder data<br>4: CV_INA4 Video Decoder data<br>5: CV_INA5 Video Decoder data<br>6: CV_INA6 Video Decoder data<br>7: CV_INA7 Video Decoder data<br>Reset to 1h |

## PIXOUT0 OUTPUT CH34 SELECT REGISTER– OFFSET E9H(Default=32H)

| BITS  | FUNCTION                          | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                         |
|-------|-----------------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | CH3 Data Selection In<br>PIXOUT_0 | RW   | 0: CV_INA0 Video Decoder data<br>1: CV_INA1 Video Decoder data<br>2: CV_INA2 Video Decoder data<br>3: CV_INA3 Video Decoder data<br>4: CV_INA4 Video Decoder data<br>5: CV_INA5 Video Decoder data<br>6: CV_INA6 Video Decoder data<br>7: CV_INA7 Video Decoder data<br>Reset to 2h |

|       |                                   |    |                                                                                                                                                                                                                                                                                     |
|-------|-----------------------------------|----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:4] | CH4 Data Selection In<br>PIXOUT_0 | RW | 0: CV_INA0 Video Decoder data<br>1: CV_INA1 Video Decoder data<br>2: CV_INA2 Video Decoder data<br>3: CV_INA3 Video Decoder data<br>4: CV_INA4 Video Decoder data<br>5: CV_INA5 Video Decoder data<br>6: CV_INA6 Video Decoder data<br>7: CV_INA7 Video Decoder data<br>Reset to 3h |
|-------|-----------------------------------|----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

**PIXOUT1 OUTPUT CH12 SELECT REGISTER- OFFSET EAH(Default=32H)**

| BITS  | FUNCTION                          | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                         |
|-------|-----------------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | CH1 Data Selection In<br>PIXOUT_1 | RW   | 0: CV_INA0 Video Decoder data<br>1: CV_INA1 Video Decoder data<br>2: CV_INA2 Video Decoder data<br>3: CV_INA3 Video Decoder data<br>4: CV_INA4 Video Decoder data<br>5: CV_INA5 Video Decoder data<br>6: CV_INA6 Video Decoder data<br>7: CV_INA7 Video Decoder data<br>Reset to 2h |
| [7:4] | CH2 Data Selection In<br>PIXOUT_1 | RW   | 0: CV_INA0 Video Decoder data<br>1: CV_INA1 Video Decoder data<br>2: CV_INA2 Video Decoder data<br>3: CV_INA3 Video Decoder data<br>4: CV_INA4 Video Decoder data<br>5: CV_INA5 Video Decoder data<br>6: CV_INA6 Video Decoder data<br>7: CV_INA7 Video Decoder data<br>Reset to 3h |

**PIXOUT1 OUTPUT CH34 SELECT REGISTER– OFFSET EBH(Default=54H)**

| BIT   | FUNCTION                          | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                         |
|-------|-----------------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | CH3 Data Selection In<br>PIXOUT_1 | RW   | 0: CV_INA0 Video Decoder data<br>1: CV_INA1 Video Decoder data<br>2: CV_INA2 Video Decoder data<br>3: CV_INA3 Video Decoder data<br>4: CV_INA4 Video Decoder data<br>5: CV_INA5 Video Decoder data<br>6: CV_INA6 Video Decoder data<br>7: CV_INA7 Video Decoder data<br>Reset to 4h |
| [7:4] | CH4 Data Selection In<br>PIXOUT_1 | RW   | 0: CV_INA0 Video Decoder data<br>1: CV_INA1 Video Decoder data<br>2: CV_INA2 Video Decoder data<br>3: CV_INA3 Video Decoder data<br>4: CV_INA4 Video Decoder data<br>5: CV_INA5 Video Decoder data<br>6: CV_INA6 Video Decoder data<br>7: CV_INA7 Video Decoder data<br>Reset to 5h |

**PIXOUT2 OUTPUT CH12 SELECT REGISTER– OFFSET ECH(Default=54H)**

| BIT   | FUNCTION                          | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                         |
|-------|-----------------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | CH1 Data Selection In<br>PIXOUT_2 | RW   | 0: CV_INA0 Video Decoder data<br>1: CV_INA1 Video Decoder data<br>2: CV_INA2 Video Decoder data<br>3: CV_INA3 Video Decoder data<br>4: CV_INA4 Video Decoder data<br>5: CV_INA5 Video Decoder data<br>6: CV_INA6 Video Decoder data<br>7: CV_INA7 Video Decoder data<br>Reset to 4h |

|       |                                   |    |                                                                                                                                                                                                                                                                                     |
|-------|-----------------------------------|----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:4] | CH2 Data Selection In<br>PIXOUT_2 | RW | 0: CV_INA0 Video Decoder data<br>1: CV_INA1 Video Decoder data<br>2: CV_INA2 Video Decoder data<br>3: CV_INA3 Video Decoder data<br>4: CV_INA4 Video Decoder data<br>5: CV_INA5 Video Decoder data<br>6: CV_INA6 Video Decoder data<br>7: CV_INA7 Video Decoder data<br>Reset to 5h |
|-------|-----------------------------------|----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

**PIXOUT2 OUTPUT CH34 SELECT REGISTER– OFFSET EDH(Default=76H)**

| BITS  | FUNCTION                          | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                         |
|-------|-----------------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | CH3 Data Selection In<br>PIXOUT_2 | RW   | 0: CV_INA0 Video Decoder data<br>1: CV_INA1 Video Decoder data<br>2: CV_INA2 Video Decoder data<br>3: CV_INA3 Video Decoder data<br>4: CV_INA4 Video Decoder data<br>5: CV_INA5 Video Decoder data<br>6: CV_INA6 Video Decoder data<br>7: CV_INA7 Video Decoder data<br>Reset to 6h |
| [7:4] | CH4 Data Selection In<br>PIXOUT_2 | RW   | 0: CV_INA0 Video Decoder data<br>1: CV_INA1 Video Decoder data<br>2: CV_INA2 Video Decoder data<br>3: CV_INA3 Video Decoder data<br>4: CV_INA4 Video Decoder data<br>5: CV_INA5 Video Decoder data<br>6: CV_INA6 Video Decoder data<br>7: CV_INA7 Video Decoder data<br>Reset to 7h |

**PIXOUT3 OUTPUT CH12 SELECT REGISTER– OFFSET EEH(Default=76H)**

| BITS  | FUNCTION                          | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                         |
|-------|-----------------------------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | CH1 Data Selection In<br>PIXOUT_3 | RW   | 0: CV_INA0 Video Decoder data<br>1: CV_INA1 Video Decoder data<br>2: CV_INA2 Video Decoder data<br>3: CV_INA3 Video Decoder data<br>4: CV_INA4 Video Decoder data<br>5: CV_INA5 Video Decoder data<br>6: CV_INA6 Video Decoder data<br>7: CV_INA7 Video Decoder data<br>Reset to 6h |
| [7:4] | CH2 Data Selection In<br>PIXOUT_3 | RW   | 0: CV_INA0 Video Decoder data<br>1: CV_INA1 Video Decoder data<br>2: CV_INA2 Video Decoder data<br>3: CV_INA3 Video Decoder data<br>4: CV_INA4 Video Decoder data<br>5: CV_INA5 Video Decoder data<br>6: CV_INA6 Video Decoder data<br>7: CV_INA7 Video Decoder data<br>Reset to 7h |

**PIXOUT3 OUTPUT CH34 SELECT REGISTER– OFFSET EFH(Default=10H)**

| BITS  | FUNCTION                          | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                 |
|-------|-----------------------------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | CH3 Data Selection In<br>PIXOUT_3 | RW   | 0: CV_IN0 Video Decoder data<br>1: CV_IN1 Video Decoder data<br>2: CV_IN2 Video Decoder data<br>3: CV_IN3 Video Decoder data<br>4: CV_IN4 Video Decoder data<br>5: CV_IN5 Video Decoder data<br>6: CV_IN6 Video Decoder data<br>7: CV_IN7 Video Decoder data<br>Reset to 0h |

|       |                                   |    |                                                                                                                                                                                                                                                                                     |
|-------|-----------------------------------|----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:4] | CH4 Data Selection In<br>PIXOUT_3 | RW | 0: CV_INA0 Video Decoder data<br>1: CV_INA1 Video Decoder data<br>2: CV_INA2 Video Decoder data<br>3: CV_INA3 Video Decoder data<br>4: CV_INA4 Video Decoder data<br>5: CV_INA5 Video Decoder data<br>6: CV_INA6 Video Decoder data<br>7: CV_INA7 Video Decoder data<br>Reset to 1h |
|-------|-----------------------------------|----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

**PIXCLK OUTPUT MODE REGISTER- OFFSET F9H (Default=00H)**

| BITS  | FUNCTION  | TYPE | DESCRIPTION                                                                                                                                         |
|-------|-----------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| [0]   | PIXCLK_PF | RW   | Output frequency mode of PIXCLK_PO pin.<br>0: Output one of 27MHz, 54MHz or 180MHz frequency.<br>1: Output one of 36MHz, 72MHz or 144MHz frequency. |
| [1]   | PIXCLK_NF | RW   | Output frequency mode of PIXCLK_NO pin.<br>0: Output one of 27MHz, 54MHz or 180MHz frequency.<br>1: Output one of 36MHz, 72MHz or 144MHz frequency. |
| [7:2] | Reserved  | R    | Reset to 0h                                                                                                                                         |

**CCIR656 CONTROL REGISTER- OFFSET FAH(Default=00H)**

| BITS  | FUNCTION                   | TYPE | DESCRIPTION                                                                                                                                             |
|-------|----------------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| [1:0] | PIXOUT format<br>Control   | W    | Control the data frequency of PIXOUT pins<br><br>0: 27M/36MHz data output<br>1: 54M/72MHz data output<br>2: 108M/144MHz data output<br><br>Reset to 00b |
| [3:2] | Reserved                   | W    | Reset to 00b                                                                                                                                            |
| [4]   | Reserved                   | R    | Reset to 0b                                                                                                                                             |
| [5]   | Reserved                   | R    | Reset to 0b                                                                                                                                             |
| [6]   | CCIR656 Output En-<br>able | RW   | 0: All outputs are tri-stated<br>1: All outputs(PIXOUT_n/PIXCLK_PO/PIXCLK_NO) are enabled                                                               |
| [7]   | Reserved                   | R    | Reset to 0b                                                                                                                                             |

## CLOCK POLARITY REGISTER– OFFSET FBH(Default=0FH)

| BITS  | FUNCTION     | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [1:0] | VDET_MODE    | RW   | Define the polarity of state register and interrupt request for video detection.<br>0: No interrupt request by the video detection<br>1: Make the interrupt request rising only when the video comes in<br>2: Make the interrupt request falling only when the video goes out<br>3: Make the interrupt request rising and falling when the video comes in and goes out |
| [3:2] | ADET_MODE    | RW   | Define the polarity of state register and interrupt request for audio detection.<br>0: No interrupt request by the audio detection<br>1: Make the interrupt request rising only when the audio comes in<br>2: Make the interrupt request falling only when the audio goes out<br>3: Make the interrupt request rising and falling when the audio comes in and goes out |
| [4]   | IRQPOL       | RW   | Select the polarity of interrupt request through the IRQ pin.<br>0: Falling edge requests the interrupt and keeps its state until cleared<br>1: Rising edge requests the interrupt and keeps its state until cleared                                                                                                                                                   |
| [5]   | IRQENA R/W   | RW   | Enable/Disable the interrupt request through the IRQ pin<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                                                    |
| [6]   | PIXCLK_P_POL | RW   | 0: The polarity of PIXCLK_P is not inversed<br>1: The polarity of PIXCLK_P is inversed                                                                                                                                                                                                                                                                                 |
| [7]   | PIXCLK_N_POL | RW   | 0: The polarity of PIXCLK_N is not inversed<br>1: The polarity of PIXCLK_N is inversed                                                                                                                                                                                                                                                                                 |

## VIDEO/AUDIO DETECTION ENABLE REGISTER–OFFSET FCH (Default=FFH)

| BITS | FUNCTION | TYPE | DESCRIPTION |
|------|----------|------|-------------|
|------|----------|------|-------------|

|       |          |    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|----------|----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:0] | AVDET_EN | RW | <p>Enable the status register updated and interrupt request if the following video or audio source is detected. The mapping of video/audio input to each bit of the register is defined as below.</p> <p>Bit0: Video input CV_IN0.<br/>           Bit1: Video input CV_IN1.<br/>           Bit2: Video input CV_IN2.<br/>           Bit3: Video input CV_IN3.<br/>           Bit4: Audio input LINE_IN0.<br/>           Bit5: Audio input LINE_IN1.<br/>           Bit6: Audio input LINE_IN2.<br/>           Bit7: Audio input LINE_IN3.</p> <p>0: Disable status register updated and interrupt request<br/>           1: Enable status register updated and interrupt request</p> |
|-------|----------|----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

**VIDEO/AUDIO DETECTION STATUS REGISTER-OFFSET FDH (Default=00H)**

| BITS  | FUNCTION | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|----------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:0] | AVDET_EN | RW   | <p>Enable the status register updated and interrupt request if the following video or audio source is detected. The mapping of video/audio input to each bit of the register is defined as below.</p> <p>Bit0: Video input CV_IN0.<br/>           Bit1: Video input CV_IN1.<br/>           Bit2: Video input CV_IN2.<br/>           Bit3: Video input CV_IN3.<br/>           Bit4: Audio input LINE_IN0.<br/>           Bit5: Audio input LINE_IN1.<br/>           Bit6: Audio input LINE_IN2.<br/>           Bit7: Audio input LINE_IN3.</p> <p>0: Disable status register updated and interrupt request<br/>           1: Enable status register updated and interrupt request</p> |

**DEVICE ID\_H REGISTER- OFFSET FEH(Default=00H)**

| BITS  | FUNCTION    | TYPE | DESCRIPTION  |
|-------|-------------|------|--------------|
| [5:0] | Reserved    | R    | Reset to 00h |
| [7:6] | Dev_ID[6:5] | R    | Reset to 00b |

**DEVICE ID - L REGISTER- OFFSET FFH(Default=F0H)**

| BIT   | FUNCTION    | TYPE | DESCRIPTION   |
|-------|-------------|------|---------------|
| [2:0] | REV_ID      | R    | Reset to 000b |
| [7:3] | Dev_ID[4:0] | R    | Reset to 1eh  |

## PAGE 1 REGISTERS

| Register Type | Descriptions |
|---------------|--------------|
| R             | Read Only    |
| RW            | Read/Write   |

## VIDEO STATUS REGISTER – OFFSET 00H/10H/20H/30H (Default: 00H)

| BIT | FUNCTION | TYPE | DESCRIPTION                                                                      |
|-----|----------|------|----------------------------------------------------------------------------------|
| 0   | DET50    | R    | 0: 60Hz source detected<br>1: 50Hz source detected                               |
| 1   | MONO     | R    | 0: Color burst signal detected<br>1: No color burst signal detected              |
| 2   | Reserved | R    | Reset to 0b                                                                      |
| 3   | VLOCK    | R    | 0: Vertical logic is not locked<br>1: Vertical logic is locked to incoming video |
| 4   | Reserved | R    | Reset to 0b                                                                      |
| 5   | SLOCK    | R    | 0: Sub-carrier sync is not detected<br>1: Sub-carrier sync is detected           |
| 6   | HLOCK    | R    | 0: Horizontal sync is not detected<br>1: Horizontal sync is detected             |
| 7   | VDLOSS   | R    | 0: Video is detected<br>1: Video not present                                     |

## BRIGHTNESS CONTROL REGISTER – OFFSET 01H/11H/21H/31H(Default=00H)

| BIT   | FUNCTION   | TYPE | DESCRIPTION                                                                                                                    |
|-------|------------|------|--------------------------------------------------------------------------------------------------------------------------------|
| [7:0] | Brightness | RW   | These Signed bits control the brightness. Value range from -128 to 127<br>8'h7F: brightest; 8'h80: darkest ; 8'h00 : no effect |

## CONTRASTCONTROL REGISTER – OFFSET 02H/12H/22H/32H(Default=64H)

| BIT   | FUNCTION | TYPE | DESCRIPTION                                                                                           |
|-------|----------|------|-------------------------------------------------------------------------------------------------------|
| [7:0] | Contrast | RW   | These unsigned bits control the luminance gain.<br>8'h7F: maximum contrast<br>8'h00: minimum contrast |

**SHARPNESSCONTROL REGISTER – OFFSET 03H/13H/23H/33H(Default=00H)**

| BITS  | FUNCTION  | TYPE | DESCRIPTION                                                                                                                                                                                               |
|-------|-----------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | Sharpness | RW   | These bits control the amount of sharpness enhancement on the luminance signals<br>"0" has no effect on the output image<br>"1" through "15" provides sharpness enhancement with "15" being the strongest |
| [7:4] | Reserved  | R    | Reset to 0h                                                                                                                                                                                               |

**CHROMA(U) GAIN REGISTER – OFFSET 04H/14H/24H/34H(Default=80H)**

| BITS  | FUNCTION        | TYPE | DESCRIPTION                                           |
|-------|-----------------|------|-------------------------------------------------------|
| [7:0] | Chroma (U) Gain | RW   | Chroma gain value of controlling the color saturation |

**CHROMA(V) GAIN REGISTER – OFFSET 05H/15H/25H/35H(Default=80H)**

| BITS  | FUNCTION        | TYPE | DESCRIPTION                                           |
|-------|-----------------|------|-------------------------------------------------------|
| [7:0] | Chroma (V) Gain | RW   | Chroma gain value of controlling the color saturation |

**HUECONTROL REGISTER – OFFSET 06H/16H/26H/36H(Default=00H)**

| BITS  | FUNCTION | TYPE | DESCRIPTION                                                    |
|-------|----------|------|----------------------------------------------------------------|
| [7:0] | Hue      | RW   | These signed bits control color hue.<br>+90C(7Fh) to -90C(80h) |

**H-Delay REGISTER – OFFSET 0AH/1AH/2AH/3AH(Default=00H)**

| BITS  | FUNCTION                     | TYPE | DESCRIPTION                                  |
|-------|------------------------------|------|----------------------------------------------|
| [7:5] | Reserved                     | R    | Reset to 0b                                  |
| [4:0] | HorizontalShift Pixels Point | R/W  | Left shift the start points of video outputs |

**STANDARD SELECTION REGISTER – OFFSET 0EH/1EH/2EH/3EH(Default=77H)**

| BITS  | FUNCTION           | TYPE | DESCRIPTION                                                                                                                |
|-------|--------------------|------|----------------------------------------------------------------------------------------------------------------------------|
| [2:0] | Standard Selection | RW   | 0: NTSC(M)<br>1: PAL(B,D,G,H,I)<br>2: Not valid<br>3: NTSC4.43<br>4: PAL(M)<br>5: PAL(CN)<br>6: PAL60<br>7: Auto detection |
| [3]   | Reserved           | R    | Reset to 0b                                                                                                                |

|       |                           |   |                                                                                                                     |
|-------|---------------------------|---|---------------------------------------------------------------------------------------------------------------------|
| [6:4] | Current Standard Detected | R | 0: NTSC(M)<br>1: PAL(B,D,G,H,I)<br>2:Not valid<br>3: NTSC4.43<br>4: PAL(M)<br>5: PAL(CN)<br>6: PAL60<br>7:Not valid |
| [7]   | Reserved                  | R | Reset to 0b                                                                                                         |

## High HBLN REGISTER – OFFSET 56H (Default=00H)

| BITS  | FUNCTION | TYPE | DESCRIPTION                                                |
|-------|----------|------|------------------------------------------------------------|
| [0]   | HBLN4[8] | R    | Display the blanking length starting from EAV to SAV code. |
| [1]   | HBLN5[8] | R    | Display the blanking length starting from EAV to SAV code. |
| [2]   | HBLN6[8] | R    | Display the blanking length starting from EAV to SAV code. |
| [3]   | HBLN7[8] | R    | Display the blanking length starting from EAV to SAV code. |
| [7:4] | Reserved | R    | Reset to 0b                                                |

## LOW HBLN REGISTER – OFFSET 57H/58H/59H/5AH(Default=90H)

| BITS  | FUNCTION                | TYPE | DESCRIPTION                                                                                                                                                                     |
|-------|-------------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:0] | HBLNn[7:0]<br>n=4,5,6,7 | R    | Display the blanking length starting from EAV to SAV code.<br><br>(1) In 27MHz D1 Mode: 90H for PAL while 8AH for NTSC<br>(2) In 36MHz WD1 Mode: C0H for PAL while B8H for NTSC |

## VIN6 COLOR KILL ENABLE-REGISTER – OFFSET 5DH(Default=C0H)

| BITS  | FUNCTION      | TYPE | DESCRIPTION                                                           |
|-------|---------------|------|-----------------------------------------------------------------------|
| [5:0] | Reserved      | RW   | Reset to 0h                                                           |
| [6]   | PAL CKILL EN  | RW   | 1:enable color kill mode in PAL<br>0:disable color kill mode in PAL   |
| [7]   | NTSC CKILL EN | RW   | 1:enable color kill mode in NTSC<br>0:disable color kill mode in NTSC |

## VIN7 COLOR KILL ENABLE-REGISTER – OFFSET 5EH(Default=C0H)

| BITS  | FUNCTION     | TYPE | DESCRIPTION                                                         |
|-------|--------------|------|---------------------------------------------------------------------|
| [5:0] | Reserved     | RW   | Reset to 0h                                                         |
| [6]   | PAL CKILL EN | RW   | 1:enable color kill mode in PAL<br>0:disable color kill mode in PAL |

|     |               |    |                                                                       |
|-----|---------------|----|-----------------------------------------------------------------------|
| [7] | NTSC CKILL EN | RW | 1:enable color kill mode in NTSC<br>0:disable color kill mode in NTSC |
|-----|---------------|----|-----------------------------------------------------------------------|

**VIN8 COLOR KILL ENABLE-REGISTER – OFFSET 5FH(Default=C0H)**

| BITS  | FUNCTION      | TYPE | DESCRIPTION                                                           |
|-------|---------------|------|-----------------------------------------------------------------------|
| [5:0] | Reserved      | RW   | Reset to 0h                                                           |
| [6]   | PAL CKILL EN  | RW   | 1:enable color kill mode in PAL<br>0:disable color kill mode in PAL   |
| [7]   | NTSC CKILL EN | RW   | 1:enable color kill mode in NTSC<br>0:disable color kill mode in NTSC |

**HI –Bits HZOOM REGISTER – OFFSET 68H(Default=00H)**

| BITS  | FUNCTION    | TYPE | DESCRIPTION  |
|-------|-------------|------|--------------|
| [1:0] | HZOOM5[9:8] | RW   | MSB of reg69 |
| [3:2] | HZOOM6[9:8] | RW   | MSB of reg6A |
| [5:4] | HZOOM7[9:8] | RW   | MSB of reg6B |
| [7:6] | HZOOM8[9:8] | RW   | MSB of reg6C |

**LOW–Bits HZOOM VIN5 REGISTER – OFFSET 69H(Default=00H)**

| BITS  | FUNCTION    | TYPE | DESCRIPTION                                                                             |
|-------|-------------|------|-----------------------------------------------------------------------------------------|
| [7:0] | HZOOM5[7:0] | R/W  | HZOOM UP register the number is from<br>3DE to 3FF if HZOOM5[9:0]=00h No HZOOM Function |

**LOW–Bits HZOOM VIN6 REGISTER – OFFSET 6AH(Default=00H)**

| BITS  | FUNCTION    | TYPE | DESCRIPTION                                                                             |
|-------|-------------|------|-----------------------------------------------------------------------------------------|
| [7:0] | HZOOM6[7:0] | R/W  | HZOOM UP register the number is from<br>3DE to 3FF if HZOOM6[9:0]=00h No HZOOM Function |

**LOW–Bits HZOOM VIN7 REGISTER – OFFSET 6BH(Default=00H)**

| BITS  | FUNCTION    | TYPE | DESCRIPTION                                                                             |
|-------|-------------|------|-----------------------------------------------------------------------------------------|
| [7:0] | HZOOM7[7:0] | R/W  | HZOOM UP register the number is from<br>3DE to 3FF if HZOOM7[9:0]=00h No HZOOM Function |

**LOW–Bits HZOOM VIN8 REGISTER – OFFSET 6CH(Default=00H)**

| BITS  | FUNCTION    | TYPE | DESCRIPTION                                                                             |
|-------|-------------|------|-----------------------------------------------------------------------------------------|
| [7:0] | HZOOM8[7:0] | R/W  | HZOOM UP register the number is from<br>3DE to 3FF if HZOOM8[9:0]=00h No HZOOM Function |

## LINE\_IN9 CONTROL REGISTER – OFFSET 73H(Default=00H)

| BITS  | FUNCTION        | TYPE | DESCRIPTION                                                                                                          |
|-------|-----------------|------|----------------------------------------------------------------------------------------------------------------------|
| [0]   | LINE_IN9 DET_EN | RW   | 0 : Disable LINE_IN9 status register update and interrupt<br>1: Enable LINE_IN9 status register update and interrupt |
| [7:1] | Reserved        | R    | Reset to 00h                                                                                                         |

## LINE\_IN9 DETECT ENABLE REGISTER – OFFSET 74H(Default=00H)

| BITS  | FUNCTION              | TYPE | DESCRIPTION                                    |
|-------|-----------------------|------|------------------------------------------------|
| [0]   | LINE_IN9 DETECT_STATE | RW   | Audio LINE_IN9 detect<br>0:Disable<br>1:Enable |
| [7:1] | Reserved              | R    | Reset to 00h                                   |

## MIX RATIO VALUE FOR LINE\_IN9 REGISTER – OFFSET 7FH(Default=00H)

| BITS  | FUNCTION   | TYPE | DESCRIPTION                                                                                                                                                            |
|-------|------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | Mix_Ratio9 | RW   | LINE_IN9 ratio value for audio mixing function<br>0 : 1/2^8<br>1 : 1/2^7<br>2 : 1/2^6<br>3 : 1/2^5<br>4 : 1/2^4<br>5 : 1/2^3<br>6 : 1/2^2<br>7 : 1/2^1<br>other : 100% |
| [7:4] | Reserved   | R    | Reset to 00b                                                                                                                                                           |

## VIN5 COLOR KILL ENABLE-REGISTER – OFFSET 96H(Default=C0H)

| BITS  | FUNCTION      | TYPE | DESCRIPTION                                                           |
|-------|---------------|------|-----------------------------------------------------------------------|
| [5:0] | Reserved      | RW   | Reset to 0h                                                           |
| [6]   | PAL CKILL EN  | RW   | 1:enable color kill mode in PAL<br>0:disable color kill mode in PAL   |
| [7]   | NTSC CKILL EN | RW   | 1:enable color kill mode in NTSC<br>0:disable color kill mode in NTSC |

**GPIO\_4\_5 MODE REGISTER- OFFSET C8H(Default=00H)**

| <b>BIT</b> | <b>FUNCTION</b>                 | <b>TYPE</b> | <b>DESCRIPTION</b>                                                                                                                                             |
|------------|---------------------------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [2:0]      | Output Mode For GPIO_4          | RW          | Select output mode for GPIO_4<br>0: Output HSYNC<br>1: Output VSYNC<br>2:Field<br>3:H-active<br>4:VH-active<br>5:27MHz clock output<br>6:VH-sync<br>7:GPP_VA1  |
| [3]        | General Purpose Value In GPIO_4 | RW          | Set general purpose value in GPIO_4                                                                                                                            |
| [6:4]      | Output Mode For GPIO_5 Pin      | RW          | Select output mode for GPIO_5<br>0: Output HSYNC<br>1: Output VSYNC<br>2:Field<br>3:H-active<br>4:VH-active<br>5:27MHz clock output<br>6: VH-sync<br>7:GPP_VA2 |
| [7]        | General Purpose Value In GPIO_5 | RW          | Set general purpose value in GPIO_5                                                                                                                            |

**GPIO\_6\_7 MODE REGISTER- OFFSET C9H(Default=00H)**

| <b>BIT</b> | <b>FUNCTION</b>                 | <b>TYPE</b> | <b>DESCRIPTION</b>                                                                                                                                            |
|------------|---------------------------------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [2:0]      | Output Mode For GPIO_6 Pin      | RW          | Select output mode for GPIO_6<br>0: Output HSYNC<br>1: Output VSYNC<br>2:Field<br>3:H-active<br>4:VH-active<br>5:27MHz clock output<br>6:VH-sync<br>7:GPP_VA1 |
| [3]        | General Purpose Value In GPIO_6 | RW          | Set general purpose value in GPIO_6                                                                                                                           |

|       |                                 |    |                                                                                                                                                              |
|-------|---------------------------------|----|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [6:4] | Output Mode For GPIO_7          | RW | Select output mode for GPIO_7<br>0:Output HSYNC<br>1: Output VSYNC<br>2:Field<br>3:H-active<br>4:VH-active<br>5:27MHz clock output<br>6:VH-sync<br>7:GPP_VA2 |
| [7]   | General Purpose Value In GPIO_7 | RW | Set general purpose value in GPIO_7                                                                                                                          |

## MIX RATIO VALUE FOR LINE\_IN5 & LINE\_IN6 REGISTER – OFFSET DDH (Default=00H)

| BITS  | FUNCTION   | TYPE | DESCRIPTION                                                                                                                                                            |
|-------|------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | Mix_Ratio5 | RW   | LINE_IN5 ratio value for audio mixing function<br>0 : 1/2^8<br>1 : 1/2^7<br>2 : 1/2^6<br>3 : 1/2^5<br>4 : 1/2^4<br>5 : 1/2^3<br>6 : 1/2^2<br>7 : 1/2^1<br>other : 100% |
| [7:4] | Mix_Ratio6 | R/W  | LINE_IN6 ratio value for audio mixing function<br>0 : 1/2^8<br>1 : 1/2^7<br>2 : 1/2^6<br>3 : 1/2^5<br>4 : 1/2^4<br>5 : 1/2^3<br>6 : 1/2^2<br>7 : 1/2^1<br>other : 100% |

**MIX RATIO VALUE FOR LINE\_IN7 & LINE\_IN8 REGISTER – OFFSET DEH (Default=00H)**

| BITS  | FUNCTION   | TYPE | DESCRIPTION                                                                                                                                                                                                                                                    |
|-------|------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [3:0] | Mix_Ratio7 | RW   | LINE_IN7 ratio value for audio mixing function<br>0 : 1/2 <sup>8</sup><br>1 : 1/2 <sup>7</sup><br>2 : 1/2 <sup>6</sup><br>3 : 1/2 <sup>5</sup><br>4 : 1/2 <sup>4</sup><br>5 : 1/2 <sup>3</sup><br>6 : 1/2 <sup>2</sup><br>7 : 1/2 <sup>1</sup><br>other : 100% |
| [7:4] | Mix_Ratio8 | R/W  | LINE_IN8 ratio value for audio mixing function<br>0 : 1/2 <sup>8</sup><br>1 : 1/2 <sup>7</sup><br>2 : 1/2 <sup>6</sup><br>3 : 1/2 <sup>5</sup><br>4 : 1/2 <sup>4</sup><br>5 : 1/2 <sup>3</sup><br>6 : 1/2 <sup>2</sup><br>7 : 1/2 <sup>1</sup><br>other : 100% |

**AUDIO DETECT TH 5678 MSB REGISTER– OFFSET E1H (Default=00H)**

| BITS  | FUNCTION    | TYPE | DESCRIPTION                                          |
|-------|-------------|------|------------------------------------------------------|
| [0]   | ADET_TH5[4] | RW   | Bit4 of audio detection threshold value for LINE_IN5 |
| [1]   | ADET_TH6[4] | RW   | Bit4 of audio detection threshold value for LINE_IN6 |
| [2]   | ADET_TH7[3] | RW   | Bit4 of audio detection threshold value for LINE_IN7 |
| [3]   | ADET_TH8[4] | RW   | Bit4 of audio detection threshold value for LINE_IN8 |
| [7:4] | Reserved    | R    | Reset to 0h                                          |

**AUDIO DETECT TH 56 LSB REGISTER– OFFSET E2H (Default=AAH)**

| BITS  | FUNCTION      | TYPE | DESCRIPTION                                              |
|-------|---------------|------|----------------------------------------------------------|
| [3:0] | ADET_TH5[3:0] | RW   | Bit3 ~ 0 of audio detection threshold value for LINE_IN5 |
| [7:4] | ADET_TH6[3:0] | RW   | Bit3 ~ 0 of audio detection threshold value for LINE_IN6 |

**AUDIO DETECT TH 78 LSB REGISTER– OFFSET E3H (Default=AAH)**

| BITS  | FUNCTION      | TYPE | DESCRIPTION                                              |
|-------|---------------|------|----------------------------------------------------------|
| [3:0] | ADET_TH7[3:0] | RW   | Bit3 ~ 0 of audio detection threshold value for LINE_IN7 |

|       |               |    |                                                          |
|-------|---------------|----|----------------------------------------------------------|
| [7:4] | ADET_TH8[3:0] | RW | Bit3 ~ 0 of audio detection threshold value for LINE_IN8 |
|-------|---------------|----|----------------------------------------------------------|

## VIDEO/AUDIO DETECTION ENABLE REGISTER-OFFSET FCH (Default=FFH)

| BITS  | FUNCTION | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|----------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:0] | AVDET_EN | RW   | <p>Enable the status register updated and interrupt request if the following video or audio source is detected. The mapping of video/audio input to each bit of the register is defined as below.</p> <p>Bit0: Video input CV_IN4<br/>           Bit1: Video input CV_IN5.<br/>           Bit2: Video input CV_IN6.<br/>           Bit3: Video input CV_IN7.<br/>           Bit4: Audio input LINE_IN5.<br/>           Bit5: Audio input LINE_IN6.<br/>           Bit6: Audio input LINE_IN7.<br/>           Bit7: Audio input LINE_IN8.</p> <p>0: Disable status register updated and interrupt request<br/>           1: Enable status register updated and interrupt request</p> |

## VIDEO/AUDIO DETECTION STATUS REGISTER-OFFSET FDH (Default=00H)

| BITS  | FUNCTION     | TYPE | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|--------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [7:0] | AVDET_STATUS | R    | <p>Display the detection status of each video or audio source according to AVDET_EN, VDET_MODE and ADET_MODE. The mapping of video/audio input to each bit of the register is defined as below. The bits will be cleared once the register is read by software except VDET_MODE =3 or ADET_MODE=3.</p> <p>Bit0: Video input CV_IN0.<br/>           Bit1: Video input CV_IN1.<br/>           Bit2: Video input CV_IN2.<br/>           Bit3: Video input CV_IN3.<br/>           Bit4: Audio input LINE_IN5.<br/>           Bit5: Audio input LINE_IN6.<br/>           Bit6: Audio input LINE_IN7.<br/>           Bit7: Audio input LINE_IN8.</p> <p>0: Inactive. No event detected after the last access to this bit.<br/>           1: Active. An event is detected.</p> |

## Electrical Characteristics

### Absolute Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

| Parameters                           |                   | Value            | Note:<br>Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. |
|--------------------------------------|-------------------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Supply Voltage Range                 | 3.3V Power Supply | -0.3V to 4.5V    |                                                                                                                                                                                                                                                                                                                                                                                                      |
|                                      | Core Power Supply | -0.3V to 1.8V    |                                                                                                                                                                                                                                                                                                                                                                                                      |
| T <sub>stg</sub> Storage Temperature |                   | -65 °C to 150 °C |                                                                                                                                                                                                                                                                                                                                                                                                      |

### Normal Operating Conditions

| Symbol              | Parameters                                                             | Min. | Typ. | Max. | Unit |
|---------------------|------------------------------------------------------------------------|------|------|------|------|
| VDD                 | Power supply voltage 3.3V (Pin name: VD33, ADC_VDD, ADAC_VDD, VD-DPLL) | 3.0  | 3.3  | 3.6  | V    |
| VDDC                | Core Power supply voltage (Pin name: VDDC)                             | 0.9  | 1.0  | 1.1  | V    |
| V <sub>I(P-P)</sub> | Analog input voltage (ac-coupling necessary)                           | 0    |      | 1.6  | V    |
| T <sub>A</sub>      | Ambient Operation temperature <sup>*1</sup>                            | 0    |      | 70   | °C   |

Note: \*1. Please refer to the Ordering Information for Industrial grade application.

### DC Electrical Characteristics

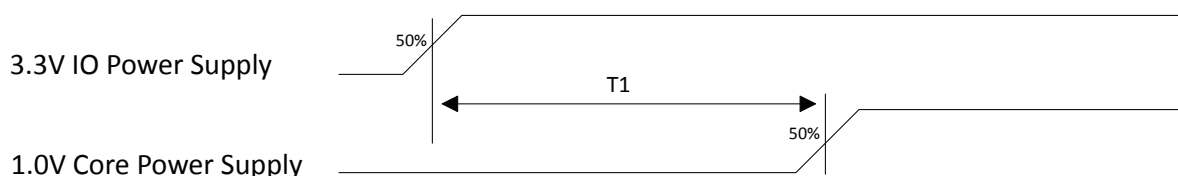
| Symbol          | Parameters                       | Conditions                            | Min. | Typ. | Max.  | Unit |
|-----------------|----------------------------------|---------------------------------------|------|------|-------|------|
| V <sub>IH</sub> | Digital input high voltage       |                                       | 2.0  |      | 3.6   | V    |
| V <sub>IL</sub> | Digital input low voltage        |                                       | -0.3 |      | 0.8   | V    |
| V <sub>OH</sub> | Digital Output high voltage      |                                       | 2.4  |      |       | V    |
| V <sub>OL</sub> | Digital Output low voltage       |                                       |      |      | 0.4   | V    |
| I <sub>L</sub>  | Input Leakage Current            | No internal pull-up or pull-down pins |      |      | +/- 1 | uA   |
| I <sub>OZ</sub> | Tri-state output leakage current |                                       |      |      | +/- 1 | uA   |
| I <sub>OH</sub> | High level output current        | VOH=2.4V                              | 11   | 17   | 24    | mA   |
| I <sub>OL</sub> | Low level output current         | VOL=0.4V                              | 8    | 13   | 16    | mA   |
| R <sub>pu</sub> | Input pull-up resistance         | Vin=0                                 | 61   | 75   | 105   | KΩ   |
| R <sub>pd</sub> | Input pull-down resistance       | Vin=DVDD33                            | 101  | 199  | 330   | KΩ   |

## Power Dissipation

| Symbol                | Parameters                 | Test Condition                      | Min. | Typ. | Max. | Unit |
|-----------------------|----------------------------|-------------------------------------|------|------|------|------|
| 3.3V <sub>TOTAL</sub> | Total 3.3V Power Voltage   | Enable 8-ch 960H Video/Audio Inputs |      | 330  |      | mA   |
| 1.0V <sub>TOTAL</sub> | Core Supply Voltage (VDDC) |                                     |      | 375  |      | mA   |
| P <sub>TOT</sub>      | Total Power Consumption    |                                     |      | 1464 |      | mW   |

## Power-On Sequence of 3.3V and 1.0V Power

| Symbol | Parameters                                            | Min. | Typ. | Max. | Unit |
|--------|-------------------------------------------------------|------|------|------|------|
| T1     | Interval Delay between IO Power and Core Power Supply | 0    | 10   | 500  | ms   |



## Oscillator input

| Parameters          | Min. | Typ. | Max. | Unit |
|---------------------|------|------|------|------|
| Frequency           |      | 27   |      | MHz  |
| Frequency tolerance |      |      | ±50  | ppm  |

## AC Electrical Characteristics

### Video Electrical

| Symbol         | Parameter                  | Test Condition                                                                                                            | Min. | Typ. | Max. | Unit            |
|----------------|----------------------------|---------------------------------------------------------------------------------------------------------------------------|------|------|------|-----------------|
| Z <sub>i</sub> | Input impedance            | Analog video inputs by design                                                                                             |      | 40   |      | kΩ              |
| C <sub>i</sub> | Input Capacitance          | Analog video inputs by design                                                                                             |      | 10   |      | pF              |
| DNL            | Differential Non Linearity |                                                                                                                           |      |      | ±2   | LSB             |
| INL            | Integral Non Linearity     |                                                                                                                           |      |      | ±3   | LSB             |
| V <sub>i</sub> | Full scale input range     | The expected full input range is only 0.5 V <sub>pp</sub> to 1.0 V <sub>pp</sub> .                                        | 0.25 |      | 1.6  | V <sub>pp</sub> |
| SNR            | Signal to Noise Ratio      | This is measured with a -1dB full scale input signal and adjusted for full scale amplitude                                | 45   |      |      | dB              |
| THD            | Total Harmonic Distortion  |                                                                                                                           |      | -45  |      | dB              |
|                | Analog input bandwidth     | This bandwidth does not include limitations due to the source impedance of 37.5 and loading on the board, 30 pF (140 MHz) |      | 300  |      | MHz             |

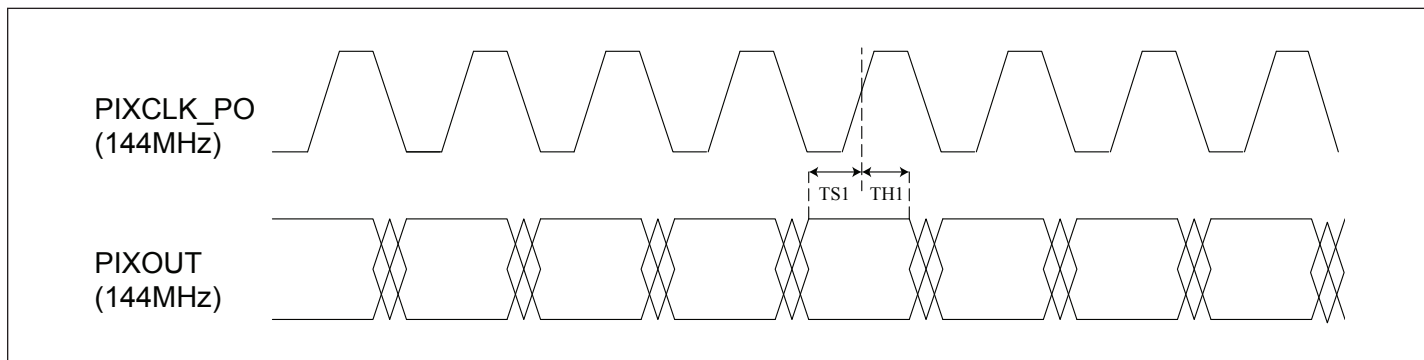
## Audio Electrical

| Symbol | Parameters                | Test Condition                | Min. | Typ. | Max. | Unit |
|--------|---------------------------|-------------------------------|------|------|------|------|
| Zi     | Input impedance           | Analog video inputs by design |      | 40   |      | kΩ   |
| Ci     | Input Capacitance         | Analog video inputs by design |      | 10   |      | pF   |
| Vi     | Maximum Input Range       |                               | 0.25 |      | 1.6  | V    |
| SNR    | Signal to Noise Ratio     |                               |      | 85   |      | dB   |
| DNR    | Dynamic Range             |                               |      | 80   |      | dB   |
| THD    | Total Harmonic Distortion |                               |      | -75  |      | dB   |

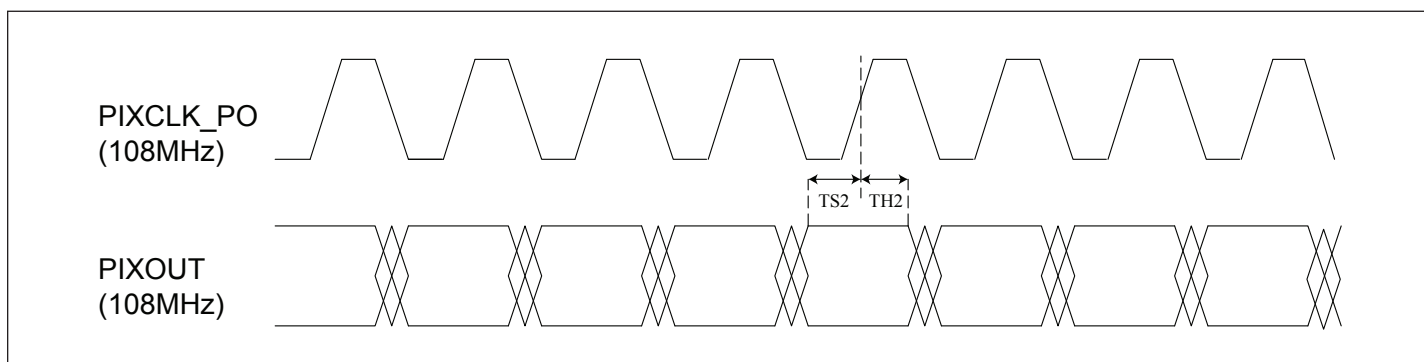
## Pixel Clock and Video Data Timing

| Symbol | Parameters                              | Min. | Typ. | Max. | Unit |
|--------|-----------------------------------------|------|------|------|------|
| TS1    | Setup from PIXCLK_PO to PIXOUT (144MHz) | 2.6  | -    | 4.3  | ns   |
| TH1    | Hold from PIXCLK_PO to PIXOUT (144MHz)  | 2.7  | -    | 4.4  | ns   |
| TS2    | Setup from PIXCLK_PO to PIXOUT (108MHz) | 3.8  | -    | 5.4  | ns   |
| TH2    | Hold from PIXCLK_PO to PIXOUT (108MHz)  | 3.9  | -    | 5.5  | ns   |
| TS3    | Setup from PIXCLK_PO to PIXOUT (72MHz)  | 5.6  | -    | 7.6  | ns   |
| TH3    | Hold from PIXCLK_PO to PIXOUT (72MHz)   | 6.3  | -    | 8.3  | ns   |
| TS4    | Setup from PIXCLK_PO to PIXOUT (54MHz)  | 8.2  | -    | 10.3 | ns   |
| TH4    | Hold from PIXCLK_PO to PIXOUT (54MHz)   | 8.3  | -    | 10.4 | ns   |
| TS5    | Setup from PIXCLK_PO to PIXOUT (36MHz)  | 14.1 | -    | 16.1 | ns   |
| TH5    | Hold from PIXCLK_PO to PIXOUT (36MHz)   | 11.7 | -    | 13.7 | ns   |
| TS6    | Setup from PIXCLK_PO to PIXOUT (27MHz)  | 19   | -    | 20.9 | ns   |
| TH6    | Hold from PIXCLK_PO to PIXOUT (27MHz)   | 16.1 |      | 18   | ns   |

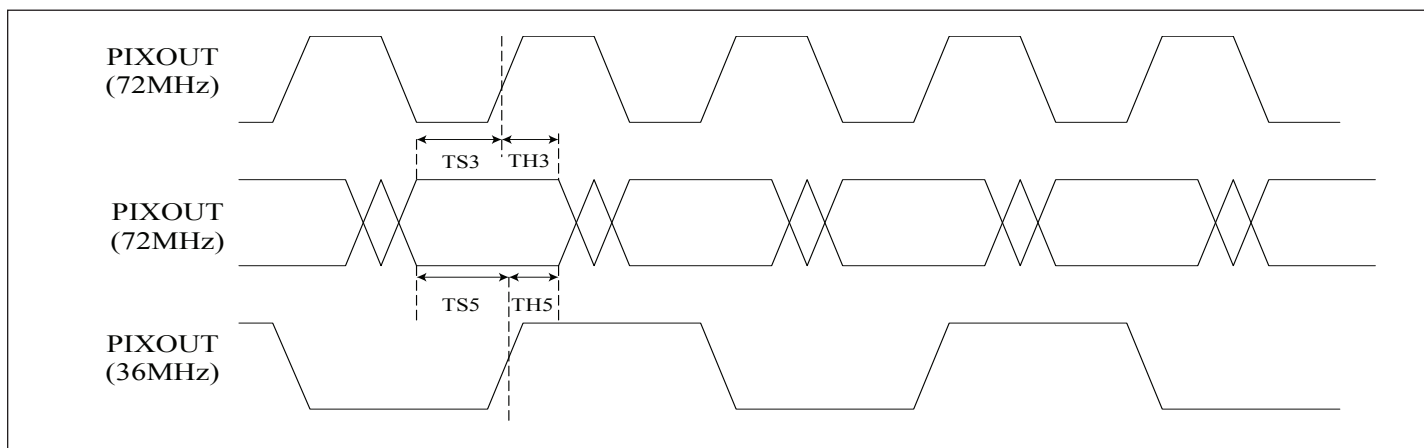
Note: The timing value is measured by the following conditions: (1) the clock delay control on PIXCLK\_PO pin is set to zero; (2) the clock polarity control on PIXCLK\_PO pin is not inverted.



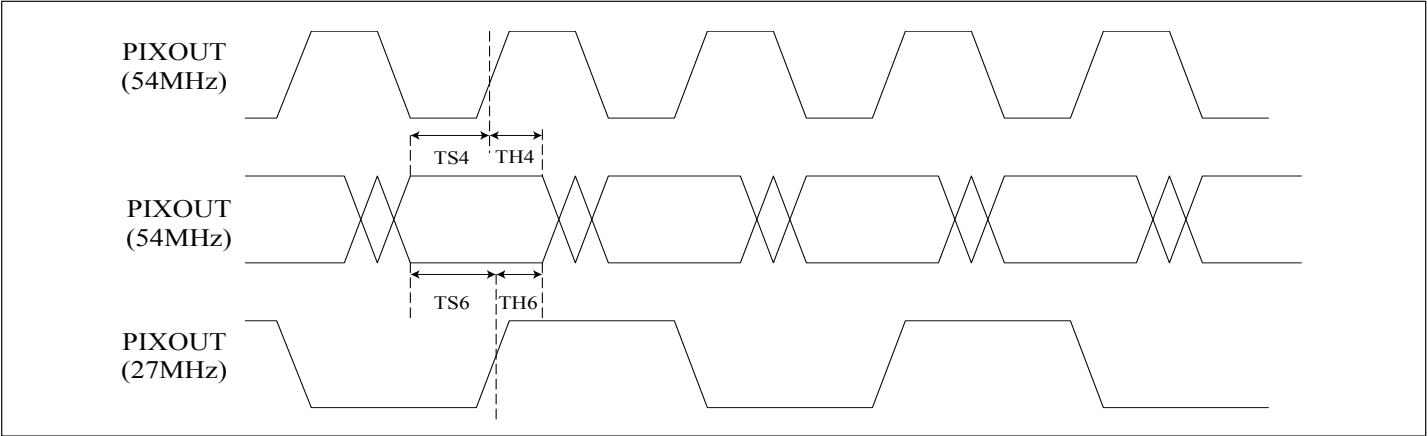
OTDM is operated at 144MHz



OTDM is operated at 108MHz



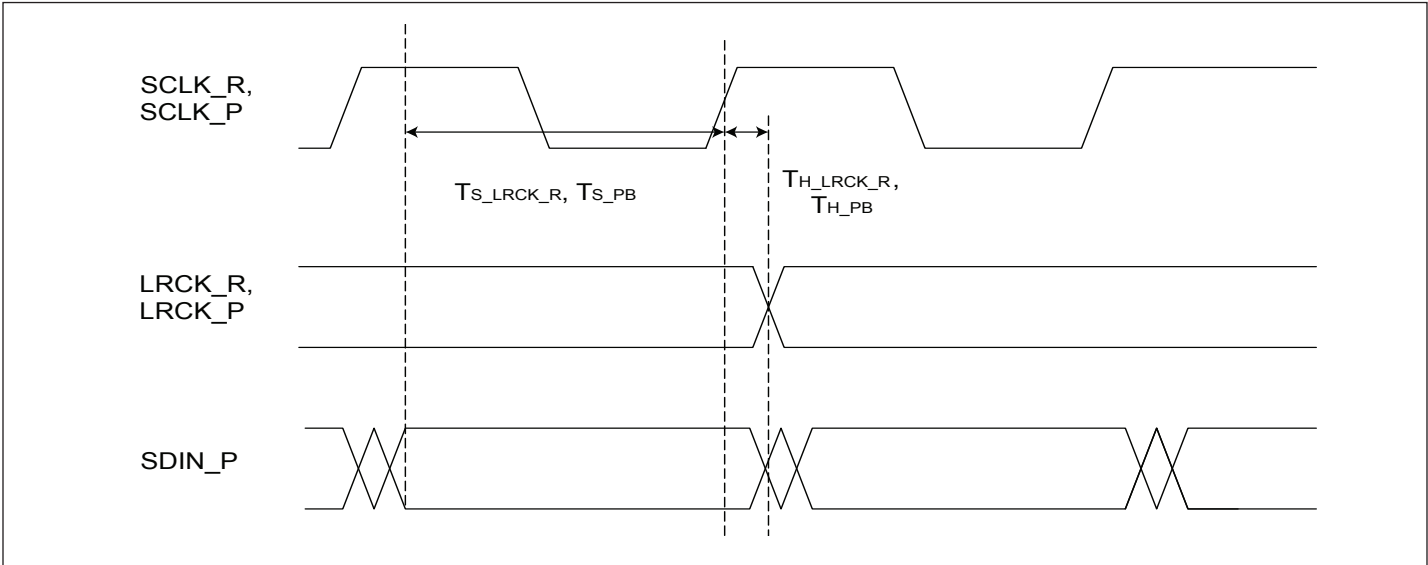
OTBM is operated at 72/36MHz



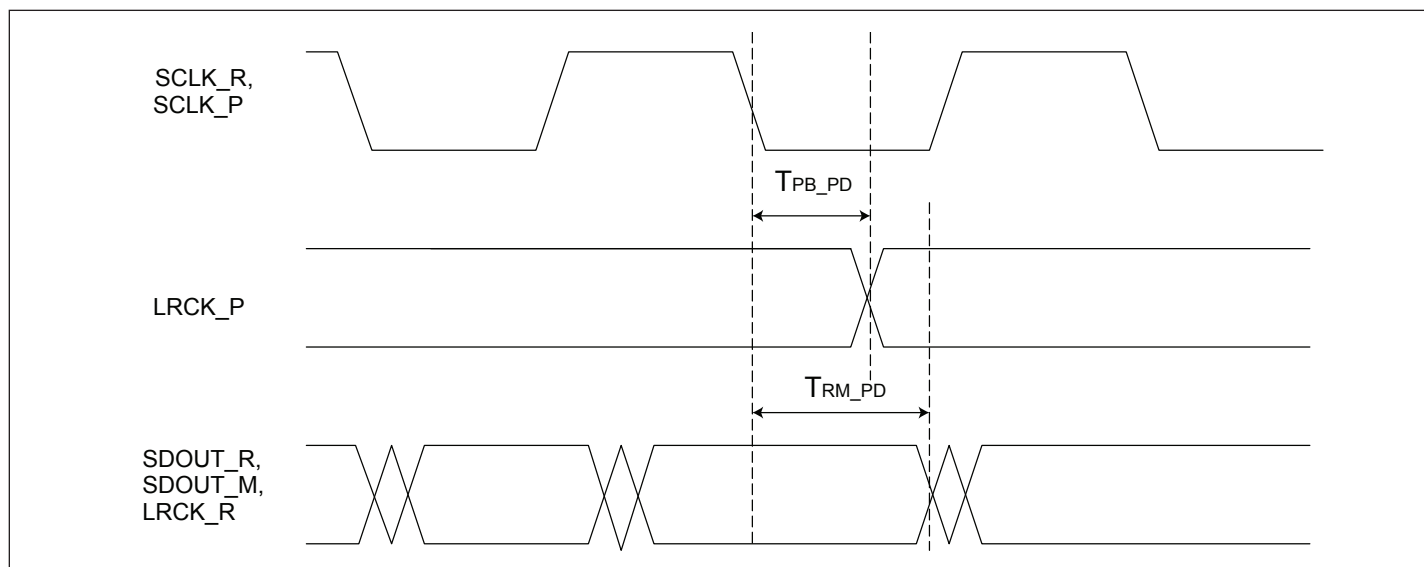
OTBM is operated at 54/27MHz

Audio Electrical Characteristics

| Symbol                | Parameters                              | Test Condition | Min. | Typ. | Max. | Unit |
|-----------------------|-----------------------------------------|----------------|------|------|------|------|
| T <sub>S_LRCK_R</sub> | Setup Time for LRCK_R                   | Slave Mode     | 0.2  |      |      | ns   |
| T <sub>H_LRCK_R</sub> | Hold Time for LRCK_R                    |                | 0.4  |      |      | ns   |
| T <sub>S_PB</sub>     | Setup Time for LRCK_P and SDIN_P        |                | 0.1  |      |      | ns   |
| T <sub>H_PB</sub>     | Hold Time for LRCK_P and SDIN_P         | Master Mode    | 0.55 |      |      | ns   |
| T <sub>RM_PD</sub>    | Propagation Delay for SDOUT_R/M, LRCK_R |                | 2.6  |      | 5.9  | ns   |
| T <sub>PB_PD</sub>    | Propagation Delay for LRCK_P            |                | 2.2  |      | 4.8  | ns   |



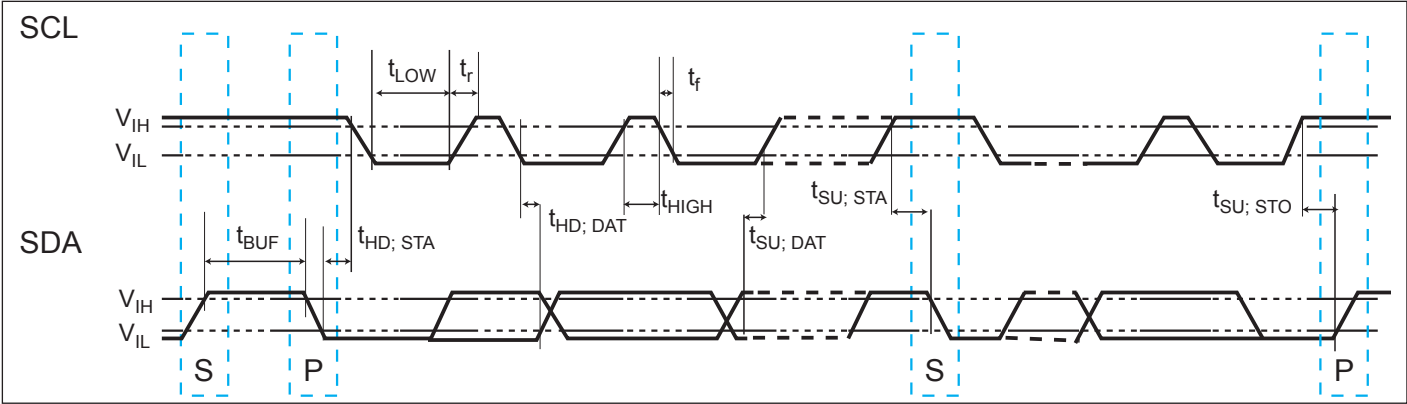
Digital Serial Audio Interface Slave Mode Timing Diagram



Digital Serial Audio Interface Master Mode Timing Diagram

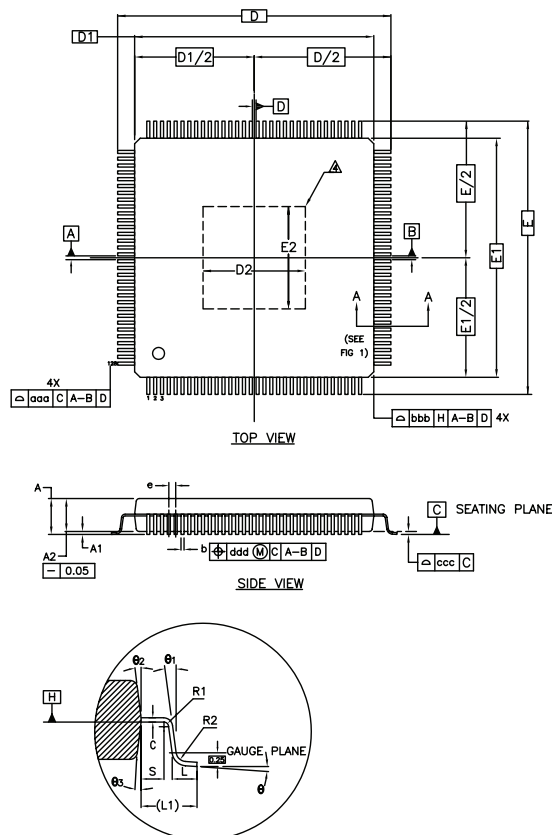
#### I2C Host Port Timing

| Symbol              | Parameters                              | Test Condition      | Min. | Typ. | Max. | Unit |
|---------------------|-----------------------------------------|---------------------|------|------|------|------|
| t <sub>BUF</sub>    | Bus free time between STOP and START    |                     | 1.3  |      |      | μs   |
| t <sub>SU;STA</sub> | Setup time, (repeated) START condition  |                     | 0.6  |      |      | μs   |
| t <sub>HD;STA</sub> | Hold time, (repeated) START condition   |                     | 0.6  |      |      | μs   |
| t <sub>SU;STO</sub> | Setup time, STOP condition              |                     | 0.6  |      |      | ns   |
| t <sub>SU;DAT</sub> | Data setup time                         |                     | 100  |      |      | ns   |
| t <sub>HD;DAT</sub> | Data hold time                          |                     | 0    |      | 0.9  | μs   |
| t <sub>r</sub>      | Rise time, VC1(SDA) and VC0(SCL) signal | Specified by design |      |      | 250  | ns   |
| t <sub>f</sub>      | Fall time, VC1(SDA) and VC0(SCL) signal | Specified by design |      |      | 250  | ns   |
| C <sub>b</sub>      | Capacitive load for each bus line       | Specified by design |      |      | 400  | pF   |
| f <sub>i2c</sub>    | I2C clock frequency                     |                     |      |      | 400  | kHz  |



Digital Serial Audio Interface Master Mode Timing Diagram

## Packaging Mechanical (LQFP)



CONTROL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL         | MILLIMETER |      |      | INCH       |       |       |
|----------------|------------|------|------|------------|-------|-------|
|                | MIN.       | NOM. | MAX. | MIN.       | NOM.  | MAX.  |
| A              | —          | —    | 1.60 | —          | —     | 0.063 |
| A1             | 0.05       | —    | 0.15 | 0.002      | —     | 0.006 |
| A2             | 1.35       | 1.40 | 1.45 | 0.053      | 0.055 | 0.057 |
| D              | 16.00 BSC. |      |      | 0.630 BSC. |       |       |
| D1             | 14.00 BSC. |      |      | 0.551 BSC. |       |       |
| E              | 16.00 BSC. |      |      | 0.630 BSC. |       |       |
| E1             | 14.00 BSC. |      |      | 0.551 BSC. |       |       |
| R2             | 0.08       | —    | 0.20 | 0.003      | —     | 0.008 |
| R1             | 0.08       | —    | —    | 0.003      | —     | —     |
| θ              | 0°         | 3.5° | 7°   | 0°         | 3.5°  | 7°    |
| θ <sub>1</sub> | 0°         | —    | —    | 0°         | —     | —     |
| θ <sub>2</sub> | 11°        | 12°  | 13°  | 11°        | 12°   | 13°   |
| θ <sub>3</sub> | 11°        | 12°  | 13°  | 11°        | 12°   | 13°   |
| c              | 0.09       | —    | 0.20 | 0.004      | —     | 0.008 |
| L              | 0.45       | 0.60 | 0.75 | 0.018      | 0.024 | 0.030 |
| L <sub>1</sub> | 1.00 REF   |      |      | 0.039 REF  |       |       |
| S              | 0.20       | —    | —    | 0.008      | —     | —     |
| b              | —          | 0.16 | —    | —          | 0.006 | —     |
| e              | 0.40 BSC.  |      |      | 0.016 BSC. |       |       |
| aaa            | 0.20       |      |      | 0.008      |       |       |
| bbb            | 0.20       |      |      | 0.008      |       |       |
| ccc            | 0.08       |      |      | 0.003      |       |       |
| ddd            | 0.07       |      |      | 0.003      |       |       |
| D2             | 5.10       | —    | 5.99 | 0.20       | —     | 0.236 |
| E2             | 5.10       | —    | 5.99 | 0.20       | —     | 0.236 |

NOTE :

FIGURE 1 SECTION A-A

1. ALL DIMENSION IN MM
2. REFER JEDEC MS-026
3. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR
4. THE OPTIONAL EXPOSED PAD IS COINCIDENT WITH THE BOTTOM SIDE OF THE PACKAGE AND NOT ALLOWED TO PROTRUDE BEYOND THAT SURFACE.



DATE: 04/22/08

DESCRIPTION: 128-pin Low Profile Quad Flat Package (LQFP)

PACKAGE CODE: FD128

DOCUMENT CONTROL #: PD-2072

REVISION: A

07-0353

Note: For latest package info, please check: <http://www.pericom.com/support/packaging>

## Ordering Information

| Ordering Code   | Package Code | Package Description                          |
|-----------------|--------------|----------------------------------------------|
| PI7VD9008ABHFDE | FD128        | 128-pin Low Profile Quad Flat Package (LQFP) |

Notes:

- Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
- Adding "E" = Pb-free, "I"=Industrial, "FP"=Package code, "X" suffix = Tape/Reel

# PI7VD9008ABH

Adaptive EQ 8-channel 960H Video Decoder



## Related Product Information

| Part Number  | Product Description                                              |
|--------------|------------------------------------------------------------------|
| PI7VD9004ABH | AEQ 960H 4-channel Video Decoder with 10-bit Audio ADC(128 pins) |
| PI7VD9401    | BT656 to PCI Express Video/Audio Media Bridge                    |

## Reference Document Information

| Document         | Description                                            |
|------------------|--------------------------------------------------------|
| Application Note | Reference schematic and board layout application notes |

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